

SC2166Q Type-C/ PD and DPDM Fast Charge Controller Supporting SCP and UFCS Protocols

1 Description

SC2166Q is a Type-C / PD and DPDM fast charge controller for automotive applications. It complies with the latest Type-C and PD 3.2 standards and supports the proprietary high voltage fast charge protocols with DPDM interface. It supports the SCP and UFCS fast charge protocols. It targets for the wall adapters, travel adapters and USB car charger applications.

SC2166Q minimizes external components by integrating USB PD baseband PHY, Type-C detection, DPDM PHY, VBUS discharging paths, VCONN supply, programmable feedback compensation, voltage and current sense, 10-bit high performance ADC, dual 10-bit DACs for CC/CV regulation, NMOS gate driver, I2C interface, UART interface and protection circuits. It contains a 32-bit high performance micro-controller core with 3k-Byte RAM and OTP ROM, which provides cost effective solutions to many applications. It reserves independent space for storing chip ID code, which is convenient for factory regulation.

SC2166Q supports various protection mechanisms including Over Voltage Protection (OVP), Under Voltage Protection (UVP), Over Current Protection (OCP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), DPDM Over Voltage Protection (DPDM OVP), CC Over Voltage Protection (CCOVP), VCONN Over Voltage (VCONN OVP), VCONN Over Current (VCONN OCP) and VCONN Short Circuit Protection (VCONN SCP), so to effectively ensure stable and reliable operation of system.

The SC2166Q is available in 24-pin QFN 4mm×4mm×0.75mm package.

2 Features

- **AEC-Q100**
 - AEC-Q100 Qualified for automotive applications
- **USB Type-C**
 - Support Type-C DFP protocols
 - Configurable resistor R_p
- **USB Power Delivery**
 - Support DFP USB PD 3.2 with PPS
 - Hardware BMC transmitter and receiver
 - Full feature physical layer
 - Hardware CRC
 - Hardware reset
 - Integrate PD 3.2 protocol engine
 - Integrate VCONN and support SOP' for e-marker
- **DPDM Fast Charging Interface**
 - Integrate firmware controlled DPDM interface
 - Support UFCS provider protocols
 - Support Apple charging, BC1.2, DCP, HVDCP, FC, AFC, FCP, SCP, VOOC, UFCS, I2C and other proprietary charging protocols
- **Power**
 - Wide operation range: 2.9V to 24V (26V tolerant)
 - Integrate programmable feedback compensation
 - Support internal or external feedback compensation
- **MCU Subsystem**
 - Integrated 32-bit high performance MCU core
 - 3k-Byte RAM and OTP ROM
 - Reserve independent space for storing chip ID code
 - Support UART interface for multiple ports application
 - Support I2C interface and multiple I/Os
 - Support sleep mode
- **Analog Block**
 - Support OPTO interface for adapter
 - Dual DACs for CC/CV loop.
 - 10-bit ADC to monitor the voltage / current / DPDM/ other signals
 - Integrated high side current sense amplifier
 - Integrated NMOS gate driver
 - Integrated VBUS discharging paths at both sides of isolation MOS
 - Integrated temperature sense module
- **Protections**
 - 26V tolerant for CC1 and CC2
 - 12V tolerant for DP and DM
 - On chip OVP, UVP, SCP, VCONN OVP, VCONN OCP, VCONN SCP, OTP, DPDM OVP, CC OVP
- **Package**
 - 24-pin QFN, 4mm x 4mm x 0.75mm

3 Applications

- Automotive USB Chargers

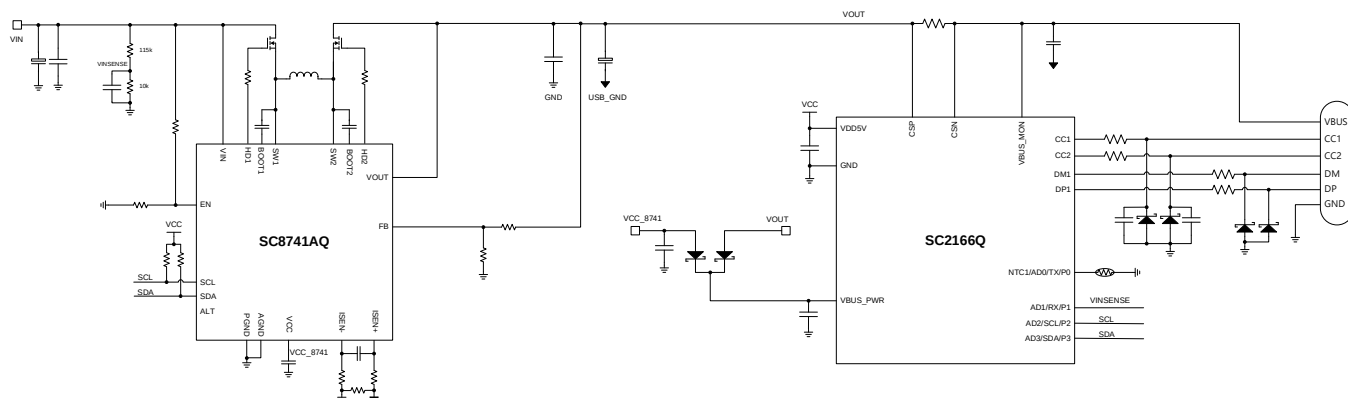
4 Device Information

Part Number	Package	Body Size
SC2166QQDLR	QFN-24	4mm x 4mm x 0.75mm



5 Typical Application Diagram

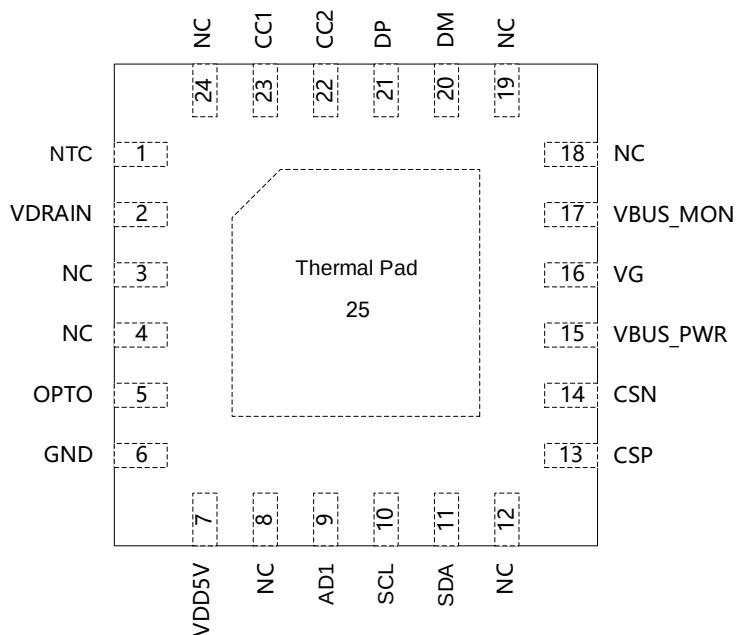
Application Diagram





6 Terminal Configuration and Functions

TOP VIEW of SC2166Q (QFN-24)



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	NTC	I	Remote thermal sensor connection node for external temperature monitoring
2	VDRAIN	I	Connect this pin to resistor divider point of the drain of SSR MOS
3	NC	I	No connect
4	NC	I	No connect
5	OPTO	I	Current sink output for optocoupler connection.
6	GND	I	Ground of the IC



7	VDD5V	O	Output of 5V LDO. Provide power supply for internal circuits. Connect a 2.2uF capacitor to ground
8	NC	-	No connect
9	AD1	I	A/D converter input channel
10	SCL	I/O	I2C interface, clock line.
11	SDA	I/O	I2C interface, data line.
12	NC	-	No connect
13	CSP	I/O	Positive input of the internal current sense amplifier. Connect to the high side current sense resistor
14	CSN	I/O	Negative input of the internal current sense amplifier. Connect to the high side current sense resistor
15	VBUS_PWR	I	IC supply input. It supports more than 100mA discharging capability for the internal VBUS capacitor and could be used to sense VBUS voltage.
16	VG	O	Load switch (NMOS) driver. Connect to the gate of loadswitch.
17	VBUS_MON	I	Connected to the VBUS line of the USB Type-C port. It can discharge the output capacitor and can be used to sense VBUS voltage of Type-C port.
18	NC	-	No connect
19	NC	-	No connect
20	DM	I/O	DM line of fast charging interface
21	DP	I/O	DP line of fast charging interface
22	CC2	I/O	Type-C configure channel2. It also supports VCONN output
23	CC1	I/O	Type-C configure channel1. It also supports VCONN output
24	NC	-	No connect
25	Thermal Pad	-	Connect this pad to GND



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	VG	-0.3	31	V
	DP, DM	-0.3	12	V
	VBUS_PWR, VBUS_MON, CC1, CC2, CSP, CSN, OPTO	-0.3	26	V
	VDD5V, P0, P1, P2, P3, VDRAIN	-0.3	5.5	V
	CSP to CSN	-5.5	5.5	V
	VG to VBUS_MON	-0.3	10	V
T _J	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) DPDMx pins should add 5.5V clamp.

7.2 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		QFN-24 (4mmX4mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	54	°C/W
θ_{JC}	Junction to case thermal resistance	25	°C/W

7.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	All pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	All pins	-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V _{BUS_PWR}	VBUS_PWR operation voltage	2.9		24	V
C _{VBUS_PWR}	Bulk capacitor at VBUS_PWR pin			1600 ⁽¹⁾	μF
C _{VBUS_MON}	Bulk capacitor at VBUS_MON pin	1	1	10	μF
R _{CS}	Sense resistor between CSP and CSN pins	3	5	10	mΩ



T _A	Operating ambient temperature	-40		125	°C
T _J	Operating junction temperature	-40		150	°C

- (1) It is recommended to add external discharge circuit on VBUS_PWR node if the bulk capacitance at VBUS_PWR node is higher than 1600 μ F.



7.5 Electrical Characteristics

T_j = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{BUS_PWR}	VBUS_PWR supply range		3.0		22	V
V _{BUS_PWR_POR}	VBUS_PWR power on threshold	VBUS_PWR rising threshold		2.9	3.0	V
V _{BUS_PWR_UVLO}	VBUS_PWR UVLO threshold	VBUS_PWR falling threshold	2.6	2.7	2.8	V
I _{q_ACT}	Quiescent current in active mode	VBUS_PWR=5V, PD is enabled, average quiescent current		3		mA
I _{q_SBY}	Quiescent current in standby mode	VBUS_PWR=5V, standby mode, digital DPDM module wakes up, all analog peripherals enabled		2		mA
I _{q_SLEEP}	Quiescent current in sleep mode	Control loop disabled, MCU and peripherals all disabled except CC		160	200	μA
5V LDO						
V _{LDO_5V}	5V LDO regulation voltage	VBUS_PWR = 5.5V~24V	4.9	5	5.1	V
V _{LDO_DROP}	5V LDO drop out voltage	V _{BUS_PWR} -V _{LDO5V} , I _{OUT} = 50 mA		150		mV
I _{LDO_LIMIT}	LDO current limit	V _{BUS_PWR} = 5V	90	100	120	mA
DISCHARGE						
I _{DIS_VBUS_PWR}	Discharging current at VBUS_PWR	Register-Programmable	25		150	mA
R _{DCHG_VBUS_MON}	Discharging resistor at VBUS_MON			1	1.4	kΩ
R _{DCHG_VBUSA}	Discharging resistor at VBUSA			1	1.4	kΩ
NMOS GATE DRIVER						
V _{DRV}	Driving voltage	V _{GATE} -V _{BUS_MON} , VBUS_PWR ≥ 3.3V		5		V
V _{CLAMP_GS}	Driver clamp voltage	V _{GATE} -V _{BUS_MON}		7		V
R _{DRIVE_UP}	Driver pull up resistance	VBUS_PWR=5V, Register-Programmable	20		200	kΩ
CURRENT SENSE						
G _{CSNS}	Gain of current sense amplifier	cs_sel_20x = 1	19.8	20	20.2	
		cs_sel_20x = 0	39.6	40	40.4	
V _{OCP}	OCP threshold, calculated as I _{BUS} *R _{SNS}	cs_sel_vocp = 01		300		mV
		cs_sel_vocp = 10		600		mV
		cs_sel_vocp = 11		960		mV
V _{OCP_DT}	OCP deglitch time			1000		μs
G _{LINE_COMP}	VBUS output compensation respect to the output of CSNS amplifier	cs_ana_comp_clamp_dis = 1		0		
		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 00b		1/4		
		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 01b		1/2		



		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 10b	7/12	
		cs_ana_comp_clamp_dis = 0, cs_ana_comp_slop = 11b	5/6	
V _{LINE_COMP_MAX}	Max VBUS output voltage compensation		160 200 240	mV
ADC				
V _{ADC_REF}	Reference voltage for ADC		2.249 2.253 2.257	V
N _{ADC}	Resolution		10	Bits
R _{SAMPLE}	ADC sample rate	Register programmable	47.5 50 52.5	ksps
			23.75 25 26.25	ksps
			9.5 10 10.5	ksps
			4.75 5 5.25	ksps
K _{ADC_VBUS_PWR}	Ratio from VBUS_PWR voltage sense		1/10	
K _{ADC_VBUS_MON}	Ratio from VBUS_MON voltage sense		1/10	
K _{ADC_CSNS}	Ratio from the output of current sense amplifier		1	
K _{ADC_DPDM}	Ratio from DP, DM, CC1, CC2		1/4	
K _{ADC_VDD5V}	Ratio from VDD5V		1/4	
K _{ADC_0_2}	Ratio from AD0, AD1, AD2 or AD3 voltage sense		1	
K _{ITC}	Internal temperature sense coefficient		2.819	mV/°C
V _{ITC_27°C}	Internal temperature sense output at 27 °C		733.94	mV
ADC _{VBUS_PWR} , ADC _{VBUS_MON} , ADC _{VBUSA}	Range		3.0 22.46	V
	LSB		22	mV
	Error	VBUS = 3.3V ~ 9V	-50 50	mV
		VBUS = 9V ~ 21V	-100 100	mV
ADC _{DP} ADC _{DM} ADC _{CC1} ADC _{CC2}	Range		0 8.983	V
	LSB		8.78	mV
	Error	Full range	-150 150	mV
ADC _{ADX} , ADC _{CSNS}	Range		0 2.25	V
	LSB		2.2	mV
	Error	Full range	-5 5	mV
INL	Integral non-linearity		-1.0 1.0	LSB
DNL	Differential non-linearity		-1.0 1.0	LSB
OPTO CV-DAC and CC-DAC				
R _{FB_VBUS_PWR}	VBUS_PWR Divider Resistance	R _{UP} + R _{DWN} on VBUS_PWR pin	2	MΩ
K _V	Ratio from VBUS_PWR to the input of ADC.	Ratio from VBUS_PWR to the input of ADC	1/10	



N _{DAC_CV}	CV loop V _{REF} resolution		10			Bits
V _{BUS_PWR_ADJ_RANGE}	VBUS_PWR adjust range ^[1]		2	22.46		V
V _{BUS_PWR_STEP_VOLT}	VBUS_PWR adjust voltage per step		20			mV
V _{DAC_ZERO_VOLT}	VBUS_PWR voltage at VDAC code = 0 ^[1]		1960	2000	2040	mV
N _{DAC_CC}	CC loop I _{REF} resolution		10			Bits
V _{REF_IDAC}	IDAC reference voltage		1.2			V
V _{REF_IDAC_STEP}	IDAC step voltage		1.172			mV
I _{REG_STEP}	Current regulation per step	RSNS=5mΩ, GSNS = 40 ×	5.86			mA
I _{OPTO}	OPTO control loop current		2			mA
FB CV-DAC AND CC-DAC						
V _{FB_VDAC_REF}	FB regulator VDAC reference		1.024			V
V _{FB_VDAC_STEP}	FB VDAC step voltage		1			mV
V _{BUS_PWR_STEP_VOLT_FB}	VBUS_PWR adjust voltage per step via FB	R _{UP} = 20×R _{FBS}	20			mV
V _{DCDC_IDAC_REF}	DCDC regulator IDAC reference		2.244	2.248	2.252	mV
I _{COMP}	Current capability from COMP pin		-4	2		μA
VBUS OVP and UVP						
V _{BUS_PWR_OVP}	VBUS_PWR OVP rising threshold	fb_sel_uvp_th = 01b	112	115	118	%
		fb_sel_uvp_th = 10b	117	120	123	%
		fb_sel_uvp_th = 11b	122	125	128	%
V _{BUS_OVP_HYS}	VBUS_PWR OVP threshold hysteresis, respect to VDAC setting		0		5	%
t _{VBUS_PWR_OVP}	VBUS_PWR over-voltage deglitch time	ovp_dgl_sel = 0	4			μs
		ovp_dgl_sel = 1	40			μs
V _{BUS_PWR_UVP}	VBUS_PWR UVP falling threshold	fb_sel_uvp_th = 01b	73	75	77	%
		fb_sel_uvp_th = 10b	82	85	88	%
		fb_sel_uvp_th = 11b	91	95	99	%
V _{BUS_UVP_HYS}	VBUS_PWR UVP threshold hysteresis, respect to VDAC setting		0		3	%
t _{VBUS_PWR_UVP}	UVP deglitch time	uvp_dgl_sel = 0	4			μs
		uvp_dgl_sel = 1	40			μs
V _{BUS_SCP_TH}	VBUS_PWR SCP threshold		2.8	2.9		V
NTC SETTING						
V _{NTC_OPEN}	NTC1/NTC2 open voltage		2.248			V
I _{NTC}	NTC pin bias current.	pwr_ntc_sel = 11b	97	100	103	μA
		pwr_ntc_sel = 10b	18.8	20	21.2	μA
		pwr_ntc_sel = 01b	4		4.3	μA
TYPE-C/ PD PROTOCOLS						



I _{CC_80μA}	CC1/2 pull up current	CSRC_I = 00b	64	80	96	μA
I _{CC_180μA}	CC1/2 pull up current	CSRC_I = 01b	165.6	180	194.4	μA
I _{CC_330μA}	CC1/2 pull up current	CSRC_I = 10b	303.6	330	356.4	μA
R _{CC_open}	CC1/2 open impedance	CC1/2 in disable status	126			kΩ
V _{CC_0P2_th_src}	CC1/2 0.2V comparison threshold	CC1/2 as source	0.15	0.2	0.25	V
V _{CC_0P4_th_src}	CC1/2 0.4V comparison threshold	CC1/2 as source	0.35	0.4	0.45	V
V _{CC_0P66_th_src}	CC1/2 0.66V comparison threshold	CC1/2 as source	0.61	0.66	0.7	V
V _{CC_0P8_th_src}	CC1/2 0.8V comparison threshold	CC1/2 as source	0.75	0.8	0.85	V
V _{CC_1P23_th_src}	CC1/2 1.23V comparison threshold	CC1/2 as source	1.18	1.23	1.28	V
V _{CC_1P6_th_src}	CC1/2 1.6V comparison threshold	CC1/2 as source	1.5	1.6	1.65	V
V _{CC_2P6_th_src}	CC1/2 2.6V comparison threshold	CC1/2 as source	2.45	2.6	2.75	V
V _{TH_CCOVP_RISING}	CCx OVP detection	CCOVP rising threshold		7.2		V
V _{TH_CCOVP_FALLING}	CCx OVP release	CCOVP falling threshold		7.0		V
Z _{Driver}	PD data Tx output impedance		33		75	Ω
V _{Swing}	High level voltage for CC PD data		1.05	1.125	1.2	V
VCONN SWITCH						
V _{VCONN}	VCONN input voltage		3		5.5	V
R _{VCONN}	VCONN switch on resistance	LV ≥ 3.3V			40	Ω
I _{VCONN}	VCONN current capability	VBUS_PWR = 5V		50		mA
I _{VCONN_OCP}	VCONN over current	Rising threshold		70		mA
DPDM PROTOCOL INTERFACES						
R _{SHORT}	DP DM short resistance	VBUS_PWR = 5V ~ 21V			40	Ω
V _{3.3V}	DPDM 3.3V buffer output voltage	VBUS_PWR = 5V ~ 21V	3.2	3.3	3.4	V
V _{2.7V}	DPDM 2.7V buffer output voltage	VBUS_PWR = 5V ~ 21V	2.6	2.7	2.8	V
V _{1.96V}	DPDM 1.96V buffer output voltage	VBUS_PWR = 5V ~ 21V	1.9	2	2.1	V
V _{TH_3V}	VTH3V comparator threshold at DPDM pin	VBUS_PWR = 5V ~ 21V	2.9	3	3.1	V
V _{TH_2.2V}	VTH2.2V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	2.1	2.2	2.3	V
V _{TH_1.35V}	VTH1.35V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	1.25	1.35	1.45	V
V _{TH_0.425V}	VTH0.425V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	0.35	0.425	0.5	V
V _{TH_0.325V}	VTH0.325V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	0.25	0.325	0.4	V
R _{OUT_30k}	Output resistance of DP or DM buffer		24	30	37.5	kΩ



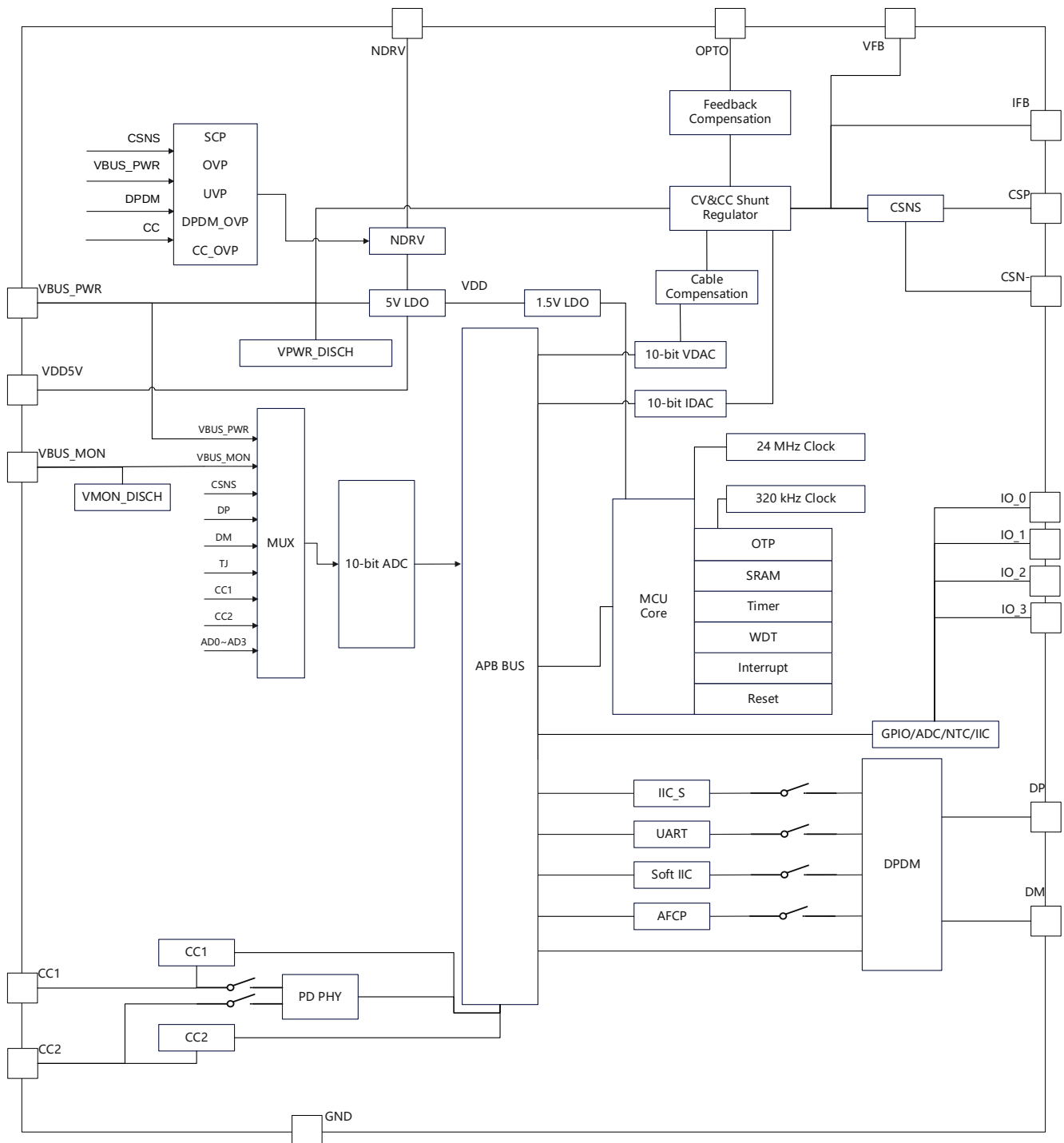
I _{OUT_OP6V}	0.6V current capability, sink/BC1.2, DP/DM		250			μA
R _{DP/DM_DWN}	DP/DM pull down resistance	source/HVDCP, DM	15	20	25	kΩ
R _{DP/DM_LKG}	DP/DM leakage		300	500	800	kΩ
V _{DATA_HIGH}	DP/DM data output high voltage	Slave data output high, VBUS ≥ 3.3V, data_high_sel = 0	3	3.3	3.6	V
		Slave data output high, VBUS ≥ 3.3V, data_high_sel = 1	1.6	1.8	2.0	V
V _{DATA_LOW}	DP/DM data output low voltage	Slave data output low			0.2	V
I _{OH_DM_3P3V}	3.3V current capability, DM		5			mA
V _{IH_TH}	DPDM input data rising threshold	dpdm_in_refh_sel = 000b	0.7	0.8	0.86	V
		dpdm_in_refh_sel = 001b	1.1	1.2	1.3	V
		dpdm_in_refh_sel = 010b	1.3	1.4	1.5	V
		dpdm_in_refh_sel = 011b	1.7	1.8	1.9	V
		dpdm_in_refh_sel = 100b	1.8	1.9	2.0	V
		dpdm_in_refh_sel = 101b	2.0	2.1	2.2	V
		dpdm_in_refh_sel = 110b	2.2	2.3	2.4	V
		dpdm_in_refh_sel = 111b	2.4	2.5	2.6	V
V _{IL_TH}	DPDM input data falling threshold	dpdm_in_refl_sel = 000b	0.5	0.6	0.7	V
		dpdm_in_refl_sel = 001b	0.9	1	1.1	V
		dpdm_in_refl_sel = 010b	1	1.1	1.2	V
		dpdm_in_refl_sel = 011b	1.4	1.5	1.6	V
		dpdm_in_refl_sel = 100b	1.7	1.8	1.9	V
		dpdm_in_refl_sel = 101b	1.8	1.9	2.0	V
		dpdm_in_refl_sel = 110b	2.1	2.2	2.3	V
		dpdm_in_refl_sel = 111b	2.2	2.3	2.4	V
V _{TH_DPDMOV}	Source/DPDM OVP detection	DPDMOV rising threshold	4.4	4.75	4.95	V
t _{DPDM_OVP}	DPDM over-voltage deglitch time	dpdm_ovp_dgl_sel = 0		4		μs
		dpdm_ovp_dgl_sel = 1		40		μs
t _{DATA_RISING}	Data output from low to high			0.3	1	μs
t _{DATA_FALLING}	Data output from high to low			0.3	1	μs
t _{UI}	Unit interval time		144	160	176	μs
t _{PING_ST}	Adapter transmit slave ping duration time		2304	2560	2816	μs
t _{PING_SR}	Adapter receive master ping duration		2304	2560	2816	μs
t _{PSR} /t _{PST}	Ping received and transmit ratio		99	100	101	%
t _{AD}	Terminal attach deglitch		450	500	550	μs
t _{DD}	Terminal detach deglitch	dp_to_set = 00b	0.475	0.5	0.525	ms
		dp_to_set = 01b	0.95	1	1.05	ms
		dp_to_set = 10b	1.9	2	2.1	ms



		dp_to_set = 11b	3.8	4	4.2	ms
SYSTEM CLOCK						
f _{HF_OSC}	High frequency OSC		22.8	24	25.2	MHz
f _{LF_OSC}	Low frequency OSC			320		kHz
GPIO PINS						
V _{IH_GPIO}	Input voltage high threshold	VBUS_PWR = 3.3V ~ 21V, measured as VIO		0.7		V
V _{IL_GPIO}	Input voltage low threshold	VBUS_PWR = 3.3V ~ 21V, measured as VIO	0.3			V
V _{OH_GPIO}	Output high voltage	VBUS_PWR = 6V, apply 4mA sink current from IO pin to GND externally	4.5			V
V _{OL_GPIO}	Output low voltage	VBUS_PWR = 6V, apply 10mA source current from VDD_5V to IO pin externally		0.5		V
V _{PU}	Pull up resistor value at GPIO pin	VBUS_PWR = 3.3V ~ 21V		5.1		kΩ
V _{PD}	Pull down resistor value at GPIO pin	VBUS_PWR = 3.3V ~ 21V		5.1		kΩ
THERMAL SHUTDOWN						
T _{TH}	Thermal shutdown threshold (LDO), SC2166Q will reset when junction temperature is over T _{TH}	T _{TH} rising	160	180		°C
T _{TH_HYS}	Over temperature hysteresis	T _J falling below T _{TH} - T _{TH_HYS} , SC2166Q will restart.		15		°C

(1). It is recommended to set VDAC code at least 60 at 3.2V on VBUS.

8 Functional Block Diagram



9 Detailed Description

9.1 Power Supply

SC2166Q contains an internal high-voltage LDO which supports wide input range. VBUS_PWR is the power supply input pin of internal LDO. It converts voltage on VBUS_PWR to 5V and supplies internal modules.

For applications, VBUS_MON should be connected to the VBUS on USB port, and VBUS_PWR should be connected to internal VBUS node. It is recommended to place a 1 μ F ceramic capacitor close to the VDD5V pin.

9.2 NMOS Gate Driver

The Type-C and USB PD specifications require the VBUS isolation implementation for the Type-C port. SC2166Q provides NMOS gate driver to control the isolation MOSFET between the internal VBUS node and the Type-C port. The gate driver is controlled by register. The voltage VGS is clamp to 7V. The IC provides 4 different pull-up capabilities from 20k Ω to 200k Ω to suit different MOSFETs.

9.3 VBUS Discharging Paths

The IC integrates VBUS discharging paths from VBUS_MON and VBUS_PWR pins to ground respectively. These paths help drain the residual charge on the bulk capacitors to meet the application requirements. The typical equivalent impedance of discharge path on VBUS_MON pin and VBUS_A pin are 1k Ω . Discharging path on VBUS_PWR pin is a constant current from 45mA to 150mA, which can be configured by registers. These discharge paths are activated at detachment or a lower VBUS voltage transition occurring. All discharging paths can be controlled by firmware.

9.4 ADC

In the Type-C, USB PD or other quick charge applications, it is necessary to monitor the VBUS voltage and current. The SC2166Q integrates a 10-bit Successive Approximation Analog to Digital Converter (SAR ADC) with a reference voltage of 2.248V at a sampling rate from 5kHz to 50kHz.

The ADC supports 10-channel input as below. For VBUS_MON VBUS_PWR, an internal ratio of 1/10 is built in. The ratio of DPDM and VDD5V channel is 1/4.

The Internal Temperature Sense (ITS) unit converts the temperature to voltage. Users can get the die temperature by sampling the channel. The ratio of voltage to temperature is 2.819mV/ $^{\circ}$ C and the output of ITS is 733.94mV at the temperature of 27 $^{\circ}$ C.

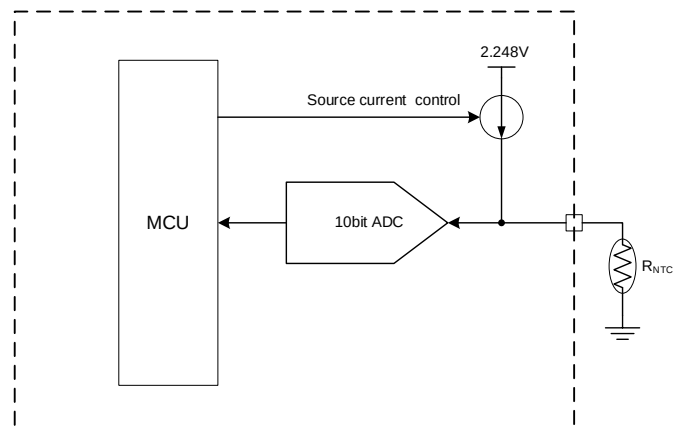
Table 1. ADC input channel

ADC_CH_SEL[3:0]	Input Signal	Note
0000	1/10 x VBUS_PWR	With 1/10 internal divider
0001	1/10 x VBUS_MON	With 1/10 internal divider
0010	VRSNS $\times$ 40 or 20	The gain of current sense amplifier can be set as 40 or 20
0011	1/4 x DPDM or CC1/CC2	With 1/4 internal divider
0100	1/4 x VDD5V	With 1/4 internal divider
0101	AD0	
0110	AD1	
0111	AD2	
1000	AD3	
1001	ITS	Internal temperature sense

9.5 NTC Setting

SC2166Q provides NTC sense function. The NTC pin outputs a bias current and detects the voltage to calculate the resistance on this pin.

As shown in the figure, NTC pin source current on the R_{NTC}, and the voltage can be sampled by 10-bit ADC. Source current can be configured as 100 μ A, 20 μ A or 4 μ A. The over-temperature protection will be triggered if the voltage is below an over-temperature protection threshold for a programmed time delay.



9.6 CV CC Control Loop for ACDC

SC2166Q contains 2 DACs and 2 error amplifiers for OPTO pin to regulate output voltage and current. For voltage regulation, VDAC is a 10-bit DAC with internal 2.048V reference voltage. SC2166Q supports at least 20mV per



step for VBUS output voltage regulation. The adjust time ranges from 20 μ s to 250 μ s which can be set by firmware.

VBUS output regulation should be as the following equation.

$$V_{REG} = 2 + VDAC\ code * 0.020$$

For example, if VDAC code = 150, the output voltage V_{REG} = 5V.

SC2166Q integrates a high side current sense amplifier for constant current regulation and output current sampling. The gain of the amplifier can be configured as 40 or 20. For 3mohm application, SC2166Q supports up to 8A constant current regulation.

The IDAC is 10-bit with 1.2V reference. The regulation current (I_{REG}) is decided by IDAC code, sense resistance (R_{SNS}) and the gain of current sense amplifier (G_{SNS}). The relationship between these parameters should be as follows.

$$I_{REG} = \frac{IDAC\ code \times 1.2}{(2^{10} \times R_{SNS} \times G_{SNS})}$$

For example, if R_{SNS} = 5m Ω , G_{SNS} = 40, IDAC code = 512, I_{REG} = 3A.

9.7 VDRAIN Detection

VDRAIN is a low voltage pin connected to the drain of SR MOSFET through divider resistor to detect AC voltage and load.

9.8 DPDM Interface

The SC2166Q contains a DPDM interface which can be configured as discharging out port (provider). The DPDM interface is available for USB-A port applications or Type-C port applications. It supports Apple-2.4A, BC1.2 DCP, HVDCP, FCP, SCP, VOOC UFCS and other proprietary fast charging protocols.

All of the DPDM pins can be configured flexible for different applications. SC2166Q supports Apple-2.4A mode, which broadcasts 2.7V voltage on both DP and DM pins with 30kohm output impedance. If 2.4A mode advertisement on DPDM is enabled, it is recommended that VBUS should be able to supply at least 2.4A of current.

SC2166Q can be also configured as a dedicated charging port (DCP), which complies with the BC1.2 specification. When DCP mode is enabled, SC2166Q shorts DP and DM pin through a 20ohm resistor.

SC2166Q supports HVDCP mode for some high voltage protocols. Under HVDCP mode, DP and DM can check the voltage by internal comparators or detect some proprietary

fast charging protocols such as SCP, VOOC, UFCS, and I2C.

9.9 CC Interface

The IC can be configured as source only. It presents Rp on CC1 and CC2. CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable. Once an attachment is detected, the IC will apply VBUS voltage and broadcast source capabilities.

Current source presented on CC can be configured to 330 μ A, 180 μ A and 80 μ A. Each of the CC pins contains comparators to decide CC_RD and CC_RA attachment.

9.9.1 VCONN Switch

SC2166Q features a more than 50mA VCONN power with a fixed Overcurrent Protection (OCP) of 70mA.

The IC supports electronically marked cables assembly for more than 3A power delivery. By default, passive cables support up to 3A. The IC can check the cable types through internal CC comparators. If an e-marker cable is detected, the IC supplies the cable with VCONN and communicates with it to check the cable current ratings. As a consequence, source power supply advertises any PDO if cable is identified as able to sustain such current. Refer to PD specification, the IC supports up to 5A power delivery application.

When VCONN switch is turned on, SC2166Q will continuously monitor current on CC pin. If VCONN output current is above 70mA, VCONN over-current flag will be set, and VCONN switch can be turned off by firmware. SC2166Q supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

When VCONN switch is turned on, the IC will continuously monitor current on CC pin. VCONN over-current flag will be set if VCONN output current is above 70mA. Once VCONN OCP is triggered, VCONN switch can be turned off by firmware. The IC supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

9.10 USB PD Protocol

The IC provides USB PD physical layer for PD protocols communication. The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.2 standard. Once the insertion direction of Type-C port is detected by CC comparator, the IC can select either CC1 or CC2



channels to send and receive PD packets. All processes of PD communication are controlled by firmware.

9.11 Protections

9.11.1 OVP, UVP and SCP

The IC monitors the VBUS voltage in real time. Once the voltage exceeds the OVP threshold for a programmed time, the flag is set and an interrupt is generated automatically. It also monitors VBUS voltage for under-voltage protection (UVP). Once VBUS voltage drops below UVP threshold for a programmed time, the UVP flag is set and an interrupt is generated. Once voltage on VBUS drops below 3.2V, Short-Circuit Protection (SCP) will be triggered. An interrupt will be generated and the SCP flag will be set.

The OVP threshold, UVP threshold and the detection deglitch time can be configured through registers. The OVP threshold can be configured as 115%, 120% and 125% of the setting voltage, while UVP threshold can be configured as 75%, 85% and 95%. The deglitch time can be configured as 4 μ s or 40 μ s.

9.11.2 Protection for DPDM

The IC supports over-voltage protection of the DP/DM pin. Once it detects any of the DP and DM voltage exceeding 4.75V, the IC will report the over-voltage status and generate an interrupt.

9.11.3 Protection for CC

SC2166Q continuously monitors CC voltage. Once CC over-voltage detected, SC2166Q will launch CC Over-Voltage Protection (CC OVP). The CCOVP flag will be set if the voltage on CC1 or CC2 is over 7.5V and will be clear after voltage falls below 7V. The OVP interrupt will be triggered if interrupt enable control bit is set.

If each of the protections including OVP, UVP, SCP is detected, SC2166Q can drive isolation MOS off by register setting.

9.12 MCU Controller

9.12.1 Clock

The SC2166Q integrates a 24MHz high frequency clock and a 320kHz low frequency clock. Under normal working condition, high frequency and low frequency clocks work simultaneously. When in sleep mode, only the 320kHz clock works to reduce the power consumption.

9.12.2 Modes

The SC2166Q supports three operating modes: active mode, standby mode and sleep mode. In active mode, each

function module operates normally. In standby mode, MCU stops, each module can be turned on and MCU restarts once any of the interrupts is triggered. In sleep mode, only the 320kHz low frequency clock works, and all other functions are turned off. The quiescent current can be as low as 200 μ A in sleep mode.

After entering sleep mode, the system can be awakened by interruptions, including GPIO interrupts, DPDM interrupts, watchdog interrupts, and the timer interrupts with the 320kHz clock source.

9.12.3 GPIO

GPIO has input/output direction settings, internal pull-up/pull-down resistor settings, and interrupt edge settings.

9.12.4 Interrupts

The IC supports various interrupts, including Timer0 interrupt, Timer1 interrupt, ADC interrupt, I2C interrupts, DPDM interrupts, analog interrupts, WDT interrupt, I/O interrupt.

9.12.5 Timer

The SC2166Q integrates two general timers. The clock source can be configured as 24MHz high frequency oscillator or 320kHz low frequency oscillator.

The timer0 is a count-down counter. Counting cycle and clock can be configured by registers. Overflow flag will be set and interrupt will be generated once timer0 counts to the end of cycle.

Timer1 is a count-up counter. The counting cycle and clock can be configured by registers. Overflow flag will be set and an interrupt will be generated once timer1 counts to CCR0 register value. In addition, timer1 could be configured as a PWM output. By default, when timer1 counter counts to CCR0, TMR1 output low. When timer1 counts to CCR1, TMR2 output high. The period and duty of PWM output is decided by the value of CCR0 and CCR1.

9.12.6 UART

UART can support Tx function and Rx function. The baud rate can be set from 9600 bit/s to 921600 bit/s.

9.12.7 I2C

The SC2166Q contains two I2C interface. One is controlled by hardware and the other is software controlled. For the software controlled I2C, it can be configured as a master interface or a slave interface.

**9.12.8 Watchdog**

The watchdog is a 16-bit counter with 1000Hz clock source (divided from 320kHz clock). Once the watchdog is enabled, the watchdog counter starts with the value of zero and counts up. The control register WDT_CTRL can be used to select whether an interrupt or reset signal, or both occurs when the counter overflows (counting to WDT_INIT).

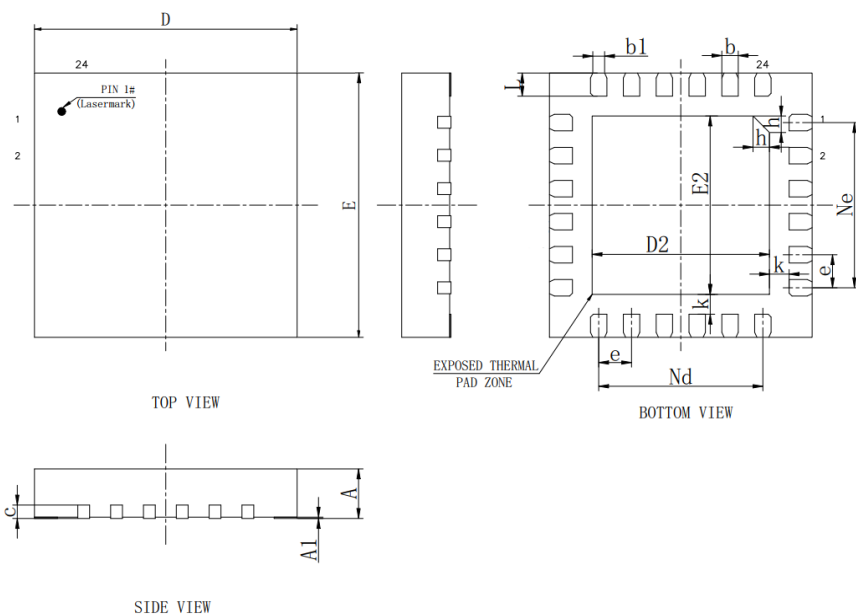
9.12.9 Programming

The SC2166Q can be programmed through I2C interface.



MECHANICAL DATA

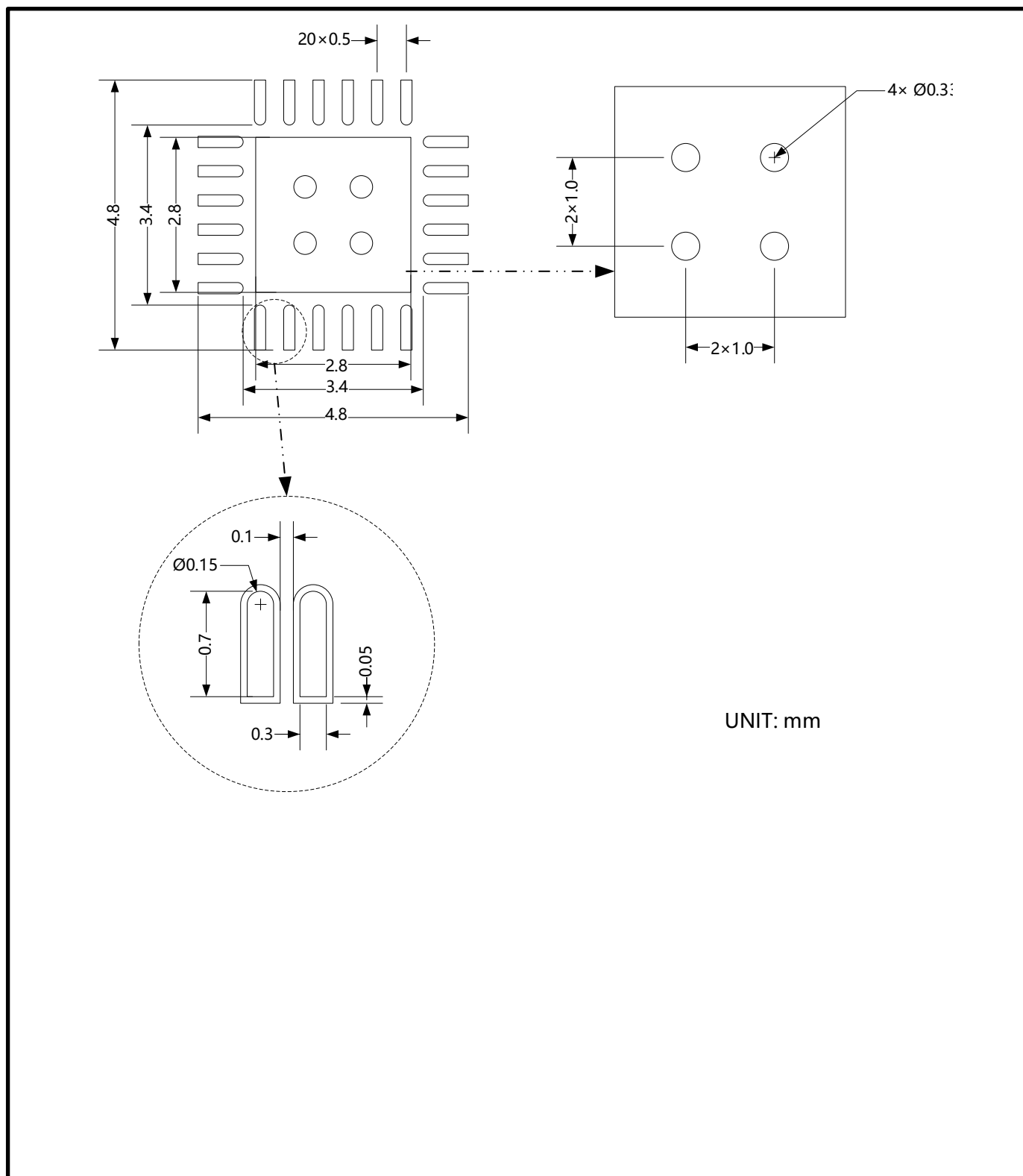
QFN 4mm × 4mm × 0.75mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
L	0.30	0.35	0.40
h	0.20	0.25	0.30
k	0.30REF		



Board Layout Example





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