

POWERQUARX® Product Family

SC3107C High Performance All-In-One Flyback Converter IC

1 Descriptions

SC3107C is a high performance, multi-mode flyback PWM converter that integrates a GaN switch, primary controller, synchronous rectification controller, and protocol controller in a single IC package. SC-PQLINK® eliminates optocoupler by using innovative and safety-approved isolation technology for secondary side regulation. SC3107C dramatically simplifies the design and manufacturing of power supply designs for portable devices.

SC3107C provides an adaptive switching frequency fold-back and multi-mode operation across entire load range to achieve higher efficiency. At no load, the IC will operate in burst mode to reduce power consumption. SC3107C offers comprehensive protections to prevent the circuit from damage under abnormal conditions.

A high-performance protocol controller is integrated in SC3107C as well. It complies with the latest Type-C and PD standards, supports the most popular high voltage fast charge protocols with DPDM interface.

2 Features

- Integrated 700V, 240mOhm GaN switch
- Multi-mode operation with ZVS support
- Integrated SC-PQLINK® to eliminate optocoupler with 5000V reinforced isolation
- 100% HIPOT testing in production
- Internal soft start

- Frequency jitter for EMI improvement
- Smart frequency fold-back
- Internal over-temperature protection
- Comprehensive Protections
 - VDD Over voltage protection
 - Cycle by cycle current limit
 - Output under voltage protection (UVP)
 - Output over voltage protection (OVP)
 - Output short protection
 - Over current protection (OCP)
 - Brown in/out with auto-recovery
 - DPDM/CC OVP
- Integrated fast charge protocol controller
 - Integrated 32bit high performance MCU core
 - 32k-Byte OTP and 2.5k-Byte SRAM
 - PD 3.2 SPR PPS and AVS supported
 - Various DPDM proprietary protocols supported (UFCS, etc.)
 - VCCON supported for E-Marker cable
 - Dual DACs for voltage and current regulation
 - Integrated high side NMOS gate driver
 - Support NTC temperature sense
- Safety and regulatory approvals
 - UL – UL 1577
 - TUV – EN IEC 62368-1
 - CQC – GB 4943.1

3 Applications

- AC-DC adapters for portable devices



4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3107CXSGER	SSOP38	12.8mm x 10.3mm x 2.5mm

SC3107CXSGER Functional Table

ORDER NUMBER	SC3107C	SC3107CM	SC3107CH
Maximum Frequency	109KHZ	132KHz	175KHz
Protections	A		
Line Compensation	Y	/	/

A: Auto-recovery;

Y: The feature is enabled

/ : The feature is not enabled

UL 1577 Recognition Ratings

Parameter	Value
Isolation Voltage	5000 Vrms



5 Typical Application Circuit

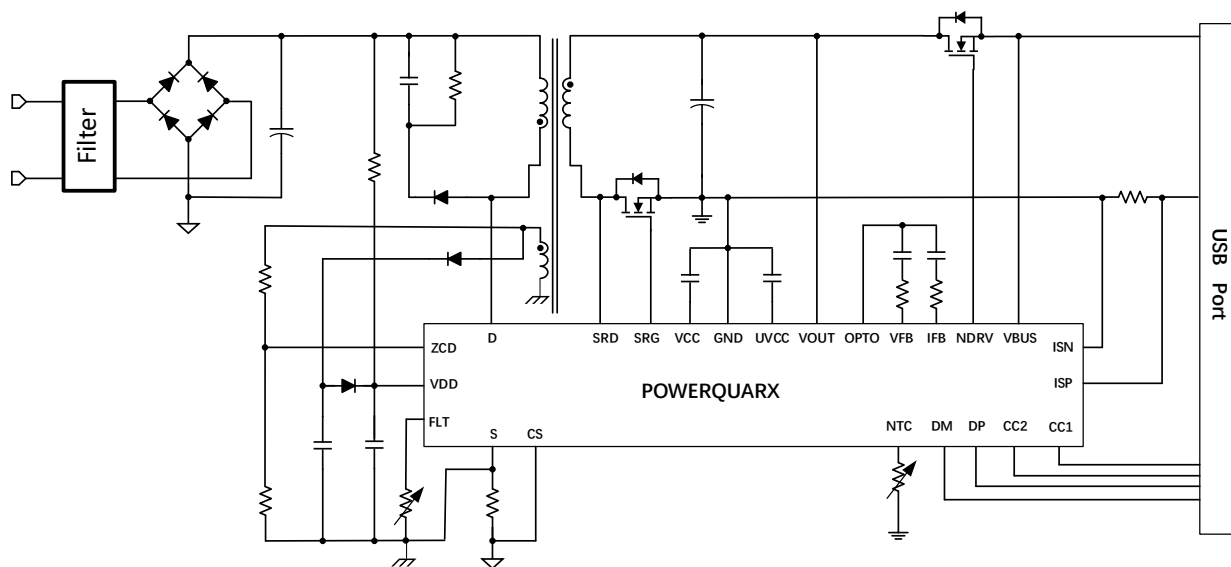


Fig. 1 Typical application circuit

6 Terminal Configuration and Functions

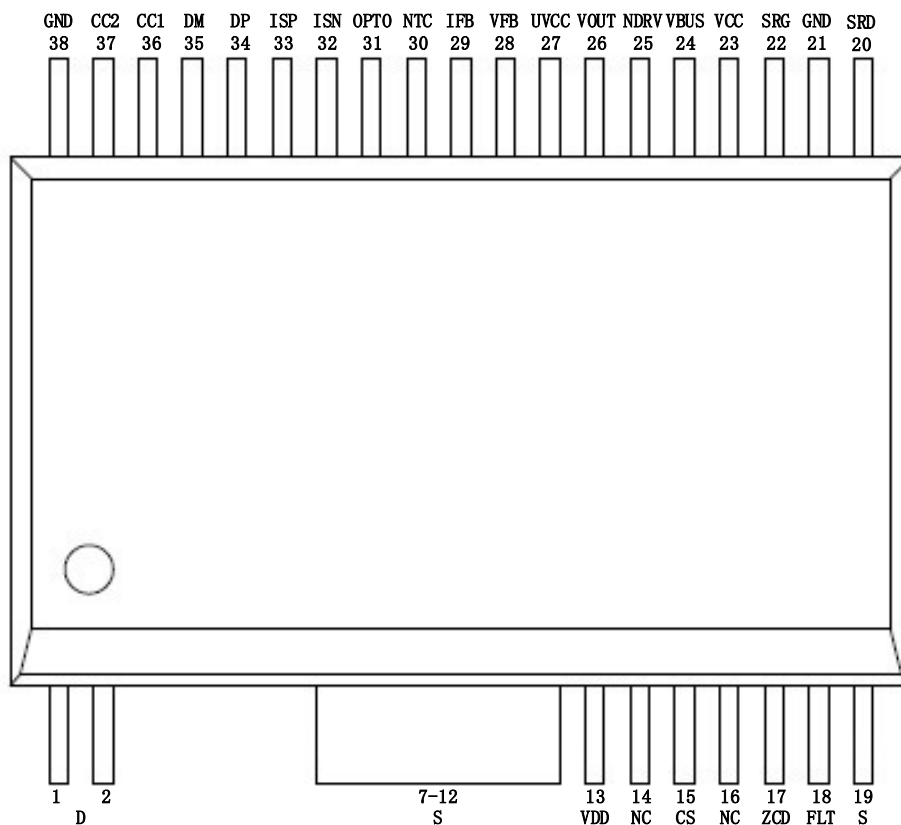


Fig. 2 Top View



TERMINAL		I/O	DESCRIPTION
SC3107C	NAME		
Primary			
1,2	D	PWR	Internal GaN switch drain terminal
7-12,19	S	PWR	Internal GaN switch source terminal. This pin connects to a current-sense resistor as the power ground
13	VDD	PWR	Primary power supply
15	CS	I	Current sense. This pin sense the GaN current for Peak-Current-Mode control
17	ZCD	I	Voltage sense. This pin detects the output voltage information and clamp current for line voltage information based on the auxiliary winding
18	FLT	O	Fault pin. This pin is typically connected to an NTC resistor
Secondary			
20	SRD	I	SR MOSFET drain voltage sense and provide power for VCC when VOUT is low
21,38	GND	PWR	Secondary ground
22	SRG	O	SR MOSFET gate driver
23	VCC	PWR	Secondary power supply
24	VBUS	I	Connected to the VBUS line of the USB Type-C port. It can discharge the output capacitor and can be used to sense VBUS voltage of Type-C port.
25	NDRV	O	Load switch (NMOS) driver.
26	VOUT	I	Output voltage sense and provide power for VCC and UVCC. It supports more than 100mA discharging capability for the output capacitor.
27	UVCC	PWR	Protocol controller power supply
28	VFB	I	Constant voltage loop EA compensation pin
29	IFB	I	Constant current loop EA compensation pin
30	NTC	O	Remote thermal sensor connection node for external temperature monitoring
31	OPTO	I	Output for EA compensation
32	ISN	I	Negative input of the internal current sense amplifier. Connect to the low side current sense resistor
33	ISP	I	Positive input of the internal current sense amplifier. Connect to the high side current sense resistor
34	DP	I/O	DM line of fast charging interface
35	DM	I/O	DP line of fast charging interface
36	CC1	I/O	Type-C configure channel1. It also supports VCONN output
37	CC2	I/O	Type-C configure channel2. It also supports VCONN output



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

Item	Description	MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	D to S		700	V
	VDD to S	-0.3	88	V
	Other Primary Pins to S	-0.3	6.5	V
	SRD to GND	-1	105	V
	SRG, VCC to GND	-0.3	9	V
	NDRV to GND	-0.3	33	V
	VBUS, VOUT, CC1, CC2 to GND	-0.3	26	V
	Other Secondary Pins to GND ⁽³⁾	-0.3	5.5	V
Temperature Range	Operating Junction, T _j	-40	150	°C
	Storage temperature range, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) DPDMx pins should add 5.5V clamp

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
VDD to S	VDD voltage reference to S	10		79	V
SRD to GND	SR MOSFET drain voltage reference to GND	-0.7		100	V
VBUS, VOUT to GND	Output voltage reference to GND	3.3		24	V
T _j	Operating junction temperature	-40		125	°C

7.4 Thermal Information

Thermal Resistance ⁽¹⁾		SSOP38	UNIT
Θ _{JA}	Junction to ambient thermal resistance	40	°C/W
Θ _{JC}	Junction to case (top) thermal resistance	17.55	°C/W

(1) Measured on JE5D51-7, 4-layer PCB.



7.5 Electrical Characteristics

VDD=20V, VCC=8V, UVCC=5V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Primary Voltage Supply (VDD)						
V _{DDON}	VDD on threshold voltage		19.6			V
V _{DDOFF}	VDD off threshold voltage		7.4	7.8	8.3	V
V _{DDOVP}	VDD over voltage protection threshold		79	81.5	84	V
I _{VDDST}	VDD start up current	V _{VDD} < V _{DDON} -1V	6		15	uA
T _{FLTRST}	Fault reset timer		1.2			S
I _{VDD}	Quiescent current	No switching	220			uA
	Operating current	F _{SW} = F _{SWMAX}			2	mA
Primary Fault Protection (FLT)						
V _{FLT}	Fault trigger threshold		0.46	0.49	0.52	V
I _{FLT}	Source current for FLT bias		84	100	116	uA
T _{FLTDE}	Fault debounce Time		560			uS
Current Sense (CS)						
F _{SW_P}	Switch frequency for primary control		20	25	30	KHz
V _{CSLIMIT}	Cycle by cycle current limit		0.2	0.21	0.22	V
T _{LEBCBC}	Leading edge blanking time for cycle by cycle current Limit		370			nS
V _{CSSSCP}	Current limit for secondary rectifier short protection		0.275			V
T _{LEBSSCP}	Leading edge blanking time for secondary rectifier short protection		190			nS
V _{CSSLOPE}	Slope compensation		9			mV/μS
I _{CSLC}	CS leakage current for line voltage compensation		28			uA
T _{ONMAX}	Maximum on Time		10.8			uS
V _{CSMIN}	CS minimum voltage		0.067			V
ΔV _{CS}	CS jitter		±6			%
N _{JIT}	CS jitter cycle		480			cycles
Zero Current Detection (ZCD)						
V _{ZCDOVP}	ZCD OVP		3.05	3.18	3.31	V
V _{ZCDCLAMP}	ZCD clamp voltage	I _{ZCDCLAMP} = 1.0mA	-135			mV
I _{ZCDBI}	Line voltage brown in clamp current threshold in ZCD		144	160	176	uA
I _{ZCDBO}	Line voltage brown out clamp current threshold in ZCD		153			uA
T _{ZCDBO}	ZCD brown out debounce time		64			mS
GaN Power Device Drain (D)						
V _{(BR)DS}	Drain-source blocking voltage		700			V
I _{DSS}	Drain-source leakage current		5			uA
R _{DSON}	Drain-source on-state resistance	T _J =25℃	165		240	mOhm
		T _J =150℃	360			mOhm
Primary Internal Over Temperature Protection						



OTP _P	Primary shutdown temperature		160	°C
OTP _{PHYS}	Primary temperature hysteresis		20	°C
Secondary Voltage Supply (VCC)				
V _{CCON}	VCC on threshold voltage		4.5	V
V _{CCOFF}	VCC off threshold voltage		2.85 3 3.15	V
V _{CCClamp}	VCC clamping Voltage	V _{OUT} >8V	7.5 8 8.5	V
I _{VCC}	Quiescent current	No Switching	255	uA
	Operating current	F _{SW} = F _{SWMAX} , C _{LOAD} =2nF, VCC=5V	2.5	mA
I _{CHG_OUT}	V _{OUT} charge current for VCC	V _{OUT} =5V	19	mA
Synchronous Rectification (SRD & SRG)				
I _{CHG_SR}	SRD charge current for VCC		70	mA
V _{SRON}	SR turn on threshold		-130	mV
V _{SROFF}	SR turn off threshold		-10 0	mV
V _{SRMON}	SRD monitor threshold		-35	mV
T _{SRMOT}	SR minimum on time		1250	nS
V _{SRGL}	SRG low level voltage	SRG 100mA Bias Current	0.2	V
V _{SRGH}	SRG high level voltage		VCC	V
R _{SRG_SO}	SRG source resistor		6	Ohm
R _{SRG_SI}	SRG sink resistor		1	Ohm
Secondary Timing				
F _{SWMAX}	Maximum switching frequency	SC3107C	102.5 109 115.5	kHz
		SC3107CM	124 132 140	
		SC3107CH	165 175 185	
F _{SWMAX_CCM}	Maximum switching frequency for CCM	SC3107C	78 83 88	kHz
		SC3107CM	94 100 106	
		SC3107CH	127 135 143	
F _{SWMIN}	Minimum switching frequency		20 25	kHz
T _{ZVSON_MAX}	Maximum SR ZVS on time		1.35	uS
Secondary Internal Over-Temperature Protection				
OTP _S	Secondary OTP temperature		160	°C
OTP _{SHYS}	Secondary OTP hysteresis		20	°C
Protocol Controller				
V _{OUT_RANGE}	V _{out} range		2.9 22	V
V _{OUT_TURNON}	V _{out} turn on threshold		2.9 3	V
I _{QAVR}	Average quiescent current	V _{OUT} = 5V~21V, control loop is enabled and PD is enabled, 100ms sleep mode, 2ms active mode toggle	2 3	mA
V _{UVCC}	LDO regulation voltage	V _{OUT} = 5.5V~21V	5	V
V _{UVCC_DROP}	LDO dropout voltage	V _{OUT} -V _{UVCC} , I _{UVCC} =50mA	250	mV
I _{UVCC_LIMIT}	LDO current limit	V _{OUT} = 5V	100	mA



IdIS_VOUT	Discharging current at VOUT	Register Programmable	45	165		mA
V_NDRV	Load switch driving voltage		4.5	5		V
Ki	Ratio from current sense to ADC/comparators		19.8	20	20.2	
			39.6	40	40.4	
Kv	Ratio from VOUT to the input of ADC		1/10			
V_LINE_COMP_MAX	Max VBUS output voltage compensation		200			mV
T_SLEW	VDAC slew rate		250			uS/step
IoPTO	OPTO control loop current		2			mA
V_ADC_REF	Reference voltage for ADC		2.253			V
N_ADC	Resolution of ADC		10			Bits
R_SHORT	DP DM short resistance	UVCC = 3.3-5V	10	40		Ohm
Icc_80uA	CC1 CC2 pull up current	UVCC = 3.3V, Tj = -25°C	64	80	96	uA
Icc_180uA	CC1 CC2 pull up current	UVCC = 3.3V, Tj = -25°C	165.6	180	194.4	uA
Icc_330uA	CC1 CC2 pull up current	UVCC = 3.3V, Tj = -25°C	303.6	330	356.4	uA
V_CONN	VCONN input voltage		3	5.5		V
F_HF_OSC	High frequency oscillator	Tj = -40-85°C	22.8	24	25.2	MHz
F_LF_OSC	Low frequency oscillator		320			kHz
OTP_M	OTP temperature for protocol controller		180			°C
OTP_MHYS	OTP hysteresis for protocol controller		15			°C



8 Functional Block Diagram

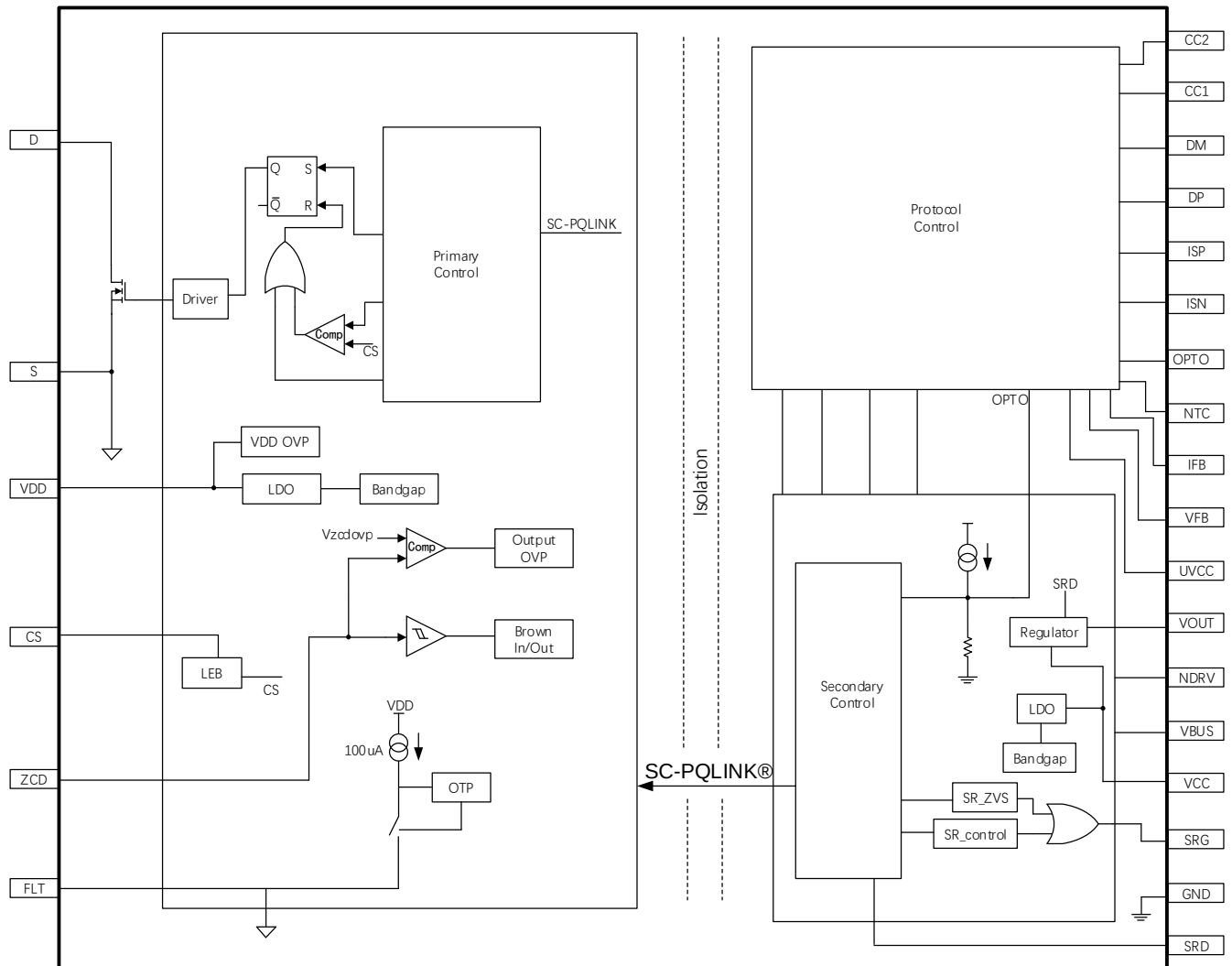


Fig. 3 Functional Block Diagram

9 Feature Description

SC3107C is a high performance isolated flyback converter IC designed for portable fast charge adapter applications. It integrates a primary GaN switch, primary controller, isolated feedback, synchronous rectification controller and protocol controller in one single IC package.

SC3107C features an adaptive switching frequency fold-back to achieve higher efficiency across entire load range. Additionally, it integrates SC-PQLINK®, which transmits high-speed information from the secondary to the primary for power cycles requests.

SC3107C supports USB-PD and various proprietary protocols, incorporating a host of integrated protection features. And it can be programmed through DPDM

9.1 Startup

After AC power-on, VDD will be charged by an external resistor, and the typical start-up current needed is IVDDST. The very low start-up current allows the SC3107C to increase the value of start-up resistor and then reduce the power dissipation.

When VDD reached UVLO, the primary switches at FSW_P with a ramping VCSLIMIT to build up bias winding voltage and SRD starts to charge VCC. When VCC reaches UVLO, the secondary start sending SC-PQLINK® requests based on Vout regulation.

9.2 VDD UVLO

A hysteresis UVLO comparator is implemented in SC3107C, fixing the turn-on and turn-off threshold levels at VDDON and VDDOFF, respectively. This hysteresis ensures that the start-up capacitor will be adequate to supply the primary during start-up.

9.3 ZCD Sensing for Brown In/Out

The ZCD pin monitors the voltage on the input bulk capacitor and performs brown in/out. When the primary switch is turned on, the voltage VAUX on the auxiliary winding is negative and proportional to the line voltage. The built-in clamp circuit on the ZCD pin clamps the voltage to VZCDCLAMP, and the clamped current is monitored to measure line voltage. The detailed equations are shown as below:

$$V_{BI} = R_{zcd-up} * I_{zcd-BI} * \frac{N_P}{N_{aux}} / 1.414$$

When IZCD rise above IZCDBI, the IC starts working and it stops working when IZCD fall below IZCDBO for TZCDBO.

9.4 ZCD Sensing for Vout OVP

The ZCD pin also monitors the voltage on the output capacitor and performs Vout OVP. The auxiliary winding demagnetization voltage VAUX is proportional to the output voltage. VZCD sensing the VAUX via the divided resistors can be used to sample the output voltage after blanking time TLEBOVP. When VZCD is above VZCDOVP for NZCDOVP cycles, the IC stops working. The output over-voltage can be calculated as:

$$V_{outovp} = \frac{V_{zcdovp} * N_S * (R_{zcd-up} + R_{zcd-down})}{(N_{aux} * R_{zcd-down})}$$

9.5 Cycle-by-Cycle Current Limit &SSCP

Two levels of overcurrent protection are integrated: cycle-by-cycle current limit and Secondary-Side Circuit Short Protection (SSCP). VCSSSCP provides fast protection for secondary rectifier or secondary winding shorts. Cycle-by-cycle current

limit adjusts based on SC-PQLINK® requests to improve light and medium load efficiency.

A turn-on spike occurs at the sense resistor each time the GaN switch is turned on, leading-edge blanking time is built for both protections to avoid fault triggers. During this period, the current-limit comparator is disabled as shown in fig. 4.

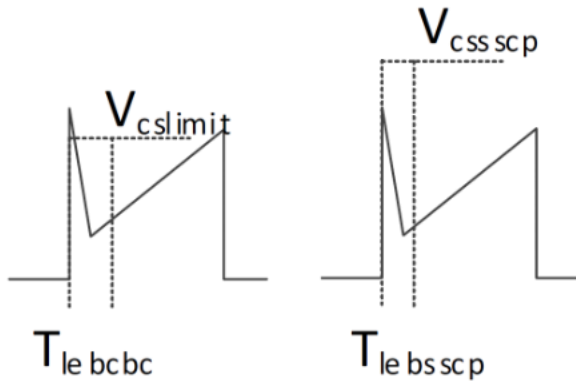


Fig. 4 LEB of OCP

9.6 CS Voltage Sensing

An external resistor is needed to limit the negative current to the CS pin, and a capacitor filters noise on the CS pin. A value of 1kOhm + 10pF is recommended. If line voltage compensation is enabled, the CS pin sources a current I_{CSLC} at low line voltage, creating an offset voltage on the resistor connected to the CS pin and removing the primary peak current difference between low and high line voltage.

A built-in slope compensation circuit is constructed in SC3107C. When the switch is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations in CCM operation.

9.7 FLT

SC3107C provides an NTC sense function on primary side. The FLT pin outputs a bias current I_{FLT} , and the over-temperature protection will be

triggered if the voltage is below the protection threshold V_{FLT} for a time delay T_{FLTDE} .

9.8 Operation Mode

SC3107C provides an adaptive switching frequency fold-back for higher efficiency across the load range as shown in fig. 5. At high line and full load, it operates with SR-ZVS for high efficiency. At low line and full load, it operates with CCM/QR for high efficiency. And at no load, the IC will operate in burst mode to reduce power consumption.

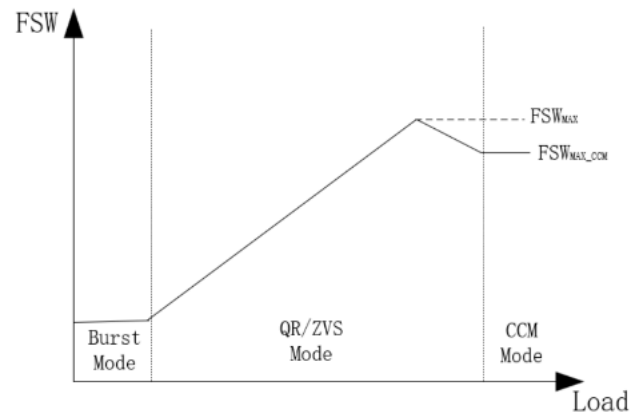


Fig. 5 Operation Mode vs Frequency

9.9 VCC UVLO

A hysteresis UVLO comparator is implemented in SC3107C, fixing the turn-on and turn-off threshold levels at V_{CCON} and V_{CCOFF} , respectively. This hysteresis ensures that the start-up capacitor will be adequate to supply the secondary during start-up.

9.10 SRD Valley/Peak switching

SC3107C detects SRD valley/peak for QR mode at low line and SR-ZVS mode at high line. After 12 resonant rings, IC is able to switch at any time in DCM mode.

9.11 SR Gate Control

SC3107C turns on SR MOSFET when SRD drops below V_{SRON} . After SRG is on, SRG will keep on



for TSTRON_MIN to avoid early turning off due to switching noise. When SRD rises above VSROFF or CCM operation is needed, SRG is pulled down pulled down immediately.

9.12 SR-ZVS

SC310x integrates SR-ZVS function which turns on SR before primary GaN switch turns on to achieve ZVS. SR gate on time adjusts inside the IC by VOUT and SRD information to achieve ZVS under different conditions.

9.13 Internal Over-Temperature Protection

An internal OTP circuit provides worst-case protection for the SC3107C. When the chip temperature exceeds the OTP threshold, the converter is disabled and remains in failure mode until the chip cools down below the OTHYS hysteresis.

9.14 UVCC

VOUT is the power supply input for UVCC, converting the voltage on VOUT to 5V to supply internal modules. A 1μF ceramic capacitor should be placed close to the UVCC pin.

9.15 NDRV

The Type-C and USB PD specifications require the VBUS isolation implementation for the Type-C port. SC3107C provides an NMOS gate driver to control the isolation MOSFET between VOUT pin and the VBUS pin. The gate driver is controlled by register, with VGS clamped to 7V. The IC offers four different pull-up capabilities from 20kΩ to 200kΩ to suit different MOSFETs.

9.16 VOUT & VBUS Discharging Paths

The IC integrates discharging paths from VBUS and VOUT pins to ground respectively. These paths help drain residual charge on the output capacitors to meet application requirements. The typical equivalent impedance of discharge path on VBUS pin is 1kΩ. The discharging path on VOUT pin is a constant current source from 45mA to 150mA, configured by registers. These discharge paths activate at detachment or lower VBUS voltage transition and can be controlled by firmware.

9.17 CV CC Control

SC3107C contains 2 DACs and 2 error amplifiers for OPTO pin to regulate output voltage and current.

For CV, an 11-bit DAC with an internal 2.048V reference voltage is used, supporting 20mV per step for VOUT regulation. The adjust time ranges from 20 μs to 250 μs, set by firmware. VOUT output regulation should be as the following equation.

$$V_{REG} = 2 + VDAC\ code * 0.010$$

For example, if VDAC code = 300, the output voltage $V_{REG} = 5V$.

For CC, A 10-bit DAC with 1.2V reference is used. The amplifier gain can be configured as 20 or 40. The regulation current (I_{REG}) is decided by the IDAC code, sense resistance (R_{SNS}) and the gain of current sense amplifier (G_{SNS}). The relationship between these parameters should be as follows.

$$I_{REG} = \frac{IDAC\ code \times 1.2}{(2^{10} \times R_{SNS} \times G_{SNS})}$$

For example, if $R_{SNS} = 5m\Omega$, $G_{SNS} = 40$, IDAC code = 512, $I_{REG} = 3A$.



9.18 NTC

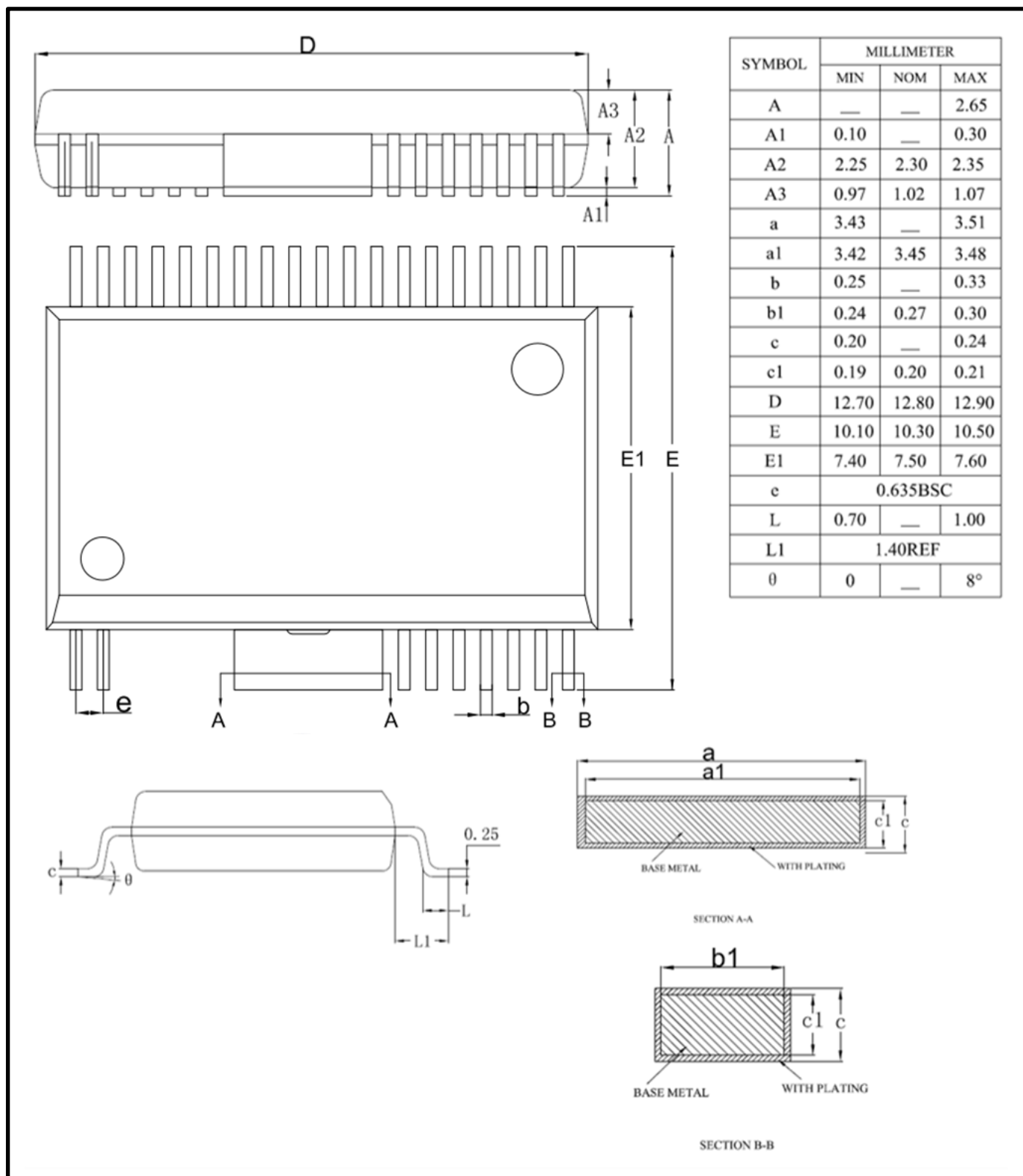
SC3107C provides an NTC sense function on the secondary side. The NTC pin outputs a bias current and detects the voltage to calculate the resistance on this pin.

The NTC pin sources current on the R_{NTC} , and the voltage can be sampled by a 10-bit ADC. The source current can be configured as 100 μ A, 20 μ A, or 4 μ A. Over-temperature protection will be triggered if the voltage is below the protection threshold for a programmed time delay.



MECHANICAL DATA

SSOP38



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