

Single Cell High Efficiency 8-A Switched Capacitor Direct Charger

1 Descriptions

SC8551A is a 97% efficiency, 8-A battery charging solution using a switched cap architecture. The switched cap architecture and the integrated FETs are optimized to enable a 50% cycle, allowing the cable current to be half the current delivered to the battery, reducing the losses over the charging cable as well as limiting the temperature rise in the application.

SC8551A adopts 56pin CSP 2.995mm X 3.255mm package.

2 Applications

- Smartphones
- Tablet PCs

3 Device Information

Part Number	Package	Body Size
SC8551ACFFR	CSP56	2.995mm x 3.255mm x 0.574mm

4 Features

- 10-way system protection
 - ✓ VAC_OVP
 - ✓ IBUS/IBAT/VBAT regulation
 - ✓ VDROPOVP
 - ✓ VBUS_OVP
 - ✓ IBUS_OCP
 - ✓ IBUS_UCP
 - ✓ VOUT_OVP
 - ✓ VBAT_OVP
 - ✓ IBAT_OCP
 - ✓ TSHUT
- 6-way charge-pump protection
 - ✓ VBUS_ERROR_HI protection before switch
 - ✓ VBUS_ERROR_LO protection before switch
 - ✓ CFLY short/open detection before switch
 - ✓ CDRV short/open detection before switch
 - ✓ PMID2OUT_OVP during switch
 - ✓ PMID2OUT_UVP during switch
- 7-channel 12-bit ADC
 - ✓ VAC,VBUS,IBUS,VOUT,VBAT,IBAT,TDIE

5 Typical Application Circuit

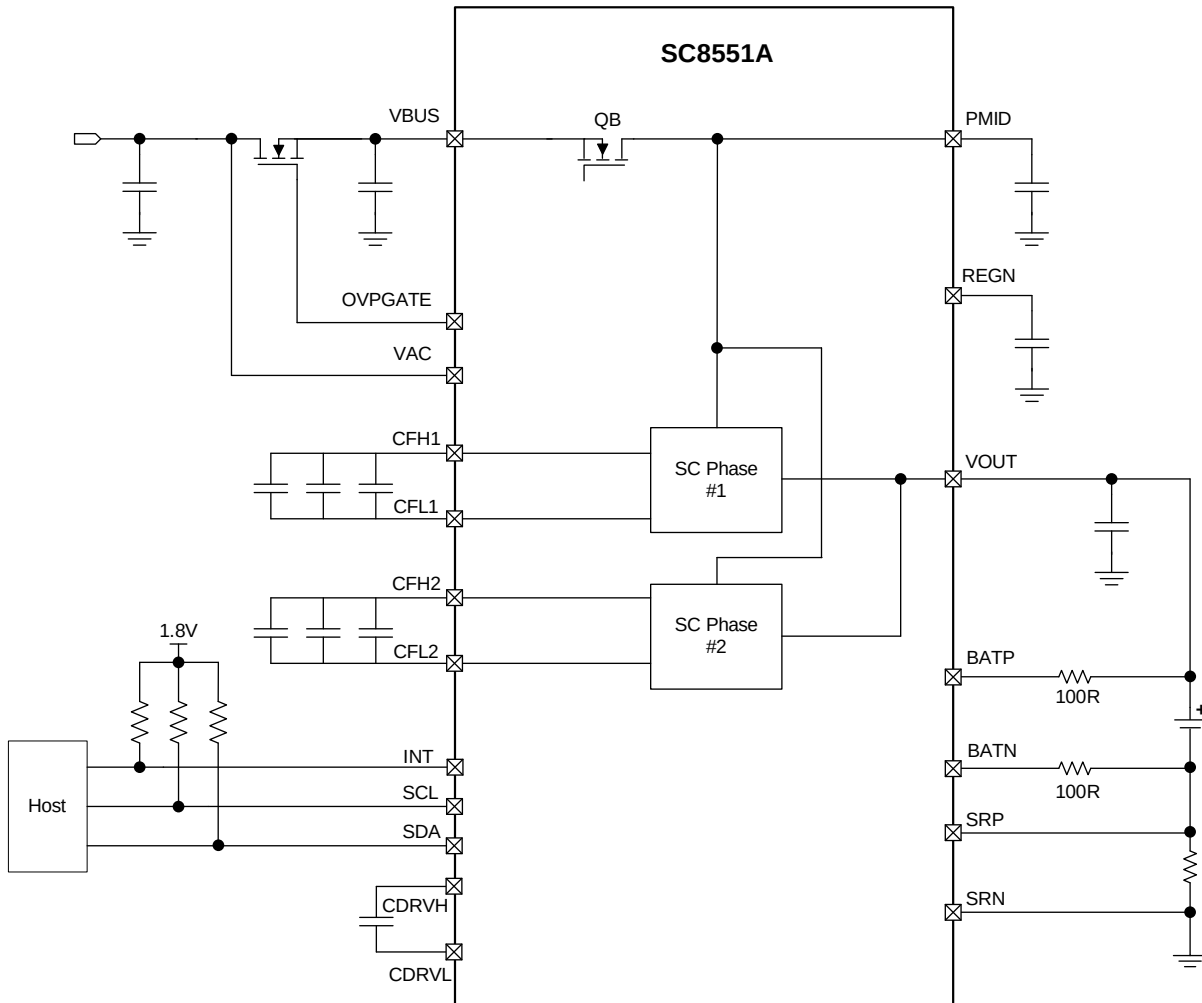
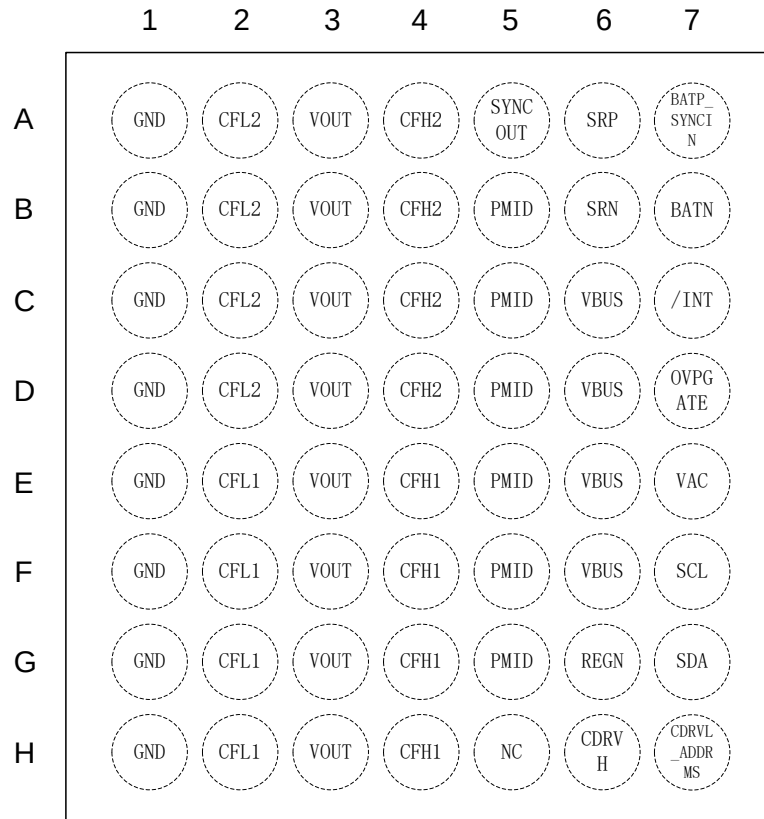


Fig1. Typical schematic of SC8551A standalone operation



6 Terminal Configuration and Functions



(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
A1,B1,C1,D1,E1,F1,G1,H1	GND	Power	Power ground
A2,B2,C2,D2	CFL2	Power	Flying capacitance 2 negative terminal
E2,F2,G2,H2	CFL1	Power	Flying capacitance 1 negative terminal
A3,B3,C3,D3,E3,F3,G3,H3	VOUT	Power	Device power output
A4,B4,C4,D4	CFH2	Power	Flying capacitance 2 positive terminal
E4,F4,G4,H4	CFH1	Power	Flying capacitance 1 positive terminal
B5,C5,D5,E5,F5,G5	PMID	Power	PMID is the input to the switched cap power stage. Connect 10-μF cap to PMID.
C6,D6,E6,F6	VBUS	Power	Device power input. Place a 1-μF bypass cap to GND as close as possible to these pins.



A5	SYNCOUT	I	In parallel operation, this pin is used to synchronous the clock to slave
A6	SRP	I	Positive input for low side battery current sensing
A7	BATP/SYNCIN	I	Positive input for battery voltage sensing. Series 100Ω to positive terminal of battery pack. In parallel operation, this pin can be used to monitor the clock input from master
B6	SRN	I	Negative input for low side battery current sensing
B7	BATN	I	Negative input for battery voltage sensing. Series 100Ω to negative terminal of battery pack
C7	/INT	O	Open drain, active low interrupt output. Pull up to voltage with 10-kΩ resistor
D7	OVPGATE	O	External OVPFET gate driver
E7	VAC	I	Input voltage sense pin
F7	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ). The IC works as a slave
G6	REGN	O	LDO output. Connect a 4.7-μF cap between this pin and GND.
G7	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ)
H5	NC	I/O	Do not connect
H6	CDRVH	I/O	Charge pump for gate drive. Connect a 0.22-μF cap between CDRVH and CDRVL
H7	CDRVL/ADDR	I/O	Charge pump for gate drive. Connect a 0.22-μF cap between CDRVH and CDRVL. In parallel operation, this pin can be used to set the I2C address

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VAC	-2	36	V
	VBUS	-2	20	V
	PMID	-0.3	20	V
	CFL1, CFL2, VOUT	-0.3	7	V
	SRP, SRN	-0.3	1.8	V
	BATP_SYNCIN, BATN, SYNCOUT	-0.3	6	V
	OVPGATE-VBUS	-0.3	14	V
	/INT, SDA, SCL, REGN	-0.3	6	V
	CDRVL_ADDRMS, CDRVH	-0.3	18	V
	CDRVH-CDRVL_ADDRMS	-0.3	6	V
	CFH1, CFH2, while maintaining CFH-VOUT=7V MAX	-0.3	14	V
	SRP-SRN	-0.3	0.3	V
	VOUT-VBUS	-16	6	V
Temperature Range	Operating Junction, T _J	-40	125	°C
	Storage temperature range, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2000	2000	V
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Voltage	VAC			11	V
	VBUS			11	V



	VOUT			5	V
	CFH1-VOUT,CFH2-VOUT,CFL1,CFL2			5	V
C _{FLY}	Flying capacitor (Effective capacitance at 5V)	20			μF
C _{VBUS}	VBUS capacitor	5			μF
C _{PMID}	PMID capacitor	5			μF
C _{OUT}	Output capacitor	5			μF
T _A	Operating ambient temperature	-40		85	°C
T _J	Operating junction temperature	-40		125	°C



7.4 Electrical Characteristic

$V_{BUS} = 8V$, $V_{OUT}=4V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$ for minimum and maximum specifications, and $T_A = 25^{\circ}C$ for typical specifications, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current						
I _{Q_VAC}	VAC quiescent current	ADC disabled, charger disabled, VOUT not present. Measure quiescent current on VAC		385		uA
		ADC enabled, charger disabled, VOUT not present. Measure quiescent current on VAC		710		uA
I _{Q_VOUT}	VOUT quiescent current	ADC disabled, charger disabled, VAC not present. Measure quiescent current on VOUT		10	18	uA
		ADC enabled, charger disabled, VAC not present. Measure quiescent current on VOUT		515		uA
Resistances						
R _{QB_ON}	QB on resistance	VBUS=9V, VOUT=4.5V		6		mΩ
R _{Q1_ON} / R _{Q5_ON}	On resistance of Q1/Q5	VBUS=9V, VOUT=4.5V		14		mΩ
R _{Q2_ON} / R _{Q6_ON}	On resistance of Q2/Q6	VBUS=9V, VOUT=4.5V		10		mΩ
R _{Q3_ON} / R _{Q7_ON}	On resistance of Q3/Q7	VBUS=9V, VOUT=4.5V		7		mΩ
R _{Q4_ON} / R _{Q8_ON}	On resistance of Q4/Q8	VBUS=9V, VOUT=4.5V		8		mΩ
R _{VBUS_PD}	VBUS pull-down resistance	VBUS_PD_EN='1'		1		kΩ
R _{VAC_PD}	VAC pull-down resistance	VAC_PD_EN='1'		100		Ω
Internal threshold						
V _{AC_UVLO}	VAC for active I2C, no battery. Also, for enable OVPGATE	Rising threshold		2.9	3.3	V
		Falling hysteresis		200		mV
V _{BUS_PRESENT}	Adapter inserting stat will be set to '1' once VBUS present	Rising threshold		3	3.3	V
		Falling hysteresis		300		mV
V _{OUT_UVLO}	VOUT for active I2C, no adapter	Rising threshold		2.5	2.7	V
		Falling hysteresis		200		mV
V _{TH_CHG_EN}	Minimum VOUT voltage for charging enable	Rising threshold		3		V
		Falling hysteresis		200		mV
Input over-voltage protection and alarm						
V _{AC_OVP}	Rising threshold	Adjustable in register 0x05h	6.5		17	V
	Step size	Step size valid for 11V through 17V only		1		V
	Falling hysteresis			500		mV
	Comparator accuracy	Accuracy for 6.5V	-2%		2%	



	Comparator accuracy	Accuracy for 11V through 17V	-2%	2%		
V _{BUS_OVP}	Rising threshold	Adjustable in register 0x06h	6	12.35	V	
	Step size		50		mV	
	Comparator accuracy	VBUS=8V	-1%	1%		
V _{DROP_OVP}	Rising threshold	Adjustable in register 0x05h, bit4=0	240	300	360	mV
	Rising threshold	Adjustable in register 0x05h, bit4=1	340	400	460	mV
Vbus in-range protection						
V _{BUS2OUT_MAX}	Rising threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.2*V _{OUT}			V
	Falling threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.17*V _{OUT}			V
V _{BUS2OUT_MIN}	Rising threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.02*V _{OUT}			V
	Falling threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0			V
Output short protection						
V _{PMID2OUT_OVP}	Rising threshold Over V _{PMID} /2-V _{OUT} (2:1 charger mode) or Over V _{PMID} -V _{OUT} (1:1 charger mode)		300			mV
Input short protection						
V _{PMID2OUT_UVP}	Falling threshold Over V _{PMID} /2-V _{OUT} (2:1 charger mode) or Over V _{PMID} -V _{OUT} (1:1 charger mode)		-100			mV
Output over-voltage protection and alarm						
V _{OUT_OVP}	Rising threshold		4.8	4.9	5	V
V _{BAT_OVP}	Rising threshold	Adjustable in register 0x00h	3.5	5.075		V
	Step size		25			mV
	Comparator accuracy	From VBAT=3.5V to 4.4V	-0.5%	0.5%		



Input over-current protection and alarm						
I _{BUS_OCP}	Rising threshold	Adjustable in register 0x08h	1	4.75	A	
	Step size		250		mA	
	Comparator accuracy	IBUS=3A	-5%	5%		
I _{BUS_UCP_RISING}	Rising threshold	Adjustable in register 0x2Bh, bit2=0	300	400	mA	
		Adjustable in register 0x2Bh, bit2=1	500	600	mA	
I _{BUS_UCP_FALLING}	Falling threshold	Adjustable in register 0x2Bh, bit2=0	10	150	mA	
		Adjustable in register 0x2Bh, bit2=1	100	250	mA	
Output over-current protection and alarm						
I _{BAT_OCP}	Rising threshold	Adjustable in register 0x02h	2	10	A	
	Step size		100		mA	
	Comparator accuracy	IBAT=6A	-5%	5%		
Timers						
f _{SW}	Switching frequency	Programmable range	300	500	750	kHz
t _{OVPGATE_ON_DG}	Deglitch time between VAC over VAC_UVLO and turn on external MOS		80			ms
t _{VAC_OVP}	VAC OVP reaction time		200			ns
t _{VAC_PD}	VAC Pull-down time		400			ms
t _{VBUS_IN_RANGE}	Minimum VBUS in-range duration before charge pump start switching	VBUS slow UVP/OVP	20			ms
t _{VBUS_OVP}	VBUS OVP reaction time		1			us
t _{IBUS_OCP}	IBUS OCP reaction time		75			us
t _{IBUS_UCP_FALLING}	IBUS UCP falling reaction time	Adjustable in register 0x2Eh, bit3=0	10			us
		Adjustable in register 0x2Eh, bit3=1	5			ms
t _{VDROP_OVP}	VDROP OVP reaction time	Adjustable in register 0x05h, bit4=0	8			us
		Adjustable in register 0x05h, bit4=1	5			ms
t _{VPMID2OUT_OVP}	VPMID/2-VOUT OVP reaction time or VPMID-VOUT OVP reaction time		0.1			us
t _{VPMID2OUT_UVP}	VPMID/2-VOUT UVP reaction time		0.1			us



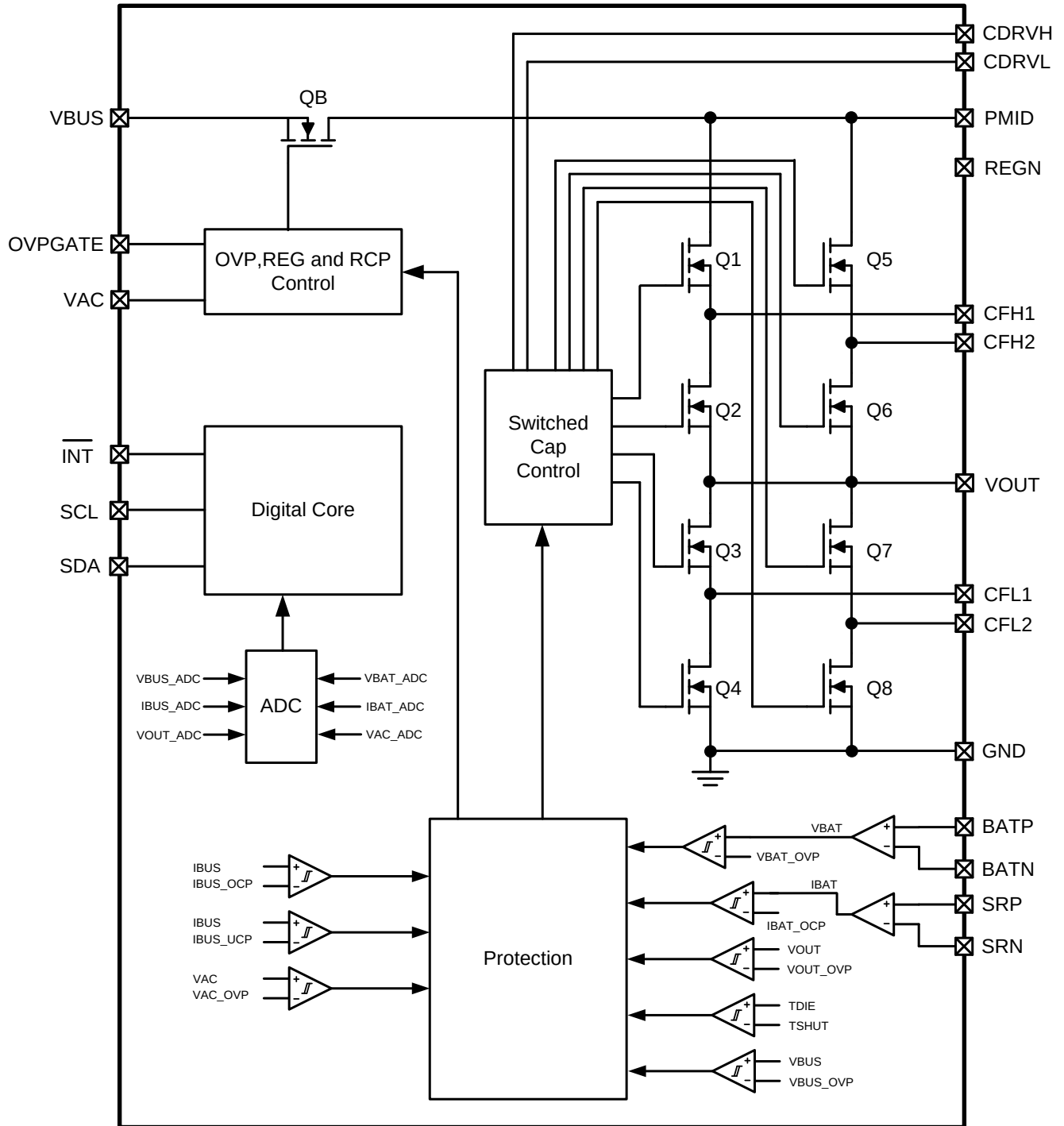
	or VPMID-VOUT UVP reaction time			
t _{VOUT_OVP}	VOUT OVP reaction time		1	us
t _{VBAT_OVP}	VBAT OVP reaction time		0.1	us
t _{IBAT_OCP}	IBAT OCP reaction time		500	us
t _{SS_TIMEOUT}	Soft start timeout	Adjustable in register 0x2Bh	0 81.92	s
t _{WD_TIMEOUT}	Watchdog timeout	Adjustable in register 0x0Bh	0.5 30	s
t _{REG_TIMEOUT}	If the part is in regulation, but below VDROP_OVP for this amount of time, the part will stop switching.		650	ms
t _{INT_LOW}	During that INT is pulled low when an event occurs		256	us
t _{INT_HIGH}	Minimum high level time after an INT low event		256	us
REGN LDO				
V _{REGN}	REGN LDO output voltage	VBUS=8V	5	V
I _{REGN}	REGN LDO current limit	VBUS=8V	50	mA
I2C Interface & Interrupt				
F _{SCL}	Serial-clock frequency		1000	kHz
V _{IH}	Input logic high		1.2	V
V _{IL}	Input logic low		0.4	V
I _{LEAKAGE}	Input leakage current		1	uA
ADC MEASUREMENT				
IBUS_ADC	Range		0 5	A
	LSB		1.5625	mA
	Accuracy	IBUS=3A	-5% 5%	
VBUS_ADC	Range		0 14	V
	LSB		3.75	mV
	Accuracy	VBUS=8V	-1% 1%	
VAC_ADC	Range		0 14	V
	LSB		5	mV
	Accuracy	VAC=8V	-1% 1%	
VOUT_ADC	Range		0 5	V
	LSB		1.25	mV
	Accuracy	VOUT=4V	-0.5% 0.5%	
VBAT_ADC	Range		0 5	V
	LSB		1.25	mV
	Accuracy	VBAT=4V	-0.5% 0.5%	



IBAT_ADC	Range		0	10	A
	LSB		3.125		mA
	Accuracy	IBAT=6A with 2mΩ R _{SENSE}	-1.5%	1.5%	
TDIE_ADC	ADC Die temperature readable in registers 0x24h and 025h	Range	0	150	°C
		LSB	0.5		°C
	Accuracy		±4		°C
TSHUT					
T _{SHUT}	Thermal shutdown temperature		150		°C



8 Function Block Diagram



9 Detailed Description

9.1 VBUS In-range

Prior to enable the charge pump (CHG_EN=1), the VBUS voltage must be between VBUS2OUT_MIN and VBUS2OUT_MAX. This VBUS in-range protection is only effect during the power-up. Once the charge pump has already been enabled, the VBUS in-range protection will be disabled.

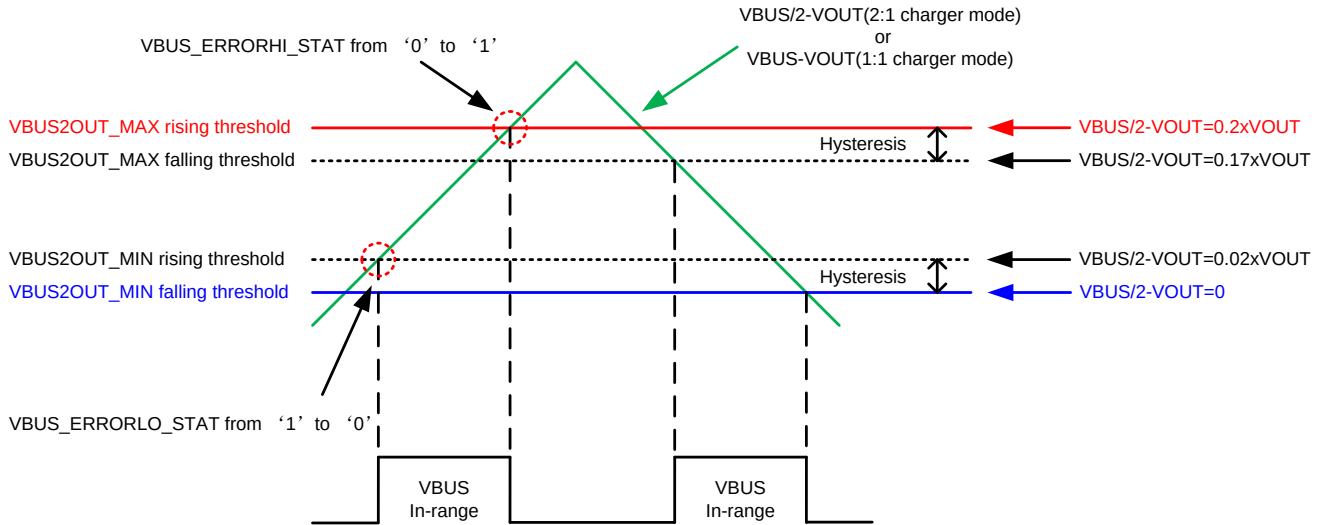


Fig3. Valid VBUS window for enabling charging

9.2 Charging Mode

The SC8551A support both 2:1 charge mode and 1:1 charger mode. User can choose different charging mode by setting different bit value in register 0x31h(bit0). The below two tips should be noted:

1. Mode register will be changed successfully only when CHG_EN=0
2. When 1:1 charger mode is selected, the actual VBUS_OVP threshold is half of the setting value in VBUS_OVP register

9.3 Parallel Operation

RESISTOR VALUE to GND on CDRV1_ADDRMS	I2C ADDRESS	AC_OVP_SETTING	MASTER, SLAVE, or STANDALONE OPERATION
Open(>150k)	0x66	6.5V	Standalone1
75k	0x65	11V	Standalone2
39k	0x66	Disable	Slave
18k	0x65	6.5V	Master



9.4 Register map and default value

ADDRESS (Hex)	ACRONYM	Standalone1 (Hex)	Standalone2 (Hex)	Slave (Hex)	Master (Hex)	WDT RST	REG RST
0x00	VBAT_OVP	0x22	0x22	0xA2	0x22	N	Y
0x02	IBAT_OCP	0x3D	0x3D	0xBD	0x3D	N	Y
0x05	AC_PROTECTION	0x07	0x00	0x00	0x07	N	Y
0x06	VBUS_OVP	0x3A	0x3A	0x3A	0x3A	N	Y
0x08	IBUS_OCP_UCP	0x0D	0x0D	0x0D	0x0D	N	Y
0x0A	CONVERTER_STAT	0x00	0x00	0x00	0x00	N	Y
0x0B	CONTROL	0x40	0x40	0x40	0x40	N	Y
0x0C	CHRG_CTRL	0x00	0x00	0x20	0x46	Only reset "CHG_EN" bit	Y
0x0D	INT_STAT	0x00	0x00	0x00	0x00	N	N
0x0E	INT_FLAG	0x00	0x00	0x00	0x00	N	N
0x0F	INT_MASK	0x00	0x00	0x00	0x00	N	Y
0x10	FLT_STAT	0x00	0x00	0x00	0x00	N	N
0x11	FLT_FLAG	0x00	0x00	0x00	0x00	N	N
0x12	FLT_MASK	0x00	0x00	0x00	0x00	N	Y
0x13	PART_INFO	0x51	0x51	0x51	0x51	N	N
0x14	ADC_CTRL	0x00	0x00	0x00	0x00	Only reset "ADC_EN" bit	Y
0x15	ADC_FN_DIS	0x00	0x00	0xF8	0x06	N	Y
0x16	IBUS_ADC1	0x00	0x00	0x00	0x00	N	Y
0x17	IBUS_ADC0	0x00	0x00	0x00	0x00	N	Y
0x18	VBUS_ADC1	0x00	0x00	0x00	0x00	N	Y
0x19	VBUS_ADC0	0x00	0x00	0x00	0x00	N	Y
0x1A	VAC_ADC1	0x00	0x00	0x00	0x00	N	Y
0x1B	VAC_ADC0	0x00	0x00	0x00	0x00	N	Y
0x1C	VOUT_ADC1	0x00	0x00	0x00	0x00	N	Y
0x1D	VOUT_ADC0	0x00	0x00	0x00	0x00	N	Y
0x1E	VBAT_ADC1	0x00	0x00	0x00	0x00	N	Y
0x1F	VBAT_ADC0	0x00	0x00	0x00	0x00	N	Y
0x20	IBAT_ADC1	0x00	0x00	0x00	0x00	N	Y
0x21	IBAT_ADC0	0x00	0x00	0x00	0x00	N	Y
0x26	TDIE_ADC1	0x00	0x00	0x00	0x00	N	Y
0x27	TDIE_ADC0	0x00	0x00	0x00	0x00	N	Y
0x2B	REG_CTRL	0xE0	0xE0	0xE0	0xE0	N	Y
0x2C	REG_THRESHOLD	0x00	0x00	0x00	0x00	N	Y
0x2D	REG_FLAG_MASK	0x00	0x00	0x00	0x00	N	Y
0x2E	DEGLITCH	0x00	0x00	0x00	0x00	N	Y

**SOUTHCHIP SOUTHCHIP SEMICONDUCTOR**

0x2F	PMID2OUT_OVP_UVP	0x50	0x50	0x50	0x50	N	Y
0x30	IBUS_REGULATION	0x08	0x08	0x08	0x08	N	Y
0x31	MODE	0x00	0x00	0x00	0x00	N	Y
0x35	VBUS_INRANGE_DIS	0x00	0x00	0x00	0x00	N	Y
0x36	OVPGATE_DIS	0x00	0x00	0x00	0x00	N	Y



9.5 Device Modes and Protection Status

FUNCTIONS	BAT-ONLY (VBUS<VBUS_PRESENT)	VBUS>VBUS_PRESENT CHG_EN=0 (Charge pump disabled)	VBUS>VBUS_PRESENT CHG_EN=1 (Charge pump enabled)	
			During charge soft start	Charging
I2C allowed	√	√	√	√
Allow user ADC	√	√	√	√
VAC FET gate drive		√	√	√
VAC_OVP			√	√
VBUS_OVP			√	√
IBUS_OCP			√	√
IBUS_UCP			X	√
VBAT_OVP			√	√
VOUT_OVP			√	√
IBAT_OCP			√	√
VBAT/IBAT_REG			√	√
IBUS_REG			√	√
VBUS In-range		√	√	√
MOS_OCP			√	√
WD_TIMEOUT			√	√
SS_TIMEOUT			√	√
PIN_DIAG_FAIL			√	√
TDIE_FLT			√	√



Table1. VBAT_OVP Register (Address=00h) [reset=22h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_DIS	R/W	0h	N/A	0: Enable the VBAT_OVP protection (default) 1: Disable the VBAT_OVP protection
6	RESERVED	R	0h	N/A	
5	VBAT_OVP[5]	R/W	1h	800mV	Battery Over-Voltage Protection Setting. When the battery voltage goes above the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Offset: 3.5V Range: 3.5V (b0000000) – 5.075V (b1111111) Default: 4.35V (b100010)
4	VBAT_OVP[4]	R/W	0h	400mV	
3	VBAT_OVP[3]	R/W	0h	200mV	
2	VBAT_OVP[2]	R/W	0h	100mV	
1	VBAT_OVP[1]	R/W	1h	50mV	
0	VBAT_OVP[0]	R/W	0h	25mV	

Table2. IBAT_OCP Register (Address=02h) [reset=3Dh]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_OCP_DIS	R/W	0h	N/A	0: Enable the IBAT_OCP protection (default) 1: Disable the IBAT_OCP protection
6	IBAT_OCP[6]	R/W	0h	6400mA	BAT Over-Current Protection Setting. When the bat current reaches the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Any setting over 10A is set to 10A Offset: 2A Range: 2A (b00000000) - 10A (b11111111) Default: 8.1A (b01111101)
5	IBAT_OCP[5]	R/W	1h	3200mA	
4	IBAT_OCP[4]	R/W	1h	1600mA	
3	IBAT_OCP[3]	R/W	1h	800mA	
2	IBAT_OCP[2]	R/W	1h	400mA	
1	IBAT_OCP[1]	R/W	0h	200mA	
0	IBAT_OCP[0]	R/W	1h	100mA	

Table3. AC_PROTECTION Register (Address=05h) [reset=07h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC_OVP_STAT	R	0h	N/A	Status of VAC_OVP. Persists until condition is no longer valid.
6	VAC_OVP_FLAG	R	0h	N/A	Set once a VAC_OVP event occurs. Cleared upon read.
5	VAC_OVP_MASK	R/W	0h	N/A	Masks an VAC_OVP event from sending an INT.
4	VDROP_OVP_THR ESHOLD_SET	R/W	0h	N/A	This is the voltage difference between VAC and VBUS that will cause the device to stop switching 0: 300mV (Default) 1: 400mV
3	VDROP_DEGLITCH H_SET	R/W	0h	N/A	0: 8us (default) 1: 5ms
2	VAC_OVP[2]	R/W	1h	4V	VAC Over-Voltage Protection Setting. When the VAC voltage reaches the programmed threshold, OVPGATE turns off the OVPFET. The setting is determined by $VAC_OVP = 11\text{ V} + VAC_OVP[2:0]*1\text{ V}$ Default: 6.5 V (b 111) Writing all '1' to these bits set the VAC_OVP to 6.5V
1	VAC_OVP[1]	R/W	1h	2V	
0	VAC_OVP[0]	R/W	1h	1V	

Table4. VBUS_OVP Register (Address=06h) [reset=3Ah]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_PD_EN	R/W	0h	N/A	0 = VBUS pull-down disabled (default) 1 = VBUS pull-down enabled Enable this will turn off the external OVPFET, and conduct current from VBUS to GND
6	VBUS_OVP[6]	R/W	0h	3200mV	VBUS Over-Voltage Protection Setting. When the bus voltage goes above the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Offset: 6V Range: 6V (b0000000) – 12.35V (b1111111) Default: 8.9V (b0111010)
5	VBUS_OVP[5]	R/W	1h	1600mV	
4	VBUS_OVP[4]	R/W	1h	800mV	
3	VBUS_OVP[3]	R/W	1h	400mV	
2	VBUS_OVP[2]	R/W	0h	200mV	
1	VBUS_OVP[1]	R/W	1h	100mV	
0	VBUS_OVP[0]	R/W	0h	50mV	



Table5. IBUS_OCP_UCP Register (Address=08h) [reset=0Dh]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_DIS	R/W	0h	N/A	0: Enable the IBUS_OCP protection (default) 1: Disable the IBUS_OCP protection
6	IBUS_UCP_RISE_FLAG	R	0h	N/A	IBUS under-current threshold rising flag. An INT is sent when this occurs, and is cleared upon read.
5	IBUS_UCP_RISE_MASK	R/W	0h	N/A	IBUS under-current threshold rising /INT mask 0: Not masked 1: Masked
4	IBUS_UCP_FALL_FLAG	R	0h	N/A	IBUS under-current threshold falling flag. An INT is sent when this occurs, and is cleared upon read. This bit is not maskable.
3	IBUS_OCP[3]	R/W	1h	2A	Bus Over-Current Protection Setting. When the bus current reaches the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Offset: 1A Range: 1A (b0000) – 4.75A (b1111) Default: 4.25A (b1101)
2	IBUS_OCP[2]	R/W	1h	1A	
1	IBUS_OCP[1]	R/W	0h	500mA	
0	IBUS_OCP[0]	R/W	1h	250mA	

**Table6. CONVERTER STATE Register (Address=0Ah) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSHUT_FLAG	R	0h	N/A	Thermal shutdown flag. An INT is sent when this event happens, and is cleared when read. This bit is not maskable.
6	TSHUT_STAT	R	0h	N/A	Thermal shutdown status. This register is 1 until the event no longer persists.
5	VBUS_ERRORLO_STAT	R	0h	N/A	This bit shows the current status of VBUS, and is '0' only when the event is not happening.
4	VBUS_ERRORHI_STAT	R	0h	N/A	This bit shows the current status of VBUS, and is '0' only when the event is not happening.
3	SS_TIMEOUT_FLAG	R	0h	N/A	Soft-start timeout flag. An INT is sent when this event happens, and is cleared when read. This bit is not maskable.
2	CP_SWITCHING_STAT	R	0h	N/A	0: Charge-pump is not switching 1: Charge-pump is switching
1	CONV_OCP_FLAG	R	0h	N/A	Internal MOSFET OCP flag. An INT is sent when this event happens, and is cleared when read. This bit is not maskable.
0	PIN_DIAG_FAIL_FLAG	R	0h	N/A	Pin diagnostic fail flag. CFLY short/open and CDRV short/open will be checked before switch. An INT is sent when this event happens and is cleared when read. This bit is not maskable.



Table7. CTRL Register (Address=0Bh) [reset=40h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	REG_RST	R/W	0h	N/A	0 = No register reset (default) 1 = Reset registers to their default values
6	FSW_SET2	R/W	1h	N/A	Set the CP switching frequency 000: 300kHz 001: 350kHz 010: 400kHz 011: 450kHz 100: 500kHz (default) 101: 550kHz 110: 600kHz 111: 750kHz
5	FSW_SET1	R/W	0h	N/A	
4	FSW_SET0	R/W	0h	N/A	
3	WD_TIMEOUT_FLAG	R	0h	N/A	
2	WD_TIMEOUT_DIS	R/W	0h	N/A	0 = Enable watchdog (default) 1 = Disable watchdog
1	WD_TIMEOUT1	R/W	0h	N/A	Watchdog Timeout protection 00: 0.5s (default) 01: 1s 10: 5s 11: 30s
0	WD_TIMEOUT0	R/W	0h	N/A	

**Table8. CHG_CTRL Register (Address=0Ch) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	CHG_EN	R/W	0h	N/A	0 = Charger disabled (default) 1 = Charger enabled
6	MS1	R	0h	N/A	00: Standalone
5	MS0	R	0h	N/A	01: Slave 10: Master 11: Reserved
4	FREQ_SHIFT1	R/W	0h	N/A	Adjust FSW for EMI
3	FREQ_SHIFT0	R/W	0h	N/A	00 = Nominal frequency 01 = +10% 10 = -10% 11 = Spread spectrum varies frequency +-10%
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

**Table9. INT_STAT Register (Address=0Dh) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	ADAPTER_INSERT_STAT	R	0h	N/A	Indicates the VBUS PRESENT threshold is exceeding
1	VBAT_INSERT_STAT	R	0h	N/A	Indicates the VBAT UVLO threshold is exceeding
0	ADC_DONE_STAT	R	0h	N/A	Indicates the ADC conversion is complete in 1-shot mode only.

Table10. INT_FLAG Register (Address=0Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	ADAPTER_INSERT_FLAG	R	0h	N/A	Indicates the VBUS UVLO threshold has been exceeded
1	VBAT_INSERT_FLAG	R	0h	N/A	Indicates the VBAT UVLO threshold has been exceeded
0	ADC_DONE_FLAG	R	0h	N/A	Indicates the ADC conversion is complete in 1-shot mode only.

**Table11. INT_MASK Register (Address=0Fh) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	ADAPTER_INSERT_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
1	VBAT_INSERT_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
0	ADC_DONE_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked

Table12. FLT_STAT Register (Address=10h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_STAT	R	0h	N/A	Indicates a VBAT over-voltage event is occurring
6	IBAT_OCP_STAT	R	0h	N/A	Indicates a IBAT over-current event is occurring
5	VBUS_OVP_STAT	R	0h	N/A	Indicates a VBUS over-voltage event is occurring
4	IBUS_OCP_STAT	R	0h	N/A	Indicates a IBUS over-current event is occurring
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

**Table13. FLT_FLAG Register (Address=11h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_FLAG	R	0h	N/A	Indicates a VBAT over-voltage event has occurred
6	IBAT_OCP_FLAG	R	0h	N/A	Indicates a IBAT over-current event has occurred
5	VBUS_OVP_FLAG	R	0h	N/A	Indicates a VBUS over-voltage event has occurred
4	IBUS_OCP_FLAG	R	0h	N/A	Indicates a IBUS over-current event has occurred
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table14. FLT_MASK Register (Address=12h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
6	IBAT_OCP_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
5	VBUS_OVP_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
4	IBUS_OCP_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

**Table15. PART_INFO Register (Address=13h) [reset=51h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	Device ID	R	0h	N/A	Device_ID: 0x51
6	Device ID	R	1h	N/A	
5	Device ID	R	0h	N/A	
4	Device ID	R	1h	N/A	
3	Device ID	R	0h	N/A	
2	Device ID	R	0h	N/A	
1	Device ID	R	0h	N/A	
0	Device ID	R	1h	N/A	



Table16. ADC_CTRL Register (Address=14h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	ADC_EN	R/W	0h	N/A	Enable ADC 0 = Disabled 1 = Enabled
6	ADC_RATE	R/W	0h	N/A	0 = Continuous conversion 1 = One-shot
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	IBUS_ADC_DIS	R/W	0h	N/A	0: Enable Conversion (default) 1: Disable Conversion

Table17. ADC_FN_DISABLE Register (Address=15h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_ADC_DIS	R/W	0h	N/A	0: Enable Conversion (default) 1: Disable Conversion
6	VAC_ADC_DIS	R/W	0h	N/A	
5	VOUT_ADC_DIS	R/W	0h	N/A	
4	VBAT_ADC_DIS	R/W	0h	N/A	
3	IBAT_ADC_DIS	R/W	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	TDIE_ADC_DIS	R/W	0h	N/A	

**Table18. IBUS_ADC1 Register (Address=16h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	IBUS ADC LSB: 1.5625mA
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBUS_ADC[11]	R	0h	N/A	
2	IBUS_ADC[10]	R	0h	N/A	
1	IBUS_ADC[9]	R	0h	N/A	
0	IBUS_ADC[8]	R	0h	N/A	

Table19. IBUS_ADC0 Register (Address=17h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_ADC[7]	R	0h	N/A	IBUS ADC LSB: 1.5625mA
6	IBUS_ADC[6]	R	0h	N/A	
5	IBUS_ADC[5]	R	0h	N/A	
4	IBUS_ADC[4]	R	0h	N/A	
3	IBUS_ADC[3]	R	0h	N/A	
2	IBUS_ADC[2]	R	0h	N/A	
1	IBUS_ADC[1]	R	0h	N/A	
0	IBUS_ADC[0]	R	0h	N/A	



Table20. VBUS_ADC1 Register (Address=18h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VBUS ADC LSB: 3.75mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VBUS_ADC[11]	R	0h	N/A	
2	VBUS_ADC[10]	R	0h	N/A	
1	VBUS_ADC[9]	R	0h	N/A	
0	VBUS_ADC[8]	R	0h	N/A	

Table21. VBUS_ADC0 Register (Address=19h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_ADC[7]	R	0h	N/A	VBUS ADC LSB: 3.75mV
6	VBUS_ADC[6]	R	0h	N/A	
5	VBUS_ADC[5]	R	0h	N/A	
4	VBUS_ADC[4]	R	0h	N/A	
3	VBUS_ADC[3]	R	0h	N/A	
2	VBUS_ADC[2]	R	0h	N/A	
1	VBUS_ADC[1]	R	0h	N/A	
0	VBUS_ADC[0]	R	0h	N/A	

**Table22. VAC_ADC1 Register (Address=1Ah) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VAC ADC LSB: 5mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VAC_ADC[11]	R	0h	N/A	
2	VAC_ADC[10]	R	0h	N/A	
1	VAC_ADC[9]	R	0h	N/A	
0	VAC_ADC[8]	R	0h	N/A	

Table23. VAC_ADC0 Register (Address=1Bh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC_ADC[7]	R	0h	N/A	VAC ADC LSB: 5mV
6	VAC_ADC[6]	R	0h	N/A	
5	VAC_ADC[5]	R	0h	N/A	
4	VAC_ADC[4]	R	0h	N/A	
3	VAC_ADC[3]	R	0h	N/A	
2	VAC_ADC[2]	R	0h	N/A	
1	VAC_ADC[1]	R	0h	N/A	
0	VAC_ADC[0]	R	0h	N/A	



Table24. VOUT_ADC1 Register (Address=1Ch) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VOUT ADC LSB: 1.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VOUT_ADC[11]	R	0h	N/A	
2	VOUT_ADC[10]	R	0h	N/A	
1	VOUT_ADC[9]	R	0h	N/A	
0	VOUT_ADC[8]	R	0h	N/A	

Table25. VOUT_ADC0 Register (Address=1Dh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VOUT_ADC[7]	R	0h	N/A	VOUT ADC LSB: 1.25mV
6	VOUT_ADC[6]	R	0h	N/A	
5	VOUT_ADC[5]	R	0h	N/A	
4	VOUT_ADC[4]	R	0h	N/A	
3	VOUT_ADC[3]	R	0h	N/A	
2	VOUT_ADC[2]	R	0h	N/A	
1	VOUT_ADC[1]	R	0h	N/A	
0	VOUT_ADC[0]	R	0h	N/A	



Table26. VBAT_ADC1 Register (Address=1Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VBAT ADC LSB: 1.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VBAT_ADC[11]	R	0h	N/A	
2	VBAT_ADC[10]	R	0h	N/A	
1	VBAT_ADC[9]	R	0h	N/A	
0	VBAT_ADC[8]	R	0h	N/A	

Table27. VBAT_ADC0 Register (Address=1Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_ADC[7]	R	0h	N/A	VBAT ADC LSB: 1.25mV
6	VBAT_ADC[6]	R	0h	N/A	
5	VBAT_ADC[5]	R	0h	N/A	
4	VBAT_ADC[4]	R	0h	N/A	
3	VBAT_ADC[3]	R	0h	N/A	
2	VBAT_ADC[2]	R	0h	N/A	
1	VBAT_ADC[1]	R	0h	N/A	
0	VBAT_ADC[0]	R	0h	N/A	

**Table28. IBAT_ADC1 Register (Address=20h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	IBAT ADC LSB: 3.125mA
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBAT_ADC[11]	R	0h	N/A	
2	IBAT_ADC[10]	R	0h	N/A	
1	IBAT_ADC[9]	R	0h	N/A	
0	IBAT_ADC[8]	R	0h	N/A	

Table29. IBAT_ADC0 Register (Address=21h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_ADC[7]	R	0h	N/A	IBAT ADC LSB: 3.125mA
6	IBAT_ADC[6]	R	0h	N/A	
5	IBAT_ADC[5]	R	0h	N/A	
4	IBAT_ADC[4]	R	0h	N/A	
3	IBAT_ADC[3]	R	0h	N/A	
2	IBAT_ADC[2]	R	0h	N/A	
1	IBAT_ADC[1]	R	0h	N/A	
0	IBAT_ADC[0]	R	0h	N/A	



Table30. TDIE_ADC1 Register (Address=26h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	TDIE_ADC[8]	R	0h	128°C	

Table31. TDIE_ADC0 Register (Address=27h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TDIE_ADC[7]	R	0h	64°C	DIE temperature = TDIE_ADC [8:0] * 0.5°C
6	TDIE_ADC[6]	R	0h	32°C	
5	TDIE_ADC[5]	R	0h	16°C	
4	TDIE_ADC[4]	R	0h	8°C	
3	TDIE_ADC[3]	R	0h	4°C	
2	TDIE_ADC[2]	R	0h	2°C	
1	TDIE_ADC[1]	R	0h	1°C	
0	TDIE_ADC[0]	R	0h	0.5°C	



Table32. REG_CTRL Register (Address=2Bh) [reset=E0h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	SS_TIMEOUT2	R/W	1h	N/A	Adjustable timeout for IBUS to rise to the IBUS_UCP_RISE_THRESHOLD 000: SS Timeout Disabled 001: 40ms 010: 80ms 011: 320ms 100: 1.28s 101: 5.12s 110: 20.48s 111: 81.92s (default)
6	SS_TIMEOUT1	R/W	1h	N/A	
5	SS_TIMEOUT0	R/W	1h	N/A	
4	EN_REGULATION	R/W	0h	N/A	Enable the device to regulation the output based on the VBAT_OVP and IBAT_OCP threshold.
3	VOUT_OVP_DIS	R/W	0h	N/A	0: Enable VOUT OVP protection (default) 1: Disable VOUT OVP protection
2	IBUS_UCP_TH	R/W	0h	N/A	IBUS_UCP rising and falling threshold IBUS must reach the rising threshold before the SS timeout. IBUS_UCP and IBUS_UCP_ALM are disabled until IBUS reaches the rising threshold When the IBUS reaches the falling threshold, an INT is sent and CHG_EN bit is set to '0' 0: 150mA falling, 300mA rising (default) 1: 250mA falling, 500mA rising
1	SET_IBAT_SNS_RES	R/W	0h	N/A	This bit selects the external BAT_SNS resistor value 0: 2mΩ (default) 1: 5mΩ
0	VAC_PD_EN	R/W	0h	N/A	When this bit is enabled, it pulls down the VAC for t _{VAC_PD} to discharge any bulk cap on VAC 0: Disable (default) 1: Enable



Table33. REG_THRESHOLD Register (Address=2Ch) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	SET_IBATREG1	R/W	0h	N/A	This two bits set the threshold below IBAT_OCP where the part starts regulation 00: 200 mA below IBAT_OCP setting (default) 01: 300 mA below IBAT_OCP setting 10: 400 mA below IBAT_OCP setting 11: 500 mA below IBAT_OCP setting
6	SET_IBATREG0	R/W	0h	N/A	
5	SET_VBATREG1	R/W	0h	N/A	This two bits set the threshold below VBAT_OVP where the part starts regulation 00: 50 mV below VBAT_OVP setting (default) 01: 100 mV below VBAT_OVP setting 10: 150 mV below VBAT_OVP setting 11: 200 mV below VBAT_OVP setting
4	SET_VBATREG0	R/W	0h	N/A	
3	VBATREG_ACTIVE_STAT	R	0h	N/A	This bit is set when VBATREG is active
2	IBATREG_ACTIVE_STAT	R	0h	N/A	This bit is set when IBATREG is active
1	VDROP_OVP_STAT	R	0h	N/A	This bit is set when VDROP_OVP is active
0	VOUT_OVP_STAT	R	0h	N/A	This bit is set when VOUT_OVP is active

**Table34. REG_FLAG_MASK Register (Address=2Dh) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBATREG_ACTIVE_FLAG	R	0h	N/A	Indicates a VBAT regulation event has occurred
6	IBATREG_ACTIVE_FLAG	R	0h	N/A	Indicates a IBAT regulation event has occurred
5	VDROP_OVP_FLAG	R	0h	N/A	Indicates a VDROP OVP event has occurred
4	VOUT_OVP_FLAG	R	0h	N/A	Indicates a VOUT OVP event has occurred
3	VBATREG_ACTIVE_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
2	IBATREG_ACTIVE_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
1	VDROP_OVP_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
0	VOUT_OVP_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked



Table35. DEGLITCH Register (Address=2Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBUS_UCP_FALL_DEGLITCH_SET	R/W	0h	N/A	This bit sets the deglitch time for IBUS_UCP_FALL 0: 10us (default) 1: 5ms
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table36. PMID2OUT_OVP_UVP (Address=2Fh) [reset=50h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	PMID2OUT_UVP_F LAG	R	0h	N/A	PMID/2-VOUT under-voltage flag. An INT is sent and CHG_EN bit is set to '0' when this event happens. This bit is cleared when read.
2	PMID2OUT_OVP_F LAG	R	0h	N/A	PMID/2-VOUT over-voltage flag. An INT is sent when this event happens, and is cleared when read.
1	PMID2OUT_UVP_S TAT	R	0h	N/A	PMID/2-VOUT under-voltage status.
0	PMID2OUT_OVP_ STAT	R	0h	N/A	PMID/2-VOUT over-voltage status.



Table37. IBUS_REGULATION (Address=30h) [reset=08h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_REG_EN	R/W	0h	N/A	0: Disable the IBUS regulation (default) 1: Enable the IBUS regulation
6	IBUS_REG_ACTIVE_STAT	R	0h	N/A	Indicates the part is in the IBUSREG status
5	IBUS_REG_ACTIVE_FLAG	R	0h	N/A	Indicates the part has entered the IBUSREG status
4	IBUS_REG_ACTIVE_MASK	R/W	0h	N/A	0 = Not Masked; 1 = Masked
3	IBUS_REG[3]	R/W	1h	2A	IBUS regulation value setting. When the IBUS regulation loop is active, an INT is sent. Offset: 1A Range: 1A (b0000) – 4.75A (b1111) Default: 3A (b1000)
2	IBUS_REG[2]	R/W	0h	1A	
1	IBUS_REG[1]	R/W	0h	500mA	
0	IBUS_REG[0]	R/W	0h	250mA	

Table38. MODE (Address=31h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	MODE	R/W	0h	N/A	This bit decides the operation mode 0 = 2:1 charger mode (default) 1 = 1:1 charger mode

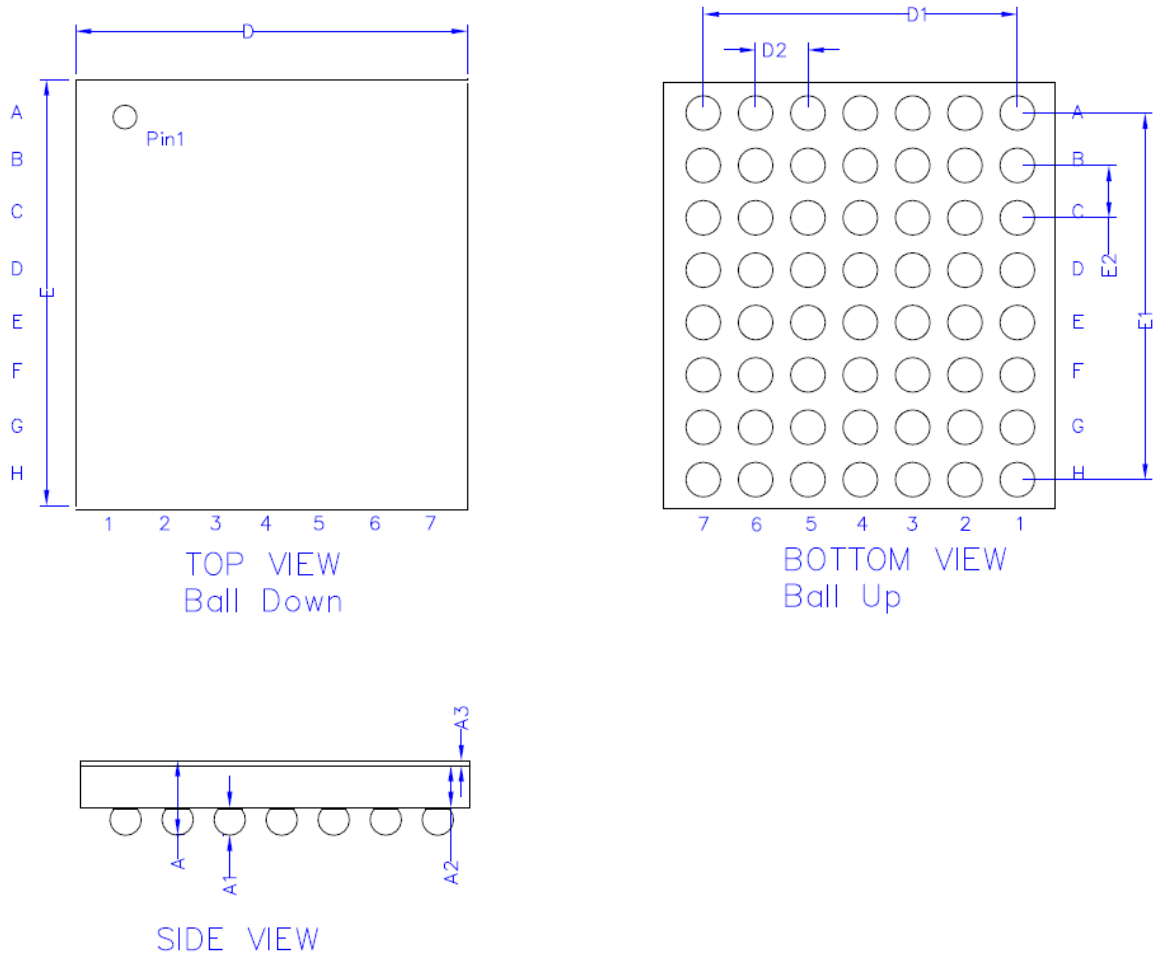
Table39. VBUS_INRANGE_DIS (Address=35h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	VBUS_INRANGE_DIS	R/W	0h	N/A	0: Enable the VBUS_IN_RANGE protection (default) 1: Disable the VBUS_IN_RANGE protection
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table40. OVPGATE_DIS (Address=36h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	OVPGATE_DIS	R/W	0h	N/A	0: Enable the OVPGATE block (default) 1: Disable the OVPGATE block
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

10 MECHANICAL DATA



	No.	Mean	Tolerance
Total Thickness	A	0.574	±0.0405
Ball Height+UBM Thickness	A1	0.216	±0.023
Wafer/Grinding Thickness	A2	0.318	±0.0125
Backside Coating Thickness	A3	0.040	±0.005
PKG Die size	X	D	2.995 ±0.025
	Y	E	3.255 ±0.025
Ball size after reflow	F	0.265	±0.020
Ball Pitch	D1	2.400	NA
	D2	0.400	NA
	E1	2.800	NA
	E2	0.400	NA