

High-Power Full-Bridge Power Stage for High-Integration, High-Efficiency Wireless Power Transmitter

1 Descriptions

The SC5025Q is a new generation of analog-front-end, designed for high-integration, high-efficiency wireless power transmitter solution. It integrates all critical function modules, such as full-bridge power stage with low-RDS(on) MOSFETs, gate drivers, bootstrap circuits, voltage regulator for power supply, current sense amplifier, communication demodulators and Q-factor-detection circuit. The SC5025Q can cooperate with a digital controller to create a high-performance high-power wireless power transmitter system.

The wireless power transmitter system supports foreign object detection (FOD) by continuously monitoring the amount of power transferred and comparing it to the amount of received power, as reported by the power receiver. In order to do this, the SC5025Q measures the input DC current very accurately using a current sense amplifier. Besides, the SC5025Q supports input under-voltage lockout (UVLO), input over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP). The protections significantly enhance the reliability of the whole wireless power transmitter system.

The SC5025Q is available in a compact 5mm x 4mm QFN package.

2 Features

- AEC-Q100 Grade 1
- Input voltage range: 1V-26V
- Support high power transfer
- Integrated four 12mohm $R_{DS(on)}$ power MOSFETs
- Integrated FET drivers and bootstrap circuits
- Integrated 5V voltage regulator
- Support external VDD power supply
- Integrated accurate current sense for FOD
- Integrated voltage and current demodulators
- Integrated reliable Q-factor-detection circuit
- UVLO/OVP/OCP/OTP
- I2C Interface
- Support programmable I2C address
- INT pin for fault indication
- 5mm x 4mm QFN package

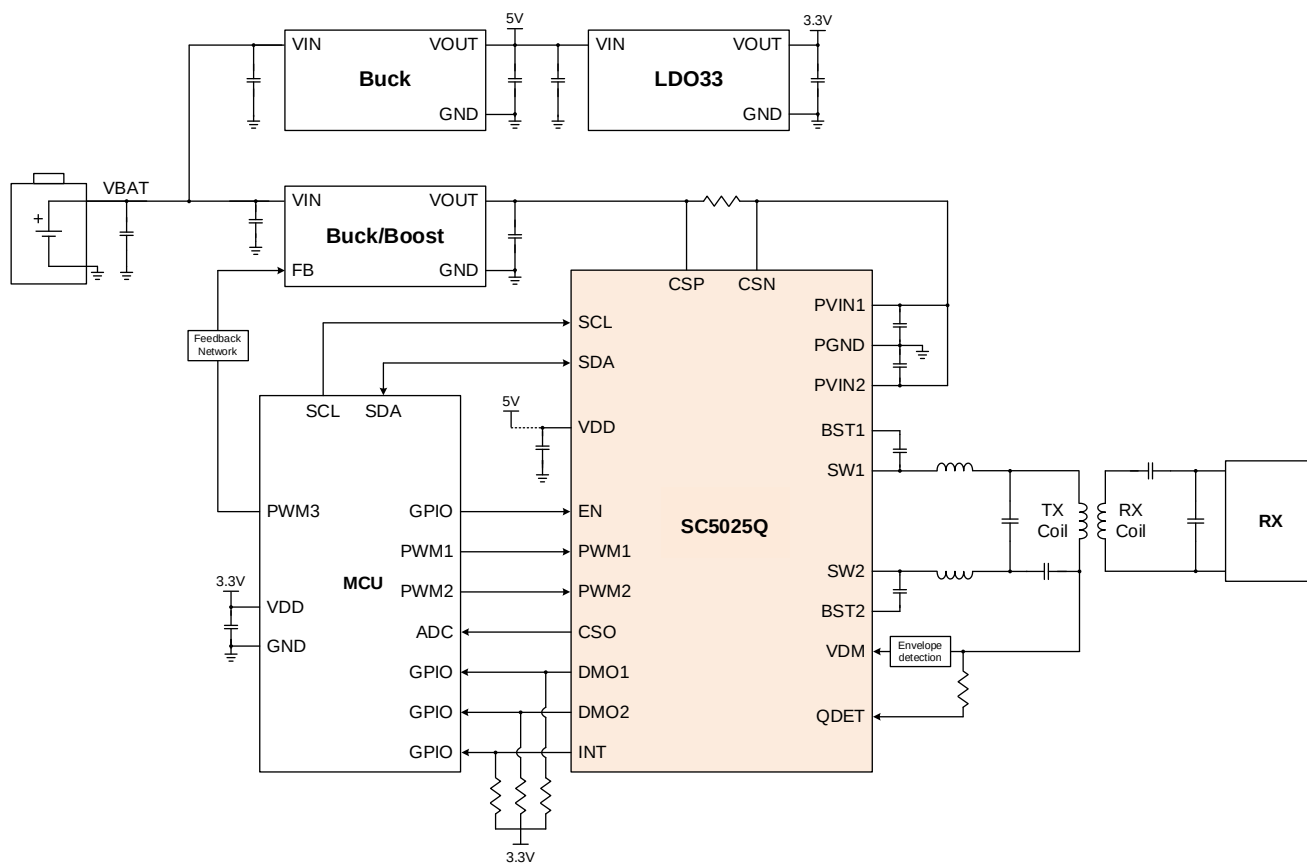
3 Applications

- WPC Compliant Wireless Power Transmitters
- Proprietary Wireless Power Transmitters

4 Device Information

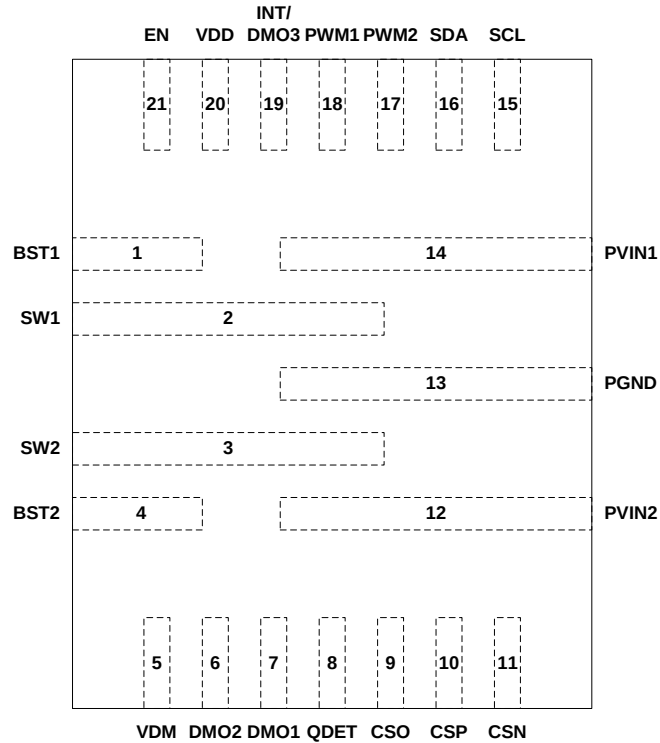
Part Number	Package	Dimension
SC5025QQFMR	FCQFN21L	5mm x 4mm x 0.75mm

5 Typical Application Circuit





6 Terminal Configuration and Functions



(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	BST1	PWR	High-side gate driver bootstrap rail. Connect a 0.1μF ceramic capacitor between the BST1 and SW1 pins.
2	SW1	PWR	Switching node of the half bridge MOSFETs Q1 and Q2.
3	SW2	PWR	Switching node of the half bridge MOSFETs Q3 and Q4.
4	BST2	PWR	High-side gate driver bootstrap rail. Connect a 0.1μF ceramic capacitor between the BST2 and SW2 pins.
5	VDM	I	Voltage demodulation pin for data packets based on coil voltage variation.
6	DMO2	O	Output of the average current demodulation or peak current demodulation according to the register configuration. This pin is simultaneously used as IIC address detection.
7	DMO1	O	Output of the voltage demodulation in default. It can also be configured as either average current or peak current demodulation output. This pin is simultaneously used as IIC address detection.
8	QDET	I	Quality factor detection input.



9	CSO	O	Current sense amplifier output.
10	CSP	I	Positive end of the current sense amplifier.
11	CSN	I	Negative end of the current sense amplifier.
12	PVIN2	PWR	Input voltage of half-bridge MOSFETs Q3 and Q4. A ceramic capacitor of 22 μ F or more is required between this pin and the PGND pin.
13	PGND	GND	Power ground.
14	PVIN1	PWR	Input voltage of half-bridge MOSFETs Q1 and Q2. A ceramic capacitor of 22 μ F or more is required between this pin and the PGND pin.
15	SCL	I	I2C interface serial clock line.
16	SDA	I/O	I2C interface serial data line.
17	PWM2	I	By default, PWM logic input for the Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns on the high-side FET Q3 and turns off the low-side FET Q4; logic LOW turns on the low-side FET Q4 and turns off the high-side FET Q3.
18	PWM1	I	By default, PWM logic input for the Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns on the high-side FET Q1 and turns off the low-side FET Q2; logic LOW turns on the low-side FET Q2 and turns off the high-side FET Q1.
19	INT/DMO3	O	Fault indication pin by default. When a certain internal fault happens, this pin is pulled down. It can also be configured as the third demodulation output pin.
20	VDD	I/O	Output of 5V LDO to power internal gate drivers and control circuits. It can also be configured as external power supply input pin. A ceramic capacitor of 2.2 μ F is required between this pin and the PGND pin.
21	EN	I	Enable pin. Logic high enables the IC and logic low disables the IC.



7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	PVIN1, PVIN2, SW1, SW2, CSP, CSN	-0.3	29	V
	BST1	-0.3	SW1+6	V
	BST2	-0.3	SW2+6	V
	DMO1, DMO2	-0.3	6	V
	VDM, CSO, SCL, SDA, PWM1, PWM2, INT, VDD, EN	-0.3	6	V
	QDET	-0.3	24	V
Differential Voltage range between terminals	CSP-CSN	-0.6	0.6	V
Temperature Range	Operating Junction, T _J	-40	150	°C
	Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		QFN-21 (5mm x 4mm)	UNIT
Θ _{JA}	Junction to ambient thermal resistance	38	°C/W
Θ _{JC}	Junction to case resistance	11.8	°C/W

- (1) Measured on JESD51-7, 4-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2000	2000	V
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-1000	1000	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V _{PVIN1} , V _{PVIN2}	Input voltage range ⁽¹⁾	4		26	V
V _{DD}	Power supply voltage range	4.75	5	5.25	V



C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 Ceramic Capacitor		22		μF
C_{BST1}, C_{BST2}	BST1-SW1, BST2-SW2 Ceramic Capacitor		0.1		μF
C_{VDD}	VDD Ceramic Capacitor		2.2		μF
T_J	Operating junction temperature	-40		150	$^{\circ}C$

(1) In the condition of external power supply, the lower limit of V_{PVIN} can be reduced to 1V.



7.5 Electrical Characteristic

$V_{PVIN1} = V_{PVIN2} = 20V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$, typical values are tested at room temperature, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{PVIN}	Operating input voltage	Internal VDD power supply	4		26	V
		External VDD power supply with 5V	1		26	V
V _{IN_UVLO}	Under voltage lockout threshold with internal VDD power supply	Rising edge		3.4		V
		Falling edge		3.15		V
V _{IN_OVP}	Input over-voltage protection	Rising edge		28		V
		Falling edge		24		V
I _Q	Quiescent current into PVIN	EN = high, no switching			0.5	mA
I _{SD}	Shutdown current into PVIN	EN = low, LDO active			160	μA
VOLTAGE REGULATOR						
V _{DD}	Internal voltage regulator output	V _{PVIN} = 5V, Cout = 2.2μF		4.75		V
		V _{PVIN} = 20V, Cout = 2.2μF	4.85	5	5.15	V
V _{DD_UVLO}	Under voltage lockout threshold for VDD	Rising edge		3.7		V
		Falling edge		3.5		
I _{VDD_LIM}	Output current capability of the voltage regulator	V _{PVIN} ≥ 5V, Cout = 2.2uF	30			mA
CURRENT SENSE AMPLIFIER						
I _{PVIN}	Input current range	Support 10V/5A RX	0		7	A
G _{CS}	Current sense gain	R _{CS} = 10mohm		50		V/V
		R _{CS} = 5mohm		100		V/V
V _{CS00}	CSO output offset voltage	Measured at the CSO pin, V _{CSP} = V _{CSN}		0.4		V
POWER SWITCH						
R _{DS(on)}	SW1 High-side MOSFET	V _{DD} = 5V		12		mΩ
	SW1 Low-side MOSFET	V _{DD} = 5V		12		mΩ
	SW2 High-side MOSFET	V _{DD} = 5V		12		mΩ
	SW2 Low-side MOSFET	V _{DD} = 5V		12		mΩ
SHORT CIRCUIT PROTECTION						
I _{LIM}	High-side current limit threshold	High limit	14.4	16	17.6	A
		Low limit	11.6	13	14.4	A
T _{OCP}	Hiccup period			40		ms
CNT _{OCP}	Peak OCP deglitch count	Programmable		2 / 4		
Full Bridge Driver						
T _{dead}	High side off to low side on & Low side off to high side on	Programmable		40/60/80 /100/120 /140/160 /180		ns



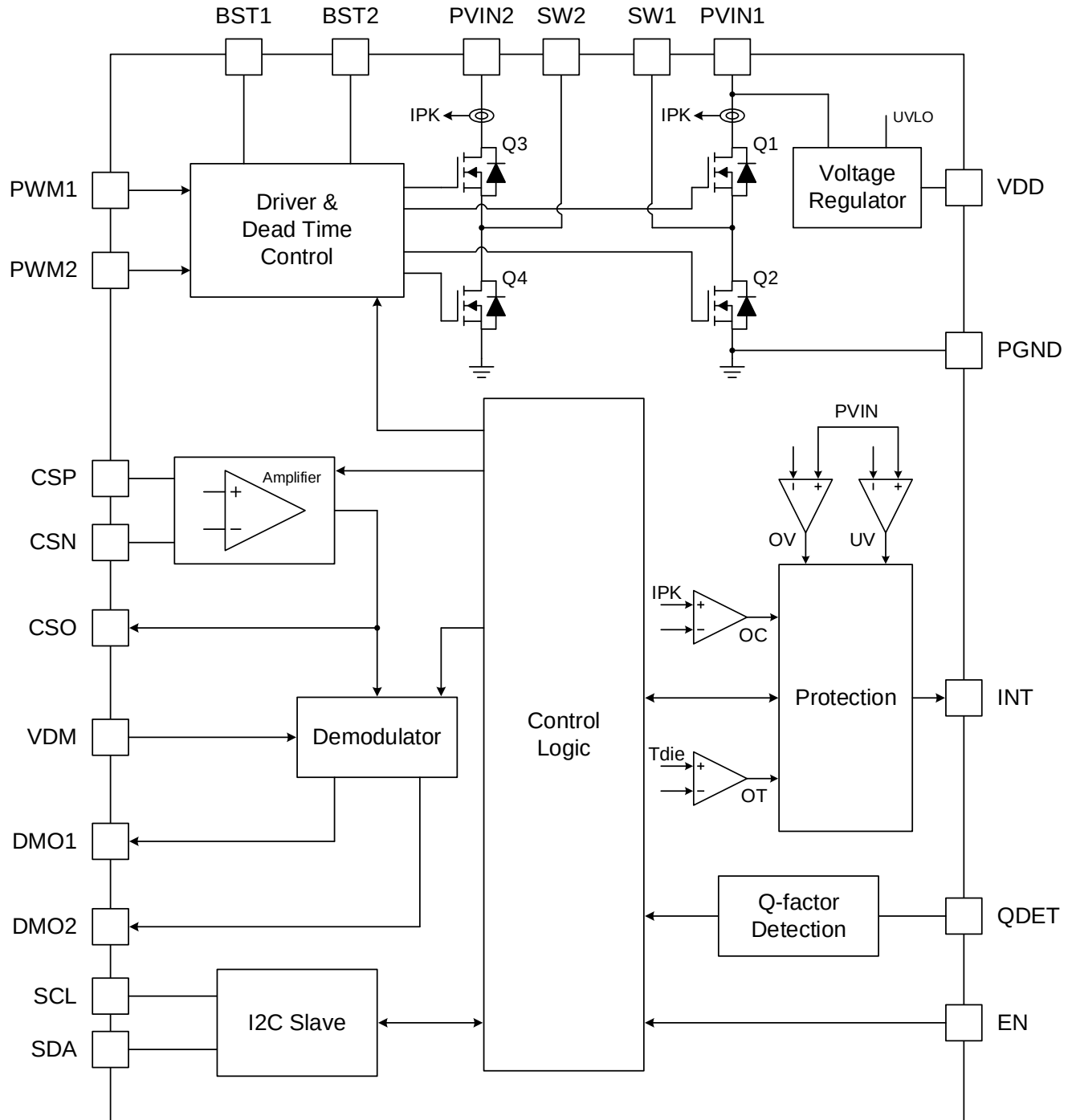
Voltage Demodulation				
V _{VDM_H}	VDM input high logic based on offset	Programmable	10/40	mV
V _{VDM_L}	VDM input low logic based on offset	Programmable	-10/-40	mV
G _{VDM}	VDM analog signal AC gain	Programmable	2/4/8/16	V/V
Current Demodulation				
V _{IDM_H}	IDM input high logic based on offset (Average & Peak)	Programmable	10/40	mV
V _{IDM_L}	IDM input low logic based on offset (Average & Peak)	Programmable	-10/-40	mV
G _{IDM}	IDM analog signal AC gain	Programmable	2/4/8/16	V/V
QDET				
V _{Q_BIAS}	Bias voltage for QDET	High Bias Voltage	2.4	V
		Low Bias Voltage	2	V
V _{Q_H}	Quality factor detection high threshold	Programmable	400/200	mV
V _{Q_L}	Quality factor detection low threshold	Programmable	100/25	mV
R _{Q_L}	Quality factor detection internal resistor	Programmable	12.5/50/ 100/250	KΩ
F _{QCLC}	Quality factor detection OSC		8	MHz
I2C (SCL, SDA)				
V _{I2C_IH}	I2C input high logic		1.1	V
V _{I2C_IL}	I2C input low logic		0.65	V
I _{I2C_LKG}	I2C pins leakage		-1 1	uA
V _{I2C_OL}	I2C output low logic	Sink = 3mA	0.35	V
F _{SCL}	SCL frequency		0 400	KHz
T _{SCL_L}	Low level cycle of SCL		1.3	us
T _{SCL_H}	High level cycle of SCL		0.6	us
C _B	Capacitive load for SCL and SDA		150	pF
C _I	SCL, SDA input capacitance		5	pF
EN				
V _{EN_H}	EN input high logic		1.8	V
V _{EN_L}	EN input low logic		0.5	V
R _{EN}	EN pin internal pull down resistance		470	KΩ
PWM1, PWM2				
V _{PWM_H}	PWM input high logic		1.8	V
V _{PWM_L}	PWM input low logic		0.5	V



R _{PWM}	PWM pin internal pull down resistance		470	KΩ
INT / DMO3				
R _{INT}	INT pin pulled low resistance		10	Ω
I _{INT_LKG}	INT pin leakage	Pulled up externally	-1 1	μA
DMO1, DMO2				
R _{DMO}	DMO pins pulled low resistance		10	Ω
I _{DMO_LKG}	DMO pins leakage	Pulled up externally	-1 1	μA
THERMAL SHUTDOWN				
T _{SD}	Thermal shutdown temperature		160	°C
	Thermal shutdown hysteresis		30	°C



8 Functional Block Diagram



9 Feature Description

9.1 Enable and UVLO Logic

The EN logic determines whether the chip is enabled or not, and the UVLO function protects the chip from operating with insufficient power supply.

By default, the power of chip comes from the input voltage source. When the PVIN pin voltage rises above 3.4V, the integrated voltage regulator is enabled at once and generates voltage at the VDD pin. It should be noted that the voltage regulator is not controlled by the EN logic. And when the PVIN pin voltage falls below 3.2V, the voltage regulator is disabled.

When the EN pin voltage exceeds the high threshold of 1.4V, the chip is enabled. At this time, if the VDD pin voltage exceeds the high threshold of 3.7V, the full-bridge power stage is allowed to respond to the control logic which is based on PWM mode selection and external PWM signals. When the VDD pin voltage falls below 3.5V, the power stage will ignore the control logic and be shut down, where all four FETs are closed.

Except for the voltage regulator, other analog circuits of the chip will be disabled when the EN pin voltage is below the low threshold of 0.5V. At this time, there are two options for full-bridge control. By default, the power stage is shut down completely where all four FETs are turned off. When the EN_FB_CTR bit is set to "1", the two switching nodes will be pulled to GND by turning on the two low-side FETs, while turning off the two high-side FETs.

9.2 Power Supply

The SC5025Q supports two power supply modes: internal power supply and external power supply.

In the internal power supply application, the chip is powered by the integrated voltage regulator. The regulator is connected to PVIN and generates regulated 5V voltage at the VDD pin. The output current capability of the regulator is about 30mA, which is sufficient to power internal gate drivers and control circuits. It is recommended to place a decoupling ceramic capacitor of 2.2uF between the VDD pin and power ground, which is in close proximity to the chip.

In the external power supply application, the chip is powered by the external voltage source having a range from 4.75V to 5.25V. At this time, the minimum input voltage can be reduced to 1V. In this mode, the EX_VDD_EN bit must be set to 1 before the PVIN voltage rises.

9.3 PWM Control

Mode 0 (Normal Mode): When the PWM-mode bit is set to "0", the PWM control logic enters mode 0. The PWM1 input controls internal FETs Q1 and Q2, and the PWM2 input controls internal FETs Q3 and Q4, as shown in the functional block diagram. The logic high of PWM input turns on the high side FET and turns off the low side FET. The logic low of PWM input turns on the low side FET and turns off the high side FET. The PWM1 and PWM2 can independently control the SW1 and SW2 duty cycle and frequency. Please be noted that the dead time between Q1 (or Q3) and Q2 (or Q4) can be implemented internally, so there is no need for dead time in external control signals PWM1 and PWM2.

Mode 1 (Parallel Mode): When the PWM-mode bit is set to "1", the PWM control logic enters mode 1. At this time, the PWM1 input controls the whole full bridge, and the PWM2 input is ignored. In this mode, the logic high of PWM1 input turns on the two high-side FETs Q1 and Q3, while turning off the two low-side FETs Q2 and Q4. The logic low of PWM1 input turns on the two low-side FETs Q2 and Q4, while turning off the two high-side FETs Q1 and Q3.

When the chip goes through a POR (Power-on Reset) event, Mode 0 is selected by default. The operation frequency of power stage can support up to 500KHz in both modes.

9.4 Current Sense

The SC5025Q has a accurate current sense circuit consisting of external sense resistor and internal amplifier. It measures the average input current of the full bridge with $\pm 1\%$ accuracy and generates a proportional voltage directly at the CSO pin. The voltage information can be employed by the transmitter controller to implement foreign object detection and over-current protection.

To ensure the accuracy of current sense, the recommended sense resistor is of 5mΩ or 10mΩ, and the integrated amplifier has a typical voltage gain of 100/50 (selectable). When the sensed current is zero, the amplifier output has a typical 0.4V offset voltage at the CSO pin, which is optimized specially. For accurate measurement of the input average current, the transmitter controller need to calibrate this offset.

9.5 Q Factor Detection

The SC5025Q integrates a low-cost and reliable Q-factor-detection circuit to implement foreign object detection before the digital ping. In the approach, a pulse of energy is injected into the resonant tank, and the decay of the ringing response is measured to obtain the quality factor.

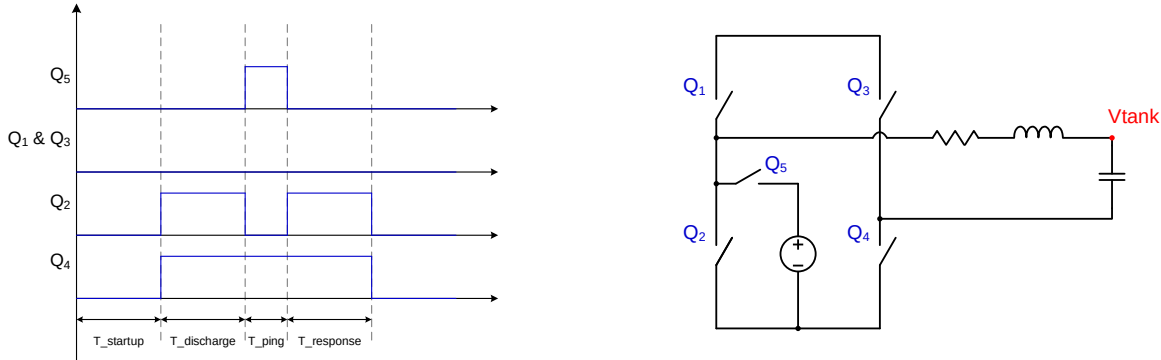


Figure 1. Implementation of Q factor detection

For most wireless power transmitters, a possible implementation of Q factor detection is provided in Figure 1. In general, the overall process can be divided into four different phases.

T_startup: During this time, the internal Q-factor-detection circuit is initialized.

T_discharge: Discharge the resonant capacitor, and thus establish the initial conditions for the next phase.

T_ping: A pulse of energy from the bias voltage source is injected into the resonant tank.

T_response: Free oscillation of the resonant tank comes out, which is then sampled and processed.

A typical oscillation waveform in the Q factor detection process is shown in Figure 2. The Q factor of the resonant tank can be calculated as follows:

$$Q = \frac{\pi * (CNT/2)}{\ln \frac{V_{Q,H}}{V_{Q,L}}}$$

In the formula, CNT is the number of zero-crossing points happening at the interval where the oscillation peak voltage at the QDET pin is between the high and low thresholds.

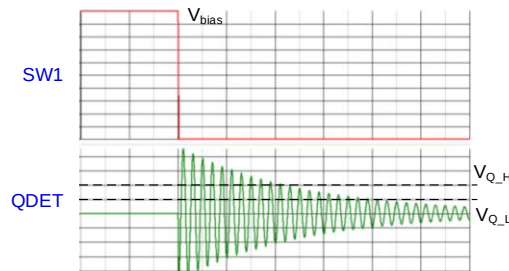


Figure 2. Q factor detection oscillation waveform



9.6 Voltage and Current Demodulation

To ensure the quality of communication, the SC5025Q integrates three demodulation schemes that are based on coil peak voltage information, input average current information and input peak current information respectively.

The voltage-mode envelope detector is implemented using a discrete solution as depicted in Figure 3. This simple circuit achieves the envelope detector function and the low-pass filter function, as well as the DC filter function at the same time. The envelope detector applies the analog signal to the VDM pin. The signal is subsequently processed and employed by the chip to do the demodulation.

The current-mode detector is implemented with the integrated current sense circuit. The chip can obtain the input average current information and input peak current information from the current sense circuit, and then do the demodulation.

There are four selectable options for demodulation results output, as depicted in Table 1.

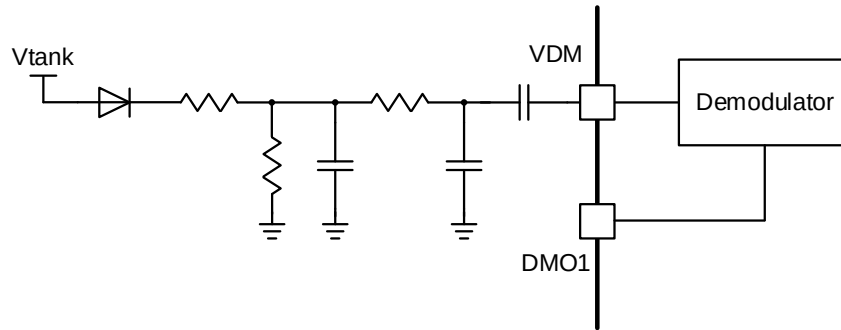


Figure 3. Voltage demodulation scheme

Table 1. Demodulation results output (DMO1&DMO2)

Register Setting	DMO1	DMO2
00	Voltage	Average Current
01	Voltage	Peak Current
10	Average Current	Peak Current
11	Peak Current	Average Current

Except for DMO1 and DMO2 pins, the INT pin can be configured as the third demodulation output pin, which can transmit any demodulation information of the three schemes. The output options of the DMO3 pin is depicted in Table 2.

Table 2. Demodulation results output (DMO3)

Register Setting	DMO3
00	Voltage
01	Average Current
1x	Peak Current



9.7 Programmable I2C Address

The SC5025Q supports programmable I2C address by detecting the differential voltage between DMO pins during the power on process. When the VDD pin voltage rises, the DMO1 and DMO2 pins are initially used as the I2C address selecting pins, which are then used as demodulation results output pins.

When powered on, the chip firstly generates two strands of current flowing from the DMO1 and DMO2 pins to GND. The two external pull-up resistors normally have the same value. However, the two strands of current have different values, and thus resulting in different DMO pin voltages. The differential voltage is then detected to determine the I2C address, as depicted in Figure 4. Once the I2C address is determined, the DMO1 and DMO2 pins disconnect with the current sources.

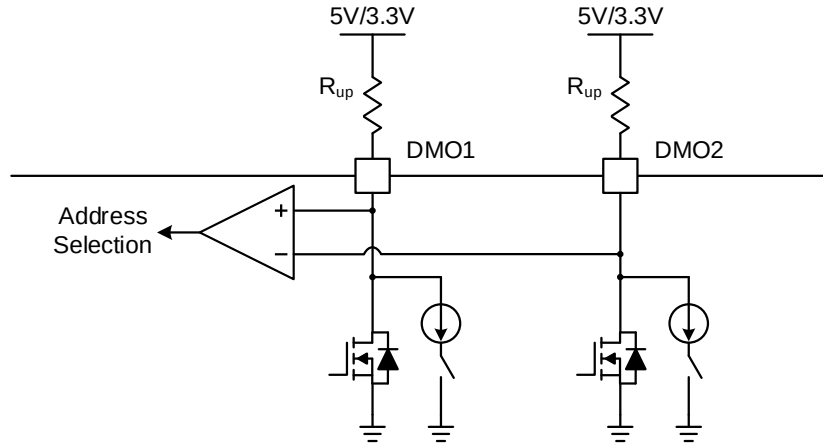


Figure 4. I2C Address Selection

Table 3 shows the relationship between the I2C address and the value of external pull-up resistance.

Table 3. I2C Address Setting

R_{up} Resistance (K Ω)*	I2C Address
2.49	0x42
7.5	0x43
13	0x44
18	0x45
*Two external pull-up resistors should have $\pm 1\%$ accuracy	

9.8 Protection Functions

The SC5025Q supports three kinds of protection functions to enhance the reliability of the whole wireless power transmitter system: Over Voltage Protection (OVP), Over Current Protection (OCP) and Over Temperature Protection (OTP). Once any of the above abnormal events occurs, the chip will terminate the switching of the power stage. And when the abnormal event ends, the chip will return to normal operation.

9.8.1 Over Voltage Protection

By detecting the voltage at the PVIN pins, the SC5025Q realizes a reliable over-voltage-protection function. The input voltage of the chip is sensed and compared to the thresholds. If the input voltage exceeds the high threshold of 28V, the power stage

will be shut down, where the two low-side FETs are turned on and the two high-side FETs are turned off. After the over-voltage fault is removed, the chip can return to normal.

9.8.2 Over Current Protection

The SC5025Q supports cycle-by-cycle current limit and hiccup mode for over current protection. The current of high side FETs Q1 and Q3 is sensed and compared to the current-limit threshold during every switching cycle. If the current exceeds the set threshold, the high side FET is turned off immediately and the low side FET is turned on in the present cycle. At this time, the normal PWM control logic is invalid.

When the sensed current reaches the threshold, the over-current fault counter is incremented. If the over-current fault of one high side FET occurs in two or four (selectable) consecutive cycles, the two high-side FETs are turned off and the two low side FETs are turned on regardless of the PWM control logic. The full-bridge power stage enters hiccup mode and attempts to restart after a time-out period of 40ms typically. The hiccup mode can reduce the average current greatly to alleviate the thermal issue in the over current condition. Once the over current fault is removed, the chip can return to normal.

9.8.3 Over Temperature Protection

The over temperature protection prevents the chip from operating at extremely high temperatures. During operation, when the silicon die temperature exceeds 160°C, the SC5025Q will be shut down, where the two low-side FETs are turned on and the two high-side FETs are turned off. And when the temperature falls below 130°C, the chip is enabled again.

9.9 Interrupt Function

The SC5025Q has an interrupt pin for fault indication, which is an open-drain output pin and an external pull-up resistor is needed. Once any fault event occurs, the INT pin will be pulled to low for 256us typically, as depicted in Figure 5. At this time, the UVLO, OVP, OCP, OTP or BST_UVP bit in the flag register will be set to “1” and stay latched.

When the digital controller receives the interrupt signal, it can read the flag register and respond accordingly. After the fault is removed, the related bits in the flag register will still be latched unless the corresponding bits in the clear-flag register are set to “1”. After the flag bits are cleared, the corresponding clear-flag bits should be set back to “0” for the next indication.

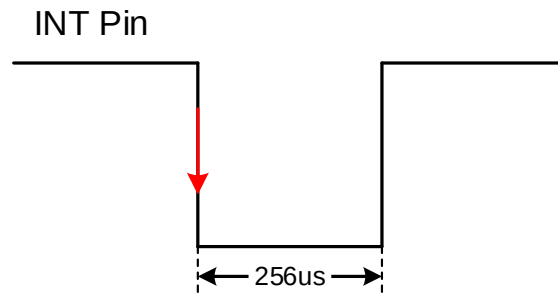


Figure 5. INT Pin Function



10 I2C Interface and Digital Register

The SC5025Q integrates I2C interface, and the followings are digital registers.

Table 1. Analog Register (0x00)

Bit	Field	Type	Default Value @ POR	Description
7	CS_AMP_Gain	R/W	0	Current Sense Amplifier Gain: 0: 50 1:100
6:5	Reserved	R/W	0	
4	EN_FB_CTR	R/W	0	EN Low Logic Controls the Full Bridge: 0: All FETs are truned off 1: Two high side FETs are truned off, and two low side FETs are truned on
3	PWM_Mode	R/W	0	PWM Control Mode: 0: Normal Mode 1: Parallel Mode
2	PK_CS_EN	R/W	0	Input Peak Current Sense Enable: 0: Disable peak current sense 1: Enable peak current sense
1	CS_AMP_EN	R/W	0	Current Sense Amplifier Enable: 0: Disable current sense amplifier 1: Enable current sense amplifier
0	EX_VDD_EN	R/W	0	External VDD Power Supply Enable: 0: Use the internal power supply 1: Use the external power supply

Table 2. Full Bridge Driver Register (0x01)

Bit	Field	Type	Default Value @ POR	Description
7:6	FB_Driver_Speed	R/W	01	Turned-off Speed of Four FETs: 00: Slow; 01: Fast; 10/11: Fastest;



5:3	FB_Dead_Time	R/W	011	Dead Time between High Side and Low Side FETs: 000: 40ns 001: 60ns 010: 80ns 011: 100ns 100: 120ns 101: 140ns 110: 160ns 111: 180ns
2	SW2_HIZ_EN	R/W	0	SW2 Half Bridge HIZ Enable 0: SW2 two FETs are in the normal state 1: SW2 two FETs are turned off
1	SW1_HIZ_EN	R/W	0	SW1 Half Bridge HIZ Enable 0: SW1 two FETs are in the normal state 1: SW1 two FETs are turned off
0	FB_HIZ_EN	R/W	0	Full Bridge HIZ Enable 0: Four FETs are in the normal state 1: Four FETs are turned off

Table 3. Demodulation Register 1 (0x02)

Bit	Field	Type	Default Value @ POR	Description
7	IAVDM_TH	R/W	0	Threshold of IAVDM Comparator: 0: $\pm 10\text{mV}$ 1: $\pm 40\text{mV}$
6:5	IAVDM_AC_Gain	R/W	0	IAVDM AC Signal Gain: 00: 2 01: 4 10: 8 11: 16
4	IAVDM_EN	R/W	0	Average Current Demodulator Enable: 0: Disable average current demodulator 1: Enable average current demodulator
3	VDM_TH	R/W	0	Threshold of VDM Comparator: 0: $\pm 10\text{mV}$ 1: $\pm 40\text{mV}$
2:1	VDM_AC_Gain	R/W	0	VDM AC Signal Gain: 00: 2 01: 4 10: 8 11: 16
0	VDM_EN	R/W	0	Peak Voltage Demodulator Enable: 0: Disable peak voltage demodulator



				1: Enable peak voltage demodulator
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Table 4. Demodulation Register 2 (0x03)

Bit	Field	Type	Default Value @ POR	Description
7:6	Reserved	R/W	0	
5	VDM_Bypass_EN	R/W	0	VDM AC Signal Bypass Enable: 0: Disable bypass, with AC gain 1: Enable bypass, initial signal
4	Reserved	R/W	0	
3	IPKDM_TH	R/W	0	Threshold of IPKDM Comparator: 0: $\pm 10\text{mV}$ 1: $\pm 40\text{mV}$
2:1	IPKDM_AC_Gain	R/W	0	IPKDM AC Signal Gain: 00: 2 01: 4 10: 8 11: 16
0	IPKDM_EN	R/W	0	Peak Current Demodulator Enable: 0: Disable peak current demodulator 1: Enable peak current demodulator

Table 5. Demodulation Register 3 (0x04)

Bit	Field	Type	Default Value @ POR	Description
7:5	Reserved	R/W	0	
4:3	DMO3_Output	R/W	00	Options for Demodulation Results Output at DMO3: 00: VDM 01: IAVDM 1x: IPKDM
2	DMO3_EN	R/W	0	INT Pin Used as DMO3 Enable: 0: INT pin used as INT function 1: INT pin used as DMO function



1:0	DMO12_Output	R/W	00	Options for Demodulation Results Output at DMO1 & DMO2: 00: DMO1-VDM; DMO2-IAVDM 01: DMO1-VDM; DMO2-IPKDM 10: DMO1-IAVDM; DMO2-IPKDM 11: DMO1-IPKDM; DMO2-IAVDM
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Table 6. QDET Register 1 (0x05)

Bit	Field	Type	Default Value @ POR	Description
7	QCAP_EN	R/W	0	QDET Comparator Enable: 0: Disable QDET comparator 1: Enable QDET comparator
6	QBIAS_EN	R/W	0	QDET Bias Voltage Source Enable: 0: Disable bias 1: Enable bias
5	QDET_EN	R/W	0	QDET Logic Enable: 0: Disable QDET Logic 1: Enable QDET Logic
4:3	QDET_R	R/W	01	QDET Internal Pull-down Resistance Selection: 00:12.5K 01: 50K 10: 100K 11: 250K
2	QDET_L	R/W	0	QDET Low Threshold Selection: 0: 100mV 1: 25mV
1	QDET_H	R/W	0	QDET High Threshold Selection: 0: 200mV 1: 400mV
0	QDET_Bias	R/W	0	QDET Bias Voltage Selection: 0: 2V



				1: 2.4V
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Table 7. QDET Register 2 (0x06)

Bit	Field	Type	Default Value @ POR	Description
7:0	QDET_CNT	R	0000 0000	The number of zero-crossing points between thresholds

Table 8. QDET Register 3 (0x07-0x08)

Bit	Field	Type	Default Value @ POR	Description
15:0	QDET_CAP	R	0000 0000	The length of time captured between thresholds

Table 9. Protection Register (0x09)

Bit	Field	Type	Default Value @ POR	Description
7:6	Reserved	R/W	0	
5	Reserved	R/W	1	Force set '1'
4	OCP_CNT	R/W	0	OCP Fault Counter Setting: 0: 2 1: 4
3	OCP_TH	R/W	0	High-Side FETs Over Current Protection Threshold: 0: 13A 1: 16A
2	OCP_EN	R/W	0	High-Side FETs Over Current Protection Enable: 0: Disable over-current detection 1: Enable over-current detection
1	OVP_FB_EN	R/W	0	Full Bridge Takes Action after OVP Enable: 0: Disable OVP action (only INT pin indication) 1: Enable OVP action
0	OVP_EN	R/W	0	Over-Voltage Protection Enable: 0: Disable over-voltage detection 1: Enable over-voltage detection



Table 10. Flag Register (0x0A)

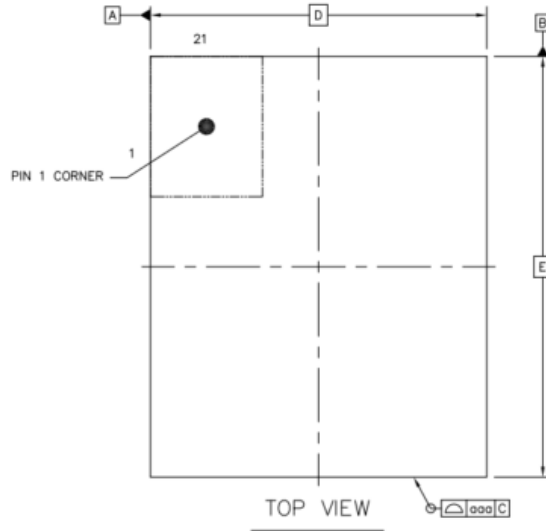
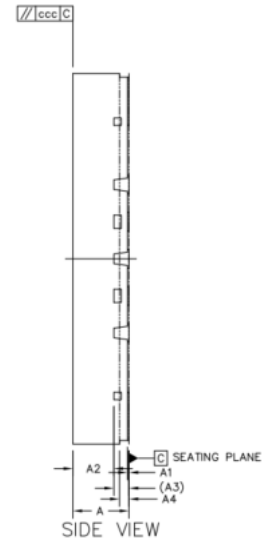
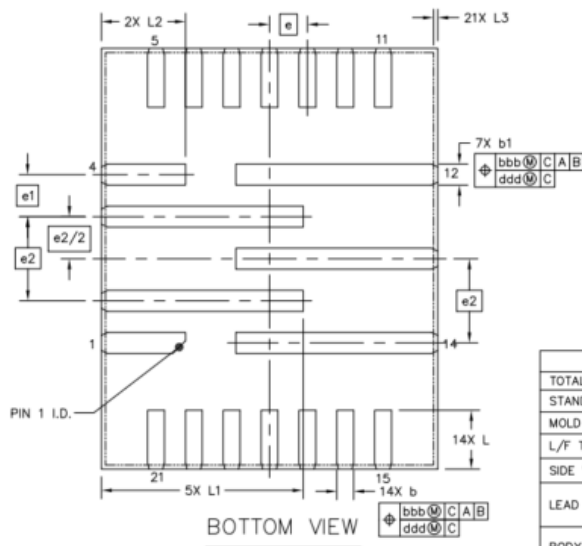
Bit	Field	Type	Default Value @ POR	Description
7:5	Reserved	R	0	
4	OTP_FLAG	R	0	Over Temperature Protection flag
3	OCP_FLAG	R	0	Over Current Protection Flag
2	VIN_OV_FLAG	R	0	PVIN Over Voltage Flag
1	VIN_UV_FLAG	R	0	PVIN Under Voltage Flag
0	BST_UV_FLAG	R	0	BST1 or BST2 Under Voltage Flag

Table 11. Clear Flag Register (0x0B)

Bit	Field	Type	Default Value @ POR	Description
7:5	Reserved	R	0	
4	OTP_CLR	W	0	Over Temperature Protection Flag Clear
3	OCP_CLR	W	0	Over Current Protection Flag Clear
2	VIN_OV_CLR	W	0	PVIN Over Voltage Flag Clear
1	VIN_UV_CLR	W	0	PVIN Under Voltage Flag Clear
0	BST_UV_CLR	W	0	BST1 or BST2 Under Voltage Flag Clear

MECHANICAL DATA

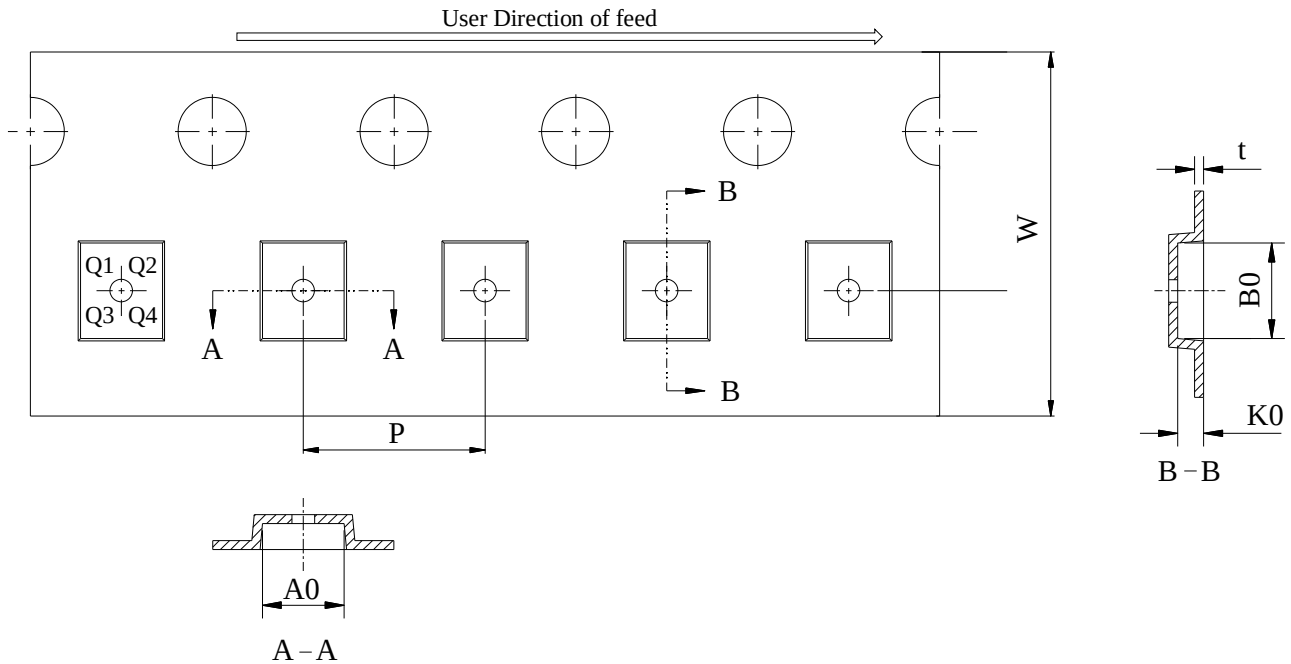
QFN 21 (5mm x 4mm x 0.75mm)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3	0.203 REF		
SIDE WETTABLE DEPTH	A4	0.075	---	0.18
LEAD WIDTH	b	0.15	0.2	0.25
	b1	0.2	0.25	0.3
BODY SIZE	X	4 BSC		
	Y	5 BSC		
LEAD PITCH	e	0.45 BSC		
	e1	0.5 BSC		
LEAD LENGTH	L	0.6	0.7	0.8
	L1	2.3	2.4	2.5
LEAD LENGTH	L2	0.9	1	1.1
	L3	0.01	---	0.09
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
LEAD OFFSET	bbb	0.1		
	ddd	0.05		

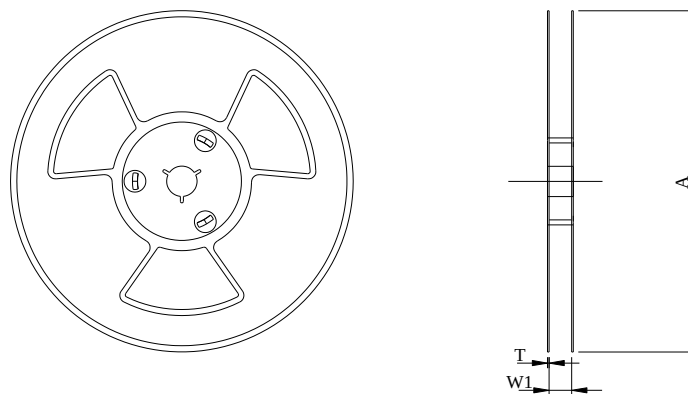
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 +0.30/-0.10	8.00 ± 0.10	4.25 ± 0.05	5.25 ± 0.05	1.02 ± 0.05	0.25 ± 0.02	Q1

REEL



Item	A	W1	T
Size (mm)	330 ± 1.0	12.4 +1/-0	2.6 ± 0.15



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