SC77401Q Quad-Channel 160mΩ Smart High Side Driver with Advanced Protections

1 Descriptions

The SC77401Q is a fully-protected quad-channel smart high-side switch with integrated 160mΩ MOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load.

2 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C4B
- Quad-Channel 160mΩ Smart High-Side Switch with Full Diagnostics
  - Version A: Open-drain digital output
  - Version B: Current-sense analog output
- Wide Operating Voltage 3.4 to 40V
- Ultralow Standby Current < 500 nA
- Operating Junction Temperature: –40 to 150°C
- Input Control, 3.3-V and 5-V Logic Compatible
- High Accuracy Current Sense: ±15% Under >25mA Load
- Adjustable Current Limit with External Resistor, ±15% Under >500 mA Load
- Protection:
  - Short-to-GND Protection by Current Limit (Internal or External)
  - Thermal Shutdown with Latch-off or Auto-retry Option
  - Thermal Swing Shutdown
  - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
  - Loss of GND and Loss of Battery Protection
  - Undervoltage lockout (UVLO) protection
- Diagnostics:
  - Open detection and short-to-battery detection in OFF state
  - Overload and short to ground detection in ON state

3 Applications

- High-side power switch for sub-module
- Power switch for low-wattage lamp
- High-side relays and solenoids
- General resistive, inductive, and capacitive loads

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4 Device Information

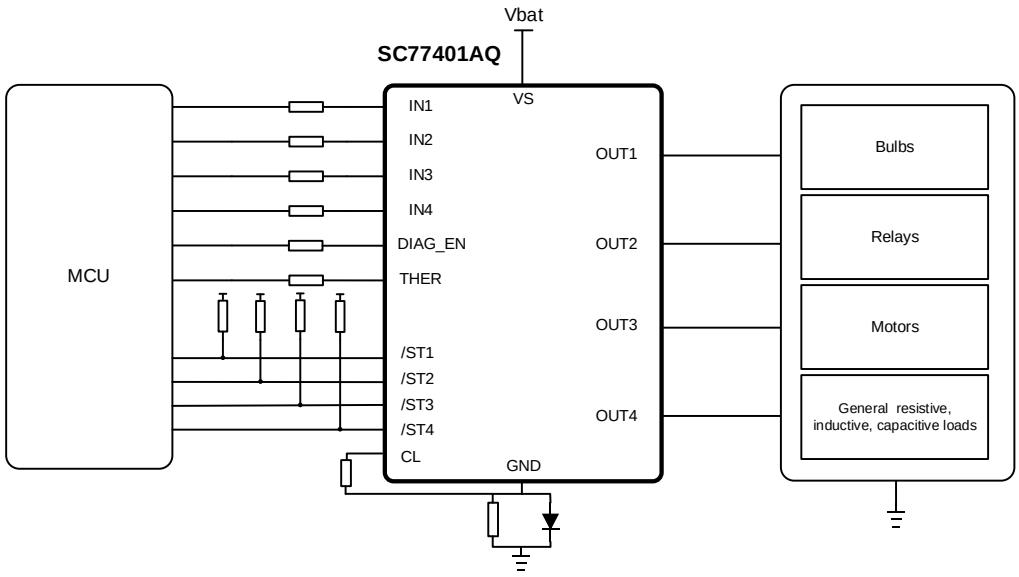
ORDER NUMBER	DESCRIPTION	PACKAGE	BODY SIZE
SC77401AQSTER	Open Drain Digital Output	eTSSOP-28	9.7mm x 6.4 mm x 1.2mm
SC77401BQSTER	Current Sense Analog Output	eTSSOP-28	9.7mm x 6.4 mm x 1.2mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
1.0	2025.4	New	Newly released.
1.1	2025.5	10-15	Add chapter 9,10
1.1.1	2025.9	5	8.3 Recommended Operating Conditions 1. "$I_{OUT,NOM}$" Updated (Typ./Max.:2.5A / NA → Typ./Max. :NA / 2.5A)

6 Typical Application Circuit



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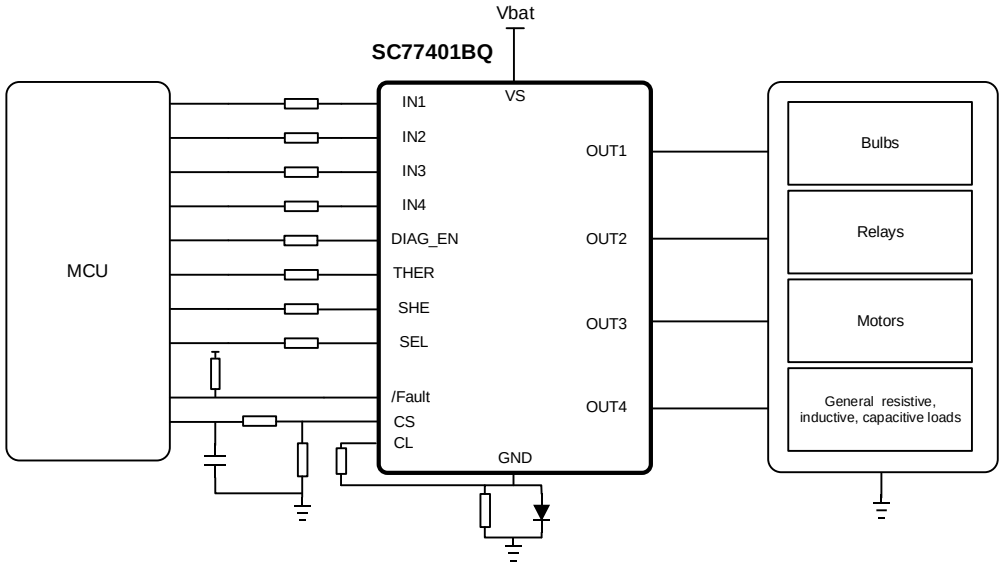
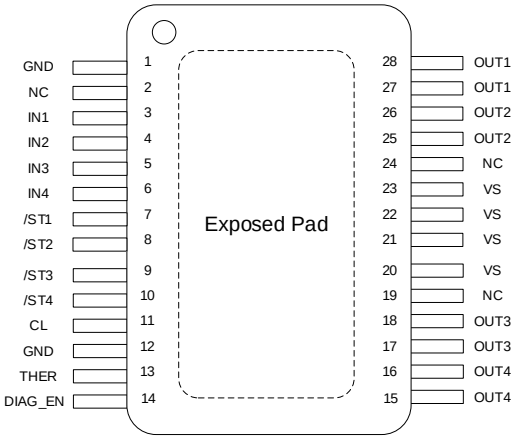


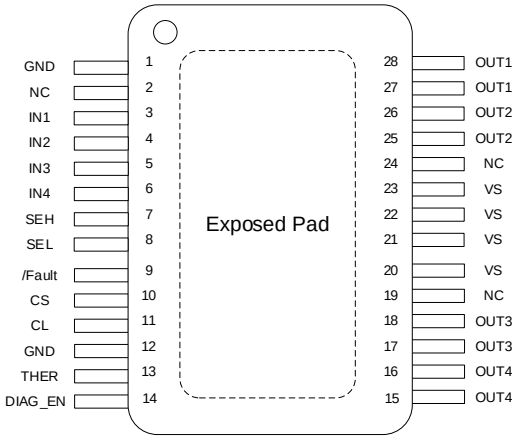
Figure 6-1. Typical Application Circuit

7 Terminal Configuration and Functions

TOP VIEW



Version A



Version B

TERMINAL				I/O	DESCRIPTION
Version A		Version B			
NUMBER	NAME	NUMBER	NAME		
1	GND	1	GND	-	Ground pin.

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2	NC	2	NC	-	Not Connected.
3	IN1	3	IN1	I	Input control for channel 1 activation; internal pull down
4	IN2	4	IN2	I	Input control for channel 2 activation; internal pull down
5	IN3	5	IN3	I	Input control for channel 3 activation; internal pull down
6	IN4	6	IN4	I	Input control for channel 4 activation; internal pull down
7	/ST1	/		O	Open-drain diagnostic status output for channel 1
8	/ST2			O	Open-drain diagnostic status output for channel 2
9	/ST3			O	Open-drain diagnostic status output for channel 3
10	/ST4			O	Open-drain diagnostic status output for channel 4
/		7	SEH	I	CS channel-selection high bit; internal pulldown
		8	SEL	I	CS channel-selection low bit; internal pulldown
		9	/FAULT	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions
		10	CS	O	Current-sense output
11	CL	11	CL	O	Adjustable current limit. Connect to device GND if external current limit is not used.
12	GND	12	GND	-	Ground pin
13	THER	13	THER	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown
14	DIAG_EN	14	DIAG_EN	I	Enable-disable pin for diagnostics; internal pulldown
15	OUT4	15	OUT4	O	Output of Channel 4.
16	OUT4	16	OUT4	O	Output of Channel 4.
17	OUT3	17	OUT3	O	Output of Channel 3.
18	OUT3	18	OUT3	O	Output of Channel 3.
19	NC	19	NC	-	Not Connected.
20	VS	20	VS	I	Power Supply
21	VS	21	VS	I	Power Supply
22	VS	22	VS	I	Power Supply
23	VS	23	VS	I	Power Supply
24	NC	24	NC	-	Not Connected.
25	OUT2	25	OUT2	O	Output of Channel 2.
26	OUT2	26	OUT2	O	Output of Channel 2.
27	OUT1	27	OUT1	O	Output of Channel 1.
28	OUT1	28	OUT1	O	Output of Channel 1.
Exposed Pad	-	Exposed Pad	-	-	Connect to device GND or leave it floating.

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8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	Supply Voltage (3)	-0.3	40	V
	Reverse Polarity Voltage(4)	-36		V
	Supply Voltage for Short Circuit Protection (7)		28	V
	Voltage on INx, DIAG_EN, SEL, SEH, THER pins	-0.3	7	V
	Voltage on /STx, /FAULT pins	-0.3	7	V
	Voltage on CL Pin	-0.3	7	V
	Voltage on CS Pin	-2.7	7	V
Current range at terminals (2)	DC Current on OUTx Pin	-3.5	Internally limited	A
	Current on GND Pin	-50 -250(5)	250	mA
	Current on INx, DIAG_EN, SEL, SEH, THER pins	-10	10	mA
	Current on /STx, /FAULT pins	-30	10	mA
	Current on CL Pin	-	6	mA
	Current on CS Pin	-	30	mA
$f_{IN,MAX}$	PWM Frequency on INx Pins		2	KHz
E_{HSD}	Inductive Load Switch-off Energy Dissipation, Single Pulse(6)		40	mJ
T_A	Operating Ambient Temperature Range	-40	125	°C
T_J	Operating Junction Temperature Range	-40	150	°C
T_{STG}	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Supply voltage to withstand 40V load dump test for 400ms, according to ISO 16750-2:2010 Test B

(4) Reverse polarity condition: t < 60 s, reverse current < I_{R1}, GND pin 1-kΩ resistor in parallel with diode.

(5) For limited time range: t < 120s

(6) Test condition: V_S = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-µm Cu, 2- × 35-µm Cu. 600-mm2 thermal pad copper area.

(7) Test according to AEC Q100-012, for cold repetitive-short pulse, cold repetitive – long pulse and hot repetitive in 3 test modes. The device gets the certification of Grade A level (1M cycles)

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human Body Model (HBM) ESD Stress Voltage (2)	All Pins	-4	4	kV
	Charged Device Model (CDM) ESD Stress Voltage (3)	All Pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per AEC-Q100-011. The human-body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.

(3) Level listed above is the passing level per AEC-Q100-011.

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8.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
VS	Voltage on VS pin	4		40	V
VIH	Input Logic High on INx, DIAG_EN, SEL, SEH, THER	2		5.5	V
VIL	Input Logic Low on INx, DIAG_EN, SEL, SEH, THER	0		0.8	V
$I_{OUT,NOM}$	Nominal DC load current for each channel			2.5	A
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE(1)		eTSSOP-28 (9.7mm x 6.4 mm)	UNIT
$R_{\Theta JA}$	Junction to ambient thermal resistance(2)	36.7	°C/W
$R_{\Theta JC(top)}$	Junction to case(top) thermal resistance	15.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	11.8	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

8.5 Electrical Characteristics

-40°C < T_J <150°C and 4V < V_S < 40V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{S,NOM}$	Nominal Operating Voltage		4	13.5	40	V
$V_{S,UVR}$	Undervoltage Restart	Rising threshold to exit UVLO	3.5	3.7	4	V
$V_{S,UVF}$	Undervoltage Shutdown	Falling threshold to enter UVLO	3	3.2	3.4	V
$V_{S,UVhys}$	Undervoltage Shutdown Hysteresis			0.5		V
OPERATING CURRENT						
I_{op}	Nominal operating current	VS = 13.5 V, VINx = 5 V, VDIAG_EN = 0 V, IOUTx = 0.5 A, current limit = 2 A, all channels on			5	mA
I_{off}	Standby current	VS = 13.5 V, VINx = VDIAG_EN = VCS = VCL = VOUTx =THER = 0 V, Tj=25°C			0.5	uA
		VS = 13.5 V, VINx = VDIAG_EN = VCS = VCL = VOUTx =THER = 0 V,			5	uA

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$I_{off,diag}$	Standby current with diagnostic enabled	VS = 13.5 V, VINx = 0 V, VDIAG_EN = 5 V, VS – VOUTx > V(ol,off), not in open-load mode			3	mA
$t_{off,diag}$	Standby mode deglitch time	IN from high to low, if deglitch time > t(off,deg), the device enters into standby mode.	9	12	15	ms
$I_{lkg(out)}$	Output leakage current in off-state	VS = 13.5 V, VINx = VDIAG_EN = VOUTx = 0			2	uA
POWER STAGE						
$R_{DS(on)}$	On-state resistance	VS >= 3.5 V, Tj=25°C		150		mΩ
		VS >= 3.5 V, Tj=125°C			260	mΩ
$I_{CL(int)}$	Internal current limit	Internal current limit value, CL pin connected to GND	4.2		7.6	A
$I_{CL(TSD),int}$	Current limit during thermal shutdown			4		A
$I_{CL(TSD),ext}$	External current limit value under thermal shutdown	The percentage of the external current limit setting value		65		%
$V_{DS(clamp)}$	Drain-to-source internal clamp voltage					
		I_{out} =2A, L=6mH,	42	48	52	V
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain-source diode voltage	IN = 0, IOUTx = 0.15 A	0.5	0.7	0.9	V
I_{R1}	Continuous reverse current from source to drain	t < 60 s, VINx = 0 V , single channel reversed, short-to-battery condition, Tj = 25°C		2.5		A
I_{R2}	Continuous reverse current from source to drain	t < 60 s, VINx = 0 V, GND pin 1-kΩ resistor in parallel with diode. Reverse-polarity condition, all channels reversed. Tj = 25°C		2		A
LOGIC INPUT (INx, DIAG_EN, SEL, SEH, THER)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{logic,pd}$	Logic-pin pulldown resistor	INx, SEL, SEH, THER, DIAG_EN, VINx = VSEL = VSEH = VTHER=V DIAG_EN = 5 V	110	200	300	KΩ
DIAGNOSTICS						
I_{lkg_GLoss}	Output leakage current under GND loss condition	INx=DIAG_EN=5V，SELx=THER=CL=CS=GND			2	uA
$V_{ol,off}$	Open-load detection threshold	IN = 0 V, when VS – VOUTx < t(ol,off), duration longer than t(ol,off), then open load is detected, off state	1.5		2.3	V
$t_{dol,off}$	Open-load detection threshold deglitch time	IN = 0 V, when VS – VOUTx < V(ol,off) , duration longer than t(ol,off), then open load is detected, off state	300	550	800	us

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$I_{ol,off}$	Off-state output sink current	VINx = 0 V, VDIAG_EN = 5 V, VS = VOUTx = 13.5 V, TJ = 125°C, open load	-40		uA
V_{OL_STx}	Status low-output voltage	ISTx = 2 mA, version A only		0.2	V
V_{OL_FAULT}	Fault low-output voltage	IFAULT = 2 mA, version B only		0.2	V
$t_{CL_deglitch}$	Deglitch time when current limit occurs	VINx = VDIAG_EN = 5 V, the deglitch time from current limit toggling to FAULT, STx, CS report.	100	300	us
TSD	Thermal shutdown threshold		165		°C
TSD,rst	Thermal shutdown status reset threshold		145		°C
TSW	Thermal swing shutdown threshold		60		°C
T_{hys}	Hysteresis for resetting thermal swing		15		°C
CURRENT SENSE (Version B) AND CURRENT LIMIT					
K_{CS}	Current-sense ratio		300		
K_{CL}	Current-limit ratio		2500		
$V_{CL(th)}$	Current limit internal threshold		0.8		V
dK_{CS}/ K_{CS}	Current-sense accuracy, (ICS × K(CS) – IOUTx) /IOUTx × 100	VS = 13.5 V, IOUTx >= 5 mA	-25	25	%
		VS = 13.5 V, IOUTx >=25 mA	-15	15	
		VS = 13.5 V, IOUTx >=50 mA	-8	8	
		VS = 13.5 V, IOUTx >=100mA	-4	4	
		VS = 13.5 V, IOUTx >=500mA	-3	3	
dK_{CL} / K_{CL}	External current limit accuracy (IOUTx – ICL × K(CL)) × 100 / (ICL × K(CL))	VS = 13.5 V, I(limit)>= 0.25 A	- 25	25	%
		VS = 13.5 V, 0.5 A <= I(limit) <=4A	-15	15	
$V_{CS,sat}$	Current-sense voltage linear range	VS >=6.5 V		4	V
V_{CS,sat_DO}	Current-sense voltage linear range dropout voltage (Vs-Vcs)	5 V<=VS < 6.5 V		2.5	V
$I_{OUTx,sat}$	Output-current linear range	VS>=6.5 V, VCS<=4 V		2.5	A
		5 V <= VS < 6.5 V, VCS <=VS – 2.5 V		2.5	A
$V_{CS,H}$	Current sense pin output voltage	VS >= 7 V, fault mode	5	6.5	V
V_{CS,H_DO}	Current sense pin output voltage dropout (Vs-Vcs,h)	5 V <= VS < 7 V, fault mode		1	V
$I_{CS,H}$	Current-sense pin output current	VCS = 4.5 V, VS = 13.5 V	14		mA
$I_{lkg,cs}$	Current-sense leakage current in disabled mode	VDIAG_EN = 0 V, Tj= 150°C		0.5	uA
Switching Characteristics					
$t_{d,on}$	Delay time, VOUTx 10% after VINx rises	VS = 13.5 V, VDIAG_EN = 5 V, IOUTx = 0.5 A, IN rising edge to 10% of VOUTx	20	40 80	us

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$t_{d,off}$	Delay time, VOUTx 90% after VINx falls	VS = 13.5 V, VDIAG_EN = 5 V, IOUTx = 0.5 A, IN falling edge to 90% of VOUTx	20	45	80	us
SR_{on}	Turn on slew rate	VS = 13.5 V, VDIAG_EN = 5 V, IOUTx = 0.5 A, VOUTx from 10% to 90%	0.1	0.3	0.5	V/us
SR_{off}	Turn off slew rate	VS = 13.5 V, VDIAG_EN = 5 V, IOUTx = 0.5 A, VOUTx from 90% to 10%	0.1	0.3	0.5	V/us
$t_{d,skew}$	$t_{d,rise} - t_{d,fall}$	VS = 13.5 V, IL = 0.5A. td, rise is the IN rising edge to VOUTx = 90%. td,fall is the IN falling edge to VOUTx = 10%.	-50		50	us
$t_{CS(off1)}$	CS settling time from DIAG_EN disabled	VS = 13.5 V, VINx = 5 V, IOUTx = 0.5 A. current limit = 2 A. DIAG_EN falling edge to 10% of VCS.			20	us
$t_{CS(on1)}$	CS settling time from DIAG_EN enabled	VS = 13.5 V, VINx = 5 V, IOUTx = 0.5 A. current limit is 2A. DIAG_EN rising edge to 90% of VCS.			20	us
$t_{CS(off2)}$	CS settling time from IN falling edge	VS = 13.5 V, VDIAG_EN = 5 V, IOUTx = 0.5 A. current limit =2 A. IN falling edge to 10% of VCS	30		100	us
$t_{CS(on2)}$	CS settling time from IN rising edge	VS = 13.5 V, VDIAG_EN = 5 V, IOUTx = 0.5 A. current limit =2 A. IN rising edge to 90% of VCS	40		150	us
t_{dCS}	Current sense transition delay from channel to channel	VDIAG_EN=5V, current sense transition delay time from channel to channel by changing SEL & SEH			50	us

(1) The current includes the leakage current at output stage.

(2) The accuracy of external current limit is only applicable to overload conditions that is over 50% greater than the current limit setting.

(3) The external current limit is recommended to be set higher than 0.5A.

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9 Functional Block Diagram

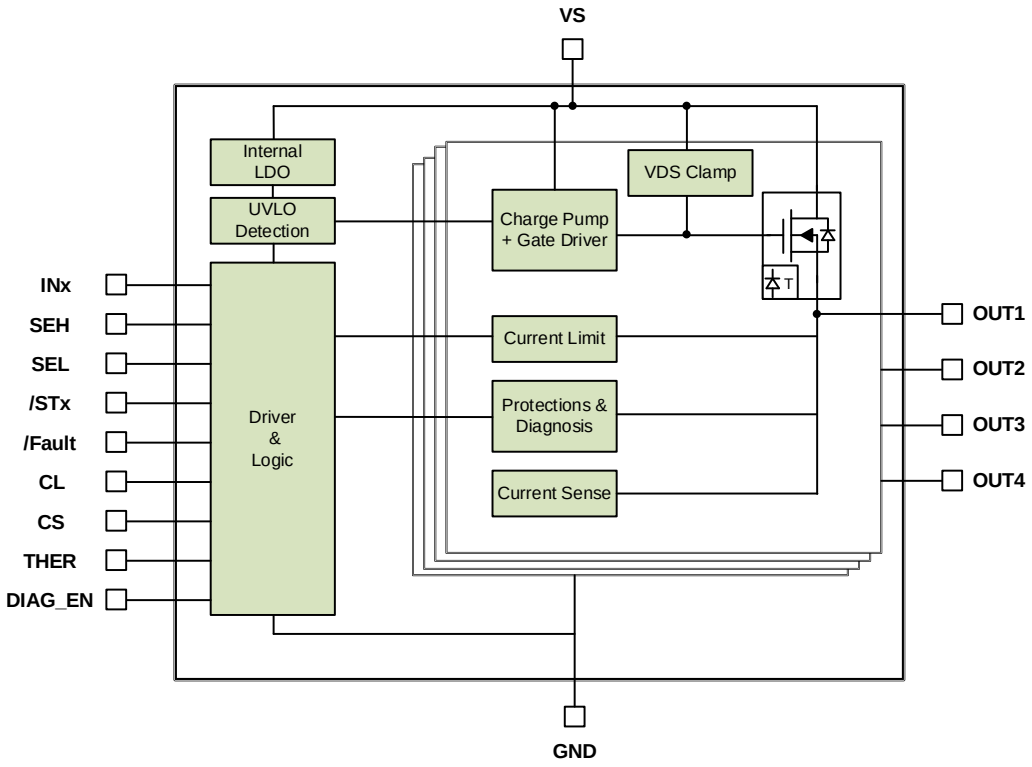

Figure 9-1. Functional Block Diagram

10 Feature Description

10.1 Operating Modes

There are three operating modes in the device: normal mode, standby mode (with diagnostic) and sleep mode (without diagnostic). Figure 10-1 shows the state machine transition diagram among the three operating modes.

If an off-state power saving is required in the system, the sleep mode can be entered with DIAG_EN low. If an off-state diagnostic is required, set DIAG_EN into high. Note that to enter standby or sleep mode requires IN low and t > $t_{off,diag}$. $t_{off,diag}$ is the standby-mode deglitch time, which is used to avoid false triggering.

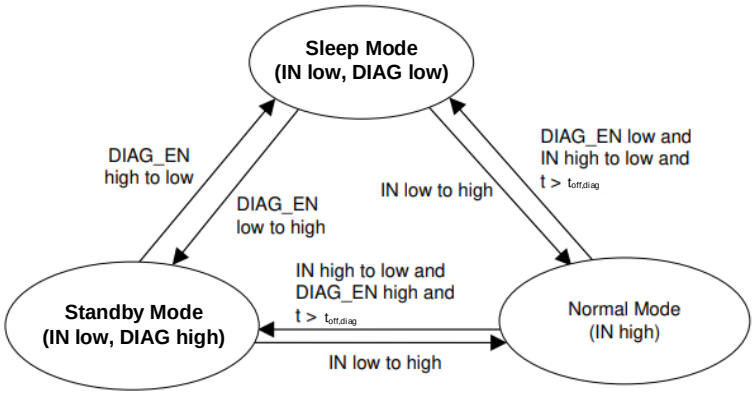

Figure 10-1 Working Mode State Machine

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10.2 Current Sense

The high-accuracy real-time current-sense function is implemented for version B. An internal current mirror is used to source 1 / K_{cs} of the load current, flowing out to the external resistor between the CS pin and GND, and reflected as voltage on the CS pin. K_{cs} is the ratio of the current at output stage and the sensing current at CS pin. It is a constant value across the temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases. To ensure the CS voltage is within the linear region, an appropriate R_{CS} is need to be calculated as below:

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS}}{I_{OUT}} \times K_{CS} \quad (1)$$

When the IC is in a fault condition, the CS pin would perform as a diagnostic report pin. For example, if current limit, thermal shutdown/swing, open load, or short to battery in the off-state occurs, the voltage of CS pin would be pulled up to $V_{CS,H}$. Please check Figure 10-2 for details.

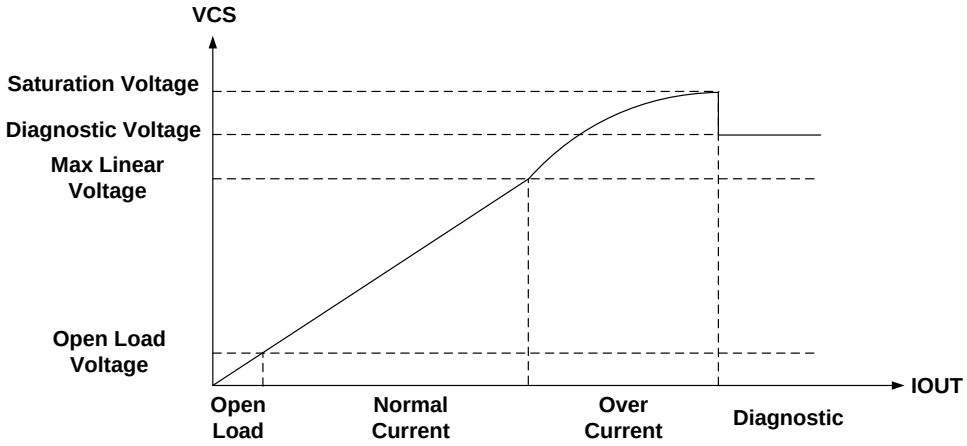

Figure 10-2 VCS in different working mode

10.3 Programmable Current Limit

A high-accuracy current limit is integrated internally, which offers protection from overstressing to the load and integrated power FET. If the current limit occurs, the IC would hold the current at the set value, and pulls up the CS pin to diagnostic voltage $V_{CS,H}$. And IC support two current-limit thresholds as below:

External programmable current limit -- An external resistor is used set the I_{CL} limit at CL pin, which is proportional to I_{OUT} with K_{CL} factor. When IOUT exceed the CL current set by the external resistor, a closed loop steps in immediately. V_{GS} voltage regulates accordingly, leading to the V_{DS} voltage regulation.

Internal current limit -- The internal current limit is fixed and typically 6 A. To connect CL pin directly to device GND would trigger the internal current limit for large-current applications.

Both the internal current limit ($I_{CL(int)}$) and external programmable current limit are always active when V_S is powered and IN is high. The lower one (of $I_{CL(int)}$ and the external programmable current limit) is applied as the actual current limit. Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the CL pin must be connected with device GND. To use the current limit in the application, an appropriate R_{CL} is need to be calculated as below:

$$R_{CL} = \frac{V_{CL(th)}}{I_{CL}} = \frac{V_{CL(th)}}{I_{OUT}} \times K_{CL} \quad (2)$$

10.4 Inductive-Load Switching-Off Clamp

If an inductive load is driven by HSD, when the load is switch on, the current through the inductor increases with a constant time given by the values of the inductance and the resistance of the load:

$$i = \frac{V_S}{R}(1 - e^{-\frac{t}{\tau}}) \quad (3)$$

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$$\tau = \frac{L}{R} \quad (4)$$

And the energy stored in the inductor is calculated as below:

$$E_{LOAD} = \frac{1}{2} \cdot L \cdot (\frac{V_S}{R})^2 \quad (5)$$

When the load is switched off, due to the inductance, the load current tempts to continue to flow in the same direction which causes the load voltage to be pulled down to negative. To protect the power FET to be breakdown in this situation, an internally clamping $V_{DS,CLP}$ between the drain and source is implemented, and the power FET is turned on for inductance-energy dissipation during the current-decay period (T_{DECAY}). Please check the graphic diagram in Figure 10-3.

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,CLP}$, the clamp diode between the drain and gate.

$$V_{DS,CLP} = V_S - V_{OUT} = V_S - R \cdot i(t) - L \cdot \frac{di(t)}{dt} \quad (6)$$

Solve equation 6,

$$i(t) = \frac{V_S}{R} \cdot e^{-\frac{t}{\tau}} + \frac{V_S - V_{DS,CLP}}{V_{DS,CLP}} \cdot (1 - e^{-\frac{t}{\tau}}) \quad (7)$$

Solve equation 7 with i(t)=0,

$$t_{DECAY} = \tau \cdot ln(\frac{V_{DS,CLP}}{V_{DS,CLP} - V_S}) \quad (8)$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. The total dissipated energy E_{HSD} is calculated as below:

$$E_{HSD} = \int_0^{t_{DECAY}} V_{DS,CLP} \cdot i(t) dt$$

$$= V_{DS,CLP} \cdot t_{DECAY} (\frac{V_S - V_{DS,CLP}}{R}) - \tau \frac{V_{DS,CLP}^2}{R} (e^{-\frac{t_{DECAY}}{\tau}} - 1) \quad (9)$$

With approximation of $R \approx 0$, then

$$t_{DECAY} = \frac{LI_L}{V_{DS,CLP} - V_S} \quad (10)$$

$$E_{HSD} = \frac{1}{2} LI_L^2 \cdot (\frac{V_{DS,CLP}}{V_{DS,CLP} - V_S}) \quad (11)$$

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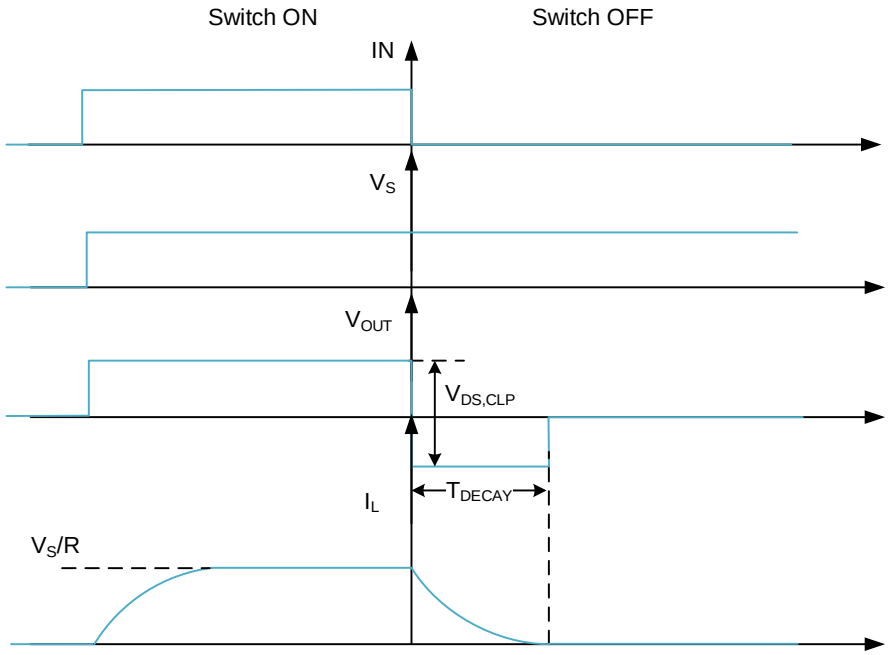

Figure 10-3 Inductive Load Switching-ON/OFF Diagram

10.5 Protections and Diagnostics

The diagnostic functions are controlled by DIAG_EN. In version B, SEL and SEH are two pins to multiplex the shared current-sense function among the four channels.

Table 10-1. Diagnosis Configuration Table

DIAG_EN	INx	SEH	SEL	Channel Selected	CS, /FAULT, /STx	Protections & Diagnostics
L	L	-	-	-	High Impedance	No protections, no diagnostic functions
	H					Full protections, no diagnostic functions
H	-	0	0	Channel 1	See Table 10-2 Fault Table	See Table 10-2 Fault Table
		0	1	Channel 2		
		1	0	Channel 3		
		1	1	Channel 4		

10.5.1 Fault Truth Table

Table 10-2 shows the fault table of OUT, CS, /STx, /FAULT signals under different fault conditions when DIAG_EN is set high.

For version A, the fault conditions will be reported at STx pins for each channel. When a fault condition occurs, STx is pulled down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the STx pins together.

For version B, a global FAULT pin is used to monitor the global fault condition for all channels. When a fault condition occurs on any channel, the FAULT pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller. With the FAULT flag, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, VCS(H), when the channel in fault is selected.

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Table 10-2. Fault Table

Application Conditions	IN	THER	Vout	/STx (Ver. A)	CS (Ver. B)	/FAULT (Ver. B)	Fault Recovery
Normal Operation	H	-	≈Vs	H	I_{Load} / Kcs	H	-
	L		≈0	H	<I_{off}	H	
Overcurrent, Short to GND	H	-	≈0	L	Vcs,h	L	Auto retry
Open Load(1), Short to Vs	L	-	>Vs-Vol,off	L	Vcs,h	L	Auto retry
Thermal Shutdown (TSD)	H	H	-	L	Vcs,h	L	Output latch off. Fault recovers when INx toggles.
		L					Output auto-retry. Fault recovers when TJ < TSD,rst or when INx toggles.
Thermal Swing (TSW)	H	-	-	L	Vcs,h	L	Auto retry

(1) An external pullup is required for open-load detection.

10.5.2 Short-to-GND and Overload Detection

When Power FET is ON, the short-to-GND fault is reported with low voltage on ST (version A) or $V_{CS,H}$ on CS (version B), when a current limit is triggered. The lower one of the internal and external set values is applied for the actual current limit.

The fault would be auto recovered when the fault condition is cleared. If it is not cleared for certain time, the current limit would further trigger the thermal shutdown to protect the power FET.

10.5.3 Open-Load Detection

When Power FET is ON, an ultra low voltage at CS pin will be detected by the microcontroller, and no fault will be reported at the /STx or /FAULT pins. The microcontroller must multiplex the SEL and SEH pins between channels to detect the on-state open load fault.

When Power FET is OFF, if $V_S - V_{OUT} < V_{OL,OFF}$, the open load fault would be reported with low voltage at /ST (version A) or $V_{CS,H}$ on CS (version B).

The fault would be auto recovered when the fault condition is cleared.

10.5.4 Short-to-Battery Detection

When Power FET is ON, the IC would report the fault with low voltage on ST for version A. For version B, this fault would not report directly. The user could detect the voltage of CS pin and judge accordingly.

When Power FET is OFF, the short to battery would lead to $V_{OUT} - V_S < V_{OUT,F}$, which would report LOW at ST (for version A) , $V_{CS,H}$ at CS and LOW at /Fault (for version B). The fault would be auto recovered when the fault condition is cleared.

10.5.5 Thermal Shutdown Protection

There are two different thermal shutdown mechanism implemented in the IC: the dynamic protection and static protection.

For the dynamic thermal swing protection, the IC would shut down the power FET when the temperature of the power FET is increasing sharply with $\Delta T = T_{DMOS} - T_{LOGIC} > T_{SW}$. The fault would be reported with LOW at ST (for Version A) , $V_{CS,H}$ at CS and LOW at /Fault pin (for Version B).

The fault would be auto recovered when $\Delta T = T_{DMOS} - T_{LOGIC} < T_{SW} - T_{HYS}$.

For the absolute thermal shutdown protection, the IC would shut down the power FET when the temperature of the power FET $T > T_{SD}$. The fault would be reported with LOW on ST (for Version A), $V_{CS,H}$ at CS and LOW at /Fault pin (for Version B).

The THER pin is used to configure the behavior after the thermal shutdown occurs.

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- When the THER pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when TJ < T(SD) – T(hys), but the current is limited to ICL(TSD) to avoid repetitive thermal shutdown. The thermal shutdown fault signal is cleared when TJ < T(SD,rst) or after toggling the related INx pin.
- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related INx pin.

10.5.6 UVLO Protection

The IC would shut down the power FET when $V_S < V_{S,UVF}$.

The fault would be auto recovered when $V_S > V_{S,UVR}$.

10.5.7 Loss of GND Protection

The IC would shut down the power FET when loss of GND occurs.

The fault would be auto recovered when the GND connection is back to normal.

10.5.8 Loss of Power Supply Protection

The IC would shut down the power FET when loss of supply occurs.

The fault would be auto recovered when the supply connection is back to normal.

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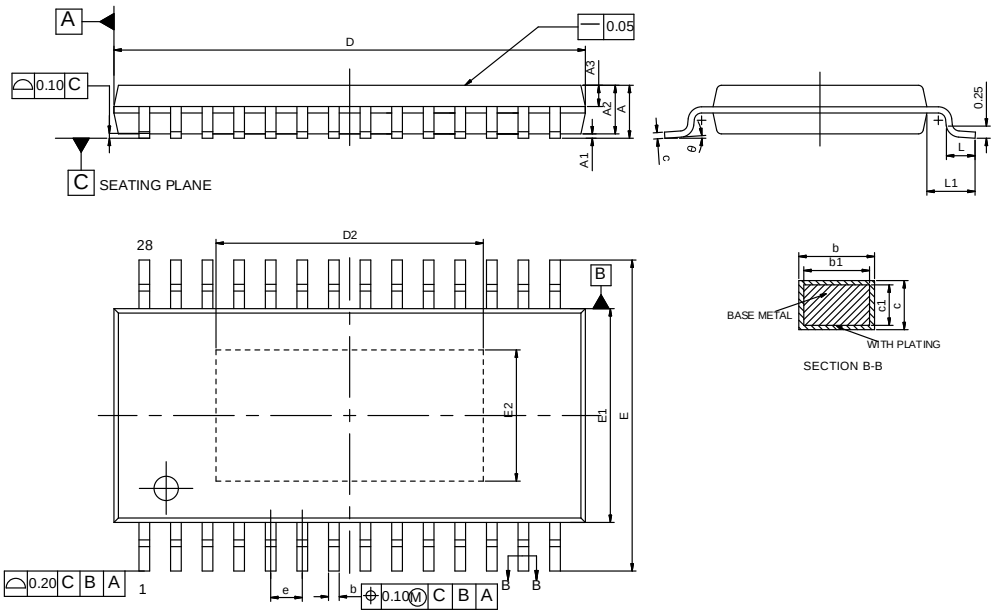
MECHANICAL DATA

eTSSOP-28



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	—	1.00
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	8°

L/F载体尺寸 (mil)	E2	D2
118*202	2.70±0.30	4.83±0.30

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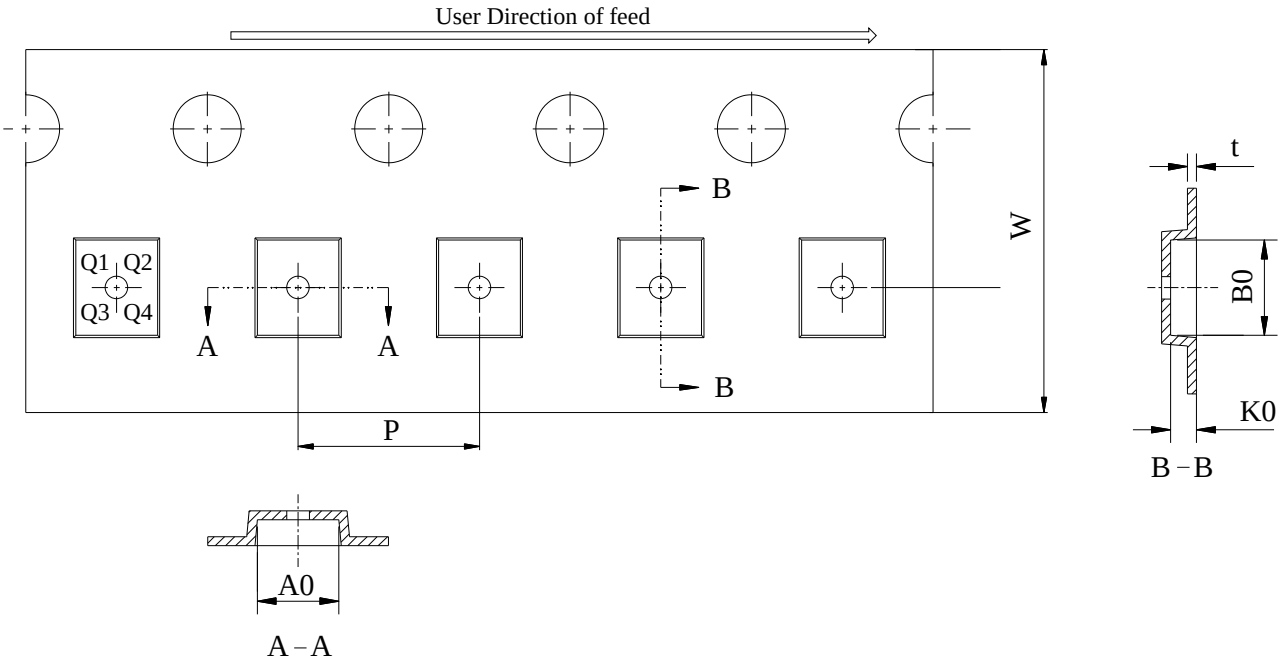
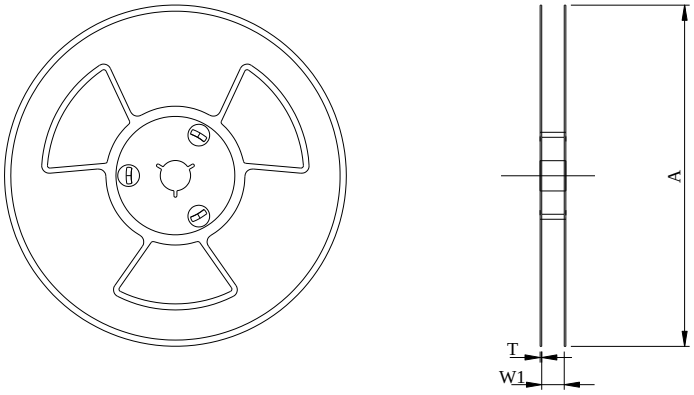
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	16.00±0.30	8.00±0.10	6.70±0.10	10.05±0.10	1.5±0.10	0.30±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	16.4 +1/-0	2.1±0.3

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