
SC8749Q 36V Automotive Buck-Boost Converter with I2C Interface

1. Descriptions

The SC8749Q is a buck-boost converter with four integrated power switches capable of regulating the output voltage at, above, or below the input voltage. The SC8749Q operates over 3.7V to 36V wide input voltage and can output 2.5V to 20V voltage to support a variety of applications.

The SC8749Q is suitable for a variety of multi-purpose automotive and industrial applications such as ADAS and automotive lighting application.

The SC8749Q employs current mode control scheme. The quasi-constant switching frequency could be set at 200kHz/400kHz/600kHz/1MHz through I2C. The SC8749Q also provides optional spread spectrum to optimize EMI performance.

The SC8749Q offers output over-voltage protection, cycle-by-cycle current limit, output under-voltage protection, input over-voltage and thermal shutdown protection.

The SC8749Q is available in 34-pin 4mm × 5mm × 0.85mm wettable flank QFN packages.

2. Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: T_A range: -40°C to 125 °C
- 4V to 36V start up input voltage, support 3.7V falling V_{IN}
- 2.5V to 20V output voltage range
- Up to 5A continuous output current
- Programmable reference voltage range: 0.5V – 2V with 10mV resolution
- I2C Interface for:
 - Converter ON/OFF
 - Input range selection
 - Output voltage dynamic scaling
 - 200kHz / 400kHz / 600kHz / 1MHz switching frequency
 - Auto PFM / Forced PWM
 - Spread spectrum dithering
 - Current limit setting
 - Soft-start time
 - Compensation network parameter
 - Protection mode selection
 - Power good threshold setting
- Protection features:
 - Output over-voltage protection
 - Cycle-by-cycle current limit
 - Output under-voltage protection
 - Input over-voltage protection
 - Thermal shutdown protection

3. Applications

- Automotive Infotainment
- Automotive ADAS
- Automotive Sensor Fusion System
- Automotive Wireless Charging



4. Device Information

ORDER NUMBER	DEFAULT VOUT	DEFAULT FSW	MAX. OUTPUT CURRENT	PACKAGE	BODY SIZE
SC8749QQFMR	Adjustable	400kHz	5 A	FCQFN-34	4mm × 5mm × 0.85mm
SC8749AQQFMR	11.6V	400kHz	5 A	FCQFN-34	4mm × 5mm × 0.85mm
SC8749BQQFMR	9.0V	400kHz	5 A	FCQFN-34	4mm × 5mm × 0.85mm
SC8748QQFMR(*)	Adjustable	400kHz	3 A	FCQFN-34	4mm × 5mm × 0.85mm

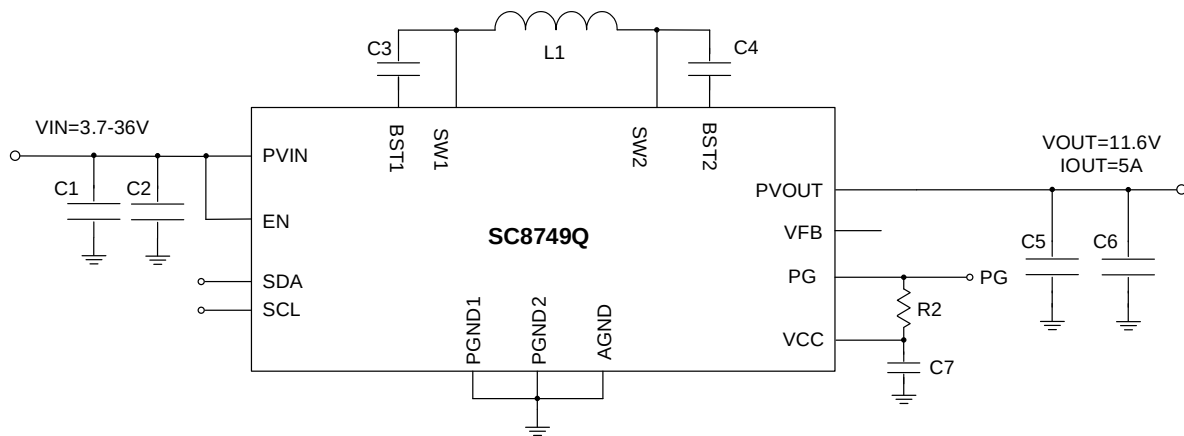
Notes: Connect Southchip for more information.

5. Revision History

Revision	Date	Page(s) Changed	Changes Description
V1.0.0	2025/5	/	1. Initial version
V1.0.1	2025/10	8	1. Adding the description of the reference voltage of SC8748QQFMR and SC8749QQFMR, and differentiate it with SC8748AQQFMR and SC8748BQQFMR.
		16	1. Differentiating the structure of the Error Amplifier between SC8748QQFMR/ SC8749QQFMR and SC8748AQQFMR/ SC8748BQQFMR.
		17	1. Adding the description of the way setting the output voltage.
		24	1. Adding the description of the default value of Reg. 0x00H on different ORDER NUMBER
V1.0.2	2026/1	5	1. The description of pin AGND and BST2 has been modified.
		7	1. Adding the max limit of all R_{DS_ON} parameter.
		8	1. Adding the max limit of all R_{DS_ON} parameter. 2. Modifying the peak current limit min value. 3. Modifying the valley current limit. 4. Modifying I_{LMT_RV} to typical value limit. 5. Modifying the I_{ZCD} typical value. 6. The accuracy of $V_{REF} = 0.9V / 1.0V / 1.05V / 1.15V / 1.2V$ and $V_{REF} = 1.8V / 2.0V$ in adjustable output version has been modified. 7. Output divider ratio accuracy has been modified.
		9	1. Modifying the spread spectrum pattern related parameter description. 2. Modifying the limit of frequency dithering span to min and max limit. 3. Adding the min and max limit of PG high limit rising threshold.
		29	1. Modifying the side wettable depth of package.



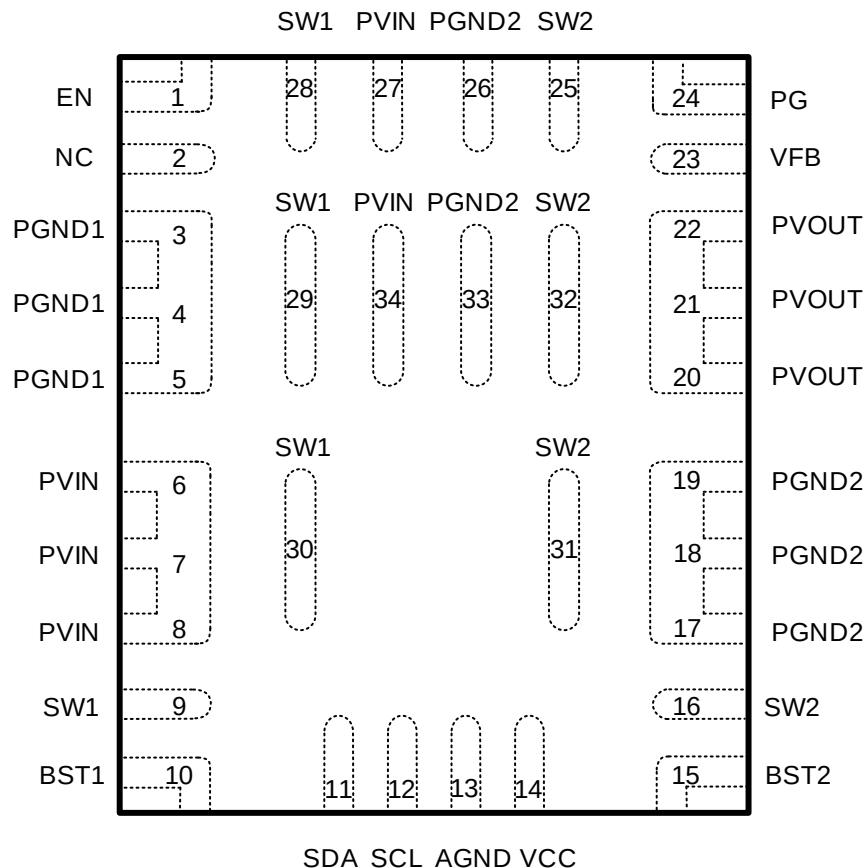
6. Typical Application Circuit





7. Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	EN	I	On/off control input and custom input UVLO setting.
2	NC	NA	Not connected. It is recommended to connect this pin to PGND1.
3, 4, 5	PGND1	PWR	Power ground for the SW1 half-bridge.
6, 7, 8, 27, 34	PVIN	PWR	Power input for the converter.
9, 28, 29, 30	SW1	PWR	Switching node pin of the buck side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
10	BST1	O	Bootstrap for SW1.



11	SDA	I	Data of I2C interface. If SDA is not used, it is recommended to connect SDA to VCC through a resistor.
12	SCL	I	Clock of I2C interface. If SCL is not used, it is recommended to connect SCL to VCC through a resistor.
13	AGND	PWR	Ground for internal analog and digital circuits.
14	VCC	O	Internal LDO regulator output. Decouple with a 4.7 μ F capacitor between this pin and the AGND pin.
15	BST2	O	Bootstrap for SW2.
16, 25, 31, 32	SW2	PWR	Switching node pin of the boost side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
17, 18, 19, 26, 33	PGND2	PWR	Power ground for SW2 half-bridge.
20, 21, 22	PVOUT	PWR	Power output of the converter. The output capacitors should be placed as close to chip as possible
23	VFB	I	Feedback input. Floating this pin if it is not used.
24	PG	O	Power good indicator. This pin is an open-drain status pin. Floating this pin if it is not used.



8. Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of $-40^{\circ}\text{C} \sim 150^{\circ}\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	PVIN, EN	-0.3	40	V
	SW1	-0.3	PVIN+0.3	V
	PVOUT	-0.3	22	V
	SW2	-0.3	PVOUT+0.3	V
	BST1	SW1-0.3	SW1+6	V
	BST2	SW2-0.3	SW2+6	V
	All other pins	-0.3	6	V
T _J	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾ , all pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range after start up	3.7		36	V
V _{OUT}	Output voltage range	2.5		20	V
F _{SW}	Buck switching frequency range	200	400	1000	kHz
I _{OUT}	Output DC current range	0		5	A
T _J	Operating junction temperature	-40		150	°C



8.4 Thermal Information

THERMAL RESISTANCE		FCQFN34 (4mm x 5mm)	UNIT
$\theta_{JA}^{(1)}$	Junction to ambient thermal resistance (JESD 51-7)	35.3	°C/W
$\theta_{JA}^{(2)}$	Junction to ambient thermal resistance (SC8749Q EVM)	23.0	°C/W
θ_{JC}	Junction to case resistance	14.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	2.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.0	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

(2) Measured on official EVM. 4-layer, 2-oz Cu per top and bottom layer and 1-oz Cu per inner layer, evaluation board.

8.5 Electrical Characteristics

Typical value is tested at $T_J = +25^\circ\text{C}$, $V_{IN} = 13.5\text{V}$ and $V_{EN} = 2\text{V}$, unless otherwise noted. Minimum and maximum value is tested at $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, $V_{IN} = 13.5\text{V}$ and $V_{EN} = 2\text{V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		3.9	4.0	V
		V_{IN} falling		3.6	3.7	V
I_Q	Quiescent current into the V_{IN} pin	$V_{EN} = 2\text{V}$, I2C set on. No switching, no load.		350	600	μA
I_{SD}	Shutdown current into the V_{IN} pin	$V_{EN} = 0\text{V}$		1.1	20	μA
V_{IN_PG}	Minimum input voltage for proper PG function	$V_{EN} = 0\text{V}$			2.0	V
VCC REGULATOR						
V_{CC}	Internal regulator output	$V_{IN} = 13.5\text{V}$	4.8	5.0	5.2	V
$V_{CC_UVLO_F}$	V_{CC} Under voltage lockout threshold	V_{CC} falling		3.5		V
$V_{CC_UVLO_HYS}$	V_{CC_UVLO} hysteresis			0.3		V
ENABLE						
$V_{EN_VCC_H}$	EN input level to turn on internal LDO				1.0	V
$V_{EN_VCC_L}$	EN input level to turn off internal LDO		0.4			V
V_{EN_H}	EN input level to start switching		1.19	1.22	1.25	V
V_{EN_L}	EN input level to stop switching		1.04	1.07	1.10	V
R_{EN_L}	EN Pull-down resistor	$V_{EN} = 2\text{V}$		2		$\text{M}\Omega$
POWER STAGE						
R_{DS_ON}	High-side MOSFET on resistance of buck side	$V_{BST1} - V_{SW1} = 5\text{V}$		6.4	11	$\text{m}\Omega$
	Low-side MOSFET on resistance of buck side	$V_{CC} = 5\text{V}$		24	40	



	Low-side MOSFET on resistance of boost side	V _{CC} = 5V	11.4	18		
	High-side MOSFET on resistance of boost side	V _{BST2} - V _{SW2} = 5V	7.5	13		
I _{LMT_PK}	Peak current limit, buck-boost mode and boost mode	I _L rising edge	9	12	14	A
I _{LMT_VL}	Valley current limit, buck mode	I _L falling edge	5	6	7	
I _{LMT_RV}	Reverse current limit	FPWM, I _L falling edge	4			A
I _{ZCD}	Zero-current detection threshold	Auto PFM, I _L falling edge	100			mA
BOOT UVLO						
V _{BOOT_UVLO}	Falling voltage on BT1/BT2 pin compared to SW1/SW2 which will turn off high-side switch		2.3			V
V _{BOOT_UVLO_HYS}	V _{BOOT_UVLO} hysteresis		150			mV
REFERENCE VOLTAGE						
V _{REF}	Reference voltage (For SC8749AQQFMR/SC8749BQQFMR)	Register program	500	2000		mV
	Reference voltage (For SC8749QQFMR/SC8748QQFMR)	Fixed	1000			
V _{REF_ACC}	Reference voltage accuracy	V _{REF} = 0.5V, adjustable output version	-2	2		%
		V _{REF} = 0.9V / 1.0V / 1.05V / 1.15V / 1.2V, adjustable output version	-2	2		
		V _{REF} = 1.8V / 2.0V, adjustable output version	-2	2		
FBDR _{ACC}	Output divider ratio accuracy	V _{IN} = 13.5V, FBDR = 1/10,	-1.5	1.5		%
I _{FB}	FB leakage current	Use external FB resistance	10	100		nA
INTERNAL COMPENSATION						
g _m ⁽¹⁾	Compensation Network g _m		25			μA/V
R _{COMP1} ⁽¹⁾	Compensation Network R _{COMP}	Register program, default is 237 kΩ	108			kΩ
R _{COMP2} ⁽¹⁾			237			
R _{COMP3} ⁽¹⁾			366			
R _{COMP4} ⁽¹⁾			603			
C _{COMP1} ⁽¹⁾	Compensation Network C _{COMP}	Register program, default is 100pF	120			pF
C _{COMP2} ⁽¹⁾			100			
C _{COMP3} ⁽¹⁾			80			
C _{COMP4} ⁽¹⁾			60			
OSCILLATOR						
F _{SW1}	Switching frequency		200			kHz
F _{SW2}			400			
F _{SW3}			600			



F _{SW4}			1000	
SPREAD SPECTRUM				
f _{FSS}	Frequency dithering span		-1515	% F _{SW}
f _M	Modulation frequency of spread spectrum pattern.		1/128	F _{SW}
MODE TRANSITION				
k _{BB_BK}	Buck-Boost to Buck transition threshold, F _{SW} = 400kHz	V _{IN} / V _{OUT}	115120125	%
k _{BB_BK_HYS}	Buck-Boost to Buck transition hysteresis, F _{SW} = 400kHz		10	
k _{BST_BB}	Boost to Buck-Boost transition threshold, F _{SW} = 400kHz		848790	
k _{BST_BB_HYS}	Boost to Buck-Boost transition hysteresis, F _{SW} = 400kHz		4	
POWER GOOD INDICATION				
V _{PG_L_F1}	PG low limit falling threshold	Register program, default is 90%	879093	%
V _{PG_L_F2}			788082	
V _{PG_L_HYS}	PG low limit hysteresis		5	
V _{PG_H_R1}	PG high limit rising threshold	Register program, default is 110%	117120123	
V _{PG_H_R2}			108110113	
V _{PG_H_HYS}	PG high limit hysteresis		5	
t _{PG_DGL}	PG flip-flop deglitch time		80	μs
V _{PG_L}	PGOOD output low voltage	IPG_SINK = 500μA	0.4	V
UNDER VOLTAGE PROTECTION & HICCUP				
t _{HC_ON}	Hiccup on time for OCP and UVP recoverable mode	Include soft-start	4	ms
t _{HC_OFF}	Hiccup off time for OCP and UVP recoverable mode		80	ms
V _{UVP}	Output UVP falling threshold		2.0	V
V _{UVP_HYS}	Output UVP hysteresis		0.2	V
OVER VOLTAGE PROTECTION				
V _{OUT_OVP_ABS_R}	Absolute output OVP rising threshold		20.421.222	V
V _{OUT_OVP_ABS_F}	Absolute output OVP falling threshold		2020.521	V
R _{DISCHARGE}	Pull down resistance at the PVOUT node under output OVP condition		210	Ω
THERMAL SHUTDOWN				
T _{SD}	Thermal shutdown temperature	T _J rising edge	165	°C
T _{SD_HYS}	Thermal shutdown hysteresis		20	°C
I2C INTERFACE				



f_{SCL}	SCL clock frequency		400	kHz
V_{IH}	SCL/SDA input logic high		1.3	V
V_{OL}	SDA output logic low		0.4	V
V_{IL}	SCL/SDA input logic low		0.4	V

(1) Guarantee by design.



8.6 Typical Characteristics

$V_{IN} = 13.5V$, $V_{OUT} = 11.6V$, $L = 4.7\mu H$, $F_{SW} = 400kHz$, forced PWM mode, $T_A = 25^\circ C$, unless otherwise noted.

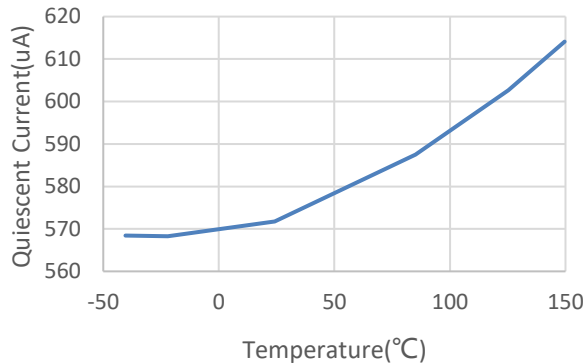


Figure 8-1 Non-Switching Input Supply Current

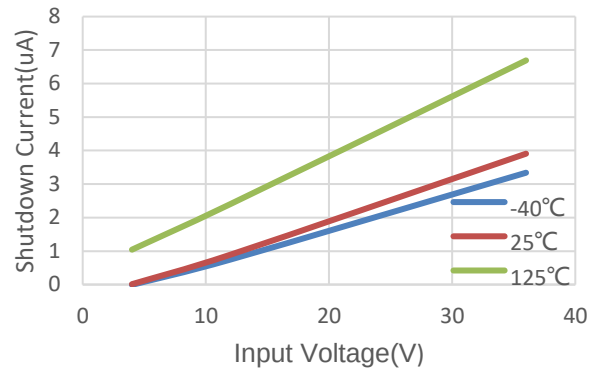


Figure 8-2. Shutdown Supply Current

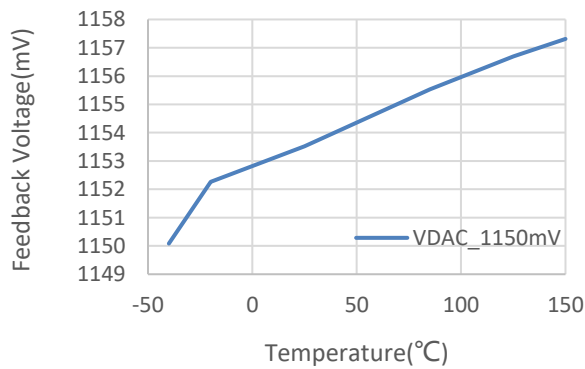


Figure 8-3. Feedback Voltage

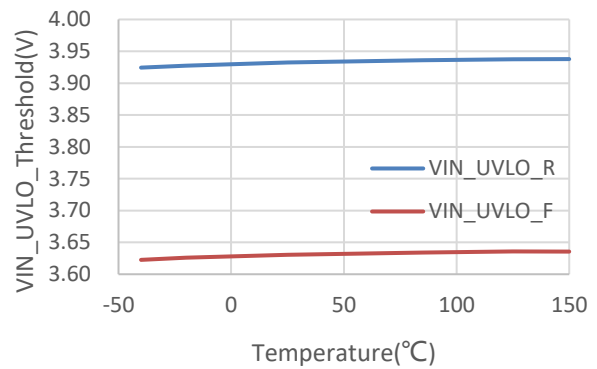


Figure 8-4. VIN UVLO Threshold

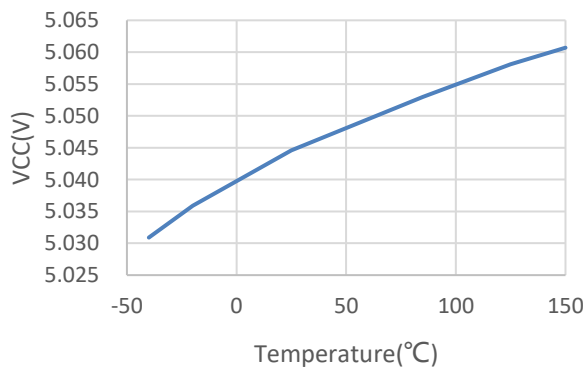


Figure 8-5. VCC Voltage

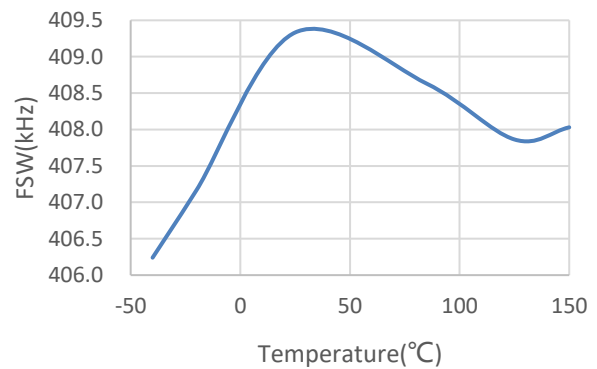


Figure 8-6. Switching Frequency

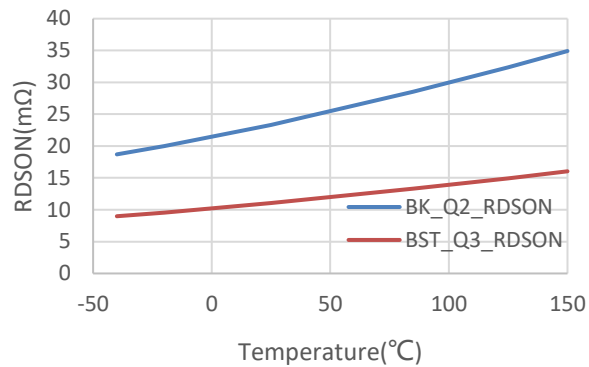


Figure 8-7. Buck and BOOST Low Side Resistance

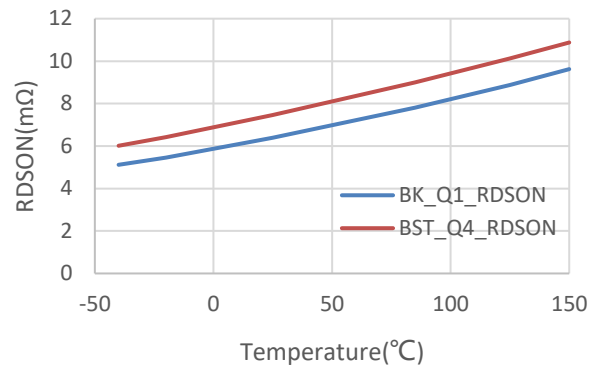


Figure 8-8. Buck and BOOST High Side Resistance

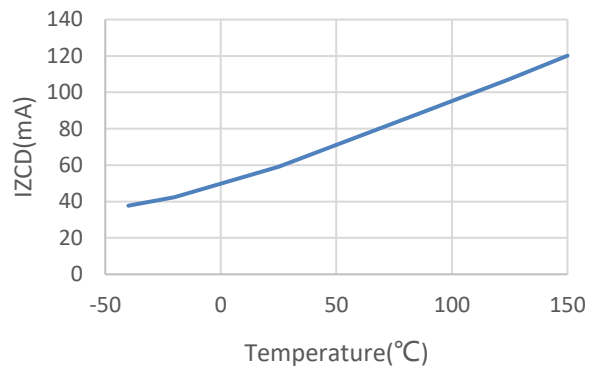


Figure 8-9. IZCD

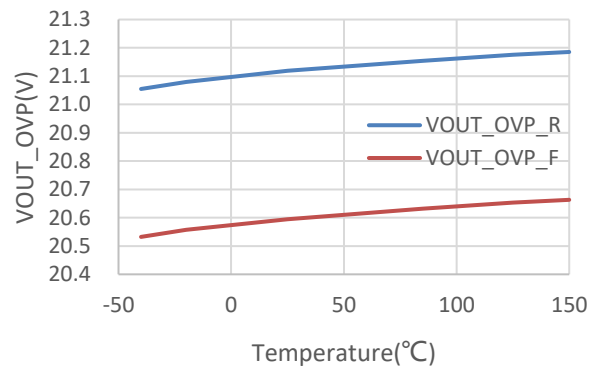
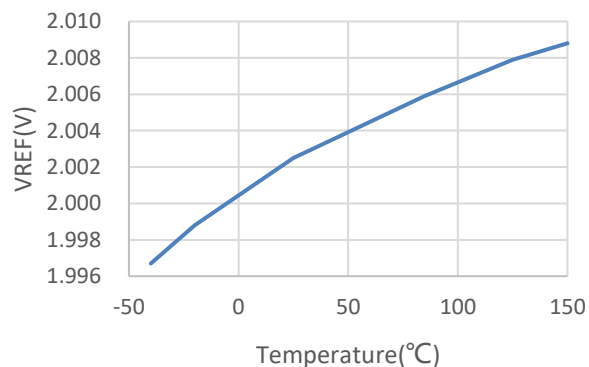
Figure 8-10. V_{OUT} OVP Threshold

Figure 8-11. Reference Voltage

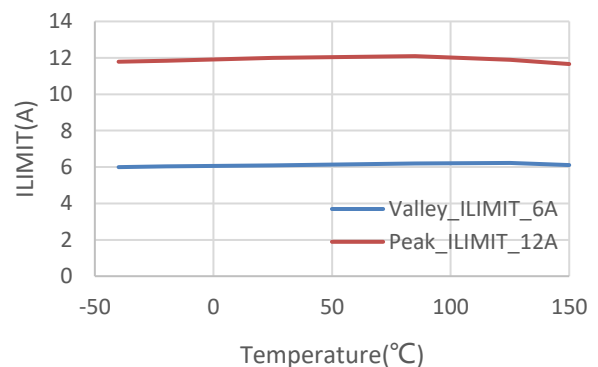


Figure 8-12. Valley and Peak Current Limit

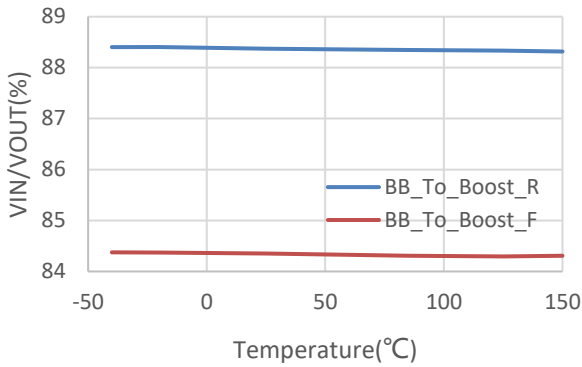


Figure 8-13 Buck-Boost to Boost transition threshold

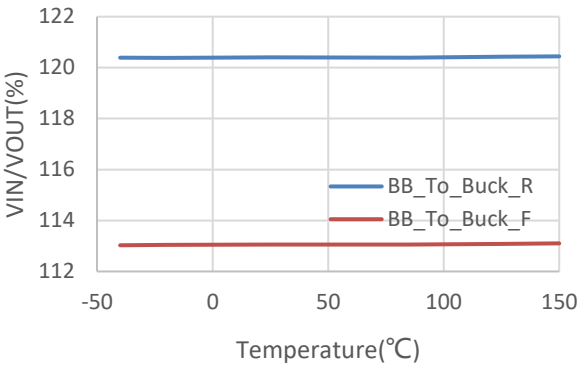


Figure 8-14. Buck-Boost to Buck transition threshold

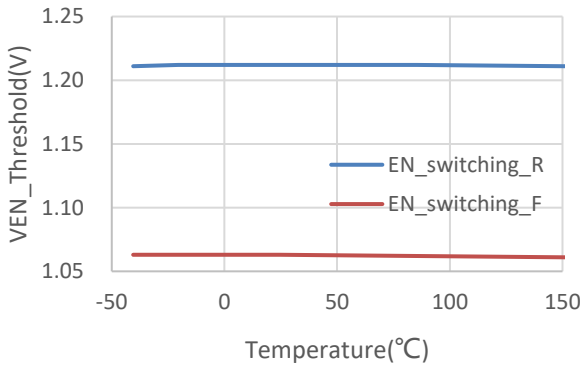
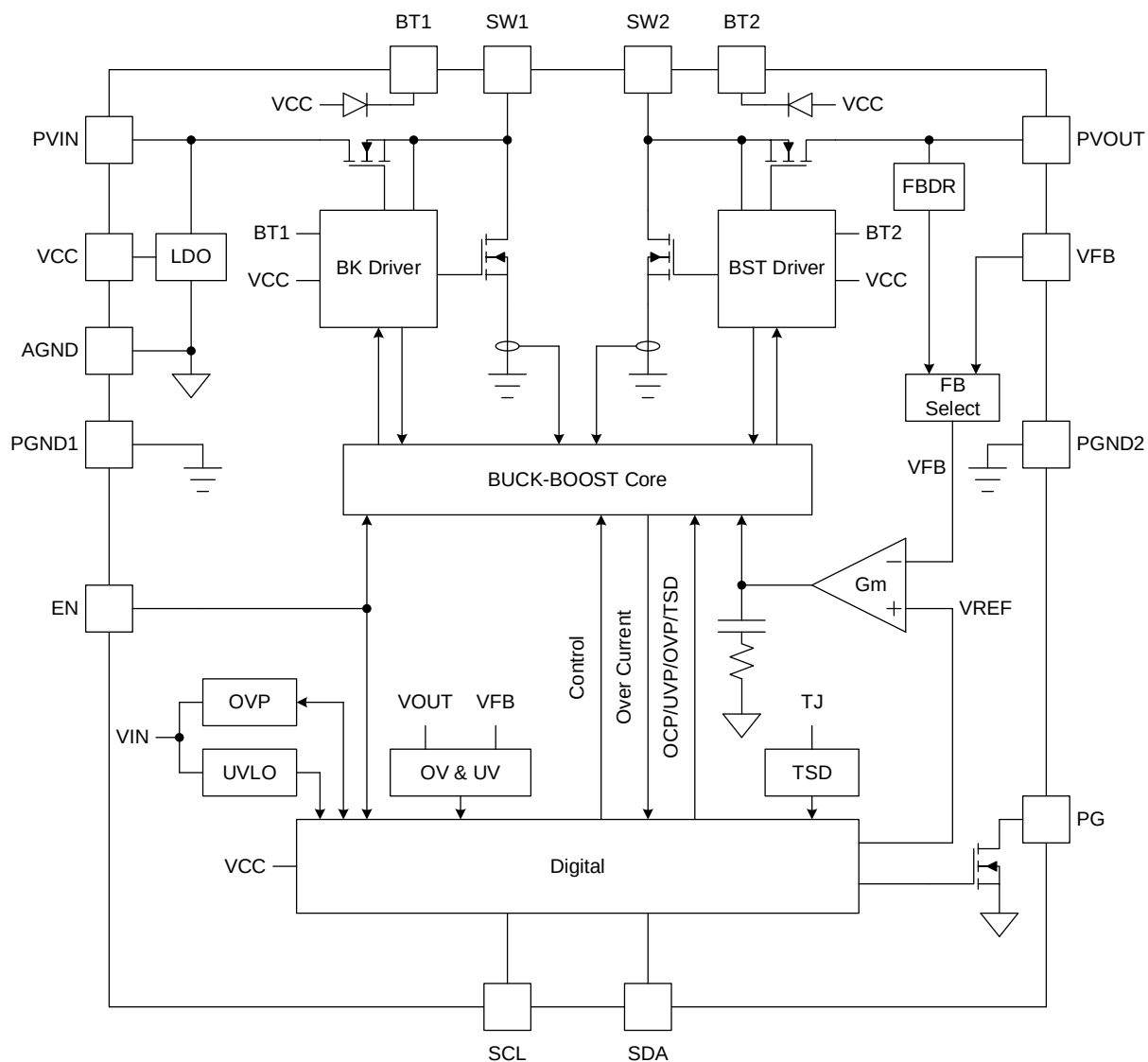


Figure 8-15. EN Threshold



9. Functional Block Diagram



10. Feature Description

The SC8749Q is a 36V, four-switch buck-boost converter with a 3.7V to 36V input voltage range. The wide input voltage (VIN) range makes this device well-suited for automotive applications.

Four integrated, low-resistance N-channel MOSFETs minimize the size of the external circuit. These N-channel MOSFETs also allow the converter to regulate the output voltage (VOUT) when VIN is above, below, or equal to VOUT. The flexible topology transitions reduce power losses to maximize efficiency.

In addition, the patent control algorithm ensures seamless transitions between the adjacent operational regions. The SC8749Q can operate across a wide 200kHz to 1MHz switching frequency. This allows applications to be optimized for board size, efficiency, and electromagnetic compatibility (EMC). Most of the electrical characteristics can be configured by I²C interface.

10.1 VCC Regulator

In normal operation, an internal low-dropout (LDO) regulator outputs a nominal 5V VCC supply from PVIN. This supplies power to both control blocks and the four MOSFETs' gate drivers. Add a 4.7μF, low-ESR ceramic capacitor to act as the bypass capacitor from VCC to AGND.

10.2 Internal Under-Voltage Lockout (UVLO)

The SC8749Q incorporates four internal, fixed UVLO comparators to monitor PVIN, VCC, BST1, and BST2.

The chip is disabled immediately if either PVIN or VCC falls below its respective UVLO threshold. BST1 / BST2 UVLO indicate that there is inadequate driving capacity for the high-side MOSFET. Under this condition, the chip stops the HS-FETs from switching. The bootstrap charger conducts the low-side MOSFET to charge the BST1 / BST2 voltage.

10.3 Enable Control

When EN is driven above its logic threshold $V_{EN_VCC_H}$, the VCC regulator is activated. Once VCC exceeds $V_{CC_UVLO_F} + V_{CC_UVLO_HYS}$, it starts to provide power to the internal control circuitry. When the EN voltage exceeds the comparator's upper threshold V_{EN_H} , the converter is enabled and soft start begins. If EN drops below the comparator's lower threshold V_{EN_L} , the converter stops switching. The VCC regulator and control circuitry continue working until the EN pin is pulled below its logic threshold $V_{EN_VCC_L}$.

In addition to serving as normal on/off logic control, the integrated EN comparator can set the EN pin to a custom

input UVLO threshold by adding an external resistor divider from PVIN to GND.

10.4 Four-Switch Power Converter

Figure 10.1 shows the topology of the four-switch buck-boost converter, which is comprised of four N-channel MOSFETs. Q1 and Q3 work as the main switches, while Q2 and Q4 act as the SR switches. The switches are properly controlled so that transitions between buck, buck-boost, and boost mode is continuous according to VIN and VOUT.

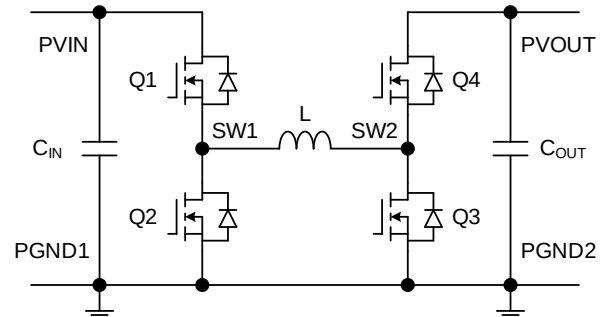


Figure10.1 Four-switch buck-boost converter

The mode transition is automatic by comparing the sensed VIN and sensed VOUT. Figure 10.2 shows the power converter's regions of operation.

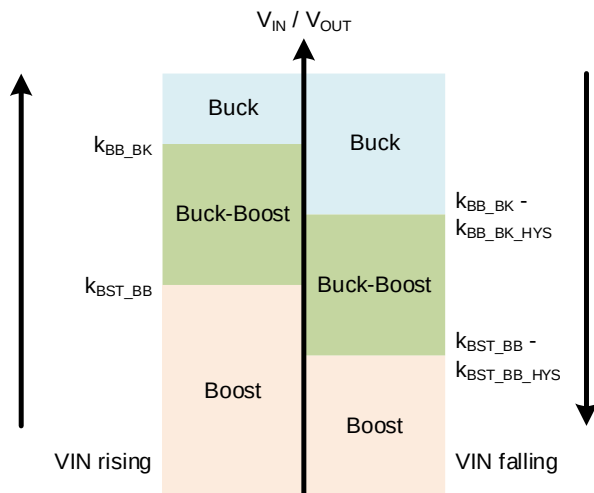


Figure10.2 Mode transient

If VIN is significantly lower than the sensed VOUT, the SC8749Q works in boost mode. When VIN exceeds $k_{BST_BB} \cdot V_{OUT}$, the device transitions into buck-boost mode. If VIN reaches $k_{BB_BK} \cdot V_{OUT}$, then buck mode is activated. Alternately, if VIN drops from a higher value to a lower one, the converter operates in buck mode, buck-boost mode, and boost mode successively.

To avoid repetitive mode transitions when VIN is close to the critical status between adjacent regions, there is a transition threshold hysteresis.

Due to the minimum on time and off time limitation, the transient threshold is different with switching frequency. In higher frequency operation, the $k_{\text{BST_BB}}$ is lower and $k_{\text{BB_BK}}$ is higher.

10.5 Bootstrap and Floating Driver

The bootstrap circuitry drives Q1 and Q4. The external flying capacitors are charged up to maintain a sufficient driving voltage above SW via the internal bootstrap regulators.

In buck-boost mode, the flying BST capacitor can be charged while the corresponding LS-FET is conducted.

However, in buck mode and boost mode, one HS-FET remains on, and its relevant LS-FET remains off for the entire switching cycle. Under this condition, the BST capacitors can charge each other through the internal charge regulator.

10.6 Error Amplifier

The SC8749Q integrates a high-performance operational amplifier to implement control loop compensation for stable VOUT regulation.

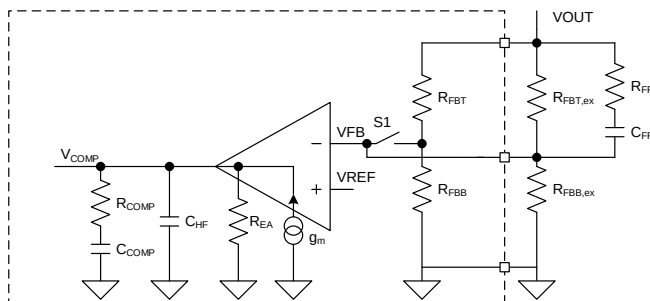


Figure 10.3 Compensation network

Figure 10.3 shows the compensation network integrated into the SC8749Q. With S1 ON, a typical Type II compensation network is implemented, where $R_{EA} = 10M\Omega$, $g_m = 25\mu A/V$, $C_{HF} = 1pF$. R_{CMOP} and C_{COMP} values can be configured via the I²C interface.

To optimize the converter's transient response, a Type III compensation network is also available. With S1 OFF, the Type III compensation network is comprised of the external feedback components and internal EA.

For SC8749QQFMR/SC8748QQFMR, S1 is set off, but for SC8749AQQFMR/SC8749BQQFMR, S1 is set on.

10.7 Spread Spectrum

To further optimize EMI performance, the SC8749Q integrates a frequency spread spectrum function. The modulation range and cycle can be set via the I²C interface.

The triangular frequency modulation varies the switching frequency higher and lower than the reference value. During a full modulation cycle, the switching frequency varies from the lowest to the highest value, then drops back to the lowest value.

10.8 APFM and FPWM under Light Loads

The SC8749Q can operate in auto pulse frequency modulation (APFM) or force pulse width modulation (FPWM) under light-load conditions.

APFM is applied to optimize efficiency under light-load conditions, in which the active SR switch stops switching once inductor current (I_L) reaches 0A. This means that I_L cannot drop to the negative value, and the output capacitor cannot be discharged further. In APFM, switching frequency (f_{sw}) is self-adjusting and does not follow the switching frequency setting.

When FPWM is enabled, I_L can drop to the negative value as long as the reverse current limit is not triggered. The converter acts as it would with a heavy load, and can maintain f_{sw} . FCCM results in a smaller output ripple, but has lower efficiency under light-load conditions.

10.9 Soft Start

Once VIN, VCC, and EN are all enabled, the converter begins switching, and the internal soft start is implemented.

The SC8749Q built-in soft start ramps up the internal reference voltage (VREF) from 0V to the expected value with a controlled slew rate. This slew rate can be configured via the I2C interface. VOUT can ramp up slowly to prevent the output voltage from overshooting.

During soft start, APFM mode is implemented for supporting pre-bias VOUT.

10.10 Dynamic Output Voltage Adjustment

If the SC8749Q operates in its normal input range (3.7V to 36V), VREF can be adjusted from 0.5V to 2.0V with a 10mV resolution. The converter features dynamic VOUT adjustments by changing VREF from the current value to the set value. VREF falls and rises in 10mV steps.

By controlling the time between steps using the I²C interface, the reference voltage variation slew rate can be adjusted. A longer time between steps results in a slower



slew rate. Figure 10.4 shows how VREF is adjusted while it increases.

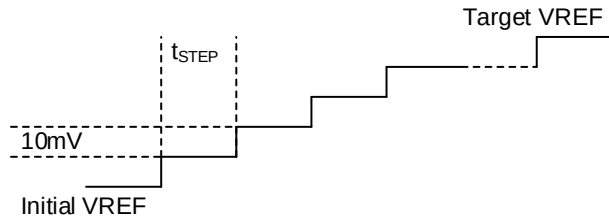


Figure 10.4 VREF increasing

Figure 10.5 shows how VREF is adjusted while it decreases. During VREF is decreasing, FPWM mode is implemented to ensure the slew-rate of VOUT.

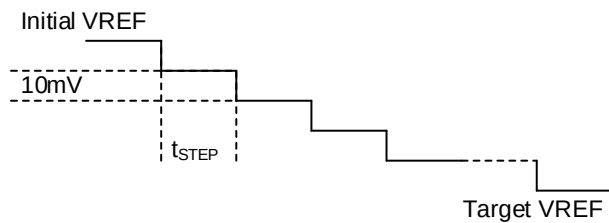


Figure 10.5 VREF decreasing

10.11 Setting the Output Voltage

For SC8749QQFMR/SC8748QQFMR, as described in 10.6, the internal output voltage feedback network was disabled, users need to choose suitable R_{Upper} and R_{Lower} to program the proper output voltage. The output voltage V_{OUT} is programmed by external voltage divider with the 1V internal voltage reference as given in equation (1). As for SC8749AQQFMR/SC8749BQQFMR, the internal feedback resistance will set working, the external feedback resistance is no longer need, as in this condition, the output voltage should be modified by I2C.

$$V_{OUT} = 1V \times \frac{R_{Upper} + R_{Lower}}{R_{Lower}} \quad (1)$$

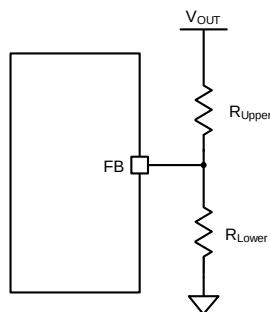


Figure 10.6 VOUT Configuration

10.12 Power Good (PG) Indicator

The PG pin is connected to the open drain of an internal MOSFET. PG should be connected to a voltage source through an external pull-up resistor to act as the power good indicator. The PG pin is pulled down to ground during soft start and regulation, or if VOUT is not within the allowable window. The over-/under-voltage threshold can be configured via the I²C interface. There is a delay time of about 80μs if the PG status flip flops.

10.13 Input Over-Voltage Protection (OVP)

The chip can provide an input OVP threshold at 33V (enabled by I²C interface). Once VIN exceeds this threshold, the converter stops switching immediately and sets the input OV fault flag. Once VIN returns to within the normal range, the SC8749Q automatically resumes normal operation.

10.14 Output Over-Voltage Protection (OVP)

The SC8749Q monitors VOUT with the PVOOUT pin. If VOUT exceeds 21.2V, the converter stops switching immediately, and an output OV fault is recorded.

There are two types of the optional output OVP modes: recoverable mode and latch-off mode, which can be selected via the I²C interface.

10.15 Over-Current Protection (OCP)

The SC8749Q provides a peak/valley current limit scheme designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device capabilities during overload or output short circuits conditions. During buck operation, the valley inductor current is limited, and Q1 does not turn on again until I_L falls below the valley limit. During boost or buck-boost operation, the peak inductor current is limited, and Q1 turns off immediately, once the I_L exceeds the peak limit.

If the internal EA's output level triggers the high clamp limit consecutively in a settled cycle, an over-current (OC) fault is recorded and OCP is activated. There are three optional OCP modes: recoverable, latch-off, and no response mode. OCP is screened during soft start.

In FPWM mode, the inductor current will below 0A during light load. To prevent damage to the part due to excessive reverse current, the SC8749Q monitors the current entering the relevant operating SR switch from the output. If this current exceeds the reverse current limit threshold, the relevant operating SR switch turns off and the relevant operating main switch conducts to reduce the reverse current.



The OCP mode and peak/valley current limit threshold can be selected via the I2C interface.

10.16 Output Under-Voltage Protection (UVP)

The SC8749Q provides output under-voltage protection (UVP) for hard output short. UVP is triggered if VOUT falls below the under-voltage (UV) threshold and OCP is triggered. There are three optional output UVP modes: recoverable, latch-off, and no response mode. The output UVP mode can be selected via the I2C interface.

10.17 Thermal Shutdown

Thermal shutdown is implemented to prevent the SC8749Q from operating at exceedingly high temperatures. If the silicon die temperature exceeds the thermal shutdown threshold, the over-temperature fault shuts down the whole chip. The thermal shutdown protection is auto-recoverable. Once the die temperature drops below its lower threshold, the chip starts up again and resumes normal operation.

10.18 Fault Response

After a fault occurs, the converter operates based on the corresponding fault mode setting. There are three operating schemes: recoverable, latch-off, and no response mode.

In recoverable mode, the converter attempts to soft start automatically, after a recovery time. If the fault condition is not removed, the converter reinitiates the fault protection and repeats the auto-recovery process in hiccup mode. If the fault condition is removed, the converter operates normally.

Latch-off mode stops the converter until the power on the input supply, EN is recycled, or EN_DCDC bit is toggled.

For OCP and UVP, no response mode can be selected. In this mode, the converter maintains switching in the peak/valley current limit unless thermal shutdown is triggered.

If FLG_CLR_MODE = 0, the fault flag can be cleared by reading relevant register. If FLG_CLR_MODE = 1, the fault flag maintains 1 until the next power on reset, EN is recycled, or EN_DCDC bit is toggled.

11. Application Curves

$V_{IN} = 13.5V$, $V_{OUT} = 11.6V$, $L = 4.7\mu H$, $F_{SW} = 400kHz$, forced PWM mode, $T_A = 25^\circ C$, unless otherwise noted.

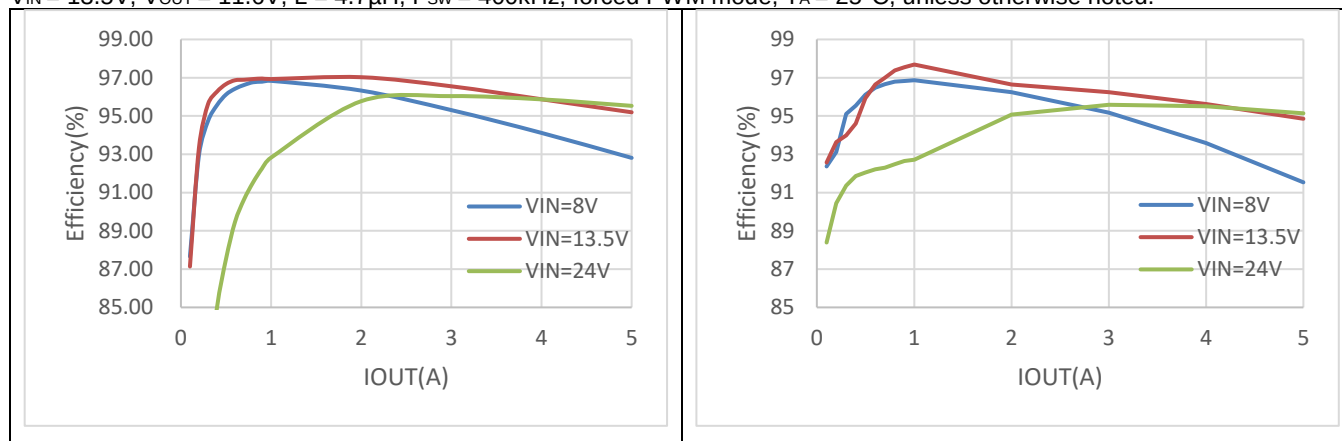
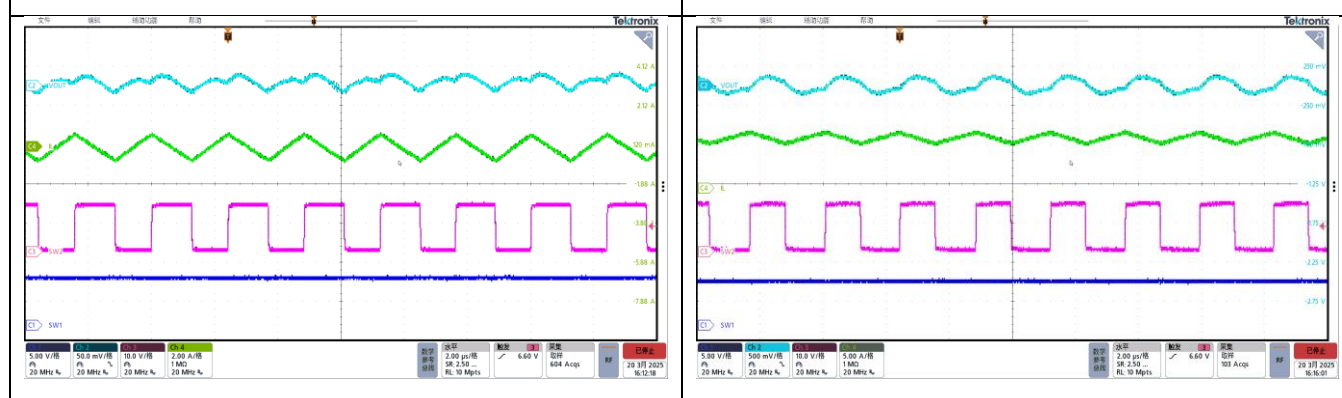


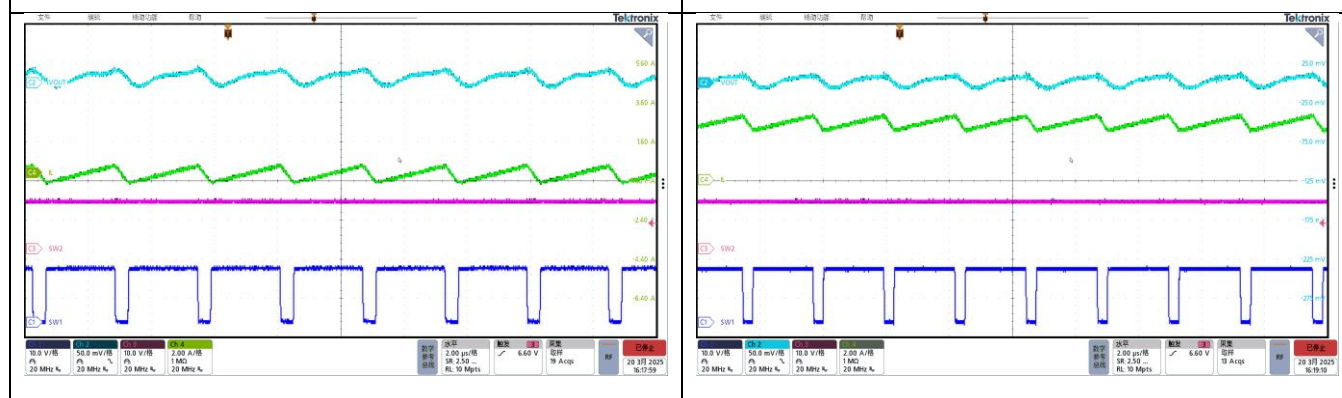
Figure 11-1 Efficiency Curve FPWM Mode

Figure 11-2. Efficiency Curve APFM Mode



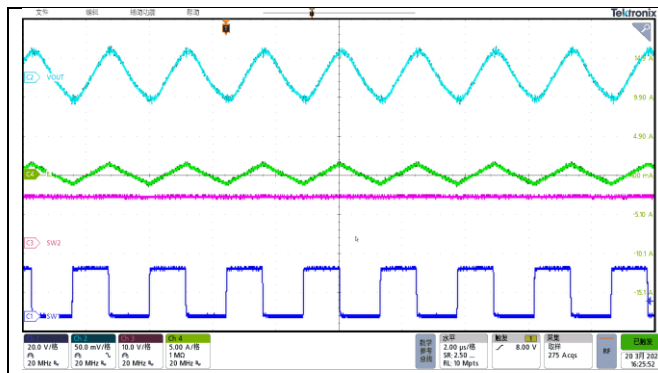
**VIN=6V VOUT=11.6V IOUT=0A FPWM Mode
Figure 11-3. Steady State**

**VIN=6V VOUT=11.6V IOUT=3A FPWM Mode
Figure 11-4. Steady State**

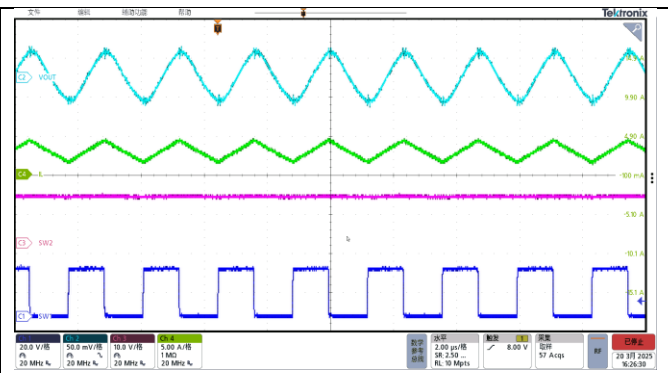


**VIN=13.5V VOUT=11.6V IOUT=0A FPWM Mode
Figure 11-5. Steady State**

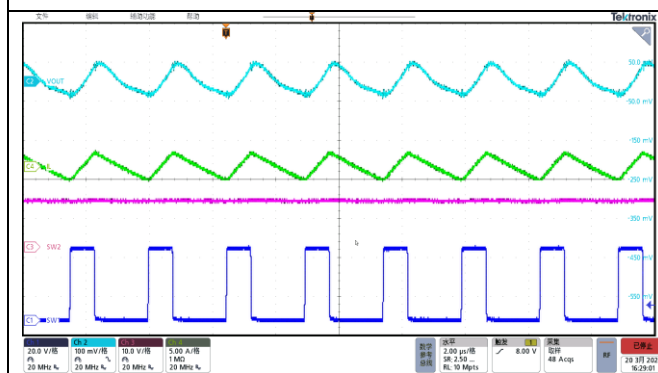
**VIN=13.5V VOUT=11.6V IOUT=3A FPWM Mode
Figure 11-6. Steady State**



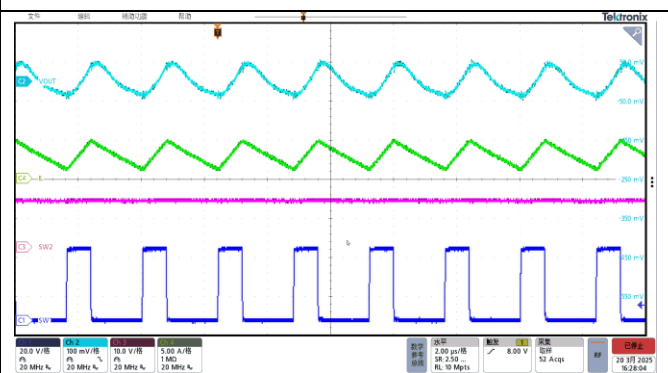
VIN=24V VOUT=11.6V IOUT=0A FPWM Mode
Figure 11-7. Steady State



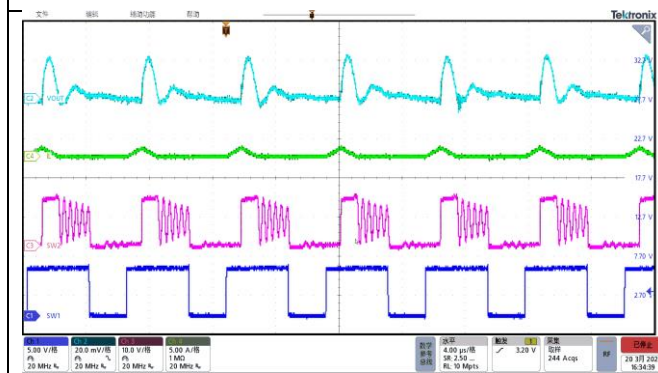
VIN=24V VOUT=11.6V IOUT=3A FPWM Mode
Figure 11-8. Steady State



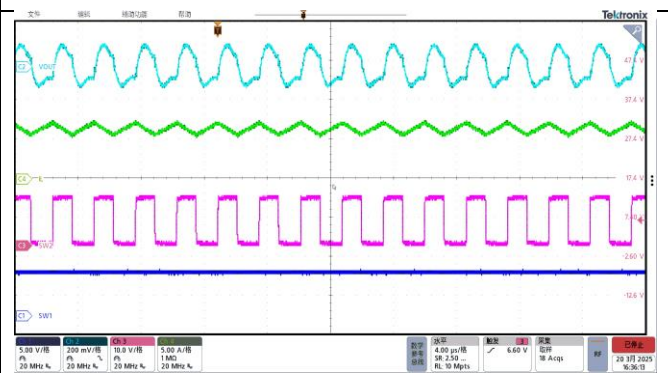
VIN=36V VOUT=11.6V IOUT=0A FPWM Mode
Figure 11-9. Steady State



VIN=36V VOUT=11.6V IOUT=3A FPWM Mode
Figure 11-10. Steady State

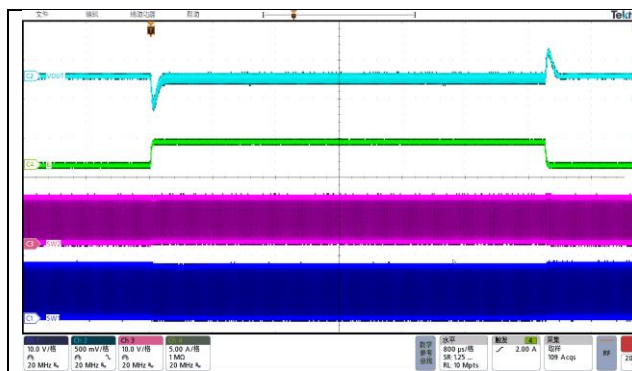


VIN=6V VOUT=11.6V IOUT=0A APFM Mode
Figure 11-11. Steady State

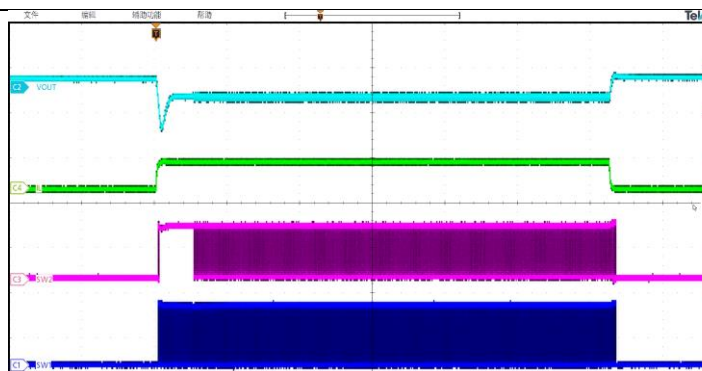


VIN=6V VOUT=11.6V IOUT=3A APFM Mode
Figure 11-12. Steady State

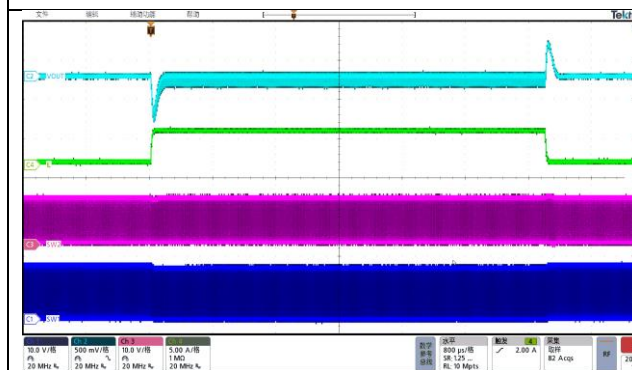




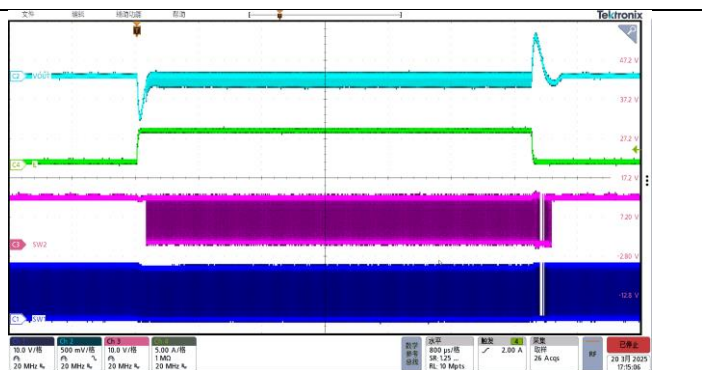
VIN=13.5V VOUT=11.6V IOUT 0A to 3A FPWM Mode
Figure 11-19. Load Transient



VIN=13.5V VOUT=11.6V IOUT 0A to 3A APFM Mode
Figure 11-20. Load Transient



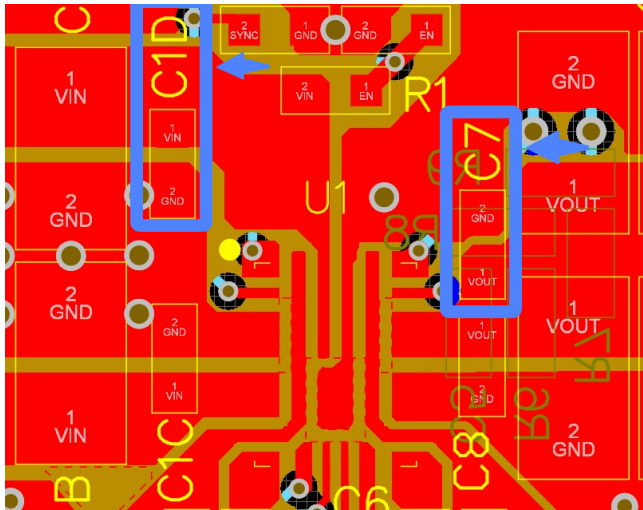
VIN=13.5V VOUT=11.6V IOUT 0.5A to 4.5A FPWM
Mode
Figure 11-15. Steady State



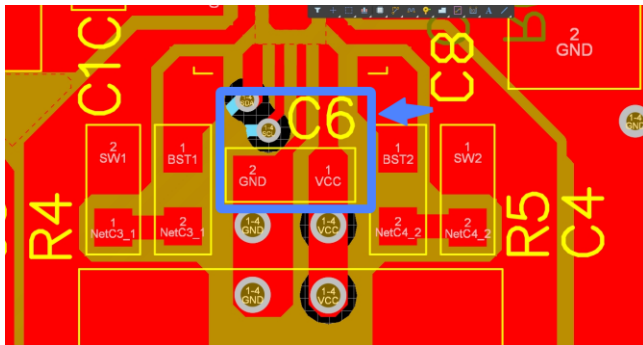
VIN=13.5V VOUT=11.6V IOUT 0.5A to 4.5A APFM Mode
Figure 11-16. Steady State

12. Layout Guide

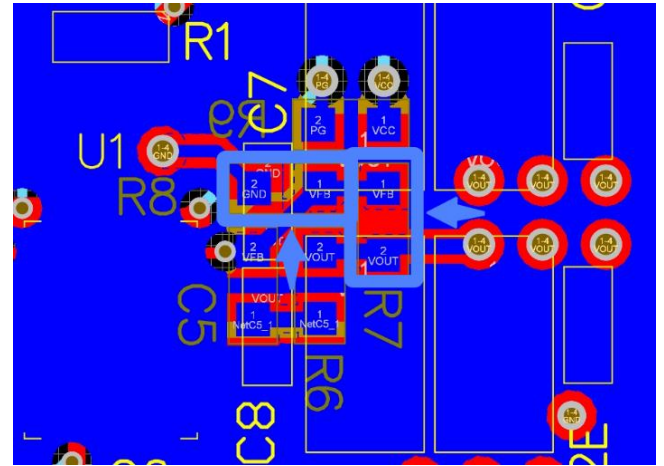
1. To minimize high-frequency noise, place the ceramic input capacitor, particularly the input/output bypass capacitor with a small package size (0603), as close as possible to the PVIN/PVOUT and PGND pins.



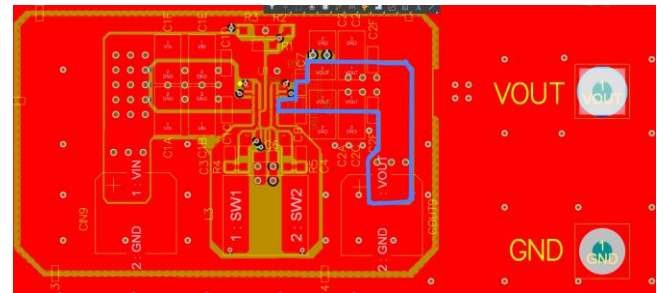
2. The 4.7 μ F capacitors connected at VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.



3. The voltage-dividing resistors for the Feedback loop should be placed as close as possible to the FB PIN of the chip.



4. Keep the connection between the input/output capacitor and PVIN/PVOUT as short and wide as possible.





13. Register Map

Device I2C address is 0x01

Register Name	Offset	Bit Field				
		Bits	Field Name	Access	Value (hex)	Description
VDAC_REG	0x00H	7:0	VDAC_REG	RW	X	Sets the reference voltage, calculated with the following equation: 00h to 31h: Reserved 32h to C8h: VREF = REF [7:0] x 10mV (resolution: 10mV) C9h to FFh: Reserved The default value(hex) depends on the IC version. SC8749QQFMR/SC8748QQFMR default value: 64h SC8749AQ default value: 74h SC8749BQ default value: 09h
CTRL	0x01H	7	EN_DCDC	RW	01h	This bit enables power converter on/off control. 0: Disabled 1: Enabled
		6:5	RESERVED	NA	00h	Reserved
		4:3	STEP_TIME	RW	02h	Sets the time of each step during soft start and output voltage dynamic adjustment mode (in μ s). 00h: 20; 01h: 40 02h: 80; 03h: 160
		2:0	FB_DR	RW	04h	Sets the divider ratio of the reference voltage and output voltage. 00h~03h: 1/5 04h~07h: 1/10
Reserved	0x02H	7:0	RESERVED	NA	00h	Reserved
FSW	0x03H	7:6	RESERVED	NA	00h	Reserved
		5:0	FSW	RW	08h	Sets the switching frequency of the converter. 00h to 06h: 200kHz 07h to 0Ah: 400kHz 0Bh to 10h: 600kHz 11h to 3Fh: 1000kHz
DITHER	0x04H	7	EN_DTHR	RW	01h	This bit enables frequency spread spectrum. 0: Disabled 1: Enabled
		6:4	DTHR_RANGE	RW	00h	Sets the dither modulation range (in 1% x fSW). 00h to 03h: ± 10 04h to 07h: ± 20
		3	RESERVED	NA	00h	Reserved



		2:0	DTHR_FREQ	RW	00h	Sets the dither modulation frequency. 00h to 01h: FSW/128 02h to 03h: FSW/512 04h to 05h: FSW/128 06h to 07h: FSW/32
CL	0x05H	Bits	Field Name	Access	Value (hex)	Description
		7	EN_FPWM	RW	01h	Selects Auto PFM or FPWM operation. 0: Auto PFM 1: FPWM
		6	RESERVED	NA	00h	Reserved
		5:3	RESERVED	NA	00h	Reserved
		2:0	RESERVED	NA	00h	Reserved
RCOMP	0x06H	Bits	Field Name	Access	Value (hex)	Description
		7	RESERVED	NA	00h	Reserved
		6	RESERVED	NA	00h	Reserved
		5:0	R_COMP	RW	08h	Selects RCOMP (in kΩ). 00h to 07h: 108 08h to 0Fh: 237 10h to 17h: 366 18h to 1Fh: 603 20h to 27h: 173k 28h to 2Fh: 302k 30h to 37h: 431k 38h to 3Fh: 668k
CCOMP	0x07H	Bits	Field Name	Access	Value (hex)	Description
		7:5	RESERVED	NA	00h	Reserved
		4:0	C_COMP	RW	18h	Selects CCOMP (in pF). 00h to 07h: 60 08h to 0Fh: 80 10h to 17h: 100 18h to 1Fh: 120
HALF	0x08H	Bits	Field Name	Access	Value (hex)	Description
		7:4	RESERVED	NA	00h	Reserved
		3	BB_HALF	RW	00h	Sets frequency mode under Buck-boost condition. 0: Keep the same frequency as Buck and Boost mode 1: Reduce frequency to half of Buck and Boost mode
		2	EN_EX_RFB	RW	00h	Selects the feedback resistance, which can be internal or external: 0: Use the internal feedback resistance 1: Use the external feedback resistance
		1:0	RESERVED	NA	00h	Reserved
Reserved	0x09H	Bits	Field Name	Access	Value (hex)	Description
		7:0	RESERVED	NA	00h	Reserved



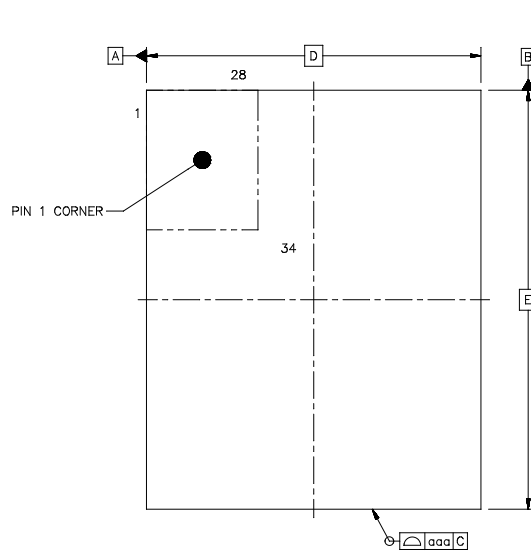
Reserved	0x0AH	Bits	Field Name	Access	Value (hex)	Description
		7:0	RESERVED	NA	00h	Reserved
PG&OCP	0x0BH	Bits	Field Name	Access	Value (hex)	Description
		7	RESERVED	NA	00h	Reserved
		6	PG_OV	RW	00h	Sets the power good high limit (VOUT rising edge). 0: VFB = 110% of VREF 1: VFB = 120% of VREF
		5	RESERVED	NA	00h	Reserved
		4	PG_UV	RW	00h	Sets the power good low limit (VOUT falling edge). 0: VFB = 90% of VREF 1: VFB = 80% of VREF
		3:2	RESERVED	NA	00h	Reserved
		1:0	OCP_MODE	RW	00h	Selects the over-current protection (OCP) mode. 00h: Recoverable mode 01h: Latch-off mode 02h to 03h: No-response mode
FLGCT&UVP	0x0CH	Bits	Field Name	Access	Value (hex)	Description
		7	FLG_CLR_MODE	RW	00h	This bit selects the fault protection mode. 0: Read-clear mode. 1: Latch-off mode. The power on EN must be cycled to reset the fault bits
		6:2	RESERVED	RW	00h	Reserved
		1:0	UVP_MODE	RW	00h	Selects the UVP mode. 00h: Recoverable mode 01h: Latch-off mode 02h to 03h: No-response mode
IN&OUT ABSOVP	0x0DH	Bits	Field Name	Access	Value (hex)	Description
		7	RESERVED	RW	00h	Reserved
		6:5	EN_VIN_OVP	RW	00h	Sets the VIN OVP threshold (rising edge) (in V). 00h to 01h: Disable 02h to 03h: Enable
		4:1	RESERVED	RW	00h	Reserved
		0	VOUT_OVP_MODE	RW	00h	Selects the VOUT OVP mode. 0: Recoverable mode 1: Latch-off mode
Reserved	0x0EH	Bits	Field Name	Access	Value (hex)	Description
		7:0	Reserved	NA	00h	Reserved
STATUS	0x0FH	Bits	Field Name	Access	Value (hex)	Description
		7:6	Reserved	NA	00h	Reserved



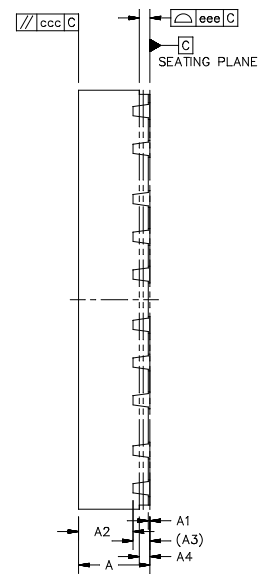
		5	PGOOD_STATUS	R	00h	This bit indicates the power good status. This bit is read-only. 0: Power not good 1: Power good
		4	VIN_OVP_FLG	R	00h	This bit indicates the VIN over-voltage (OV) status. This bit is read-only. 0: No VIN OVP condition has occurred 1: VIN OVP condition has occurred
		3	OCP_FLG	R	00h	This bit indicates the over current (OC) status. This bit is read-only. 0: No OCP has occurred 1: OCP has occurred
		2	VOUT_OVP_FLG	R	00h	This bit indicates the VOUT over-voltage (OV) status. This bit is read-only. 0: No VOUT OVP has occurred 1: VOUT OVP has occurred
		1	UVP_FLG	R	00h	This bit indicates the VOUT under-voltage (UV) status. This bit is read-only. 0: No VOUT UVP has occurred 1: VOUT UVP has occurred
		0	TSD_FLG	R	00h	This bit indicates the thermal shutdown (TSD) status. This bit is read-only. 0: No TSD has occurred 1: TSD has occurred

MECHANICAL DATA

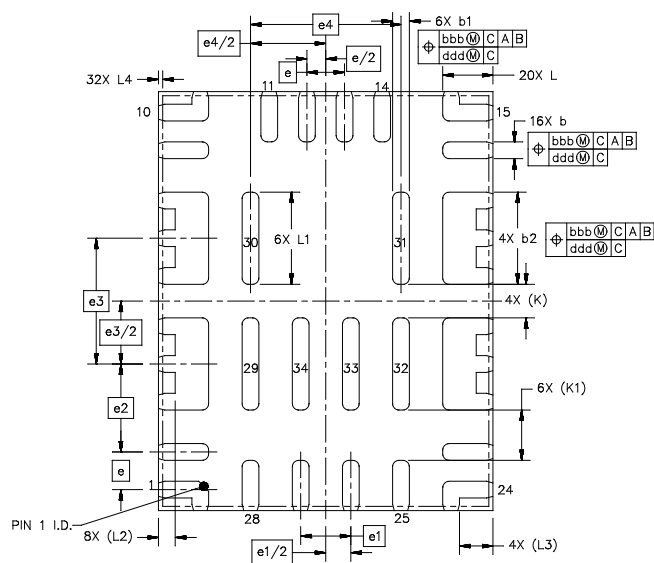
QFN-34 (4mm x 5mm)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

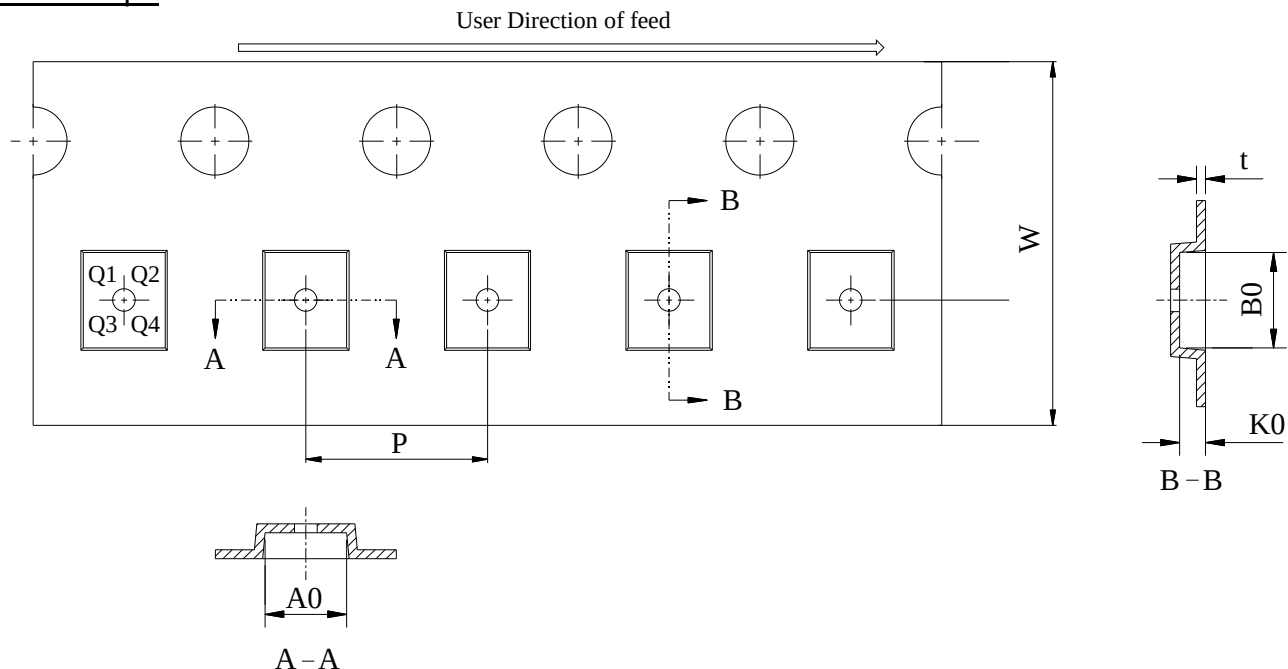


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS	0.01	A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
SIDE WETTABLE DEPTH		A4	0.1	---	0.18
LEAD WIDTH		b	0.15	0.2	0.25
		b1	0.1	0.2	0.3
		b2	1.05	1.1	1.15
BODY SIZE	X	D	4 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.45 BSC		
		e1	0.6 BSC		
		e2	1.05 BSC		
		e3	1.5 BSC		
		e4	1.8 BSC		
LEAD LENGTH		L	0.5	0.6	0.7
		L1	1	1.1	1.2
LEAD EDGE TO PACKAGE		L2	0.2 REF		
		L3	0.4 REF		
SIDE WETTABLE WIDTH		L4	0.01	---	0.09
LEAD TIP TO LEAD TIP		K	0.4 REF		
		K1	0.6 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		

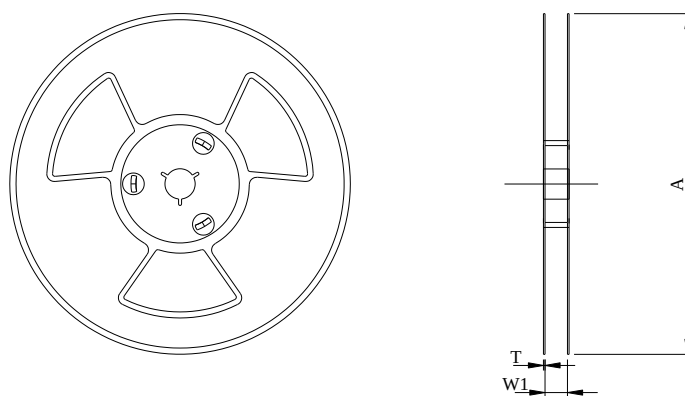


TAPE AND REEL INFORMATION

QFN-34 (4mm x 5mm)

Carrier Tape

Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	$12.0^{+0.3}_{-0.1}$	8.0 ± 0.10	4.25 ± 0.05	5.25 ± 0.05	1.02 ± 0.05	0.25 ± 0.02	Q1

REEL

Item	A	W1	T
Size (mm)	330.0 ± 1.0	$12.4^{+1.0}_{-0.0}$	$2.6^{+1.0}_{-0.0}$



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