



SC6201Q High-Performance PMIC with Buck Converters and LDO for Automotive Camera Module

1. Descriptions

The SC6201Q is a high-performance Power Management IC (PMIC) for automotive camera modules. It includes a high-voltage buck converter for a primary regulator, dual low-voltage buck converters and a LDO for secondary regulators.

The device is powered by a primary high-voltage buck converter with an input voltage range from 4V to 19V through a Power Over Coax (POC) connection. The dual low-voltage buck converters and the LDO are powered by the output of the high-voltage buck converter and the input voltage ranges from 2.7V to 5.5V. The high-voltage buck converter supports adjustable output voltage and 2A output current. The low-voltage buck converters adopt fixed output voltage and support 1.5A and 0.75A output current, respectively. All the switching converters operate in a forced fixed-frequency of 2.2MHz PWM mode with spread spectrum and phase shift. The LDO features a high Power Supply Rejection Ratio (PSRR) and provides adjustable output voltage through an external resistor.

The CMOS Image Sensors(CIS) not only require different drive voltage settings and sequence control depending on the manufacturer but are typically configured utilizing many external components. The SC6201Q adopts a small 3mm x 3mm QFN package and configure pins for setting CIS sequence and voltage control to reduce external components, contributing to the design of smaller automotive camera modules.

The device integrates full protections, including input under-voltage and over-voltage protection, output under-voltage and over-voltage protection, cycle-by-cycle current limitation, and thermal shutdown protection.

3. Applications

- Automotive Camera Module
- Automotive Sensor Applications

2. Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: T_A range: -40°C to 125°C
- 3 Buck converters (HVBuck1, LVBuck2, LVBuck3)
 - Peak current mode with FPWM Operation
 - Fixed frequency at 2.2MHz
 - Spread spectrum for better EMI
- Primary high-voltage buck converter 1 (HVBuck1)
 - 4V~19V input voltage range
 - Adjustable output with 2A output current
- Secondary low-voltage buck converter 2 (LVBuck2)
 - 2.7V~5.5V input voltage range
 - Fixed output with 1.5A output current
- Secondary low-voltage buck converter 3 (LVBuck3)
 - 2.7V~5.5V input voltage range
 - Fixed output with 0.75A output current
- Secondary LDO
 - 2.7V~5.5V input voltage range
 - High PSRR 60dB at 100KHz
 - 400mA output current
 - Program output voltage through RSET pin
- 10 Flexible power sequence settings through SEQ Pin
- Open drain pin as power good indication
- Open drain pin as external power sequence control
- Secondary converters LVbuck2/3 allow unused
- Compact QFN-16 3 x 3 wettable flank package



4. Device Information

ORDER NUMBER	PIN11 FUNCTION	HVBUCK1 OUTPUT	LVBUCK2 OUTPUT(*)	LV BUCK3 OUTPUT(*)	PG DELAY(*)	BODY SIZE
SC6201QA1QDKR	PG	Adjustable	1.1V	1.8V	10ms	3mm x 3mm x 0.75mm
SC6201QA2QDKR	PG	Adjustable	1.2V	1.8V	10ms	3mm x 3mm x 0.75mm
SC6201QB1QDKR(*)	EXT	Adjustable	1.1V	1.8V	10ms	3mm x 3mm x 0.75mm
SC6201QB2QDKR(*)	EXT	Adjustable	1.2V	1.8V	10ms	3mm x 3mm x 0.75mm

(1) For other output voltage, EXT function or PG delay option, please contact Southchip.



5. Revision History

Revision	Date	Page(s) Changed	Changes Description
V1.0.0	2024/9	NA	1. Initial version
V1.0.1	2024/12	NA	2. Update EC table limit with large samples test data



6. Typical Application Circuit

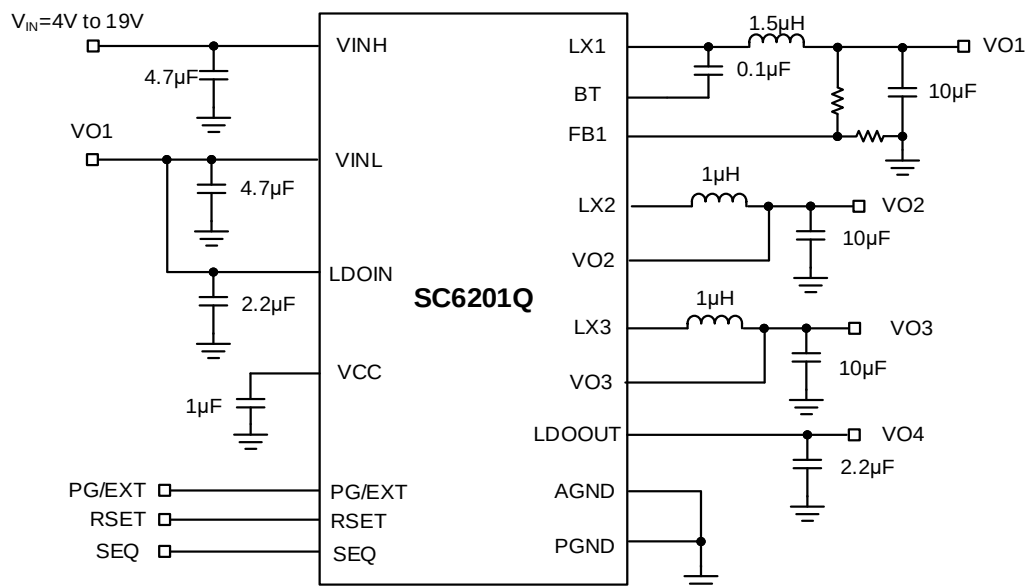
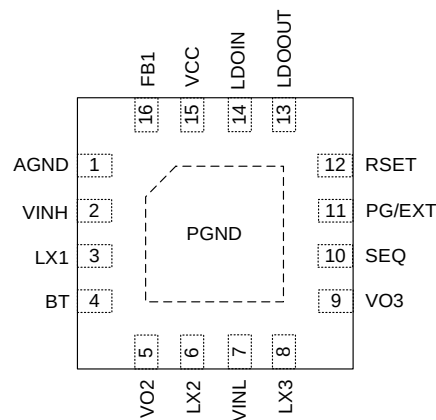


Figure 6-1 Typical Application Circuit of SC6201Q



7. Terminal Configuration and Functions

TOP VIEW



QFN 3X3-16

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	AGND	G	Analog ground
2	VINH	I	Power supply input of primary high-voltage buck converter 1
3	LX1	O	Switching node of primary high-voltage buck converter 1
4	BT	O	Bootstrap of primary high-voltage buck converter 1. Connect a 100nF capacitor between the BT pin and LX1 pin to bootstrap a bias voltage for the high-side MOSFET driver.
5	VO2	I	Feedback sense of secondary low-voltage buck converter 2
6	LX2	O	Switching node of secondary low-voltage buck converter 2
7	VINL	I/O	Power supply input of secondary low-voltage buck converters 2 & 3
8	LX3	O	Switching node of secondary low-voltage buck converter 3
9	VO3	I	Feedback sense of secondary low-voltage buck converter 3
10	SEQ	I	Power-on sequence selection
11	PG	O	Open drain output of power-good.PG at high impedance if all activated rails are well regulated. Available for SC6201QA only
	EXT	O	Open drain output for external power sequence control. Available for SC6201QB only
12	RSET	I	Output voltage selection of secondary LDO
13	LDOOUT	O	Output of secondary LDO
14	LDOIN	I/O	Power supply input of secondary LDO
15	VCC	O	Internal analog power output. Connect a 1μF ceramic capacitor from VCC to the ground.
16	FB1	I	Feedback sense of primary high-voltage buck converter 1
17	PGND	G	Power ground of the all converters.



8. Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C ~ 150°C (unless otherwise noted) ⁽¹⁾

PARAMETER		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	VINH, LX1 to AGND, PGND	-0.3	25	V
	BT to AGND, PGND	-0.3	28	V
	BT to LX1	-0.3	6	V
	VINL, FB1, VO2, VO3, LDOIN, LDOOUT, VCC, SEQ, RSET, PG/EXT,	-0.3	6	V
	LX2, LX3 to AGND, PGND	-0.3	6.5	V
T _j	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V _{INH}	Input voltage range for primary high-voltage buck	4		19	V
V _{INL}	Input voltage range for secondary low-voltage buck and LDO	2.7		5.5	V
L _{HV}	Inductor for primary high-voltage buck	1	1.5	2	μH
L _{LV}	Inductor for secondary low-voltage buck	0.68	1	1.2	μH
C _{OUT}	Output capacitor for buck converters	4.5	10	14	μF
C _{INLDO}	Input capacitor for secondary LDO	0.7	2.2	10	μF
C _{OUTLDO}	Output capacitor for secondary LDO	0.7	2.2	10	μF
T _A	Operating ambient temperature	-40		125	°C
T _j	Operating junction temperature	-40		150	°C



8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		QFN-16 (3mm x 3mm)	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance	30	°C/W
$R_{\theta JC}$	Junction to case resistance	17	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.3	°C/W

(1) Measured on JESD51-7, 4-layer PCB.



8.5 Electrical Characteristics

$T_J = -40 \sim +125^{\circ}\text{C}$ and $V_{\text{INH}} = 8\text{V}$, $V_{\text{O1}} = 3.6\text{V}$, $V_{\text{O2}} = 1.1\text{V}$, $V_{\text{O3}} = 1.8\text{V}$, $V_{\text{O4}} = 3.3\text{V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATE CONDITION						
V _{INH}	High input voltage range for primary buck converter		4		19	V
V _{INL}	Low input voltage range for secondary buck converters		2.7		5.3	V
V _{INH_UVLO}	Input under voltage lockout threshold	Rising edge	3.6	3.8	4.0	V
		Falling edge	3.1	3.3	3.5	V
V _{INH_OVP}	Input over voltage protection threshold for primary HVBuck1	Rising edge	20	21	22	V
		Falling edge	19	20	21	V
V _{INL_OVP}	Input over voltage protection threshold for secondary LVBuck2&3	Rising edge	5.5	5.9	6.3	V
		Falling edge	5.0	5.4	5.9	V
V _{LDOIN_OVP}	Input over voltage protection threshold for LDO	Rising edge	5.5	5.9	6.3	V
		Falling edge	5.0	5.4	5.8	V
T _{SD}	Thermal shutdown temperature threshold	Rising edge		160		°C
		Falling edge		140		°C
SWITCHING CHARACTERISTICS OF BUCK CONVERTERS						
F _{SW}	Switching frequency		2.0	2.2	2.4	MHz
R _{SS}	Spread spectrum range			6		%
VO1 HVBUCK 1						
V _{O1_RANGE}	VO1 output volage range	Normal buck mode	2.7		5.3	V
V _{FB1}	VO1 feedback voltage		0.788	0.8	0.812	V
I _{PCL_HVB1}	High side switch current limit		2.4	3.0	3.6	A
I _{VCL_HVB1}	Low side switch current limit		2.1	2.7	3.5	A
I _{NCL_HVB1}	Negative inductor peak current limit		1	2.5	4	A
R _{ON_HVB1_H}	High side MOSFET on resistance			200	330	mΩ
R _{ON_HVB1_L}	Low side MOSFET on resistance			110	190	mΩ
T _{MIN_ON_HVB1}	HVBUCK1 minimum on time				70	ns
T _{MIN_OFF_HVB1}	HVBUCK1 minimum off time			55	110	ns
R _{VO1}	Fast discharge resistance		210	270	330	Ω
T _{SS_VO1}	Soft start-up time	From 0 to 90% of V _{O1} , no load	0.4	1	1.5	ms
P _{FB1_UVP}	Output under voltage falling threshold			50		%
P _{FB1_OVP}	Output over voltage rising threshold		103	110	117	%
	Output over voltage falling threshold		100	106	112	%
VO2 LVBUCK 2						
V _{O2}	VO2 output voltage	SC6201QA1, SC6201QB1	1.084	1.1	1.117	V



		SC6201QA2, SC6201QB2	1.182	1.2	1.218	V
I _{PCL_LVB2}	High side switch current limit		1.8	2.2	2.8	A
I _{VCL_LVB2}	Low side switch current limit		1.6	2.0	2.7	A
I _{NCL_LVB2}	Negative inductor peak current limit		0.7	1.7	2.9	A
R _{ON_LVB2_H}	High-side PMOS on resistance			150	280	mΩ
R _{ON_LVB2_L}	Low-side NMOS on resistance			80	130	mΩ
T _{MIN_ON_LVB2}	LVBUCK2 minimum on time				70	ns
T _{MIN_OFF_LVB2}	LVBUCK2 minimum off time				60	ns
R _{VO2}	Fast discharge resistance	V _{O2} =0.3V	4	6	10	Ω
T _{SS_VO2}	Soft start-up time	From 0 to 90% of V _{O2} , no load	0.2	0.5	1	ms
P _{VO2_UVP}	Output under voltage falling threshold		40	50	60	%
P _{VO2_OVP}	Output over voltage rising threshold		114	120	126	%
	Output over voltage falling threshold		104	110	116	%
VO3 LVBUCK 3						
V _{O3}	VO3 output voltage		1.773	1.8	1.827	V
I _{PCL_LVB3}	High side switch current limit		0.96	1.2	1.6	A
I _{VCL_LVB3}	Low side switch current limit			1.0		A
I _{NCL_LVB3}	Negative inductor peak current limit		0.7	1.3	2.2	A
R _{ON_LVB3_H}	High-side PMOS on resistance			350	530	mΩ
R _{ON_LVB3_L}	Low-side NMOS on resistance			150	250	mΩ
T _{MIN_ON_LVB3}	LVBUCK3 minimum on time			50	70	ns
T _{MIN_OFF_LVB3}	LVBUCK3 minimum off time				60	ns
R _{VO3}	Fast discharge resistance	V _{O3} =0.3V	4	6	10	Ω
T _{SS_VO3}	Soft start-up time	From 0 to 90% of V _{O3} , no load	0.2	0.5	1	ms
P _{VO3_UVP}	Output under voltage falling threshold		40	50	60	%
P _{VO3_OVP}	Output over voltage rising threshold		114	120	126	%
	Output over voltage falling threshold		104	110	116	%
VO4 LDO						
V _{O4_RANGE}	LDO Output Range	V _{O4} selected by RSET pin	1.8		3.5	V
P _{VO4}	VO4 accuracy	V _{LDOIN} -V _{LDOOUT} >0.3V, I _{O4} =0~400mA	-1.5		1.5	%
I _{VO4_MAX}	Maximum output current capability				400	mA
I _{CL_LDO}	LDO current limit		400			mA
V _{DROP_LDO}	LDO dropout voltage	I _{O4} =150mA			150	mV
		I _{O4} =300mA			300	mV
R _{VO4}	Fast discharge resistance		30	60	100	Ω
T _{SS_VO4}	Soft start-up time	From 0 to 90% of V _{O4} , no load	0.2	0.7	1.3	ms
P _{VO4_UVP}	Output under voltage falling threshold		40	50	60	%



P _{VO4_OVP}	Output over voltage rising threshold		120	125	130	%
	Output over voltage falling threshold		105	110	115	%
VCC REGULATOR						
V _{O_VCC}	Internal VCC output voltage		4.33	4.58	4.83	V
I _{CL_VCC}	Internal VCC current limit	V _{CC} >2.6V	20	45	70	mA
LOGIC AND INTERFACE						
V _{PG_LOW}	PG pin pull-low voltage	Current into PG pin is 5mA	35	100		mV
I _{PG_LKG}	PG pin leakage	PG = 1.8V		1		μA
T _{d_PG}	PG pin output delay time		9	10	12	ms
V _{EXT_LOW}	EXT pin pull-low voltage	Current into EXT pin is 5mA	35	100		mV
I _{EXT_LKG}	EXT pin leakage	EXT = 1.8V		1		μA



8.6 System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. ($T_J = -40 \sim +125^\circ\text{C}$, $V_{\text{INH}} = 8\text{V}$, $V_{\text{O1}} = 3.6\text{V}$, $V_{\text{O2}} = 1.1\text{V}$, $V_{\text{O3}} = 1.8\text{V}$, $V_{\text{O4}} = 3.3\text{V}$, unless otherwise noted, unless otherwise specified.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VO1 HVBUCK 1						
$I_{\text{MAX_OUT1}}$	Maximum Output Current		2			A
$V_{\text{LOAD_REG1}}$	Load Regulation	$I_{\text{OUT1}} = 0\text{A to } 2\text{A}$			0.1	%/A
$V_{\text{LINE_REG1}}$	Line Regulation	$V_{\text{IN}} = 5\text{V to } 19\text{V}$, $I_{\text{OUT1}} = 2\text{A}$			1	%
$V_{\text{LOAD_TRAIN1}}$	Load Transient	$I_{\text{OUT1}} = 10\text{mA to } 500\text{mA to } 10\text{mA}$, $1\mu\text{s}$	-120		120	mV
$V_{\text{LINE_TRAIN1}}$	Line Transient	$V_{\text{IN}} = 5\text{V to } 19\text{V to } 5\text{V}$, $100\mu\text{s}$, $I_{\text{OUT1}} = 10\text{mA}/500\text{mA}$	-50		50	mV
V_{RIPPLE1}	Output Ripple	Peak to peak in one switching cycle			20	mV
VO2 LVBUCK 2						
$I_{\text{MAX_OUT2}}$	Maximum Output Current		1.5			A
$V_{\text{LOAD_REG2}}$	Load Regulation	$I_{\text{OUT2}} = 0\text{A to } 2\text{A}$			0.1	%/A
$V_{\text{LINE_REG2}}$	Line Regulation	$V_{\text{IN}} = 3\text{V to } 5\text{V}$, $I_{\text{OUT2}} = 1.5\text{A}$			1	%
$V_{\text{LOAD_TRAIN2}}$	Load Transient	$I_{\text{OUT2}} = 10\text{mA to } 500\text{mA to } 10\text{mA}$, $1\mu\text{s}$	-50		50	mV
$V_{\text{LINE_TRAIN2}}$	Line Transient	$V_{\text{IN}} = 3\text{V to } 5\text{V to } 3\text{V}$, $100\mu\text{s}$, $I_{\text{OUT2}} = 10\text{mA}/500\text{mA}$	-50		50	mV
V_{RIPPLE2}	Output Ripple	Peak to peak in one switching cycle			10	mV
VO3 LVBUCK 3						
$I_{\text{MAX_OUT3}}$	Maximum Output Current		750			mA
$V_{\text{LOAD_REG3}}$	Load Regulation	$I_{\text{OUT3}} = 0\text{A to } \text{A}$			0.1	%/A
$V_{\text{LINE_REG3}}$	Line Regulation	$V_{\text{IN}} = 3\text{V to } 5\text{V}$, $I_{\text{OUT3}} = 750\text{mA}$			1	%
$V_{\text{LOAD_TRAIN3}}$	Load Transient	$I_{\text{OUT3}} = 10\text{mA to } 300\text{mA to } 10\text{mA}$, $1\mu\text{s}$	-40		40	mV
$V_{\text{LINE_TRAIN3}}$	Line Transient	$V_{\text{IN}} = 3\text{V to } 5\text{V to } 3\text{V}$, $100\mu\text{s}$, $I_{\text{OUT3}} = 10\text{mA}/300\text{mA}$	-50		50	mV
V_{RIPPLE3}	Output Ripple	Peak to peak in one switching cycle			10	mV
VO4 LDO						
PSRR_{LDO}	Power Supply Rejection Ratio	$I_{\text{OUT_LDO}} = 100\text{mA}$, $f = 100\text{kHz}$		60		dB
		$I_{\text{OUT_LDO}} = 100\text{mA}$, $f = 1\text{MHz}$		40		dB
$e_{\text{N_LDO}}$	Output Noise Voltage	$I_{\text{OUT_LDO}} = 100\text{mA}$, $f = 100\text{Hz to } 100\text{kHz}$		60		μV
$V_{\text{LOAD_TRAIN3}}$	Load Transient	$I_{\text{OUT_LDO}} = 10\text{mA to } 200\text{mA to } 10\text{mA}$, $1\mu\text{s}$	-25		25	mV
$V_{\text{LINE_TRAIN3}}$	Line Transient	All $V_{\text{OUT_LDO}}$, $V_{\text{IN_LDO}}$ step 600mV , LDO not in dropout condition, $10\mu\text{s}$, $I_{\text{OUT_LDO}} = 1\text{mA}/300\text{mA}$	-25		25	mV



8.7 Typical Characteristics

$V_{INH}=8V$, $V_{O1}=V_{INL}=V_{LDOIN}=3.6V$, $V_{O2}=1.1V$, $V_{O3}=1.8V$, $V_{O4}=3.3V$, unless otherwise noted.

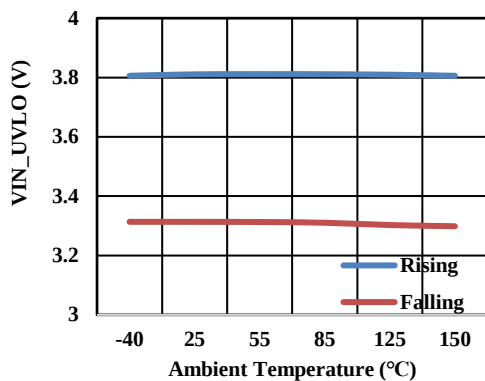


Figure 11-1, V_{IN_UVLO} vs Temperature

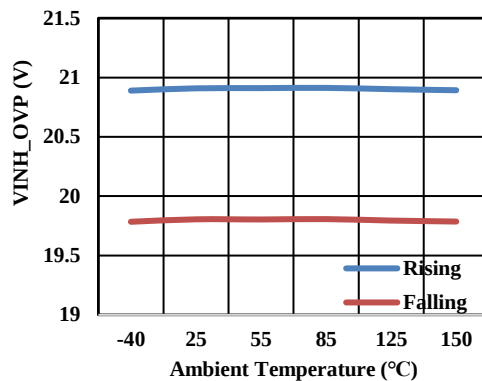


Figure 11-2, V_{INH_OVP} vs Temperature

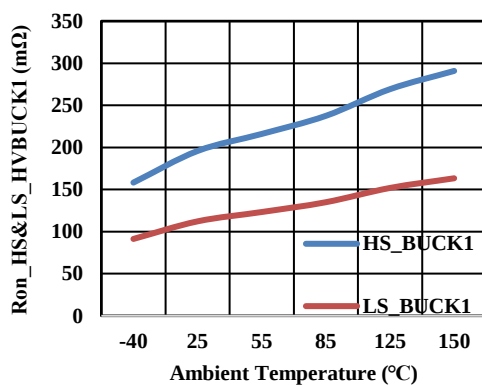


Figure 11-3, $R_{DS(on_HVBUCK1)}$ vs Temperature

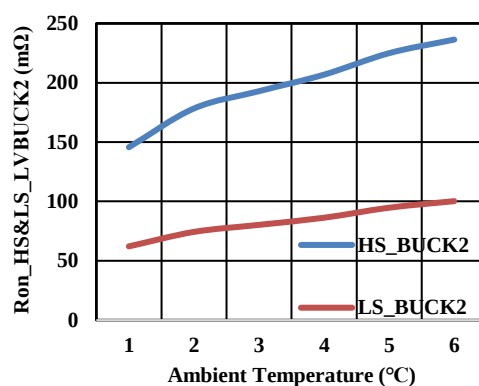


Figure 11-4, $R_{DS(on_LVBUCK2)}$ vs Temperature

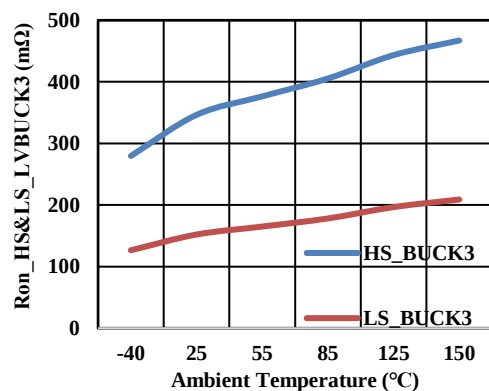


Figure 11-5, $R_{DS(on_LVBUCK3)}$ vs Temperature

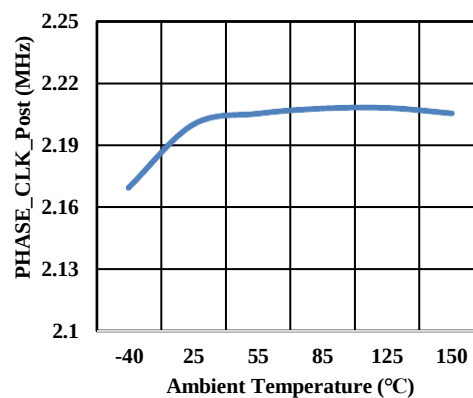
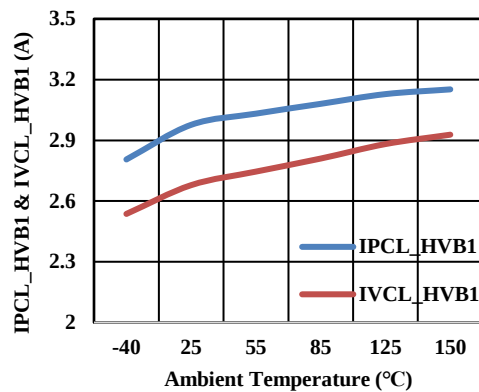
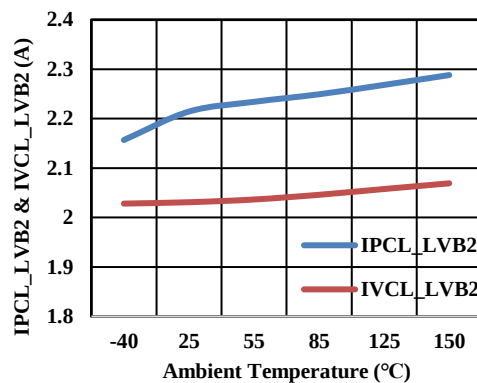
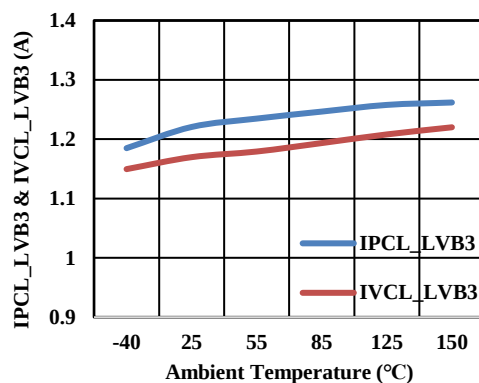
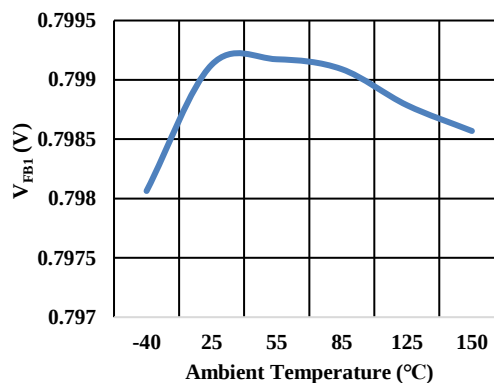
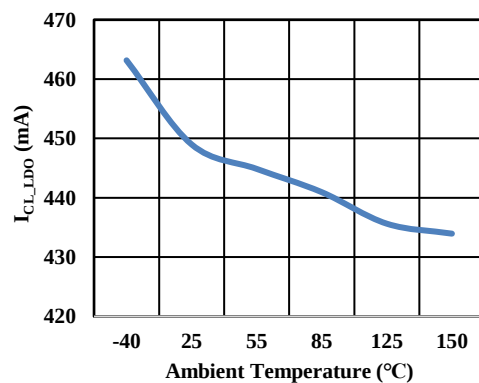


Figure 11-6, $PHASE_CLK$ vs Temperature

Figure 11-7, I_{PCL_HVB1} & I_{VCL_HVB1} vs TemperatureFigure 11-8, I_{PCL_LVB2} & I_{VCL_LVB2} vs TemperatureFigure 11-9, I_{PCL_LVB3} & I_{VCL_LVB3} vs TemperatureFigure 11-10, V_{FB1} vs TemperatureFigure 11-11, I_{CL_LDO} vs Temperature



9. Functional Block Diagram

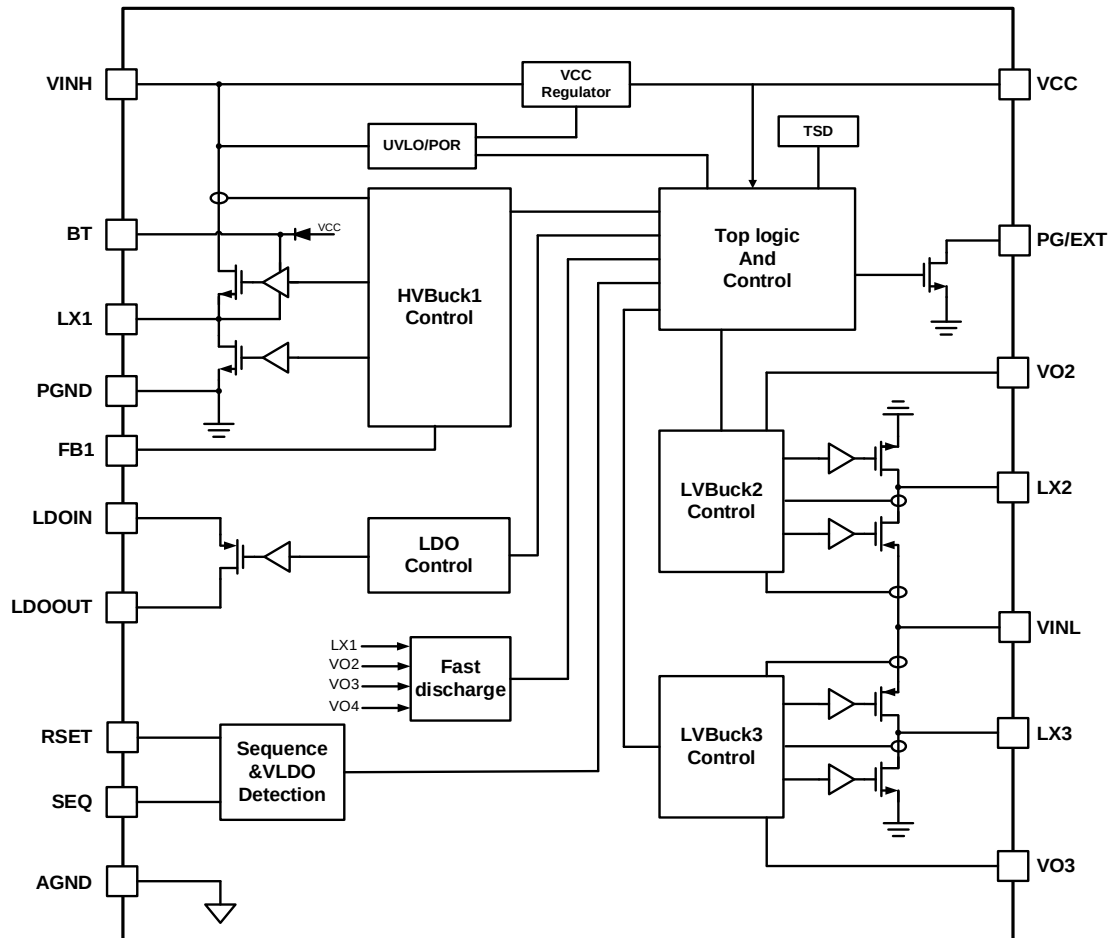


Figure 9-1 Functional Block Diagram



10. Feature Description

The SC6201Q PMIC is designed to optimize the power supply systems of CMOS image sensors. It allows voltage settings and sequence control to be performed with a single IC, reducing mounting area and contributing to the miniaturization of automotive camera modules. The device consists of a high-voltage buck converter for a primary regulator, dual low-voltage buck converters and a LDO regulator for secondary regulators.

10.1 Buck Converters

The three buck converters use a peak current mode control scheme and operate at forced-PWM mode with a fixed frequency of 2.2MHz. The topology benefits lower output voltage ripple, fast load and line transient with a compact solution size.

Meanwhile, the device adopts a spread-spectrum function with phase-shifted to optimize EMI performance. The spread spectrum is implemented by a pseudo-random sequence with a 6% (Typ.) spread of the switching frequency. With this feature, the switching frequency of the device varies from 2MHz to 2.4MHz (Max.) and does not drop into the 1.8MHz AM band limit. The phase shift scheme among the three buck converters avoids the simultaneous switching energy radiation.

All the buck converters integrate power switches. The high-voltage buck converter(HVBuck1) integrates an NMOS for the high-side power switch, while the low-voltage buck converters(LVBuck1&2) adopt PMOS for its high-side power switch. A 100nF bootstrap capacitor is needed between the BT and SW pin to drive the high-side NMOS of HVBuck1. All the low-side power switches adopt NMOS and are driven by the internal VCC.

The HVBuck1 acts as a primary regulator and provides its output voltage VO1 as the input power source of secondary LVBuck and LDO. The HVBuck1 adopts an adjustable output voltage through the FB pin. The VO1 can be set from 2.7V to 5.3V via a resistor divider connected from VO1 to the ground according to secondary LVBuck and LDO input voltage requirements. The LVBucks adopt fixed output voltage.

All the buck converters have a separate output discharge path to the ground, and the discharge patch activates automatically when the corresponding converter is disabled.

10.2 LDO Regulator

The LDO regulator is designed to meet the requirements of sensitive analog circuits by providing low noise with high

PSRR operation. The LDO regulator can provide up to 400mA output current. To decrease the impact of switching noise from the buck converters, the LDO regulator has a dedicated input voltage pin that can be tied to the output of the HVBuck1 independently.

The LDO regulator provides ten kinds of output voltages from 1.8V to 3.5V. The output voltage setting of the LDO regulator is controlled through an RSET pin by setting the appropriate resistor from the RSET pin to the ground. The RSET detection is executed automatically during the device power-up. Changing the output voltage in real-time is not supported. All the buck converters have a separate output discharge path to the ground, and the discharge patch activates automatically when the corresponding converter is disabled.

The LDO regulator has a separate output discharge resistor to the ground, and the discharge resistor activates automatically when the regulator is disabled.

Table 10-1 LDO output voltage VS. RSET pin configuration

RSET	VO4	Resistor of RSET pin		
		MIN	TYP	MAX
0	3.5V	1.07M	1.1M	1.13M
1	3.4V	319K	330K	341K
2	3.2V	164K	169K	174K
3	3.1V	81.6K	84.5K	87.4K
4	3.0V	45.4K	47K	48.6K
5	2.8V	26.1K	27K	27.9K
6	2.7V	14.5K	15K	15.5K
7	1.8V	7.78K	8.06K	8.34K
8	2.9V	Tie to VCC		
9	3.3V	Tie to GND		

10.3 Power Sequence Control

The device supports ten power-on sequences to control the start-up sequence of the two LVbuck converters and one LDO regulator. Like the RSET pin, the power-on sequencing can also be programmed through the SEQ pin by setting the appropriate resistor from the SEQ pin to the ground. There is only simultaneous power-off for all regulators.

The SEQ detection is executed automatically during the device power-up. The output of the HVbuck1 converter acts as the input voltage source of the LVbuck converters and the LDO regulator. For most conditions, the power-on sequence is conducted by the power good of the previous regulator. The LVbuck converters support unused by floating the corresponding LXx and VOx pin (The VINL



floating is not allowed), and the power-on mechanism skips the unused rails automatically.

Table 10-2 Unused Channel Pin Configuration

Unused Channel	Unused Pin Number	Unused Pin Name	Pin Configuration
LVBUCK2	5	VO2	Floating
	6	LX2	Floating
	7	VINL	Connect to a fixed voltage
LVBUCK3	7	VINL	Connect to a fixed voltage
	8	LX3	Floating
	9	VO3	Floating

For the SC6201QB, the EXT pin can link the power-on sequence to an external regulator. The next channel proceeds with the power-on sequence after the EXT output high state 1ms passed. For the SC6201QA, the high state of PG output reflects that the power-on sequence is complete and all the outputs of the active rails are regulated.

Table 10-3 Power-on sequence VS. SEQ pin configuration

SEQ	SEQ Sequence					Resistor of SEQ pin (KΩ)		
						MIN	TYP	MAX
0	CH1	CH4	CH3	CH2	EXT	1070	1100	1130
1	CH1	CH2	CH3	EXT	CH4	319	330	341
2	CH1	CH2	EXT	CH3	CH4	164	169	174
3	CH1	EXT	CH2	CH4	CH3	81.6	84.5	87.4
4	CH1	CH2, CH3, CH4, EXT				45.4	47	48.6
5	CH1, CH2, CH3, CH4, EXT					26.1	27	27.9
6	CH1	CH3	CH2	CH4	EXT	14.5	15	15.5
7	CH1	CH3	CH4	CH2	EXT	7.78	8.06	8.34
8	CH1	EXT	CH2	CH3	CH4	Tie to VCC		
9	CH1	CH2	CH3	CH4	EXT	Tie to GND		

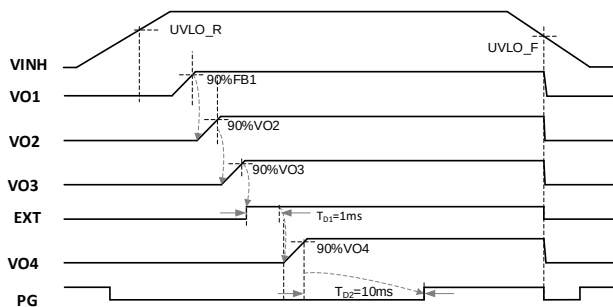


Figure 10-1 Example of SEQ1 power on/off

Note:

1) The PG pin is only available in SC6201QA, and the EXT pin is only available in SC6201QB.

(2) For SC6201QA, a 1ms time interval will substitute the EXT output, which has a +/-5% variation. Below is the SEQ1 example.

For SC6201QA: CH1 → CH2 → CH3 → 1ms → CH4 → 10ms → PG

For SC6201QB: CH1 → CH2 → CH3 → EXT → 1ms → CH4

10.4 Protection Mechanism

The device integrates rich protection mechanisms to prevent damage from abnormal operations or fault conditions.

10.4.1 Under-Voltage-Lock-Out (UVLO)

The VINH pin has an Under-Voltage-Lock-Out (UVLO) circuit. The VINH UVLO keeps all the regulators off until the VINH UVLO threshold is surpassed. The device can only be enabled when VCC and VINH are higher than their UVLO rising thresholds and will shut down when VCC or VINH triggers their UVLO falling thresholds.

10.4.2 Output-Under-Voltage Protection (UVP)

The PMIC integrates an output Under Voltage Protection (UVP) for each rail. Once the under-voltage is detected, the device disables all buck converters and LDO regulator and goes to the latch-off state and the device can only restart with VINH ON/OFF.

10.4.3 Input-Over-Voltage Protection (IOVP)

The VINH/VINL/LDOIN pins have an Input-Over-Voltage-Protection (IOVP). Once the IOVP is detected, the device disables all buck converters and the LDO regulator and is in the latch-off state. The device won't recovery to the power-on process until there is VINH/VINL/LDOIN toggle in the input side.

10.4.4 Output-Over-Voltage Protection (OVP)

The device integrates an output Over-Voltage Protection (OVP) for each rail. For the HVbuck1, when the VO1 is higher than its OVP threshold, the HVbuck1 stops switching immediately and recovers to the normal operation once VO1 falls to the OVP threshold. The other rails are not influenced directly by the VO1 OVP event. For the LVbucks and LDO, once only the OVP is detected for more than 5ms, the device disables all buck converters and LDO regulator. The device can auto-recovery to the power-on process when the corresponding output falls to its OVP threshold for more than 5ms.

**10.4.5 Over-Current Protection (OCP)**

For the three bucks converters, the device provides peak and valley current limits designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device's capabilities. For the LDO regulator, when the load reaches the current limit threshold, the current limit loop will regulate the LDO current. These current limit mechanisms protect the device from being damaged during an overload or output short circuit conditions.

When the device continuously triggers the current limit of more than 10ms, the Over-Current Protection(OCP) activates, and the device disables all buck converters and LDO regulator and goes to the latch-off state. The device can only restart with VINH ON/OFF.

10.4.6 Thermal Shutdown Protection (TSD)

The SC6201Q monitors the junction temperature of the device internally. If the junction temperature exceeds the threshold of 160°C, the device disables all buck converters and LDO regulator and goes to the latch-off state, and the device can only restart with VINH ON/OFF.



Table 10-4 Protection Logics

Channel	Type	Threshold (Typ.)	Deglintch Time (Typ)	Protection	Reset and Threshold (Typ.)
System	VCC_UVLO	$V_{CC} < 3V$	NA	Disable all channels	$V_{CC} > 3.7V$
	VINH_UVLO	$V_{INH} < 3.3V$	32 μ s	Disable all channels	$V_{INH} > 3.8V$
	IOVP ⁽¹⁾	$V_{INH} > 21V$	5ms	Disable all channels then latch-off protection	$V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
	OTP	$T_J > 160^{\circ}C$	5 μ s	Disable all channels then latch-off protection	$T_J < 140^{\circ}C$ and $V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
HVBuck1	UVP	$V_{FB1} < 0.8 \times 50\%$	5 μ s	Disable all channels then latch-off protection	$V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
	OVP	$V_{FB1} > 0.8 \times 110\%$	NA	Disable HVBuck1	$V_{FB1} < 0.8 \times 107\%$
	OCP	$I_{L1_peak} > 3A$	10ms	Cycle-by-cycle current limit If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, $V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
VINL	VINL_UVLO	$V_{INL} < 1.3V$	32 μ s	Disable all channels	$V_{INL} > 2.3V$
	IOVP	$V_{INL} > 5.9V$	5 μ s	Disable all channels	$V_{INL} < 5.4V$
LVBuck2	UVP	$V_{O2} < 1.1 \times 50\%$	5 μ s	Disable all channels then latch-off protection	$V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
	OVP	$V_{O2} > 1.1 \times 120\%$	5ms	Disable all channels	$V_{O2} \leq 1.1V \times 110\%$ with deglitch 5ms
	OCP	$I_{L2_peak} > 2A$	10ms	Cycle-by-cycle current limit If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, $V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
LVBuck3	UVP	$V_{O3} < 1.8 \times 50\%$	5 μ s	Disable all channels then latch-off protection	$V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
	OVP	$V_{O3} > 1.8 \times 120\%$	5ms	Disable all channels	$V_{O2} \leq 1.8V \times 110\%$ with deglitch 5ms
	OCP	$I_{L3_peak} > 1.2A$	10ms	Cycle-by-cycle current limit If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, $V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
LDO	LDOIN_UVLO	$V_{LDOIN} < 1.3V$	NA	Disable all channels	$V_{LDOIN} > 1.5V$
	IOVP	$V_{LDOIN} > 5.9V$	5 μ s	Disable all channels	$V_{IN_LDO} \leq 5.4V$ with deglitch 5 μ s
	UVP	$V_{O4} < V_{O4} \text{ setting} \times 40\%$	5 μ s	Disable all channels then latch-off protection	$V_{INH} < 3.3V$, then $V_{INH} > 3.8V$
	OVP	$V_{O4} > V_{O4} \times 125\%$	5ms	Disable all channels	$V_{O4} < V_{O4} \times 110\%$ with deglitch 5ms
	OCP	$I_{OUT_LDO} > 450mA$	10ms	Disable all channels then latch-off protection	$V_{INH} < 3.3V$, then $V_{INH} > 3.8V$

(1) It is optional for VINH_OVP with auto recovery version: the device will disable all chennels when VINH > 21V with 5 μ s deglitch time, and auto recovery all channels output in the corresponding sequence while VINH < 20V with 5ms deglitch time.



11. Application Curves

$V_{INH}=8V$, $V_{O1}=3.6V$, $V_{O2}=1.1V$, $V_{O3}=1.8V$, $V_{O4}=3.3V$, unless otherwise noted

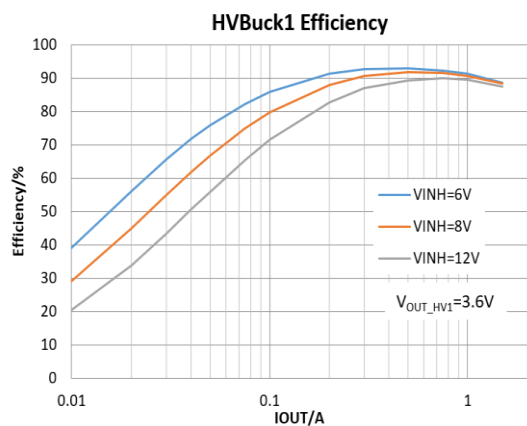


Figure 11-1, HVbuck1 Efficiency

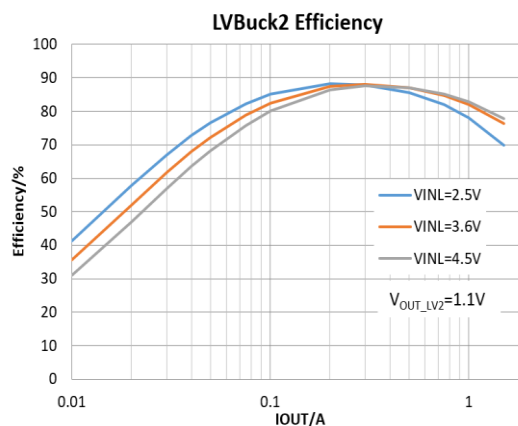


Figure 11-2, LVBuck2 Efficiency

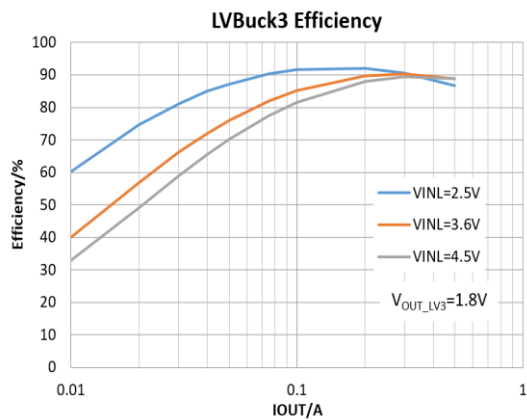


Figure 11-3, LVBuck3 Efficiency

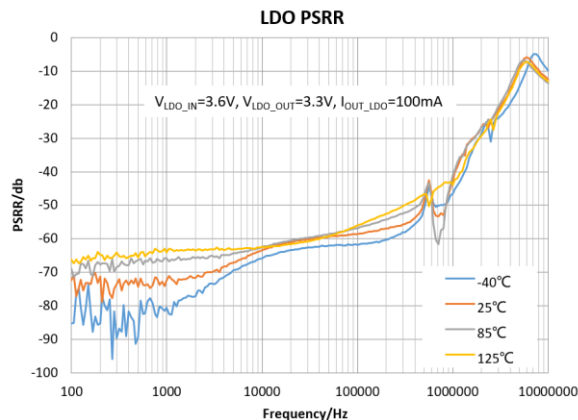


Figure 11-4, LDO PSRR

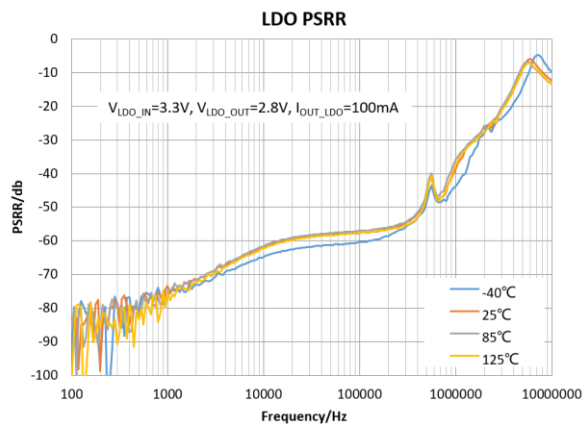


Figure11-5, LDO PSRR

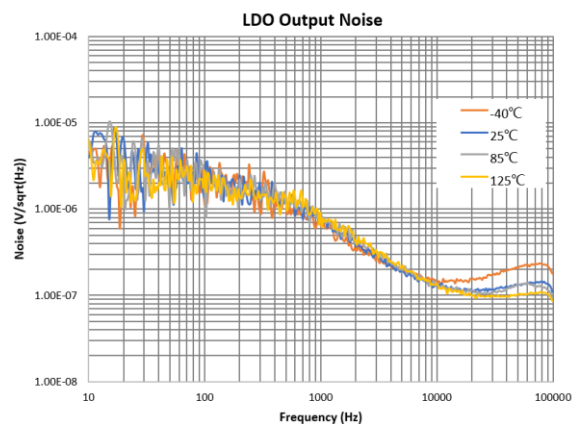


Figure11-6, LDO Output Noise

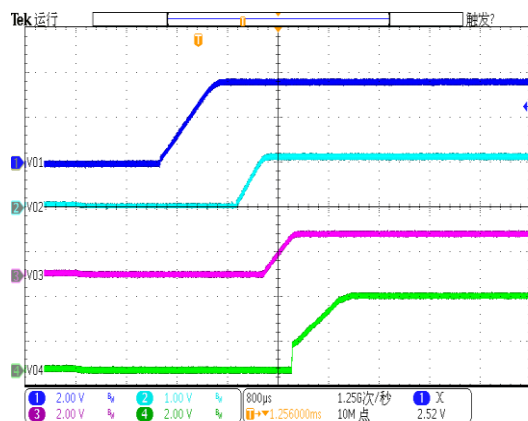


Figure 11-7, SEQ9 Power ON Sequence

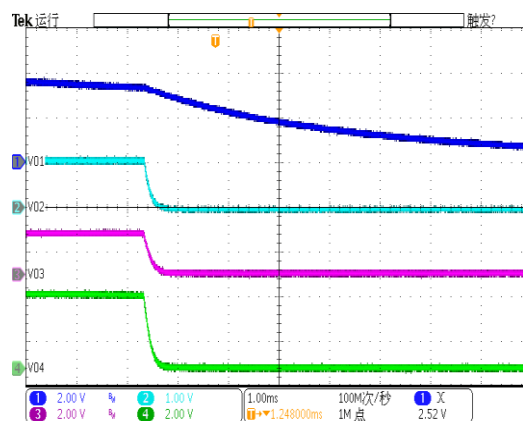


Figure 11-8, SEQ9 Power OFF Sequence

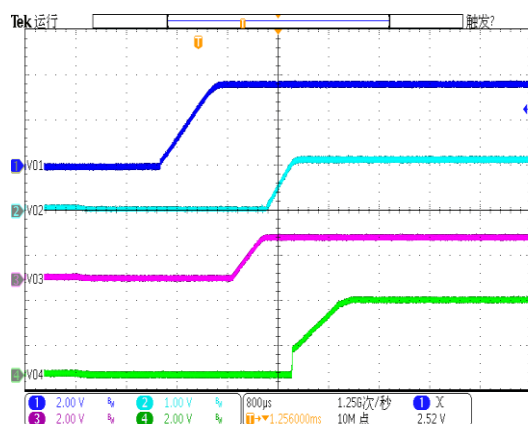


Figure 11-9, SEQ6 Power ON Sequence

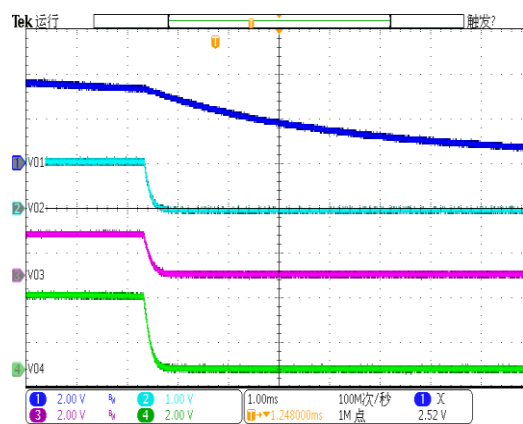


Figure 11-10, SEQ6 Power OFF Sequence

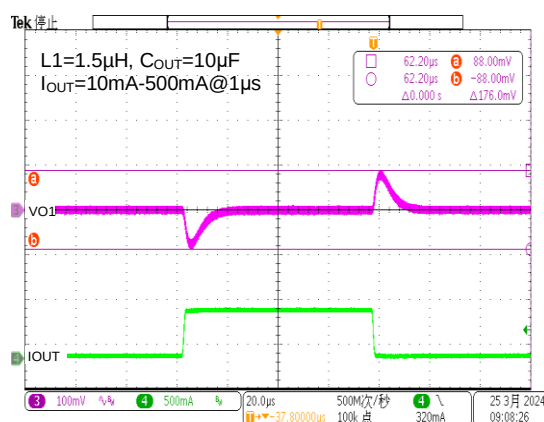


Figure 11-11, HVBUCK1 Load Transient

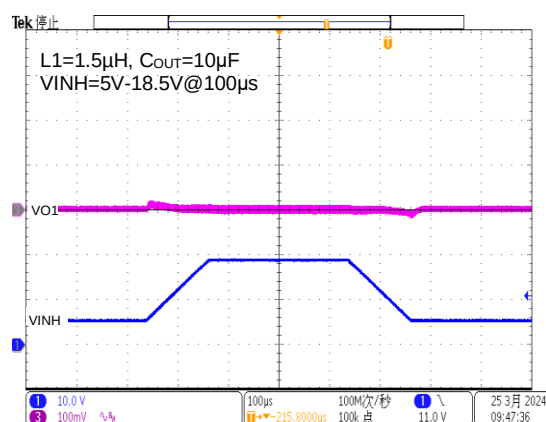


Figure 11-12, HVBUCK1 Line Transient

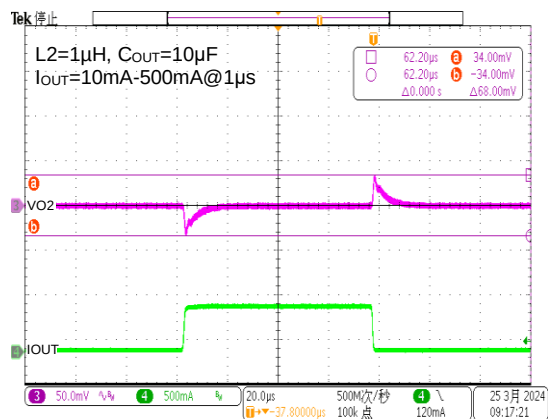


Figure 11-13, LVBuck2 Load Transient

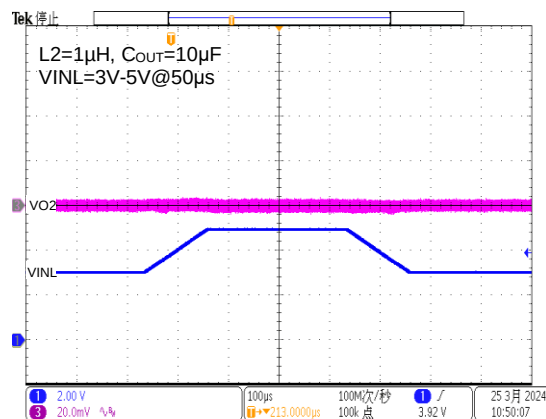


Figure 11-14, LVBuck2 Line Transient

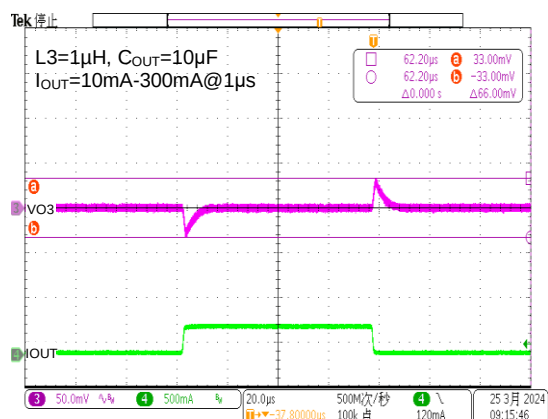


Figure 11-15, LVBuck3 Load Transient

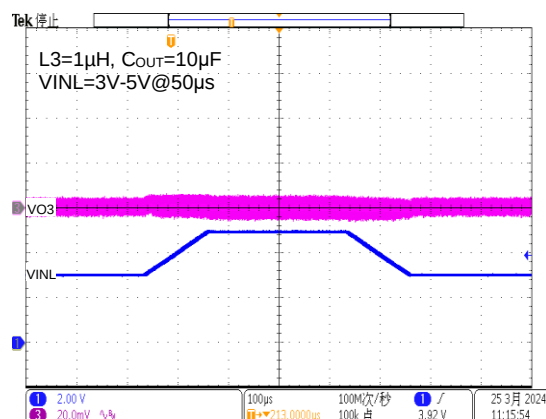


Figure 11-16, LVBuck3 Line Transient

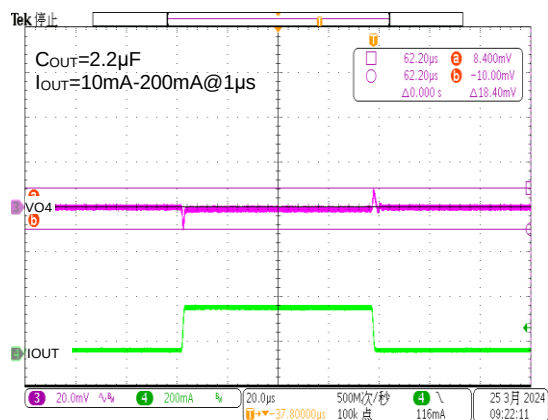


Figure 11-17, LDO Load Transient

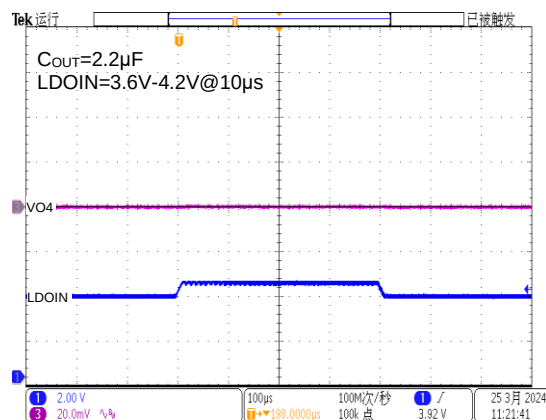


Figure 11-18, LDO Line Transient

12. Layout Guide

12.1 PCB Layout Guide

The PCB layout should be carefully designed for best performance to avoid instability, switching noise interference, and EMI issues. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI.

Here are some guidelines for reference:

- 1) The VINH, VINL and LDOIN pins must each be bypassed to the PGND with a low-ESR ceramic bypass capacitor. Use the typical bypass capacitance of 4.7~10 μ F for the DC-DC converters and 2.2 μ F for the LDO with an X7R dielectric. The optimum capacitor placement is closest to the VINx and VINLDO pins of the device. Minimize the loop area formed by the bypass capacitor connection from the VINx and the thermal pad of the device. Minimize the loop area formed by the bypass capacitor connection from the VINLDO and the AGND pin of the device.
- 2) The FB pin feedback traces must be routed away from any potential noise source to avoid coupling.
- 3) The optimum placement of the VCC and LDOOUT output capacitors is directly at their respective pins. Excessive input and output capacitor distances for regulator pins may cause poor converter performance.
- 4) Minimize the loop area of the bootstrap capacitor from the LX1 to the BT pin.
- 5) Connect the AGND and PGND to a strong ground plane for better noise and thermal performance.
- 6) The thermal pad must be tied to the PCB ground plane with multiple vias.

12.2 Layout example

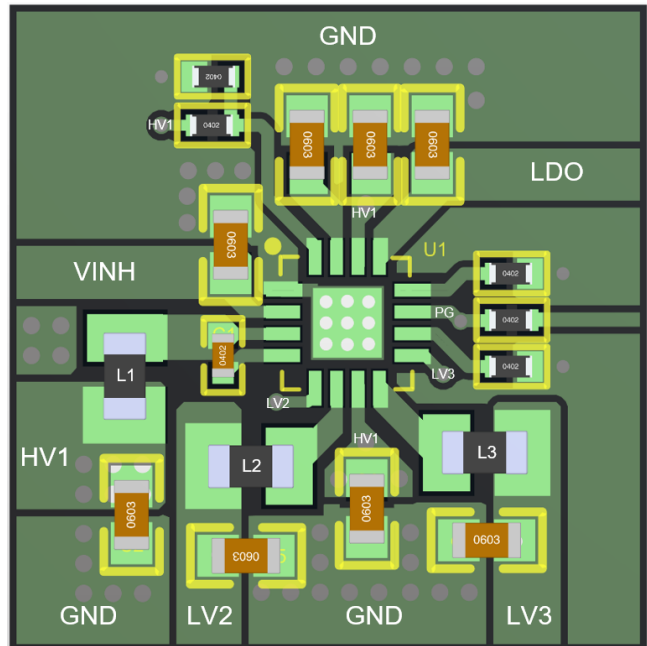
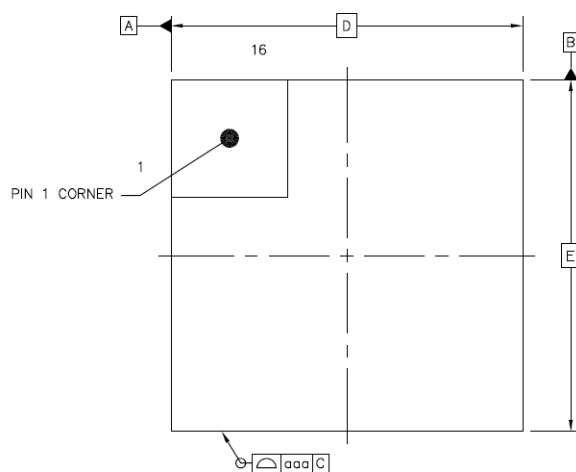


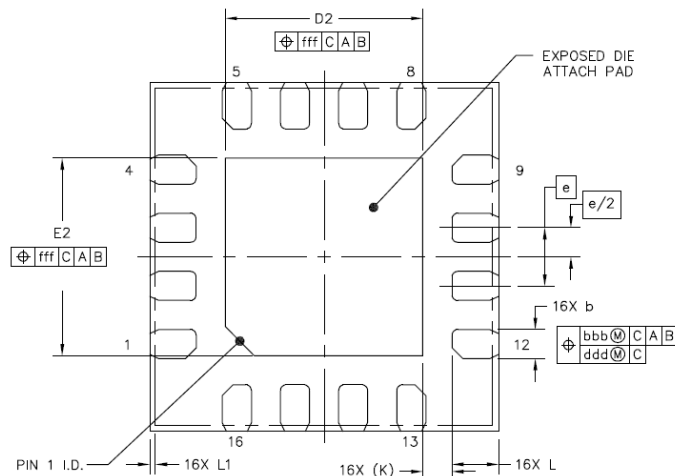
Figure 12-1, PCB Layout Guide

MECHANICAL DATA

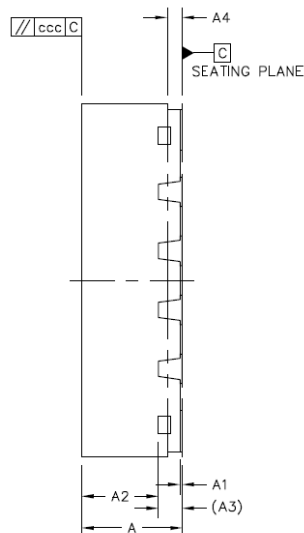
QFN-16 3 x 3 Wettable Flank



TOP VIEW



BOTTOM VIEW



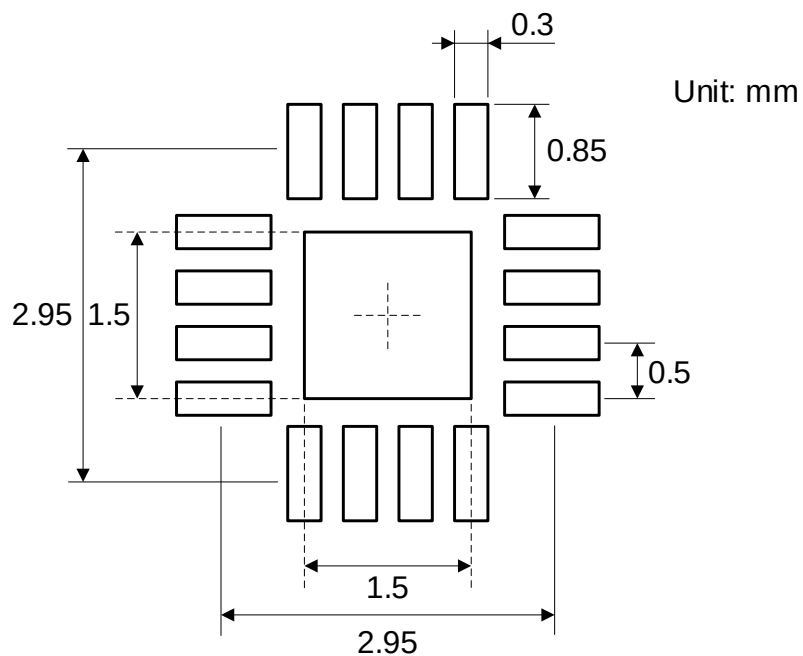
SIDE VIEW

SYMBOL		MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.9
STAND OFF		A1	0	0.05
MOLD THICKNESS		A2	---	---
L/F THICKNESS		A3	0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	0.18
LEAD WIDTH		b	0.2	0.3
BODY SIZE	X	D	3 BSC	
	Y	E	3 BSC	
LEAD PITCH		e	0.5 BSC	
EP SIZE	X	D2	1.6	1.8
	Y	E2	1.6	1.8
LEAD LENGTH		L	0.3	0.5
SIDE WETTABLE WIDTH		L1	0.01	0.09
LEAD TIP TO EXPOSED PAD EDGE		K	0.25 REF	
PACKAGE EDGE TOLERANCE		aaa	0.1	
MOLD FLATNESS		ccc	0.1	
LEAD OFFSET		bbb	0.1	
		ddd	0.05	
EXPOSED PAD OFFSET		fff	0.1	



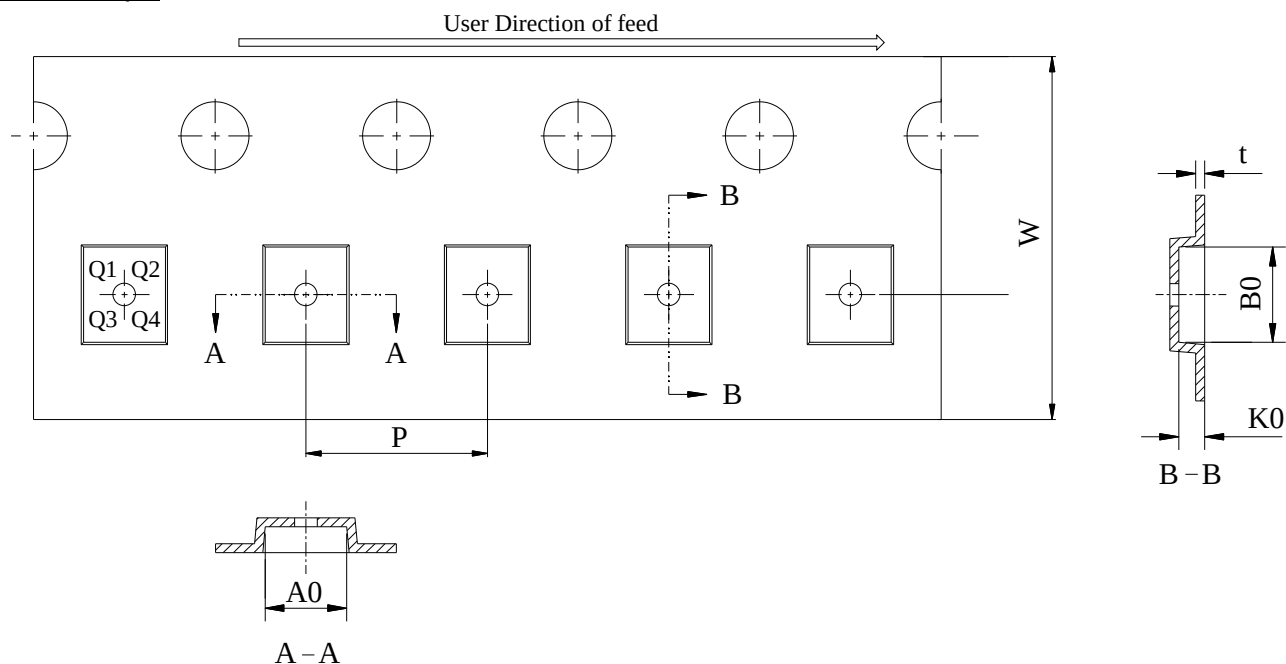
RECOMMENDED FOOTPRINT

QFN-16 3 x 3 Wettable Flank

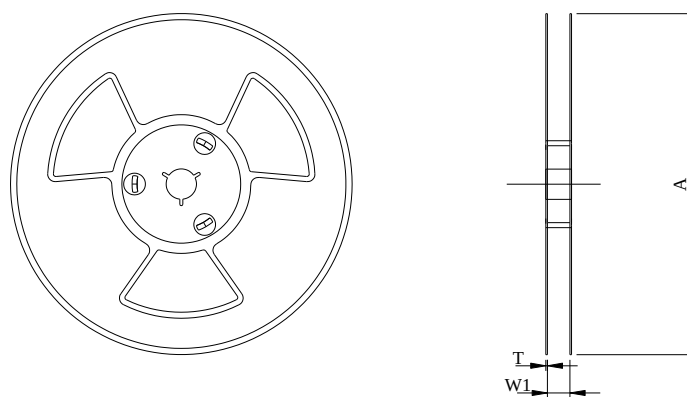




TAPE AND REEL INFORMATION

Carrier Tape

Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	$12.0^{+0.3}_{-0.1}$	8.0 ± 0.1	3.35 ± 0.10	3.35 ± 0.10	1.13 ± 0.10	0.25 ± 0.02	Q1

REEL

Item	A	W1	T
Size (mm)	330.0 ± 1.0	$12.4^{+1.0}_{-0.0}$	$2.6^{+1.0}_{-0.0}$



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