

High Efficiency, Synchronous 32V/5A Buck Converter

1 Descriptions

SC8101 is a synchronous buck converter with a wide input voltage from 4.4V to 32V. The SC8101 regulates the output voltage at a fixed 5.1V or customized voltage by setting the divider resistor. It also provides high accurate output current limit. The converter enters Constant Current (CC) Mode in case the output reaches the setting current limit. The total output power can be programmed by a resistor, which makes it easy for constant power (CP) control.

SC8101 integrates 45mΩ high side NMOS and 30mΩ low side NMOS to achieve high efficiency. Besides, it provides low side gate driver (LSD) to drive external NMOS and works with build-in NMOS.

SC8101 adopts programmable line drop compensation, programmable frequency setting with minimum external components, maximum functions can be achieved for user's different applications.

SC8101 also supports full protections including under voltage protection, over voltage protection, short current protection and auto-restart, over temperature protection.

SC8101 adopts 19 pin QFN 3x3 package.

3 Applications

- Car Charger
- USB Power supplies with PD or Fast charge
- MFP Power Supply
- Industrial applications

2 Features

- Wide input operating voltage from 4.4V to 32V
- Max output capacity 5V/5A with internal MOSFETs
- External low side NMOS gate driver
- Almost 100% duty cycle operation
- Ultra-low quiescent current
- $\pm 2\%$ output voltage reference accuracy
- $\pm 4.5\%$ output current limit accuracy
- Programmable output power limit
- Programmable line drop compensation
- PFM mode
- Fixed-150K switching frequency or adjustable by external resistor
- Hiccup and auto-restart
- Full protection of UVLO, IN/OUT-OVP, OCP, OTP
- Available in QFN-19 3x3 Package

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8101QFKR	19 pin QFN	3mm x 3mm x 0.55mm

5 Typical Application Circuit

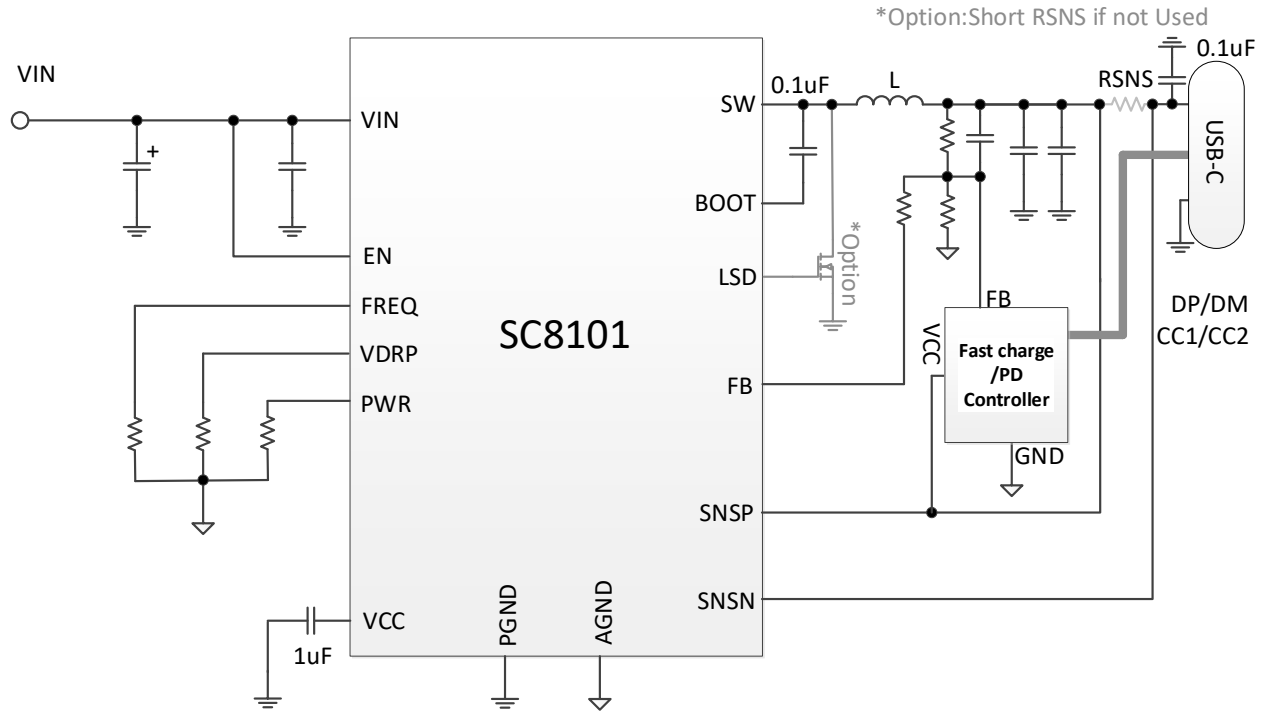


Figure.1 Typical Application Circuit for Fast charge/PD Application

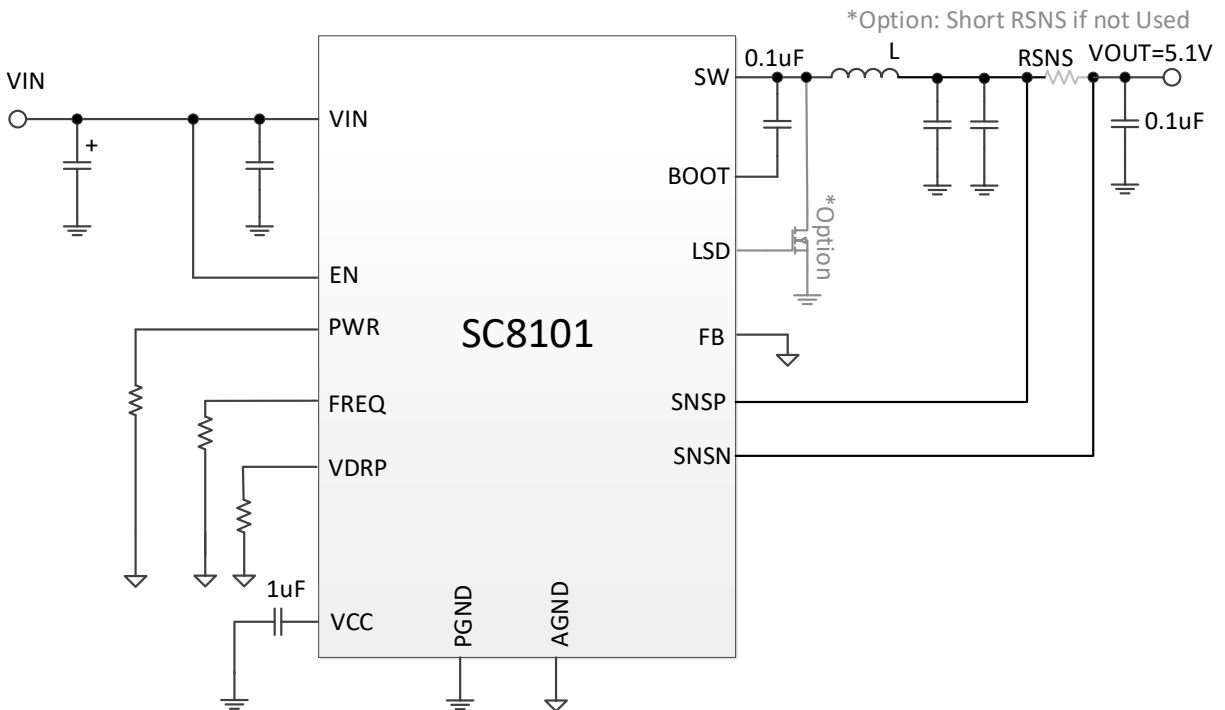
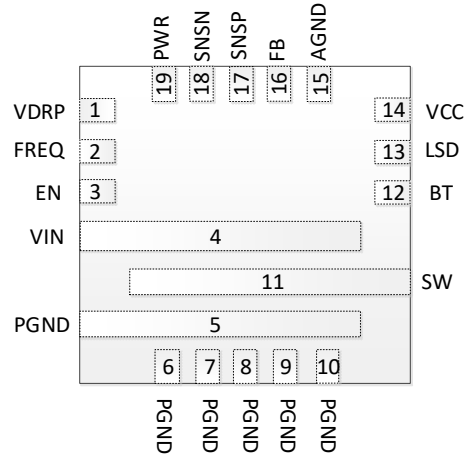


Figure.2 Typical application with 5.1V output

6 Terminal Configuration and Functions



QFN 19 Package Reference (Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VDRP	I	Line drop compensation configuration pin.
2	PREQ	I	Connect a resistor to GND to set switching frequency.
3	EN	I	Enable logic input. Logic high level enables the device and logic low level disables the device.
4	VIN	PWR	Power Input
5~10	PGND	PWR	Power Ground
11	SW	PWR	Switching node.
12	BT	PWR	Connect a capacitor between BT and SW to bootstrap a voltage to provide the bias for high side MOSFET driver.
13	LSD	PWR	External low side power N-MOSFET gate driver.
14	VCC	PWR	Output of internal regulator to provide 5.2V voltage for the bias voltage of internal gate drivers.
15	AGND	I/O	Analog Ground.
16	FB	I	Connect to feedback resistors. If internal voltage is used, connect this pin to GND.
17	SNSP	I	Positive terminal of current sense. Output sense node of the Buck.
18	SNSN	I	Negative end of output current sense amplifier.
19	PWR	I	Output power limit pin. Setting the output power limit by connecting a resistor to AGND

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VIN, EN	-0.3	40	V
	SNSN, SNSP	-0.3	40	V
	SW	-1	40	V
	FB, VCC, FREQ, PWR	-0.3	6.5	V
	BT	-0.3	40	V
Temperature Range	Operating Junction, T _j	-40	150	°C
	Storage temperature range, T _{stg}	-65	150	°C
	Continuous power dissipation (TA=25°C), P _D ⁽³⁾		2.2	W
	Junction to ambient thermal resistance, T _{ΘJA} ⁽³⁾	55		°C/W
	Junction to case (top) thermal resistance, T _{ΘJC} ⁽³⁾	13		°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Measured on JESD51-7, 4-layer PCB.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
	Human body model (HBM) ESD stress voltage for other pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range	4.4		32	V
V _{OUT}	Output voltage range	3		32	V
C _{IN}	Input Capacitance	10			μF
C _{OUT}	Output capacitance	22			μF
L	Inductance	1			μH
f _{SW}	Operating frequency range	80	150		kHz



7.4 Electrical Characteristic

$T_J = 25^{\circ}\text{C}$ and $V_{IN} = 12\text{V}$, $V_{OUT} = 5.1\text{V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{IN}	Operating voltage		4.4		32	V
V _{IN_UVLO}	Under voltage lockout threshold	Rising edge			4.4	V
		Hysteresis		0.2		V
V _{IN_OVP}	Over voltage lockout threshold	Rising edge	32.5	34	35.5	V
		Hysteresis		2		V
I _Q	Quiescent current into VIN	VIN=12V, EN= high, no switching		90	120	μA
I _{SD}	Shutdown current into VIN	VIN=12V, EN = low			2	μA
OUTPUT						
V _{OUT}	Operating voltage		3		32	V
		FB=LOW	5	5.1	5.2	V
V _{FB_REF}	FB reference voltage		1.18	1.2	1.22	V
V _{LDM}	Max Internal line drop compensation	I _{OUT} = 2.4A, RSNS=20mΩ,VDRP=0R	240	300	360	mV
D _{MAX}	Max duty cycle		99%			
VCC AND DRIVER						
V _{CC}	VCC clamp voltage		4.9	5	5.2	V
I _{VCC_LIM}	VCC current limit	VIN=12V, V _{CC} = 5 V	90			mA
R _{LD_E}	External low side driver pull up/down resistance	Pull up		2.3		Ω
		Pull down		0.76		Ω
POWER SWITCH						
R _{DS(on)}	High-side MOSFET on-resistance	VCC=5V		45		mΩ
	Low-side MOSFET on-resistance	VCC=5V		30		mΩ
CURRENT LIMIT						
I _{LIM_Peak}	Internal peak current limit		7.5		11.5	A
V _{LIM_OUT}	Output current limit threshold	RSNS=20mΩ	51.8	54.2	56.6	mV
P _{LIM_OUT}	Output power limit accuracy	VIN=12V, VOUT=5.1V, FSW=150K	-20%		20%	
SWITCHING FREQUENCY						
f _{SW}	Switching frequency		80			kHz
		R _{FREQ} = Floating (default)	125	150	175	kHz
T _{ON_MIN}	Minimum on time of high-side MOFET ⁽¹⁾	-40°C <T _J <+125°C		220	300	ns
SOFT START						
t _{SS}	Internal soft-start time	VOUT from 10% to 90%		6	8	ms
LOGIC CONTROL						
V _{EN_R}	EN rising threshold				1.4	V
V _{EN_F}	EN falling threshold		0.9			V

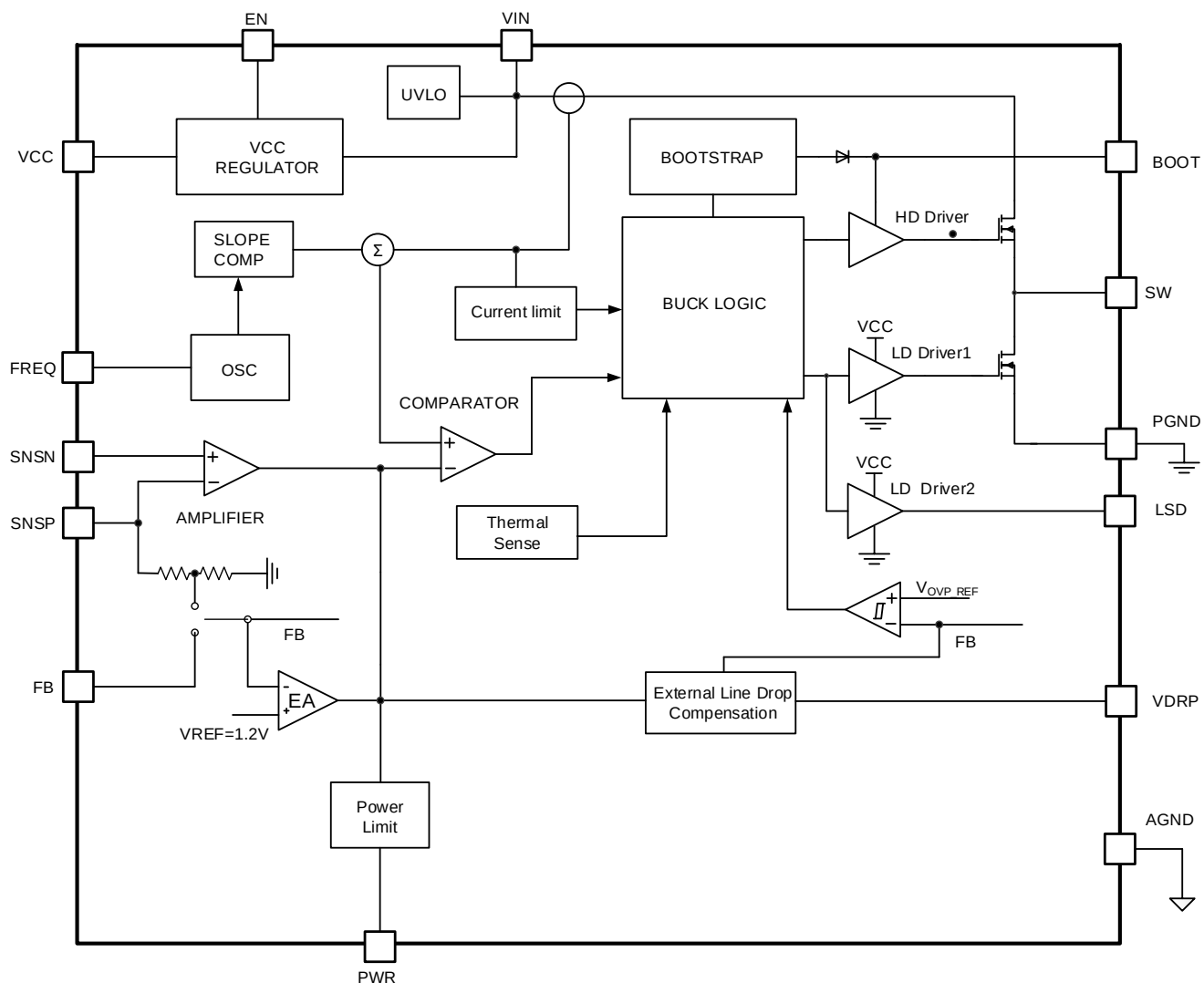


PROTECTION						
OVP_OUT	Output over voltage protection	FB connected to feedback network	107%	109%	111%	
		FB connected to GND	5.55			V
T_ON_Delay	Delay time of fault condition	Trigered by VIN/VCC UVLO/OVP /OTP	120			ms
V_HICP	Hiccup trigger threshold voltage		2	2.42		V
T_HICP_ON	On time of Hiccup Mode	VOUT<2.0V	26			ms
T_HICP_OFF	Off time of Hiccup Mode	VOUT<2.0V	600			ms
THERMAL SHUTDOWN						
T_SD	Thermal shutdown temperature ⁽¹⁾		165			°C
	Thermal shutdown hysteresis ⁽¹⁾		15			°C

(1) Guarantee by design



8 Functional Block Diagram



Function Block Diagram

9 Feature Description

9.1 Startup and Shutdown

The SC8101 integrates an internal circuit that controls the ramp up of output voltage during start-up and prevents the converter from the large inrush current. During the startup phase, the internal soft-start circuit increases the voltage on FB pin gradually so that the output voltage slope follows the FB pin voltage slope until the target voltage is reached.

9.2 Almost 100% Duty Cycle Operation

The device is able to work in almost 100% duty cycle operation mode and is able to exit this mode without any over voltage on the output.

9.3 Enable and Programmable UVLO

SC8101 has an enable control pin EN: pulling it high enables the IC and pulling it low disables the IC. Connect EN to VIN for automatic startup.

EN pin can also be reused for VIN under voltage protection. Connecting the center tape of the divider resistors between VIN and GND programs the VIN under voltage threshold and restart voltage, as shown in Figure. 3

The VIN under voltage threshold can be calculated as the following equation.

$$V_{IN_LOW} = 1.0V \times \left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

When the input voltage is higher than the startup threshold, the SC8101 goes back to normal operation.

$$V_{IN_HIGH} = 1.22V \times \left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

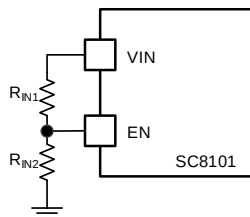


Figure.3 UVLO Threshold Programming

9.4 Output Voltage Setting

SC8101 can be configured for two fixed 5.1V output ports with FB pin connected to GND. The output voltage can also be configured for customized values by using external feedback resistors. The FB status is only detected when IC is powered up, so the FB configuration setting is latched

and cannot be changed until SC8101 is powered down and restart again.

If alternative output voltage is required, the following equation can be used to calculate the divider resistor.

$$V_{OUT} = V_{FB_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

Where:

V_{FB_REF} = Internal reference voltage 1.2V

R_{UP} and R_{DOWN} = Resistor divider at FB connected to VOUT and AGND.

9.5 Cable Drop Compensation

SC8101 is capable of compensating the output voltage drop, caused by a long trace, to keep a fairly constant load-side voltage. The cable drop compensation is adjusted by the internal current source, which sinks a certain current from FB to GND. The current slop can be adjusted by VDRP pin with a resistor connected to GND (3.8uA, max).

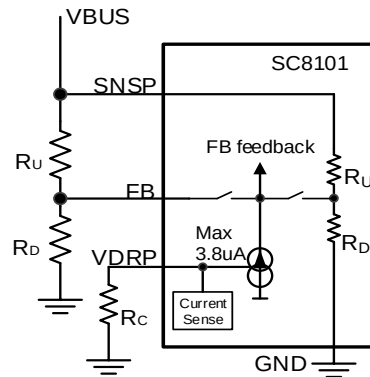


Figure.4 Cable Drop Compensation Diagram

The compensation voltage is calculated by the following formulas:

$$I_{SOURCE} = \frac{5.55}{R_C} \times V_{SENSE} - 0.3 \times 10^{-6}$$

$$V_{SENSE} = I_{OUT} \times R_{SENSE}$$

$$V_{DCOMP} = I_{SOURCE} \times R_U$$

Where:

I_{SOURCE} is the internal current source which limited in 0~3.8uA.

R_U is the upper resistor of FB divider.

R_C =VDRP setting resistor.

V_{SENSE} is the output current sampling voltage (54mV, max).

I_{OUT} = output voltage

R_{SENSE} = output current sampling resistor

The maximum compensation voltage: $\Delta V_{DCOMP} = 3.8 \times R_U$. For FB pin connected to GND application, R_U is 78.5 K Ω and the maximum compensation voltage $\Delta V_{OUT-MAX}$ is about 300mV.

Here are 2 typical applications with different R_C :

Example 1, FB pin connected to GND application:

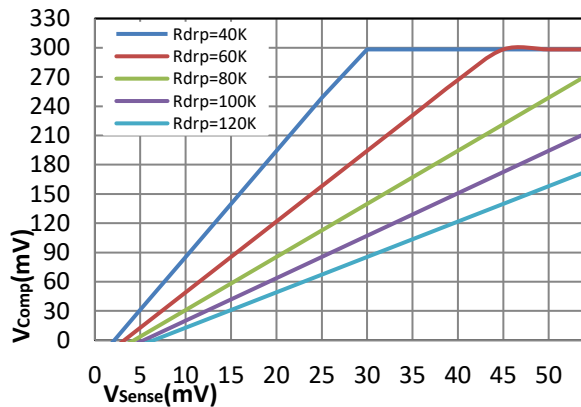


Figure.5 5 V_{COMP} vs. V_{SENSE} ($R_U=78.5$ K Ω)

Example 2, FB pin is set with 100K upper resistor:

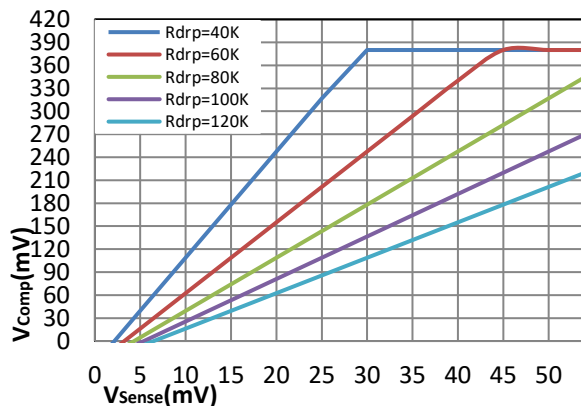


Figure.6 5 V_{COMP} vs. V_{SENSE} ($R_U=100$ K Ω)

Using proper R_C/R_U user can set the compensation slop and the maximum amplitude. The cable drop compensation amplitude increases linearly with the load current increasing.

The cable drop compensation is disabled when the VDRP pin is floating.

9.6 Switching Frequency

The switching frequency can be set by a resistor between FREQ pin and GND. The following equation shows the

relationship between operating frequency and resistor value.

$$f_s(\text{kHz}) = \frac{17300}{R_{FREQ}(\text{k}\Omega)}$$

For minimal external components and simplifying the design process, the SC8101 also supports 150-kHz operating frequency if FREQ pin is floating. The minimum on-time of the high-side NMOS is 220ns(typ.) If the frequency and duty cycle need a lower on-time, SC8101 will skip some switching cycles and makes sure the output voltage is regulated. But this over minimum on-time operating always increases the output ripple, therefore, setting a right frequency to avoid the skip mode if possible.

9.7 Output Power Limit

The power limit function is only available when the on-time of the high-side NMOS is more than 0.6 μ s. The output power limit can be set by connecting a resistor between PWR pin and GND. The following table shows the relationship between output power limit and the resistor.

$$P_{LIM}(W) = \frac{1035}{R_{PWR}(\text{k}\Omega)} - 0.575 \quad (T_{on} > 0.6\mu\text{s})$$

The output power limit function helps customer to control the total power delivery of the system. Especially in the application of fast charge, the total power delivery should be same even though the VOUT is different. Due to this function, the output current limit can be different according to different output voltage. The SC8101 supports 24W application with 30W(typ.) power limit if PWR pin is floating. The power limit function also can be disabled if the PWR pin is connected to GND.

9.8 Constant Voltage / Constant Current Mode

SC8101 operates either in CV (constant voltage) mode or CC (constant current) mode and automatically changes from CV to CC smoothly. In CV mode, it regulates the output voltage. As long as output current limit threshold is reached, SC8101 enters CC mode and the output voltage drops while output current is clamped at the setting values.

SC8101 monitors the output current limit. When the output current reaches setting current limit, it enters CC mode. The current limit can be set by the current sensing resistors by the following equation.

$$I_{LIM_OUT} = \frac{54\text{mV}}{R_{SNS}}$$

Where R_{SNS} is the value of current sense resistor.



Usually, if current limit is set at 2.7A by default with an external sensing resistor $RSNS=20m\Omega$. When the voltage drop across the sensing resistor gets higher than 54mV, the driver is turned off. In this way, the output current is limited. Table.1 shows some typical $RSNS$ value and output current limit relationship.

Table. 2 Relationship between $RSNS$ and current limit

$RSNS$ (m Ω)	Output Current Limit (A)
16	3.38
20	2.70
24	2.25
30	1.80

9.9 Under-Voltage Lockout (UVLO)

The UVLO function protects the chip from operating at insufficient power supply. The chip disables all the function if input voltage is lower than 4.0V and it doesn't start up again until input voltage is higher than 4.6V.

9.10 Input / Output Over-Voltage Protection

SC8101 adopts an output over-voltage protection (OVP) with $\pm 2\%$ accuracy. When FB pin is connected to GND, in case the output voltage is higher than 5.55V, the buck converter stops switching until OVP status is removed. When FB is connected with two divider resistors, OVP is triggered in case the FB voltage is higher than 110% normal reference voltage.

SC8101 integrates an input over-voltage protection (input OVP) besides the output OVP. If input voltage exceeds 34V, the switching is stopped to protect system from input surge voltage. The response time is less than 1 μ s. The system resumes switching after V_{IN} falls below 32V with 100ms delay.

9.11 Short Circuit Protection and Hiccup

The SC8101 integrates a hiccup mode which is triggered once the output voltage is lower than 2V. In hiccup mode, SC8101 periodically stops switching for 550ms and then tries to restart with output current increasing to current limit for 25ms. This protection mode is especially useful when the output is dead-shortened to ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit

condition is removed, SC8101 exits hiccup mode and goes back to normal operation.

9.12 Over Temperature Protection

The over temperature protection (OTP) prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165 °C, SC8101 is shut down. When the temperature drops below threshold (typically 150°C), the chip is enabled again.

10 Application Information

10.1 Input and Output Capacitor Selection

The input current of the Buck converter is discontinuously and the input capacitor should be carefully selected. At least 30μF input capacitor is required for small input voltage ripple and stability. The input capacitor can be electrolytic, tantalum or ceramic. MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60 μF X5R or X7R capacitors with higher voltage rating than operating voltage with margin is recommended. A 10μF ceramic capacitor must be placed close to IC's VIN pin, to improve the high frequency performance (stability and EMI radiation).

To avoid input hot swapping spike, a low ESR aluminum electrolytic or solid capacitor is recommend to suppress the input voltage spike. Aluminum solid electrolytic capacitor is highly recommended to improve efficiency.

The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The output capacitor is recommended to be larger than 80μF. The output voltage ripple is estimated as the following equation

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

If electrolytic or tantalum capacitor is used, low ESR capacitor is recommended and 10μF ceramic capacitor is needed in parallel.

10.2 Inductor Selection

For better power limit regulation, a larger inductance is recommended to make sure the system operates in CCM mode at the max load, especially the max VIN and the max VOUT. The min inductance is calculated as follows:

$$L \geq \frac{V_{OUT}}{r \times I_{OUT} \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Where r is the current ripple ratio, and it is recommended to select its value considering the overall efficiency, inductor size, and the peak current limit.

r is limited by the peak current limit at the max VIN as follows:

$$r < \left(\frac{I_{L_{Peak}}}{I_{OUT}} - 1 \right) \times 2$$

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so smaller DCR is recommended for the first selection. If the current is relatively small, higher DCR inductor with larger inductance can be selected. The inductor saturation current I_{SAT} should be higher than input / output current with sufficient margin.

10.3 PCB Layout Guide

For best performance, PCB layout should be carefully designed to avoid instability, noise and EMI. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI. For a BUCK converter, the critical loop area is showed in figure 7:

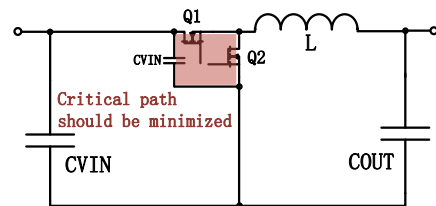


Figure.7 Minimizing the critical path helps mitigate EMI

Here show some guidelines for reference:

- 1) The input capacitor (CVIN, MLCC) should be close to IC to minimize the critical path area and make sure the current flows through the CVIN first, then VIN pin.
- 2) The VCC capacitor (CVCC, 1uF, MLCC) should be close to VCC pin and connected to PGND pin directly, to avoid noise and instability.
- 3) The power limit resistor and line drop compensation resistor (R-PWR) is sensitive, it should be close to the corresponding pin (keep away from switching node) and connected to AGND pin directly.
- 4) The FB feedback resistor should be close to FB pin and be away from switching node. A feed-forward capacitor is highly recommended to prevent instability.
- 5) The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing)

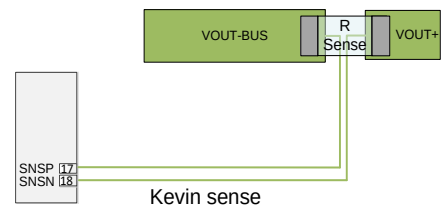


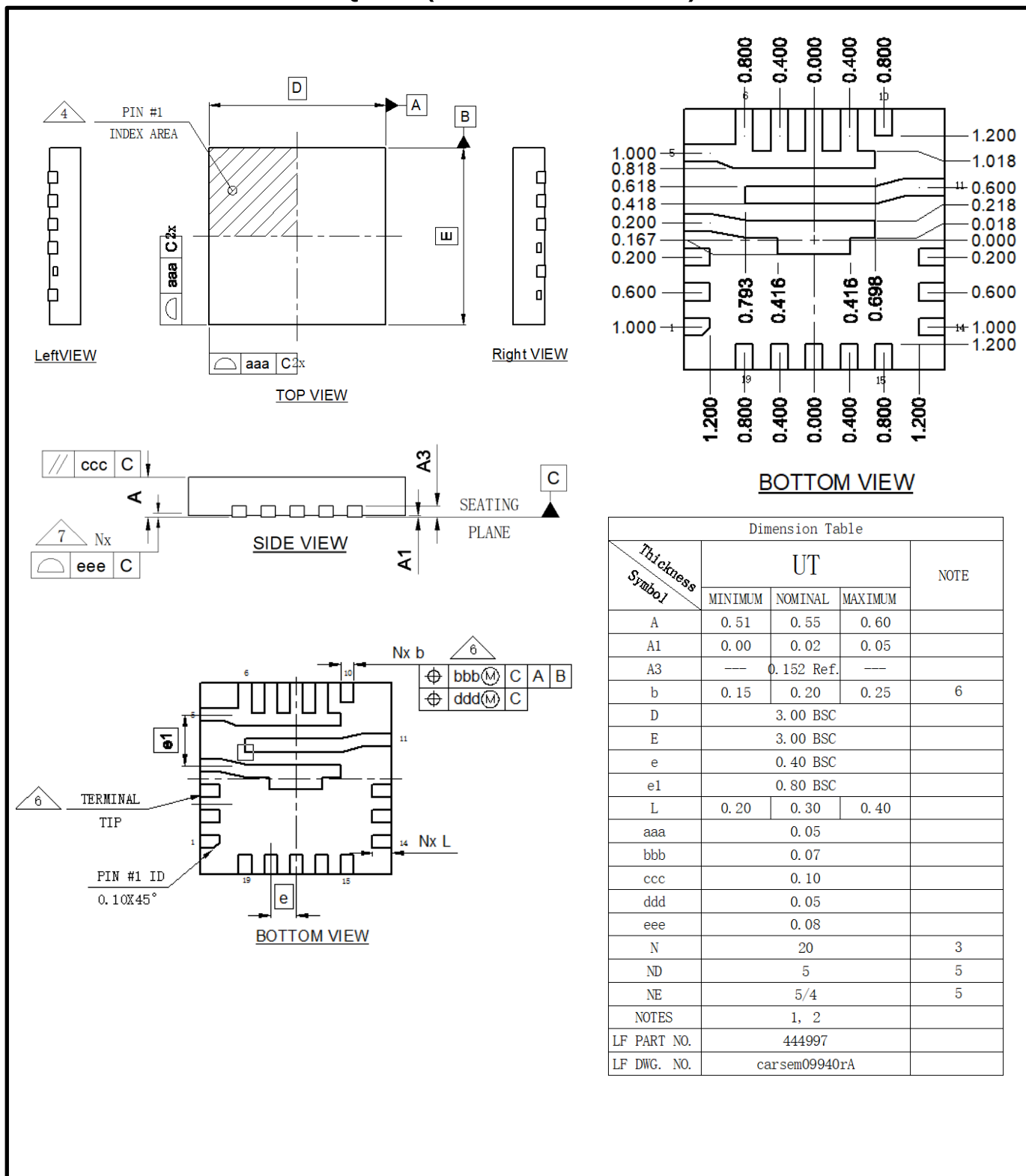
Figure.8 Current sense layout example



- 6) The RC snubber is connected between SW and PGND to absorb switching noise. The snubber should be close to SW and GND pin and minimize the loop area to optimize EMI.
- 7) The boot capacitor should be close to SW and BOOT pin

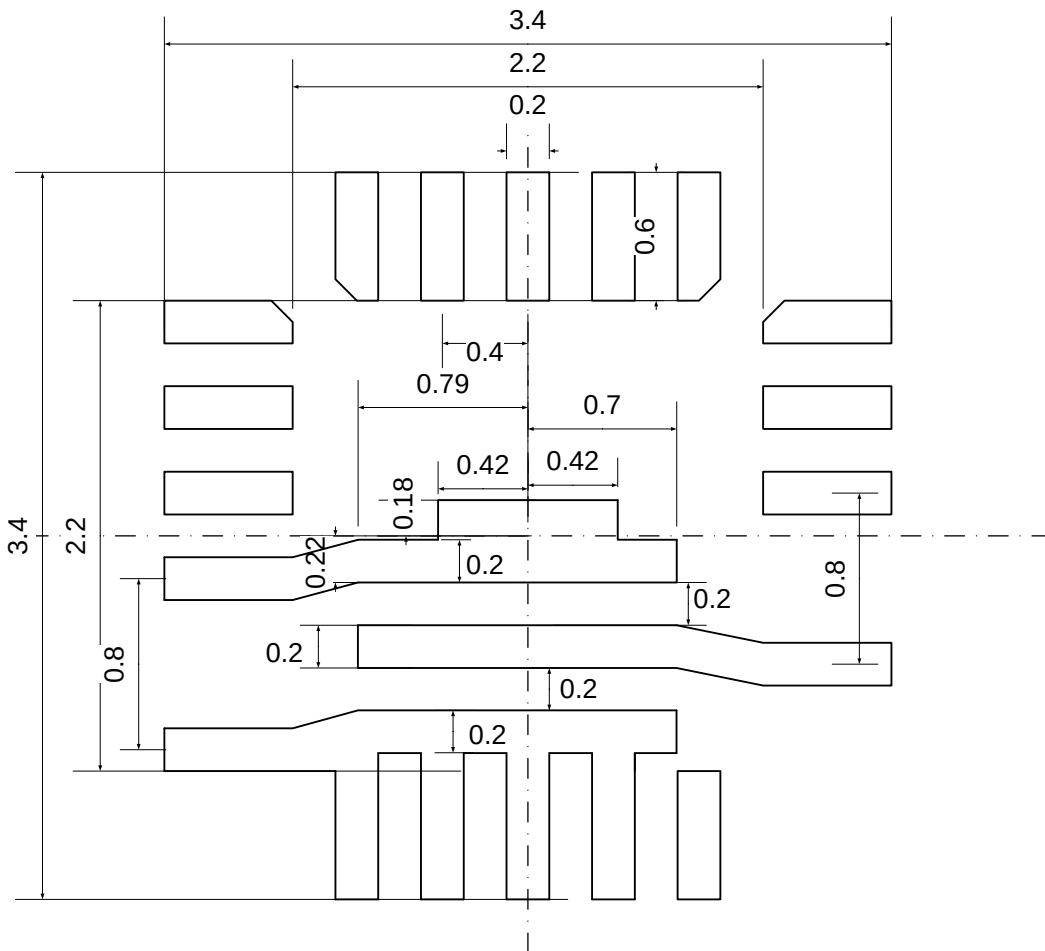
Packaging Information

QFN19 (3mm x 3mm x 0.55mm)



Recommend Footprint

QFN19 (3mm x 3mm x 0.55mm)



NOTES:

- A. All linear dimensions are in millimeters
- B. Publication IPC-7351 is recommended for alternate designs
- C. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad