

High-Efficiency Dual Buck Converters with Load Switch for LPDDR5/5X and LPDDR4X Power Solution

1 Descriptions

The SC6301 is a total power solution PMIC for LPDDR5, LPDDR5X, and LPDDR4X memory. It can meet the requirement of the output voltage and power sequence from the JEDEC standard and support flexible power state operation S3/S5 with EN and VDDQEN control.

The device integrates two synchronous, high-frequency buck converters (VDD2 and VDDQ). The converters adopt a constant on-time control mode with internal ramp compensation which features excellent load transient performance and supports very low ESR output capacitors such as ceramic capacitors. It also provides high efficiency with internal low $R_{DS(on)}$ power MOSFETs. The VDD2 can support up to 14A peak output current, and the VDDQ can support up to 3A output current.

The device also integrates an 18m Ω load switch for VDD1. The VDD1 supports up to 3A output current with 1.8V input voltage.

The SC6301 integrates rich protections to extend the operating range without damaging itself or the system load. The protection features include UVLO, OVP, OCP, UVP, and thermal shutdown protection.

The SC6301 adopts a 3mmx3mm FCQFN3X3 package.

2 Features

- 3.1V to 28V Input Voltage Range for VDD2
 - Low Quiescent Current
 - LPDDR5 Memory Power Solution Compatible with LPDDR5X and LPDDR4X
 - 10A Continuous Outout for VDD2
 - 14A Peak Output Current for VDD2
 - 3A Peak Output Current for VDD1
 - 3A Continuous Output Current for VDDQ
 - Constant on-time Control for Fast Transient Response
 - Stable with Low ESR Capacitors
 - 650kHz Switching Frequency for VDD2
 - Low $R_{DS(ON)}$ Internal Power MOSFETs
 - High Output Accuracy
 - Power Sequencing Control
 - Internal Soft Start
 - Power Good Indication
 - Output Discharge Function
 - UVLO, OCP, OVP, UVP, and Thermal Shutdown
 - Non-Latch for UVLO and Thermal Shutdown
- Package: 3mmx3mm, FCQFN3X3

3 Applications

- Notebook, PC Computers
- Tablets, Portable Instrument
- Network Systems
- Distributed power systems

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC6301DFHR	FCQFN3X3	3mm x 3mm

5 Revision History

Revision	Date	Page(s) changed	Changes Description
v0.4.0	2024/9/24	16, 17, 18	1, Change the high in MECHANICAL DATA (Side View) from 0.9 to 0.75 2, Increase TAPE AND REEL INFORMATION
V0.4.1	2025/1/20	1	1, Increase continuous current for VDD2

6 Typical Application Circuit

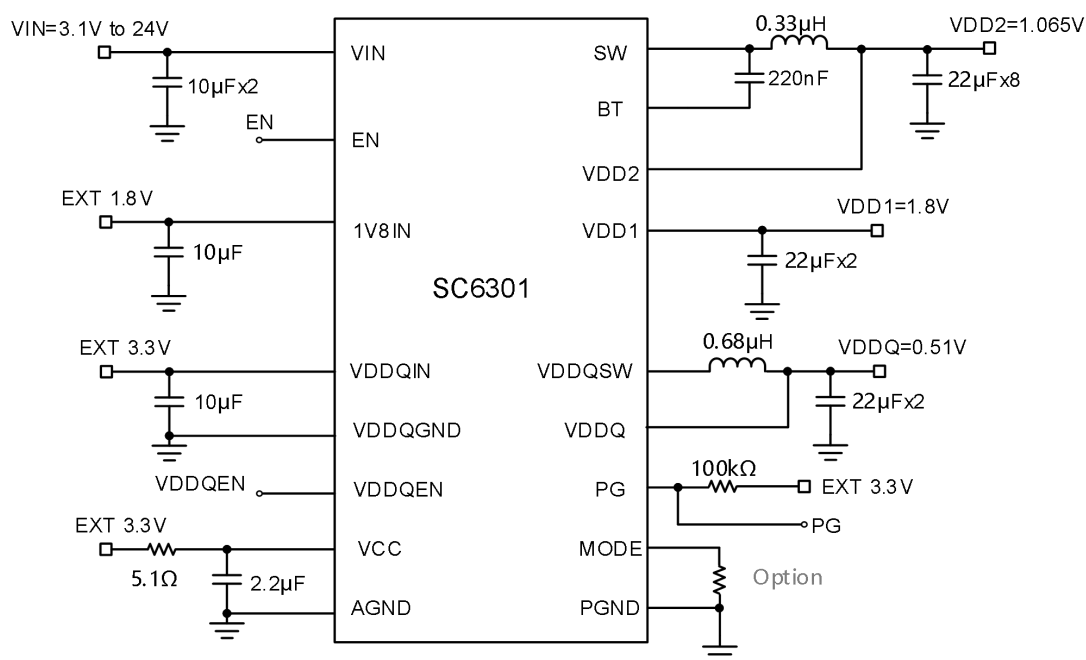
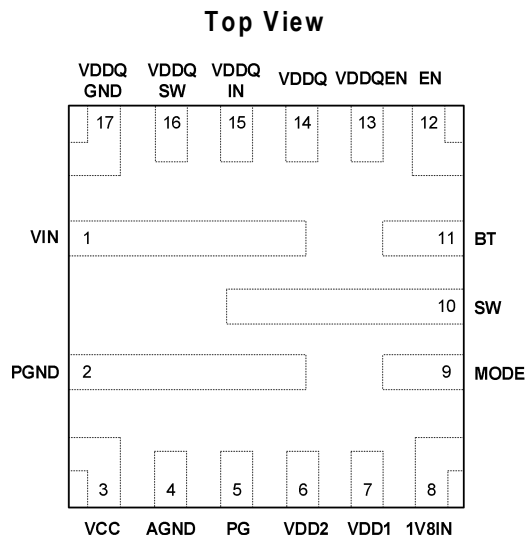


Figure 1 Typical Application

7 Terminal Configuration and Functions



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VIN	PWR	The power input node of the VDD2 buck converter.
2	PGND	PWR	Power ground.
3	VCC	PWR	External 3.3V power input for the control circuit.
4	AGND	PWR	Analog ground.
5	PG	O	Power good output with an open drain. Connect to a voltage source with an external pull-up resistor. PG goes high when the output range is within the target value.
6	VDD2	I	VDD2 output voltage sense for control loop, connect to the VDD2 output node.
7	VDD1	PWR	Load switch output for VDD1.
8	1V8IN	PWR	External 1.8V power input for VDD1.
9	MODE	I	MODE pin is to program the output voltage for the LPDDR5, LPDDR5X, and LPDDR4X applications.
10	SW	PWR	VDD2 switching node, connect to the inductor and bootstrap capacitor.
11	BT	I	Connect a capacitor between the BT pin and SW pin to provide the boosted bias voltage for the high side gate driver of VDD2.
12	EN	I	Enable logic input pin. Logic high level enables the device and logic low level disables the device. EN is internally pulled low.
13	VDDQEN	I	VDDQ enables logic input pin. When EN=1 and VDDQEN=1, the VDDQ can be enabled with a specific timing sequence; when EN=0 or VDDQEN=0, the VDDQ will be disabled. VDDQEN is internally pulled low.
14	VDDQ	I	VDDQ output voltage sense for control loop, connect to the VDDQ output node.
15	VDDQIN	PWR	The power input node of the VDDQ buck converter.
16	VDDQSW	PWR	VDDQ switching node, connect to the inductor and bootstrap capacitor.
17	VDDQGND	PWR	VDDQ Power ground.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾



PARAMETER	DEFINITION	MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VIN	-0.3	28	V
	SW	-0.3	28	V
	SW (10ns transient)	-4	30	V
	BT to SW	-0.3	4.5	V
	VDDQIN	-0.3	5.5	V
	VDDQSW	-0.3	5.5	V
	VDDQSW (10ns transient)	-4	7	V
	PG, VDD2, VDD1, MODE, EN, VDDQEN, VDDQ	-0.3	6	V
	VCC, 1V8IN	-0.3	4.5	V
Temperature Range	Operating Junction, T _J	-40	150	°C
	Storage temperature range, T _{slg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
VIN	Input voltage range for VDD2 buck converter	3.1		24	V
VCC	Input voltage range for control logic circuit	3.1		3.5	V
1V8IN	Input voltage range for VDD1	1.7		1.9	V
VDDQIN	Input voltage range for VDDQIN	1.7		3.5	V
T _J	Operating junction temperature	-40		125	°C



8.5 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		SOIC8EP	UNIT
θ_{JA}	Junction to ambient thermal resistance	53	°C/W
θ_{JC}	Junction to case resistance	15	°C/W

(1) Measured on JESD51-7, 4-layer PCB.



8.6 Electrical Characteristics

VIN = 12V, VCC = 3.3V, EN = VDDQEN = 2V, MODE = Float, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VCC_ON}	VCC supply current with all rail active	EN = VDDQEN = 2V, 1V8IN = VDDQIN = 1.8V, No load		242		μA
I _{VCC_1}	VCC supply current with VDD2 active	EN=2V, No 1V8IN and VDDQIN, No load		170		μA
I _{VCC_2}	VCC supply current with VDD2 and VDDQ both active	EN = VDDQEN = 2V, VDDQIN = 1.8V, No 1V8IN, No load		190		μA
I _{VCC_3}	VCC supply current with VDD1 and VDD2 both active	EN = 2V, 1V8IN = 1.8V, No VDDQIN, No load		220		μA
I _{VCC_SD}	VCC supply current with EN shutdown	EN = 0V			1.5	μA
VDD2 BUCK CONVERTER						
R _{DSOH_VDD2}	High-side switch on resistance			20		mΩ
R _{DSOL_VDD2}	Low-side switch on resistance			9		mΩ
SW _{LK_VDD2}	Switch Leakage	EN = 0V, SW = 0V			1	μA
I _{LMT_LS_VDD2}	Low-side valley current limit		14	15.5	18	A
f _{sw_VDD2}	Switching frequency			650		kHz
t _{ON(MIN)_VDD2}	Minimum on time			70		ns
t _{OFF(MIN)_VDD2}	Minimum off time			180		ns
VDD2 PROTECTION						
V _{OVP_VDD2}	OVP threshold voltage		125	130	135	%V _{REF}
V _{UVP-1_VDD2}	UVP-1 threshold voltage		70	75	80	%V _{REF}
V _{UVP-2_VDD2}	UVP-2 threshold voltage		45	50	55	%V _{REF}
VDD1 LOAD SWITCH						
R _{DSOH_VDD1}	Load switch on resistance			18		mΩ
I _{LMT_VDD1Fast}	Fast current limit			7		A
I _{LMT_VDD1Slow}	Slow current limit		3	4.5	5.5	A
VDD1 PROTECTION						
V _{UVP_VDD1}	UVP threshold voltage		60	65	70	%V _{1V8IN}
V _{OVP_VDD1}	OVP threshold voltage		2.9	3.1	3.3	V
VDDQ BUCK CONVERTER						
R _{DSOH_VDDQ}	High-side switch on resistance	VDDQIN = 3.3V, VCC = 3.3V		48		mΩ
R _{DSOL_VDDQ}	Low-side switch on resistance	VDDQIN = 3.3V, VCC = 3.3V		26		mΩ
SW _{LK_VDDQ}	Switch Leakage	EN = 0V, VDDQSW = 0V			1	μA
I _{LMT_VDDQ}	Low-side valley current limit		3	3.5	4	A
f _{sw_VDDQ}	Switching frequency			600		kHz
t _{ON(MIN)_VDDQ}	Minimum on time			70		ns



t _{OFF(MIN)_VDDQ}	Minimum off time		180	ns		
VDDQ PROTECTION						
V _{OVP_VDDQ}	OVP threshold voltage		0.75	0.8	0.85	V
V _{UVP_VDDQ}	UVP threshold voltage		45	50	55	%V _{REF}
VDD2/VDDQ REFERENCE AND MODE						
V _{REF_VDD2}	VDD2 Reference Voltage	RMODE=Float or 150kΩ	1.055	1.065	1.075	V
		RMODE=100kΩ	1.1			V
		RMODE=0Ω	0.9			V
V _{REF_VDDQ}	VDDQ Reference Voltage	RMODE=Float	0.505	0.51	0.515	V
		RMODE=100kΩ	0.607			V
		RMODE=0Ω or 150kΩ	0.307			V
VDD1/VDD2/VDDQ TIMING PARAMETERS						
t _{DLY_VDD1}	EN on to VDD1 start-up delay time		400			μs
t _{SS_VDD1}	VDD1 soft-start time	VDD1 = 1.8V (10% to 90%)	350			μs
t _{SS_ON_VDD2}	VDD2 soft-start time	VIN = 12V, VDD2 = 1.065V (10% to 90%)	1.5			ms
t _{SS_ON_VDDQ}	VDDQ soft-start time	VDDQIN = 3.3V, VDDQ = 0.51V (10% to 90%)	900			μs
t _{OFF_DLY_VDD1}	VDD2 off to VDD1 off delay time		5			ms
t _{SS_OFF_VDD2}	VDD2 soft-shutdown time	VIN = 12V, MODE = Float, VDD2 = 1.065V (90% to 10%)	2			ms
EN AND VDDQEN LOGIC THRESHOLD						
V _{TH_EN} / V _{TH_VDDQEN}	EN/VDDQEN rising threshold		1.1	1.2	1.3	V
V _{HYS_EN} / V _{HYS_VDDQEN}	EN/VDDQEN threshold hysteresis		100			mV
UVLO THRESHOLD						
V _{TH_VCC}	VCC under-voltage lockout rising threshold		2.9	3.0	3.1	V
V _{HYS_VCC}	VCC under-voltage lockout threshold hysteresis		230			mV
V _{TH_VIN}	VIN under-voltage lockout rising threshold		2.9	3.0	3.1	V
V _{HYS_VIN}	VIN under-voltage lockout threshold hysteresis		300			mV
V _{TH_VDDQIN}	VDDQIN under-voltage lockout rising threshold		1.5	1.55	1.6	V
V _{HYS_VDDQIN}	VDDQIN under-voltage lockout threshold hysteresis		120			mV
V _{TH_1V8IN}	1V8IN under-voltage lockout rising threshold		1.5	1.55	1.6	V



POWER GOOD				
PG _{VDD2_F} (FAULT)	PG for VDD2 falling threshold (Fault)		90	%V _{REF}
PG _{VDD2_R} (GOOD)	PG for VDD2 rising threshold (Good)		95	%V _{REF}
PG _{VDD2_R} (FAULT)	PG for VDD2 rising threshold (Fault)		115	%V _{REF}
PG _{VDD2_F} (GOOD)	PG for VDD2 falling threshold (Good)		105	%V _{REF}
PG _{VDD1_F} (FAULT)	PG for VDD1 falling threshold (Fault)		65	%V _{REF}
PG _{VDD1_R} (GOOD)	PG for VDD1 rising threshold (Good)		85	%V _{REF}
PG _{VDDQ_F} (FAULT)	PG for VDDQ falling threshold (Fault)		50	%V _{REF}
PG _{VDDQ_R} (GOOD)	PG for VDDQ rising threshold (Good)		80	%V _{REF}
PG _{TD_LTOH} ⁽¹⁾	PG Low to High delay		20	μs
PG _{TD_EN LOW} ⁽¹⁾	EN Low to PG Low delay		2	μs
V _{PG}	PG Sink Current Capability	Sink 4mA	0.4	V
THERMAL SHUTDOWN				
T _{SD}	Thermal shutdown temperature ⁽¹⁾		155	°C
	Thermal shutdown hysteresis ⁽¹⁾		25	°C

(1) Guarantee by design

9 Functional Block Diagram

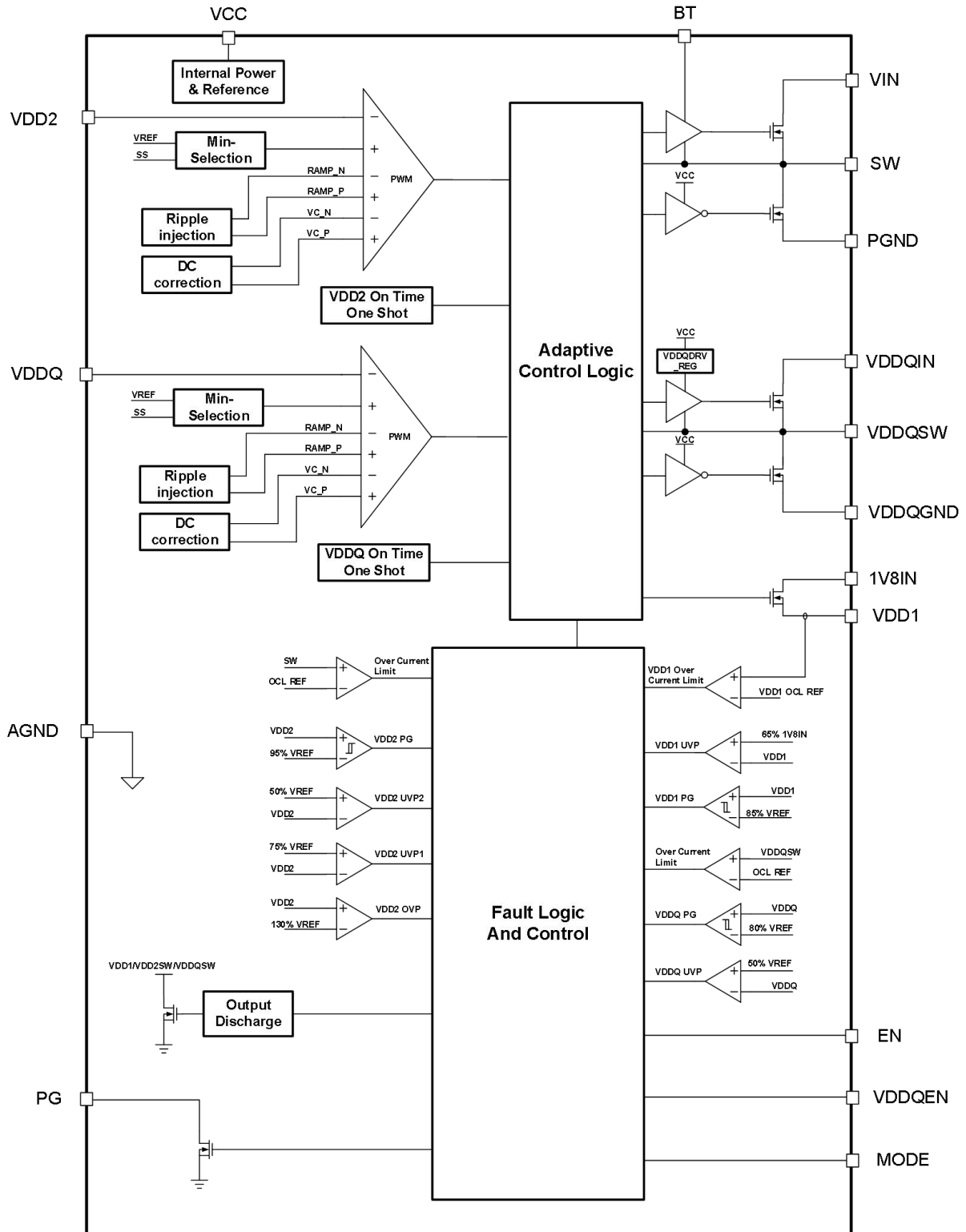


Figure 2 Functional Block Diagram

10 Feature Description

10.1 Power Converter

10.1.1 PWM Operation

The SC6301 integrates two synchronous buck converters for VDD2/VDDQ. The converters adopt a constant on-time control (COT) mode for the buck converters, with a pseudo-fixed switching frequency. It can provide a fast transient loop response. Both converters integrate an internal ramp compensation circuit, which makes the converters work stable with low ESR or ceramic output capacitors.

10.1.2 CCM Operation

The buck converter operates in continuous conduction mode (CCM) when the valley inductor current exceeds zero amps. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback (FB) voltage is below the reference voltage V_{REF} . The on period is set proportional to the converter input voltage and inversely proportional to the output voltage, maintaining a pseudo-fixed frequency over the input voltage range, then the HS-FET is turned off after the on period. The low-side MOSFET (LS-FET) is turned on when the HS-FET is turned off. The on period is reset, and the HS-FET turns on again when the FB voltage falls below the V_{REF} . A dead-time control scheme is internally integrated to avoid shoot-through between the LS-FET and HS-FET.

10.1.3 DCM Operation

As the load current decreases, the converter enters discontinuous conduction mode (DCM) after the inductor current crosses zero. In this operation, when the FB voltage is below the V_{REF} , the HS-FET is turned on for a fixed period. Then the inductor current decreases with LS-FET turned on. The LS-FET driver enters the Hi-Z state when the inductor current reaches zero. It takes a longer time to discharge the output capacitor with a light load current. The HS-FET will turn on again when the FB voltage drop to V_{REF} . With this mechanism, the SC6301 reduces the switching frequency and improves the efficiency at light load. The device can also revert to CCM operation once the output current exceeds the critical level. The critical current can be calculated by the below equation:

$$I_{OUT(CRIT)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

10.2 VDD1

The SC6301 provides a high-performance, low $R_{DS(on)}$ load switch for VDD1 output. The VDD1 can support 3A peak output current, with a 4.5A slow current limit and 7A fast current limit protection. When EN=high, the device will detect VDD1 (1V8IN) voltage input. If the 1V8IN voltage exceeds the UVLO threshold, the VDD1 can be enabled. Otherwise, the VDD1 will be disabled and latched, and the PG will not indicate the VDD1 output.

10.3 VDD2

The SC6301 integrates a buck converter with low $R_{DS(on)}$ for VDD2 output. The VDD2 can support 14A peak output current. When EN=high, the device will detect VDD2 (VIN) voltage input. If the VIN voltage is higher than the UVLO threshold, the VDD2 will be enabled. Otherwise, the VDD2 will remain off but non-latched.

10.4 VDDQ

The VDDQ is a buck converter with low $R_{DS(on)}$ for VDDQ output. The VDDQ can support 3A output current. When VDDQEN=high, the device will detect VDDQ (VDDQIN) voltage input. The VDDQ will be enabled when the VDDQIN voltage exceeds the UVLO threshold. Otherwise, the VDD1 will remain off but non-latched. The VDDQ pin can be used as a feedback input to set the output voltage by a resistor divider.

10.5 Device Control

10.5.1 Enable/Disable Control (EN and VDDQEN)

The SC6301 has two enable input pins of EN and VDDQEN to provide simple control logic for the power state. All the power rails of VDD1, VDD2, and VDDQ are turned on at the S0 state (EN = VDDQEN = High). In the S3 state (EN = High, VDDQEN=Low), the VDD1 and VDD2 are turned on, and VDDQ is turned off with discharge enabled. In S4/S5 state (EN = Low, VDDQEN=Low), all the output rails will be turned off with a specific time sequence.

Table 1 EN and VDDQEN Control Scheme

State	VDDQEN	EN	VDD1	VDD2	VDDQ
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

10.5.2 Mode Config (MODE)

The device adopts a MODE Pin to set the VDD2 and VDDQ output voltage. Connect a resistor($\pm 1\%$ Tolerance) between the MODE pin and GND to configure the VDD2 and VDDQ output voltage. The corresponding relation is shown in Table 2. The mode detection is activated during the initial start-up by detecting the MODE pin voltage through a fixed current source from the MODE pin. After that, the output voltage of the VDD2 and VDDQ configurations is latched.

Table 2 MODE pin Config

State	R _{MODE}	VDD2(V)	VDDQ(V)
M1	Float or 232k	1.065	0.51
M2	150k	1.065	0.3
M3	100k	1.1	0.6
M4	0R	0.9	0.3

10.5.3 Power Good (PG)

The device integrates a power-good indicator to indicate whether the active rails' output voltage is ready. The Power Good (PG) pin is an open-drain output. Connecting PG to a voltage source through a 100k resistor is recommended. The PG signal is high when the active power rails reach the target threshold. The PG pin is low with the below event:

1. During the process of EN Off
2. VIN or VCC UVLO
3. VDD1 OCP and UVP, VDD2/VDDQ UVP and OVP, OTP

10.5.4 Soft Start

The SC6301 has the soft-start (SS) function for all the power rails, which makes the output smooth during powering up. Ensure all input voltage is ready before toggling the EN pin from low to high. When the EN becomes high, the output voltage increases slowly with the SS function. Once the output reaches the target value, the SS process is finished.

If the output of the power rails is pre-biased by a specific voltage during start-up, the device will not activate switching until the internal SS voltage becomes higher than the pre-bias voltage. This scheme ensures a smooth soft-start process.

10.5.5 Power-On Sequence

There are specified power sequence requirements from JEDEC standards for the LPDDR5, LPDDR5X, and

LPDDR4X. According to the standards, the VDD1 is always greater than VDD2, and VDD2 is always greater than VDDQ-200mV when any output exceeds 0.3V.

The typical power-on sequence is shown in Figure 3.

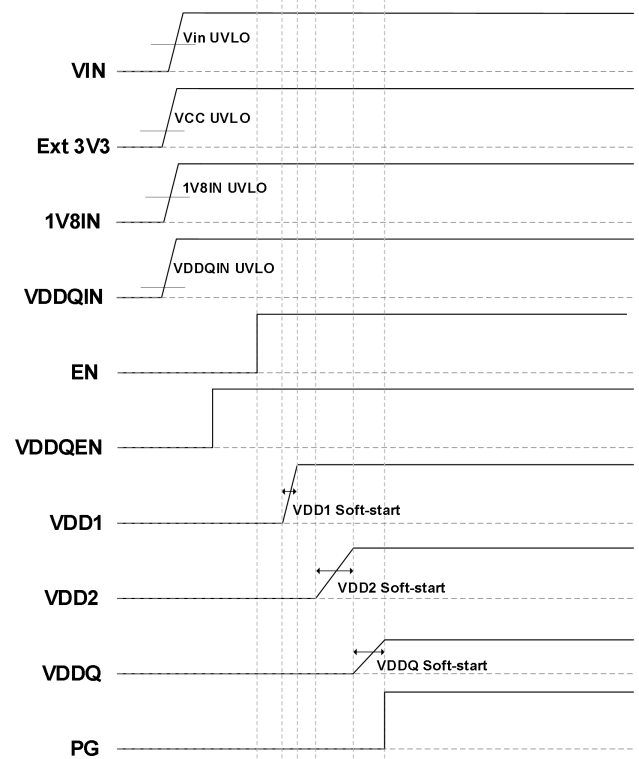


Figure 3 Power-On Sequence

Note:

1. The VCC power supply must be ready before 1V8IN power is applied.
2. To enable VDD1, the voltage of 1V8IN should exceed the ULVO rising threshold before EN on.
3. To activate the PG pin to indicate VDDQ after the start-up process, the voltage of VDDQIN and VDDQEN must exceed their threshold before VDD2 finishes the soft start.
4. After all the soft starts have been finished, the PG pin will keep high even if the VDDQ rail is turned off
5. If VDD1 or VDDQ is unused, PG still indicates the activated rails.

10.5.6 Power Off Sequence

The SC6301 features a specified power-off sequence to meet the requirement of the JEDEC standard. The VDD1 is disabled after a 5ms delay since the EN pin is pulled low; The VDD2 supports a soft shutdown function to ramp

down VDD2 output in a controlled time. All rails integrate a discharge function and activate when the corresponding rail is turned off. The power-off sequence is shown in Figure 4.

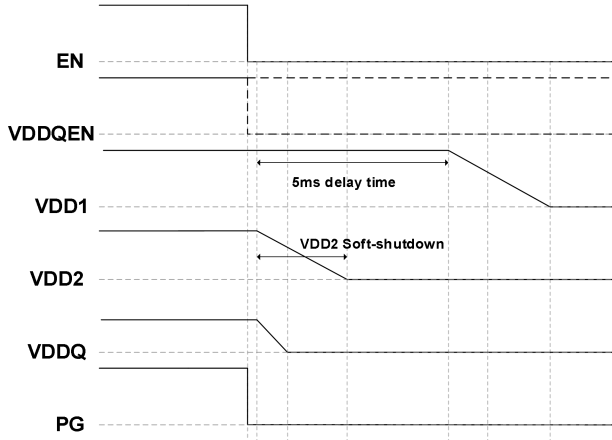


Figure 4 Power Off Sequence

10.6 Protection Functions

10.6.1 VDD1 Over Current Protection

The VDD1 has a 4.5A slow current limit. When the load current reaches to 4.5A current limit, the internal driver will regulate to hold a constant current for about 200μs. After that, the VDD1 is turned off and latched.

If the load current increases rapidly due to a short GND event, the current may exceed the 4.5A current limit before the control loop responds. Once the VDD1 reaches the secondary current limit (Typ. 7A), a fast turn-off circuit is activated to turn off the VDD1 immediately.

After the over-current protection latches off the VDD1, the PG is pulled low, and the other rails are latched off with discharge enabled.

10.6.2 VDD1 Over Voltage Protection

To protect the device at the output terminal, the VDD1 has a fixed OVP threshold. The SC6301 monitors the VDD1 to detect the over-voltage state. When VDD1 exceeds the OVP threshold, the OVP comparator output goes high, and the VDD1 turns off and latches. After the VDD1 is latched off, the PG is pulled low, and the other rails are latched off with discharge enabled.

10.6.3 VDD1 Under Voltage Protection

The SC6301 monitors VDD1 output voltage to detect under-voltage protection. Once the VDD1 output drops below 65% of the input voltage (1V8IN), it will be turned off

and latched. After the VDD1 is latched off, the PG is pulled low, and the other rails are latched off with discharge enabled.

10.6.4 VDD2/VDDQ Over Current Protection

VDD2 and VDDQ have inductor overcurrent limit (OCL) protection through cycle-by-cycle valley current detection. The switching current is sensed by the drain to the source voltage of LS-FET.

The switching current increases at a linear slew rate during the HS-FET turns on. During the HS-FET turns off, the current decreases linearly. If the sensed current exceeds the OCL threshold, the LS-FET will remain on even if the FB voltage is lower than the reference. The new switching cycle can be delayed until the switch current drops to the OCL threshold. Thus, the VDD2 and VDDQ maximum load current is shown below:

$$I_{max} = I_{OCL} + \frac{\Delta I_L}{2}$$

When the OCL is triggered, the inductor current is limited, and the output voltage will drop due to higher load conditions. When the output voltage of VDD2 or VDDQ drops below the UVP threshold, the VDD2 and VDDQ rails will be turned off and latched.

10.6.5 VDD2/VDDQ Over Voltage Protection

Both VDD2 and VDDQ have over-voltage protection. When the VDD2 exceeds 130% of V_{REF} , or the VDDQ exceeds the 0.8V threshold, the OVP comparators go high, and the output will be discharged and latched.

10.6.6 VDD2/VDDQ Under Voltage Protection

Both VDD2 and VDDQ have under-voltage protection.

For the VDD2, when VDD2 voltage drops below 75% but exceeds 50% of V_{REF} , the UVP-1 comparator goes high, and the converter will latch off after 30μs delay time. The HS-FET will turn off, and LS-FET will remain on until the inductor reaches 0A. During this period, the OCL helps to control the inductor current. When the VDD2 drops below 50% of the V_{REF} , the UVP-2 comparator goes high, and the converter will latch off directly.

For VDDQ, when VDDQ drops below 50% of V_{REF} , the UVP comparator goes high, and the device will latch off directly, the same as VDD2 triggers UVP-2.

10.6.7 Input UVLO Protection

The SC6301 has 3 input UVLO protection: VCC UVLO(3V), VIN UVLO(3V), and VDDQIN UVLO(1.55V).



The device can only be enabled when both VCC and VIN are higher than their UVLO rising thresholds and will shut down when VCC or VIN triggers their UVLO falling thresholds.

10.6.8 Output Voltage Discharge

All rails integrate a discharge function and activate when the corresponding rail is turned off, whether controlled by EN/VDDQEN pin or triggered by some fault events. The discharge path can be turned on to discharge the output voltage. The VDD2 discharge resistor is 15Ω, and the VDDQ discharge resistor is 10Ω.

10.6.9 Thermal Shutdown

The SC6301 monitors the junction temperature of the device internally. If the junction temperature exceeds the threshold of 155°C, the part will shut down and the output will be discharged. The device restarts when the temperature drops below the OTP recovery threshold of 130°C.

11 Application Information

11.1 Output Voltage

The VDDQ output voltage can be configured for customized values using external feedback resistors.

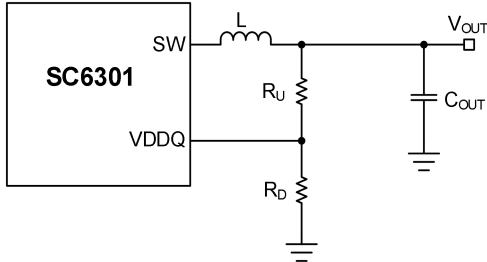


Figure 5 Output Voltage Setup with Divide Resistor

$$V_{OUT} = V_{REF} \times \left(\frac{R_U + R_D}{R_D} \right)$$

Where:

V_{REF} is the internal reference voltage VDDQ;

R_U and R_D are the resistors connected from VOUT to GND.

Use 1% tolerance or higher accuracy resistors and keep the feedback resistors close to the FB pin on the PCB layout. The R_D is typically between 10KΩ to 50KΩ, considering the accuracy and standby loss.

11.2 Inductor Selection

The inductor selection is a tradeoff between size, cost, efficiency, and transient response performance. The critical parameters of an inductor are inductance, DC resistance, and saturation current.

Generally, choose the inductor current ripple ΔI_L to be approximately 30% to 50% of the maximum load current. The switching frequency, input voltage, output voltage, and output ripple determine the inductor value:

$$L = \frac{V_{OUT}}{\Delta I_L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The inductor saturation current I_{SAT} should be higher than the inductor peak current I_{PEAK} with a sufficient margin.

$$I_{PEAK} = 0.5 \Delta I_L + I_{OUT_MAX}$$

11.3 Input Capacitor Selection

The input current of the Buck converter is discontinuous and the input capacitor should be carefully selected. The

SC6301 requires input decoupling capacitors and sufficient bulk capacitors.

A low ESR input decoupling capacitor close to the IC's VIN pin and GND pin is the best choice, such as an X5R or X7R ceramic capacitor. It's recommended to use 20μF ceramic capacitor with a sufficient voltage rating for the VDD2 buck input pin VIN, and 10μF ceramic capacitor for the VDDQ buck input pin VDDQIN.

The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

11.4 Output Capacitor Selection

Since ceramic capacitor has low ESR and good high-frequency filtering, the X7S or X7R ceramic capacitor is recommended for the best ripple performance across temperature and input voltage variations. The output voltage ripple is estimated as the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right) \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Based on the voltage coefficient of ceramic, it normally loses its most capacitance at the rated voltage, so leave margin on voltage rating to ensure adequate effective capacitance. Larger capacitors cause lower output voltage ripple and higher load transient performance. If the output capacitor is too large, the SC6301 maybe not reach the target output voltage within SS time and latch-off. The maximum output capacitor value can be calculated as below:

$$C_{out_max} = \frac{(I_{LIM} - I_{OUT}) \times t_{ss}}{V_{out}}$$

Where I_{LIM} is the start-up current, restricted by current limit.

12 Layout Guide

12.1 PCB Layout Guide

The PCB layout should be carefully designed for the best performance to avoid instability, switching noise interference, and EMI issues. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI.

Here are some guidelines for reference:

- 1) The input capacitor (C_{VIN} , MLCC) should be close to the IC to minimize the critical path area and ensure the current flows through the C_{VIN} first, then the VIN pin. The PCB trace should be wide and short.
- 2) Place the decouple capacitor as close as to the VCC PIN.
- 3) The feedback resistor should be close to the FB pin (VDD2/VDDQ) and be away from the switching node.
- 4) Keep the switching node SW with a short trace.
- 5) Use a wide and short GND trace to minimize ground inductance which causes VOUT drops during heavy load.
- 6) Use a ground plane in one of the middle layers as a noise shielding and a heat-sinking PCB ground plane.

Connect these ground traces and planes with proper vias.

12.2 Layout example

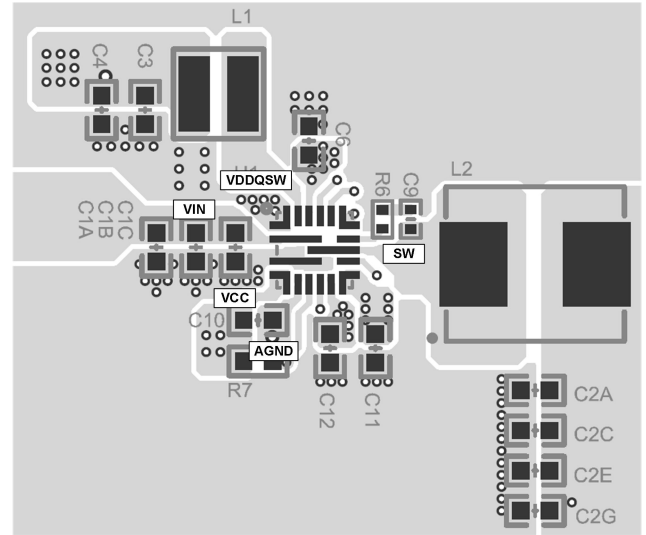
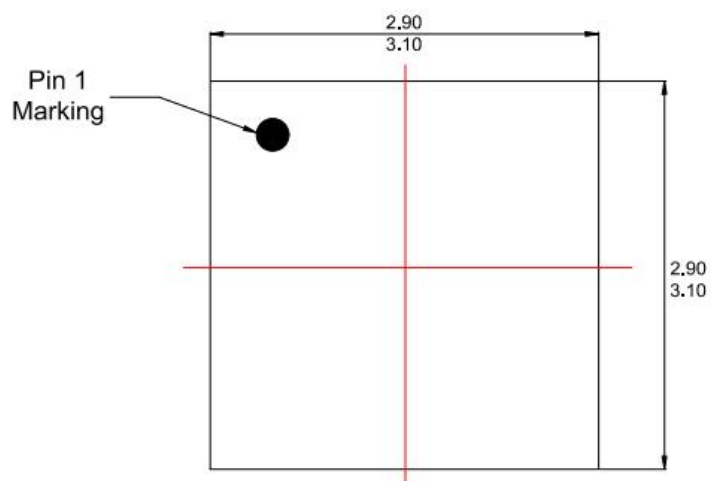


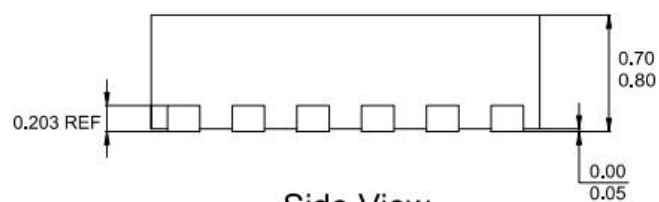
Figure 6 PCB layout example

MECHANICAL DATA

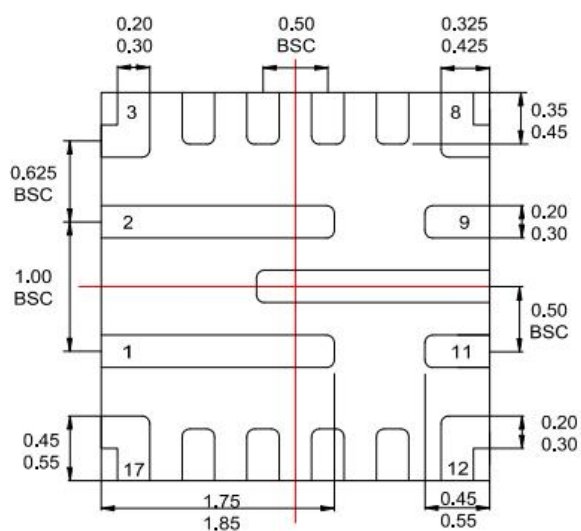
FCQFN3X3 (3mm x 3mm)



Top View



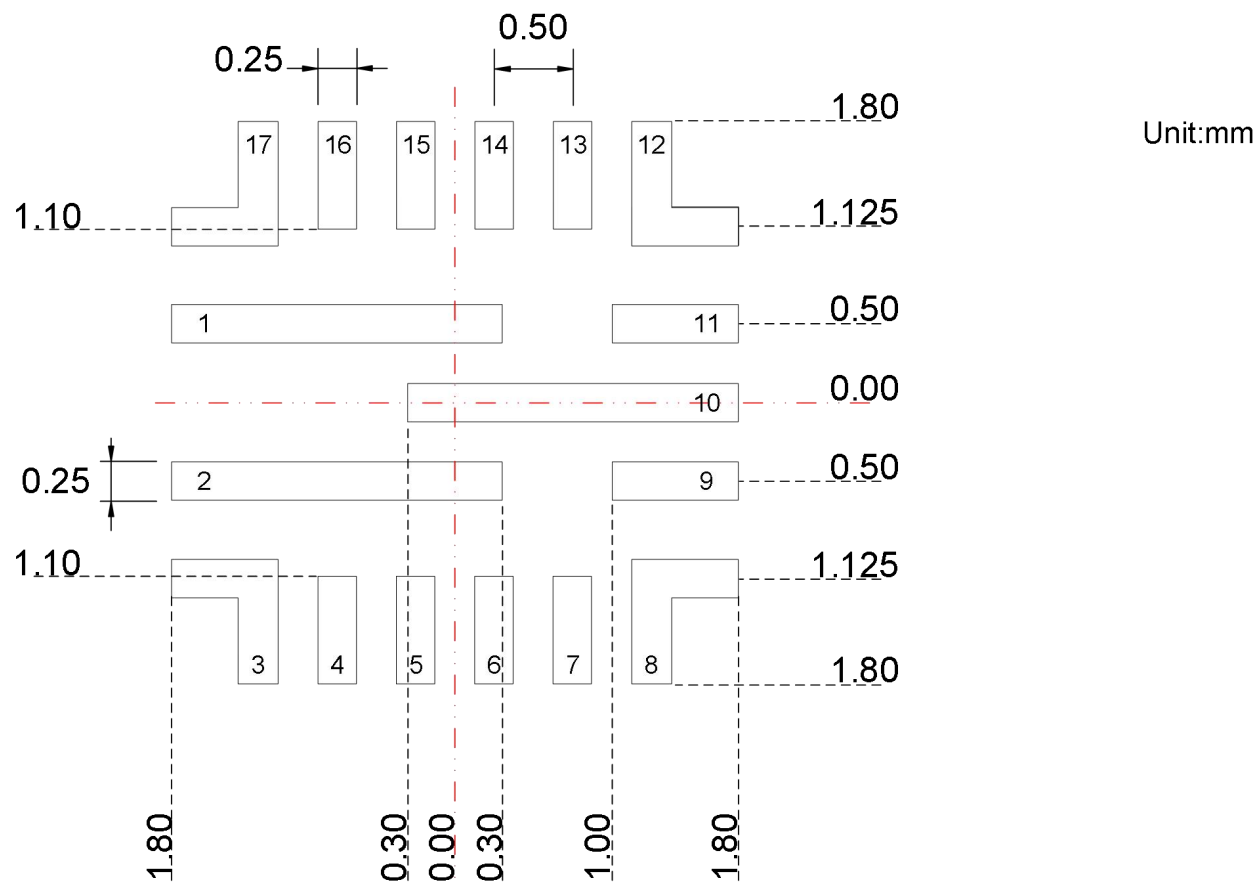
Side View



Bottom View

Unit:mm

RECOMMENDED FOOTPRINT

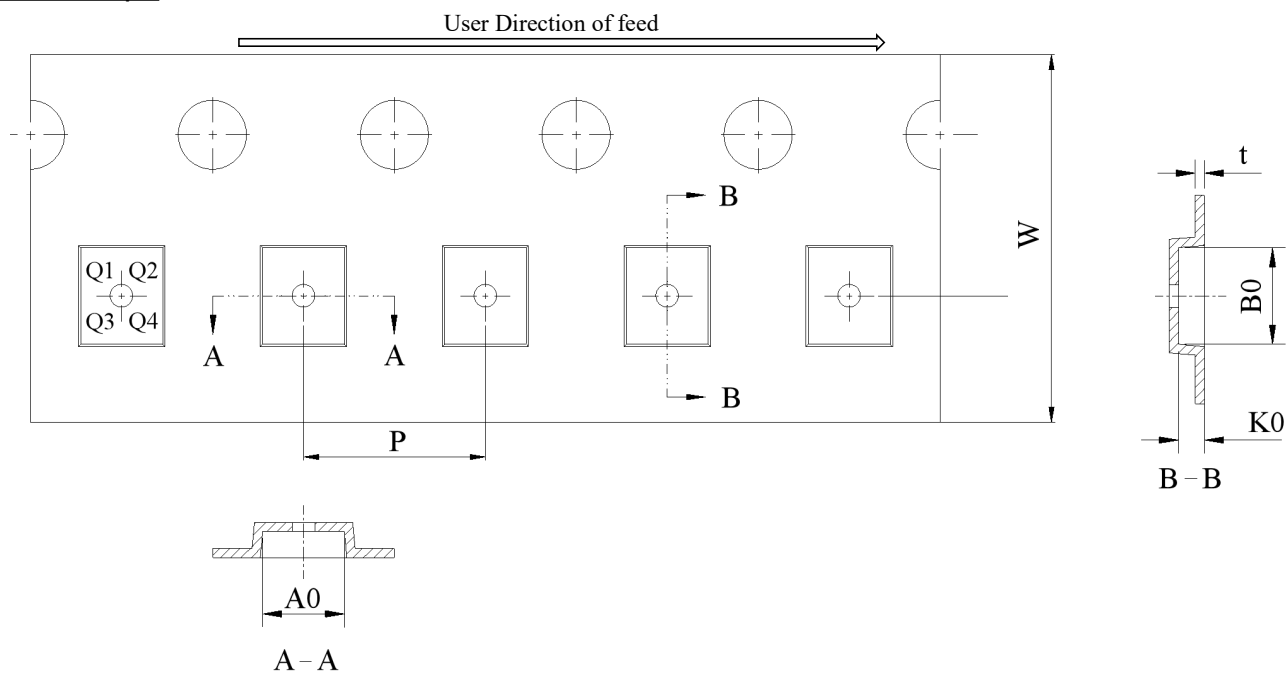


Top View

Land Pattern Example

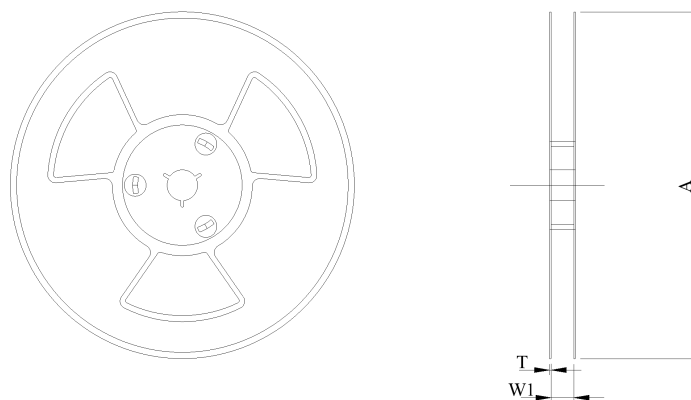
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12 ± 0.3	8 ± 0.1	3.3 ± 0.1	3.3 ± 0.1	1.13 ± 0.1	0.25 ± 0.05	Q1

REEL



Item	A	W1	T
Size (mm)	329 ± 1	12.4^{+2}_0	2.0 ± 0.3



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