Synchronous, 80V Bi-directional Buck-Boost Charger Controller with I2C interface and MPPT

1 Descriptions

SC8808 is a synchronous buck-boost charger, which supports buck mode, boost mode and buck-boost mode during forward charging or reverse discharging operation. SC8808 manages multi types of battery charging from wide input range from 4.5V to 80V, supporting trickle charge, pre-charge, constant current charge, constant voltage charge and autonomous termination. The battery discharging mode supports wide output range from 5V to 48V. SC8808 also provides input current and battery current monitoring function.

Through I2C interface, user can set the charging/discharging mode easily, and program the charging current, charging voltage, input voltage regulation, input current limit, OTG output voltage adjustment, current limits and other parameters flexibly. Besides, input/output current limit, charge voltage/discharging voltage, and switching frequency could be set by external resistors.

SC8808 supports frequency dithering to meet better EMI performance and integrates synchronization feature to switching under same frequency with external clock.

SC8808 integrates 11-bit ADC to monitor voltage, current. Full protection is supported including input and battery over-voltage protection, input over-current, over-temperature protection.

SC8808 is available in a 5mm x 6mm QFN-36 Package.

2 Features

- Wide Input Range: 4.5V to 80V, 88V sustainable
- High Efficiency Buck-Boost Conversion
- Buck-Boost Battery Charger up to 16 cells Li-on battery, 18 cells LiFePO4 battery, lead-acid battery
- Charging Management including Trickle charge, Pre-Charge, CC Charge, CV Charge, Auto-recharge
  - Charge current : 1000mA~20A，150mA/step，for 5mΩ
  - Pre-charge current: 400mA~10A, 100mA/step，for 5mΩ
  - Termination Current: 400mA~6700mA，100mA/step ，for 5mΩ
- Support reverse discharging mode:
  - Power up USB port from battery (USB OTG), Compliant with PD 3.1
  - OTG output voltage 5~48V
  - EPR 28V/36V/48V
  - Output Current: 2375mA~50A, 375mA/step for 2mΩ
- I2C interface
- Input current limit set by external resistor and register, up to 50A, support 2mΩ/5mΩ sense resistor
- Input voltage regulation to avoid adapter overload
- Support external supply for driver, up to 12V
- Switching frequency: 80kHz~480kHz and support frequency dithering and frequency synchronization
- Current monitor for input and output current
- Automatic MPPT algorithm to support solar charging
- Integrated 11-bit high accuracy ADC for current/voltage monitor
- Protection including UVP, OVP, OCP, SCP, OTP
- QFN 5x6-36 Package, 0.5mm pitch

3 Applications

- Outdoor Power Station
- Industrial Equipment
- Power Backup
- Equipment with Rechargeable Batteries

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8808QDGR	36 pin QFN	5mm x 6mm x 0.75mm

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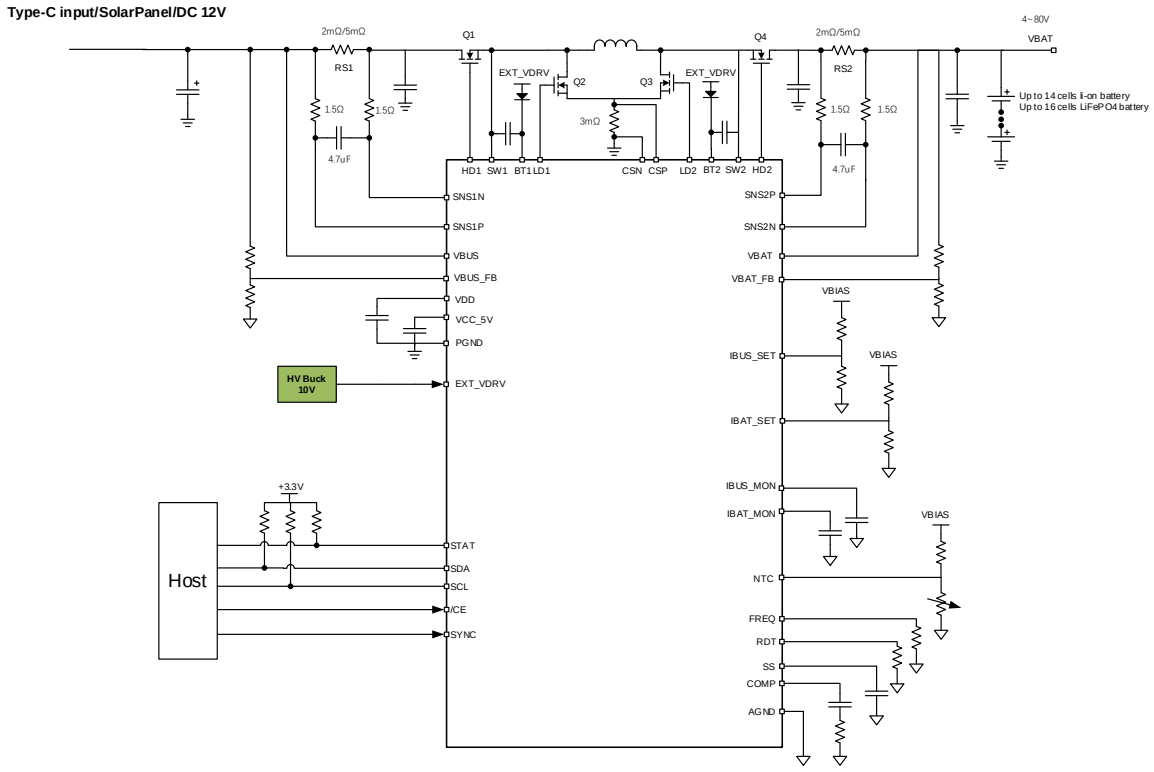
5 Typical Application Circuit

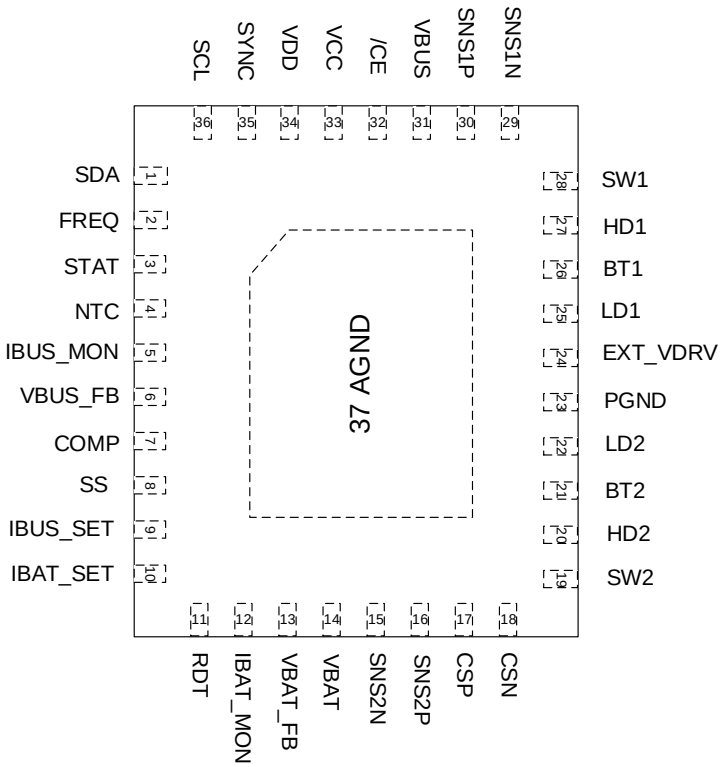


Typical Application: driver is supplied by external power

6 Terminal Configuration and Functions

TOP VIEW

QFN 5X6-36



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	SDA	I/O	I2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10kΩ pullup resistor according to I2C specifications.
2	FREQ	I	switching frequency selection pin. Connect a resistor to gnd to set switching frequency among 80kHz to 480kHz
3	STAT	O	Charger Version：Open drain active high output. Charger status indication pin, connect with external pull-up supply.
4	NTC	O	Charger Version：Battery temperature input pin. Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. Short this pin to ground to disable this function.
5	IBUS_MON	O	IBUS current monitoring output pin including both charging and discharging mode, connect a capacitor to GND.
6	VBUS_FB	I	Feedback input of VBUS in discharging mode, connect to resistor divider from VBUS.
7	COMP	O	Connect RC network with this pin to compensate the control loop.

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8	SS	O	Soft-start setting pin. Connect a capacitor to configure soft start time.
9	IBUS_SET	I	IBUS current limit setting pin. Set IBUS/IOTG current by connecting a resistor to GND.
10	IBAT_SET	I	IBAT current limit setting pin. Set IBAT current by connecting a resistor to GND.
11	RDT	O	Dead time setting pin. Connect a resistor to GND to set a proper deadtime.
12	IBAT_MON	O	IBAT current monitoring output pin including both charging and discharging mode, connect a capacitor to GND.
13	VBAT_FB	I	Battery external feedback pin, connect to a resistor divider from battery positive terminal to GND.
14	VBAT	PWR	Charger supply input pin, connect to battery positive terminal.
15	SNS2N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from battery.
16	SNS2P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from battery.
17	CSP	I	Positive input of Inductor current sense node.
18	CSN	I	Negative input of Inductor current sense node.
19	SW2	PWR	Switching node 2. Connect this pin to the inductor
20	HD2	O	Gate driver output to control the external high side power MOSFET(Q4).
21	BT2	PWR	Connect a 100nF capacitor between BT2 pin and SW2 pin to bootstrap a bias voltage for high side MOSFET driver.
22	LD2	O	Gate driver output to control the external low side power MOSFET(Q3).
23	PGND	I/O	Power ground.
24	EXT_VDRV	PWR	Gate driver supply input, Place at least 2.2μF ceramic capacitor near this pin to PGND pin close to the IC. Connect with external supply or connect directly to VCC_5V.
25	LD1	O	Gate driver output to control the external low side power MOSFET(Q2).
26	BT1	PWR	Connect a 100nF capacitor between BT1 pin and SW1 pin to bootstrap a bias voltage for high side MOSFET driver.
27	HD1	O	Gate driver output to control the external high side power MOSFET(Q1).
28	SW1	PWR	Switching node 1. Connect this pin to the inductor
29	SNS1N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from VBUS
30	SNS1P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 10mΩ) on the power path to sense the current into or out from VBUS
31	VBUS	PWR	The power input node of charger in charging mode and the power output node of the converter in discharging node.
32	/CE	I/O	IC enable pin. This pin is internally pulled low. When this pin is pulled high, IC is disabled. When this pin is pulled high. IC is reset and enter shutdown mode.

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			/CE is also used for hardware rest function.
33	VCC	PWR	Output of an internal 5.25V LDO regulator. Connect a at least 2.2 μF ceramic capacitor from VCC to PGND pin close to the IC
34	VDD	PWR	Used for NTC/IBUS_SET/IBAT_SET bias power supply
35	SYNC	I	Frequency setting and external clock signal input pin, the internal frequency is synchronized to the external clock frequency when external clock signal is applied to this pin.
36	SCL	I	I2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10kΩ pullup resistor according to I2C specifications.
37	AGND	/	Connect to AGND with PGND.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VBUS, VBAT, SNS1N, SNS1P, SNS2N, SNS2P,	-0.3	88	V
	SW1, SW2	-0.3	88	V
	BT1-SW1, HD1-SW1, BT2-SW2, HD2-SW2,	-0.3	13.2	V
	BT1, BT2, HD1, HD2	-0.3	90	V
	VBUS_FB, VBAT_FB	-0.3	6	V
	SYNC, FREQ, /CE, COMP, SS, SDA, SCL, IBUS_MON, IBAT_MON, NTC, IBUS_SET, IBAT_SET，RDT，STAT	-0.3	6	V
	LD1, LD2	-0.3	13.2	V
	VCC,	-0.3	6	V
	EXT_VDRV	-0.3	13.2	V
	SNS1P to SNS1N, SNS2P to SNS2N	-0.3	0.3	V
	BT1 to SW1, BT2 to SW2, HD1 to SW1, HD2 to SW2	-0.3	13.2	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins except	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)		-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VBUS	VBUS voltage range	4.5		80	V
VBAT	VBAT voltage range			80	V
T_A	Operating ambient temperature	-40		105	°C
T_J	Operating junction temperature	-40		125	°C

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R_{S1}	IBUS current sense resistor	2	2	10	mΩ
R_{S2}	IBAT current sense resistor	2	5	10	mΩ
R_{S3}	Inductor peak/valley current sense resistor	2	3	5	mΩ
Inductance	L	4.7	10	47	μH
Fsw	Switching frequency	100	200	480	kHz

7.4 Thermal Information

THERMAL RESISTANCE(1)		**QFN-36 (5mmX6mm)**	**UNIT**
θ_{JA}	Junction to ambient thermal resistance	33.7	°C/W
θ_{JC}	Junction to case thermal resistance	14.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	10.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

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7.5 Electrical Characteristics

T_J= +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
I_{Q_VBAT}	Quiescent current into VBAT pins	VBAT = 80V, No VBUS; , I2C enabled，VCC short to EXT_VDRV，ADC disabled, /CE= Low Tj<85°C		54	80	μA
		VBAT = 80V, No VBUS; VCC short to EXT_VDRV and all ADC channel enabled, /CE= Low Tj<85°C		1200		μA
		VBAT = 58.8V, VBUS=4.5~80V EOC state; /CE= Low Tj<85°C		100		μA
		VBAT = 80V, VBUS=4.5~80V /CE=high, in shutdown mode; Tj<85°C		5	17	μA
I_{Q_VBUS}	Quiescent current in charging mode (I_{SNS1P}+I_{SNS1N}+I_{BUS})	Non-switching， ADC disabled		0.8		mA
$I_{Q_VBUS_SHUTDOWN}$	Quiescent current into VBUS pin in shutdown mode	VBUS = 48V, no battery, /CE= high, Tj=25°C		50		μA
		VBUS = 80V, no battery, /CE= high Tj=25°C		80		μA
POWER SUPPLY						
V_{UVLO_VBUS}	VBUS under-voltage lockout threshold	VBUS rising		4.5	4.7	V
		VBUS falling	3.9	4.1		V
V_{UVLO_VBAT}	VBAT under-voltage lockout threshold	VBAT rising		4.5	4.7	V
		VBAT falling	3.9	4.1		V
V_{CC}	VCC regulation voltage	V_{BUS} = 6V~80V	5	5.25	5.5	V
V_{DROP_VCC}	Drop out voltage of VCC regulator	V_{BUS} =5V, I_{VCC} = 20mA		100	200	mV
I_{VCC_LIM}	VCC regulator current capability	V_{BUS} = 10V, V_{CC} > 3V	70	130		mA
		V_{BUS} = 10V, V_{CC} = 1V		20	30	mA
V_{VCC_OK}	VCC supply voltage to work	Rising edge		4.5	4.7	V
		Falling edge	3.9	4.1		V
Driver						
$V_{EXT_VDRV_UVLO}$	EXT_VDRV supply voltage to work	Rising edge		4.5	4.7	V
		Falling edge	3.9	4.1		V

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$V_{EXT_VDRV_OVP}$	EXT_VDRV overvoltage	Rising edge		13	13.6	V
		Falling edge	12.2	12.6		V
$V_{DRV_ON_Q1_Q4}$	Buck/Boost high side driver turn on resistance	V_{BTx}-V_{SWx}=5.25V，100mA sourcing		0.1	0.2	V
$V_{DRV_OFF_Q1_Q4}$	Buck/Boost high side driver turn off resistance	V_{BTx}-V_{SWx} =5.25V，100mA sinking		0.04	0.15	V
$I_{DRV_ON_Q1_Q4}$	Buck/Boost high side driver turn on resistance	V_{BTx} - V_{SWx} = 5.25V	1.5	3		A
$I_{DRV_OFF_Q1_Q4}$	Buck/Boost high side driver turn off resistance	V_{BTx} - V_{SWx} = 5.25V	1.5	3		A
$V_{BTx_REFRESH_TH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST1}-V_{SW1} when low side refresh pulse is requested	2.5	3.2	3.7	V
	Rising edge			3.4	3.8	V
$V_{DRV_ON_Q2_Q3}$	Buck/Boost low side driver turn on resistance	100mA sourcing		0.1	0.2	V
$V_{DRV_OFF_Q2_Q3}$	Buck/Boost low side driver turn off resistance	100mA sinking		0.05	0.15	V
$I_{DRV_ON_Q2_Q3}$	Buck/Boost low side driver turn on resistance	V_{EXT_DRV} = 5.25V	1.3	3		A
$I_{DRV_OFF_Q2_Q3}$	Buck/Boost low side driver turn off resistance	V_{EXT_DRV} = 5.25V	2	3		A
SWITCHING FREQUENCY						
F_{SW}	Switching frequency	R_{FREQ}= 52kΩ		400		kHz
		R_{FREQ}= 62.5kΩ		345		kHz
		R_{FREQ}= 115kΩ		200		kHz
		R_{FREQ}= 240kΩ		100		kHz
SYNC	SYNC pin threshold	Input high voltage threshold	1.3			V
		Input low voltage threshold			0.4	V
t_{SYNC_MIN}	Minimum external clock pulse width		100			ns
DEAD TIME SETTING						
t_{DT}	Dead time setting	R_{DT}= 0kΩ		40		ns
		R_{DT}= 10kΩ		55		ns
		R_{DT}= 27kΩ		70		ns
		R_{DT}= 51kΩ		85		ns
		R_{DT}= 100kΩ		100		ns
		R_{DT}= 200kΩ		115		ns
		R_{DT}= 510kΩ		130		ns

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		R_{DT}= float	145			ns
Input Current Regulation						
I_{INDPM_INT}	Input current regulation accuracy, set by register	R_{SNS1}= 2mΩ, IINDPM= 40A setting	-3		3	%
		R_{SNS1}= 2mΩ, IINDPM= 20A setting	-3		3	%
		R_{SNS1}= 2mΩ, IINDPM= 9.875A setting	-5		5	%
		R_{SNS1}= 2mΩ, IINDPM= 5A setting	-10		10	%
I_{INDPM_EXT}	Input current regulation accuracy, set by IBUS_SET pin	R_{SNS1}= 2mΩ, IINDPM= 40A setting IBUS_SET=1.595V	-3		3	%
		R_{SNS1}= 2mΩ, IINDPM= 20A setting IBUS_SET=0.8V	-3		3	%
		R_{SNS1}= 2mΩ, IINDPM= 10A setting IBUS_SET=0.4V	-5		5	%
		R_{SNS1}= 2mΩ, IINDPM= 5A setting IBUS_SET=0.2V	-10		10	%
Input Voltage Regulation						
V_{INDPM_FB}	VBUS_FB feedback for VINDPM loop regulation	VBUS_FB=1.123V	-1		1	%
		VBUS_FB=0.6V	-3		3	%
Charging Mode						
V_{BAT_SHORT}	Battery short detection and trickle charge threshold	VBAT falling	3	3.2	3.4	V
		VBAT rising	3.4	3.6	3.8	V
V_{BAT_LOWV}	Pre-charge to CC charge threshold	VBAT rising,, respect to Charge Voltage	28.5	30	31.5	%
		VBAT rising，respect to ChargeVoltage	53.5	55	56.5	%
		VBAT rising，respect to ChargeVoltage	65.5	67	68.5	%
		VBAT rising，respect to ChargeVoltage	69.4	71	72.5	%
V_{BAT_REG}	Battery voltage reference regulation accuracy	V_{BAT_FB}=1.536V for 0~85° C	-0.5		0.5	%
		V_{BAT_FB}=1.536V for -40~125° C	-0.75		0.75	%
V_{RECH}		Recharge threshold= 93%	91.5	93	94.5	%

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	Recharge threshold, VBAT falling, below V_{BAT_REG}	Recharge threshold= 94.3%	93	94.5	96	%
		Recharge threshold= 95.2%	93.5	95	96.5	%
		Recharge threshold= 97.6%	96	97.5	99	%
V_{FLOAT}	Float charge threshold	Float charge voltage, respect to V_{BAT_REG}	89	90.5	92	%
			91.5	93	94.5	%
			93	94.5	96	%
			93.5	95	96.5	%
I_{PRECHG_INT}	Pre-charge current accuracy 400mA ~ 10000mA	R_{SNS2}=5mΩ, I_{PRECHG} = 10A, set by reg	-3		3	%
		R_{SNS2}=5mΩ, I_{PRECHG} = 4A, set by reg	-5		5	%
		R_{SNS2}=5mΩ, I_{PRECHG} = 1A , set by reg	-10		10	%
		R_{SNS2}=5mΩ, I_{PRECHG} = 400mA , set by reg	-25		25	%
I_{PRECHG_EXT}	Pre-charge current accuracy 400mA ~ 10A	R_{SNS2}=5mΩ, I_{PRECHG} = 4A , set by ext	-6		6	%
		R_{SNS2}=5mΩ, I_{PRECHG} = 1A Set by ext	-25		25	%
		R_{SNS2}=5mΩ, I_{PRECHG} = 400mA Set by ext	-60		60	%
I_{BAT_INT}	IBAT Charging current accuracy 1000mA ~ 20000mA set by ICC register	R_{SNS2}=5mΩ, I_{CC} = 20A	-3		3	%
		R_{SNS2}=5mΩ, I_{CC} = 10A	-3		3	%
		R_{SNS2}=5mΩ, I_{CC} = 5A	-3		3	%
		R_{SNS2}=5mΩ, I_{CC} = 1000mA	-20		20	%
I_{BAT_EXT}	IBAT Charging current accuracy set by IBAT_LIM pin	R_{SNS2}=5mΩ, I_{CC} = 20A IBAT_SET=2V	-3		3	%
		R_{SNS2}=5mΩ, I_{CC} = 10A IBAT_SET=1V	-3		3	%
		R_{SNS2}=5mΩ, I_{CC} = 5A IBAT_SET=0.5V	-5		5	%
		R_{SNS2}=5mΩ, I_{CC} = 1000mA IBAT_SET=0.1V	-20		25	%
I_{TERM}	Termination current accuracy 400mA ~ 6.7A, set by Iterm register	R_{SNS2}=5mΩ, I_{TERM} = 2A	7.5		7.5	%
		R_{SNS2}=5mΩ, I_{TERM} = 1A	-15		15	%

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		R_{SNS2}=5mΩ，I_{TERM} = 500mA	-30		30	%
I_{TERM_EXT}	set by IBAT_SET pin	R_{SNS2}=5mΩ，I_{TERM} = 1A， Set by external	-20		20	%
Current Monitor Function						
V_{IBUS_MON}	Suggested IMON output voltage range		0		3	V
G_{IMON_IBUS}	IBUS current sensing ratio	V_{IBUS_MON} / $V_{SNS1P-SNS1N}$， R_{SNS1} = 2mΩ		30		V/V
$V_{IMON_IBUS_ACC}$	IBUS current monitor accuracy in charging mode	V_{SNS1P}-V_{SNS1N}=40mV IBUS = 20A, R_{SNS1} = 2mΩ	-3		3	%
		V_{SNS1P}-V_{SNS1N}=20mV IBUS = 10A, R_{SNS1} = 2mΩ	-10		10	%
G_{IBAT_MON}	IBAT current sensing ratio	V_{IBAT_MON} / $V_{SNS2P-SNS2N}$， R_{SNS2} = 5mΩ		30		V/V
$V_{IMON_IBAT_ACC}$	IBAT current monitor accuracy in charging mode	IBAT = 20A, R_{SNS2} = 5mΩ	-1.5		1.5	%
		IBAT = 10A, R_{SNS2} = 5mΩ	-3		3	%
		IBAT = 1A, R_{SNS2} = 5mΩ	-20		20	%
OTG mode						
$V_{BAT_OTG_UVLO}$	VBAT threshold to enable OTG mode	VBAT rising		4.5	4.7	V
		VBAT falling	3.9	4.1		V
$V_{OTG_REG_INT}$	VBUS regulation accuracy in OTG mode, set by register	VOTG=5V setting	-4		4	%
		VOTG=20V setting	-2.5		2.5	%
		VOTG=28V setting	-3		3	%
		VOTG=48V setting	-2		2	%
$V_{OTG_EXT_FB}$	OTG feedback reference voltage，set by VBUS_FB pin	VBUS_FB pin reference voltage	1.112	1.123	1.134	V
$I_{BUS_OTG_INT}$	IBUS regulation accuracy in OTG mode, range from 0.5A ~ 50A	R_{SNS1}= 2mΩ，IOTG= 10A setting Set by register	-3		3	%
		R_{SNS1}= 2mΩ，IOTG= 5A setting Set by register	-6		6	%
$I_{BUS_OTG_EXT}$	IBUS regulation accuracy in OTG mode, range from 0.5A ~ 50A	R_{SNS1}= 2mΩ，IOTG= 10A setting Set by IBUS_SET pin	-5		7	%
		R_{SNS1}= 2mΩ，IOTG= 5A setting Set by IBUS_SET pin	-10		10	%
NTC COMPARATOR (Charging mode)						
V_{T1}	NTC Cold threshold V_{T1}	VNTC rising, as percentage to VCC	72.4	73.3	74.2	%
		VNTC falling, as percentage to VCC	71.5	72	72.5	%

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V_{T2}	NTC cool threshold V_{T2}	5°C Rising，±0.5% accuracy	70.25	70.75	71.25	%
		5°C falling，±0.5% accuracy	68.75	69.25	69.75	%
		10°C Rising，±0.5% accuracy	67.75	68.25	68.75	%
		10°C falling，±0.5% accuracy	66.5	67	67.5	%
		15°C Rising，±0.5% accuracy	64.75	65.25	65.75	%
		15°C falling，±0.5% accuracy	63.75	64.25	64.75	%
		20°C Rising，±0.5% accuracy	61.75	62.25	62.75	%
		20°C falling，±0.5% accuracy	60.75	61.25	61.75	%
V_{T3}	NTC warm threshold V_{T3}	40°C Falling，±0.5% accuracy	47.75	48.25	48.75	%
		40°C Rising，±0.5% accuracy	48.75	49.25	49.75	%
		45°C Falling，±0.5% accuracy	44.25	44.75	45.25	%
		45°C Rising，±0.5% accuracy	45.25	45.75	46.25	%
		50°C Falling，±0.5% accuracy	40.25	40.75	41.25	%
		50°C Rising，±0.5% accuracy	41.25	41.75	42.25	%
		55°C Falling，±0.5% accuracy	37.25	37.75	38.25	%
		55°C Rising，±0.5% accuracy	38.5	39	39.5	%
V_{T5}	NTC hot threshold V_{T5}	Falling	33.75	34.25	34.75	%
		Rising	34.75	35.25	35.75	%
I_{CC_JEITA}	Charge current foldback ratio	40% option		40		%
		20% option		20		%
$V_{BAT_REG_JEITA}$	Charge voltage foldback ratio in jeita	97.5% option		97.		%
		95% option		95		%
		93% option		93		%
COLD / HOT COMPARATOR (OTG MODE)						
V_{OTG_COLD}	OTG COLD comparator threshold.	VNTC rising, as percentage to VCC -20C setting	79.5	80.0	80.5	%
		VNTC rising, as percentage to VCC -10C setting	76.5	77	77.5	%
		VNTC falling, as percentage to VCC -20C setting	78.5	79	79.5	%
		VNTC falling, as percentage to VCC	75.5	76	76.5	%

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		-10C setting				
V_{OTG_HOT}	OTG HOT comparator threshold.	VNTC falling, as percentage to VCC 55C setting	37.25	37.75	38.25	%
		VNTC falling, as percentage to VCC 60C setting	34.25	34.75	35.25	%
		VNTC falling, as percentage to VCC 65C setting	30.65	31.25	31.75	%
		VNTC rising, as percentage to VCC 55C setting	40.25	40.75.	41.25	%
		VNTC rising, as percentage to VCC 60C setting	37.25	37.75	38.25	%
		VNTC rising, as percentage to VCC 65C setting	34	34.5	35	%
Protections						
V_{BUS_OVP}	VBUS OVP threshold	VBUS rising		82		V
		VBUS falling	78	80		V
V_{BAT_OVP}	VBAT OVP threshold	VBAT rising, as percentage of the regulation target, to stop switching	102.5	104	105.5	%
		VBAT falling, as percentage of the regulation target, to recover	100.5	102	103.5	%
$V_{BAT_ABS_OVP}$	VBAT abs OVP threshold	VBAT rising	80	82	84	V
		VBAT falling	78	80	82	V
V_{OTG_OVP}	VBUS OVP threshold in OTG mode, OTG voltage set by Internal register	VBUS rising, as percentage of the regulation target, to stop switching	120	125	130	%
		VBUS falling, as percentage of the regulation target, to recover	115	120	125	%
$V_{OTG_SHORT/UVP}$	VBUS OTG short/UVP threshold in OTG mode	VBUS falling, to stop switching	3	3.2	3.4	V
		VBUS rising, to recover	3.4	3.6	3.8	V
I_{VALLEY_CLP}	Cycle by cycle valley current limit	3mΩ sense resistor		40		A
		3mΩ sense resistor		25		A
		3mΩ sense resistor		15		A
		VBAT< 3V, BAT SHORT	1	2	3	A
I_{PK_CLP}	Cycle by cycle peak current limit	3mΩ sense resistor		40		A
		Default for charger/DCDC version，3mΩ sense resistor		25		A
		3mΩ sense resistor		15		A
R_{BUS_DIS}	Discharging current at VBUS pin when VBUS OVP happens			7	12	kΩ

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R_{BAT_DIS}	Discharging current at VBAT pin when VBAT OVP happens			5	8	kΩ
ADC						
ADC_VBUS	Vbus voltage reading	Range	0		81.88	V
		LSB		40		mV
ADC_VBAT	Battery voltage reading	Range	0		81.88	V
		LSB		20		mV
ADC_IBUS	Input current reading, 2mΩ	Range	0		51175	mA
		LSB		25		mA
ADC_IOTG	Output discharging current reading, 2mΩ	Range	0		51175	mA
		LSB		25		mA
ADC_ICHG	Battery Charging current reading, 5mΩ	Range	0		20.47	A
		LSB		10		mA
ADC_IDCHG	Battery discharging current reading, 5mΩ	Range	0		20.47	A
		LSB		10		mA
ADC_NTC	NTC voltage ratio relative to VCC	Range	0		99.9	%
		LSB		0.0488		%
I2C INTERFACE AND IO LOGIC						
V_{IL}	SCL, SDA input low voltage				0.4	V
V_{IH}	SCL, SDA input high voltage		1.2			V
f_{SCL}	I2C clock frequency				400	kHz
I_{SINK_SDA}	SDA pin sink current	V_{SDA} = 0.4V	70	100		mA
/CE IO LOGIC						
V_{IL}	/CE input low voltage				0.4	V
V_{IH}	/CE input high voltage		1.2			V
STAT I/O LOGIC						
STAT pin	Output saturation voltage	5 mA drain current			0.4	V
THERMAL REGULATION AND SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Temperature rising, 150°C setting		150		°C
		Thermal shutdown hysteresis		20		°C

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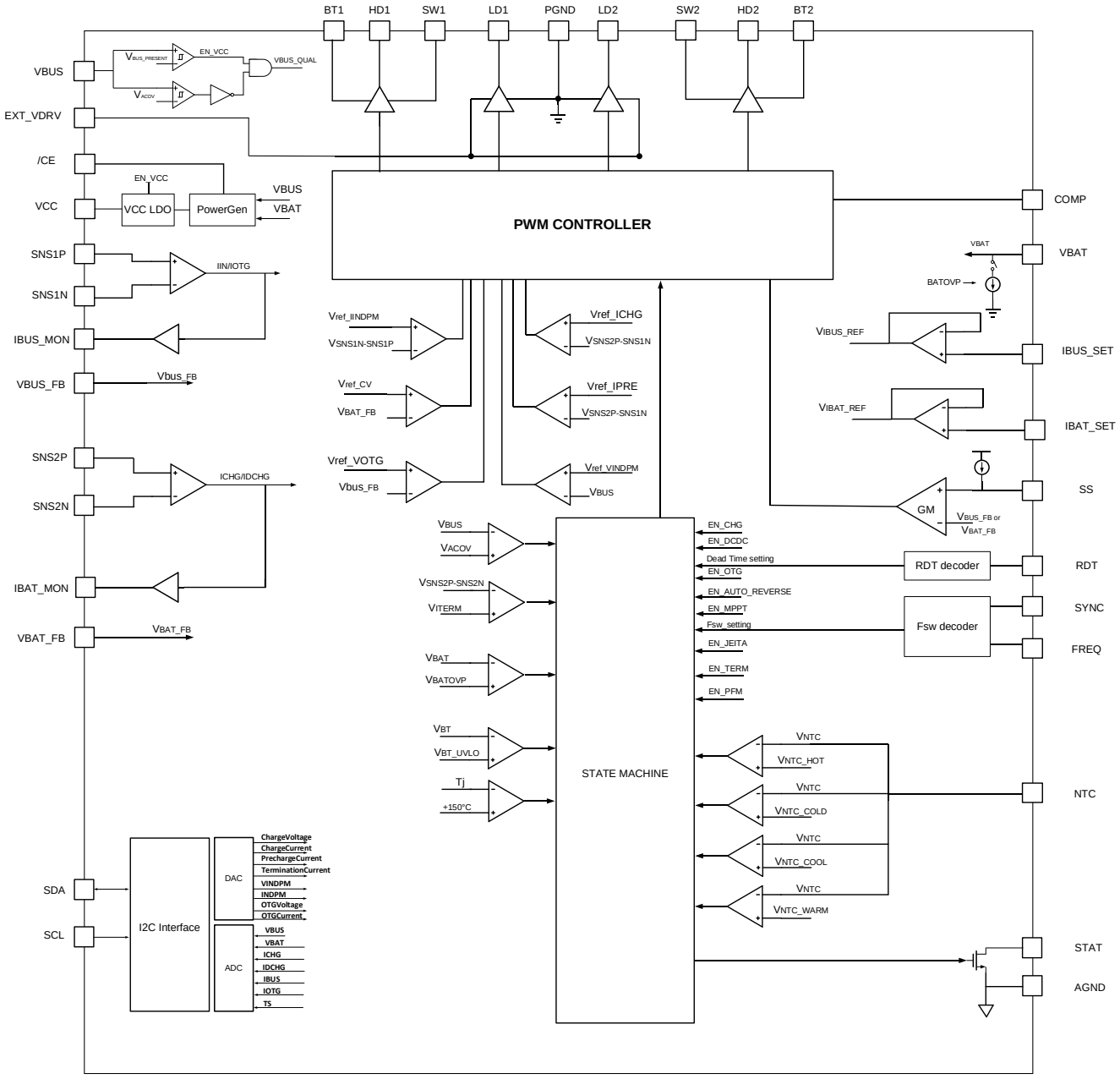
8 Functional Block Diagram



9 Feature Description

9.1 Power On Reset

The IC is powered up when either VBUS > VBUS_UVLO or VBAT > VBAT_UVLO, and the I2C register becomes accessible to the host. The internal bias circuit of the IC is powered by VBUS or VBAT pin

9.1.1 Chip Enable and Shutdown Mode

The device adopts /CE pin as hardware IC enable pin. When the /CE pin is tied to logic HIGH, the IC is disabled and all the I2C registers is reset. Thus, /CE pin can be used as hardware reset function. Do not keep /CE pin float, an external pull-up or pull-down resistor is needed to establish a robust control logic.

When battery is plugged-in and /CE is pulled high, IC consumes lower quiescent current from VBAT pin by turning off most of block.

9.1.2 Standby Mode

The device enters standby mode by set Reg0x10<1>=1. When IC enters standby mode, controller stop switching with adapter present.

9.1.3 Battery Only Mode

After the IC is powered up, if there is only VBAT voltage and the OTG mode is not enabled, the IC works in battery only mode. There is Low power mode and Performance mode for battery only mode, Set by Reg0x11<0>.

In Low power mode (Reg0x11<0>=1, default), the VCC_5V LDO is activated, but VDD is turn-off to minimize the quiescent current. It is suggested that NTC, IBUS_SET, IBAT_SET resistor divider connect to VDD network. In Low power mode, the I2C interface is enabled, the V_{BUS_UVLO} comparator is on to detect adapter plug-in.

In Performance mode (Reg0x11<0>=0), VDD is also activated. All block is activated, ADC can be enabled by Host control.

9.1.4 Power Up from VBUS

If the IC detects that VBUS > V_{BUS_UVLO}, no matter the battery is connected or not, the IC determines a power source is connected at VBUS. The IC starts poor source detection with VBUS discharging path turning on for around 100ms. If a good source is detected, the IC sets the PG_STAT register to 1 to inform the host that the adapter is plugged in.

If VBUS > VBUS_OVP at any time, the IC sets the PG_STAT register to 0, VBUS_OVP_STAT to 1, and stop any switching operation.

9.1.5 VCC regulator power up

VCC regulator provides operation current to the internal circuit of the IC, driver circuit can be powered by VCC or EXT_DRV. When VBUS and VBAT are both higher than>7.7V, VCC is powered by the lower one of VBUS and VBAT to minimize VCC LDO power loss

The VCC LDO regulator can provide 130mA load capability, but its current limit is fold-back to 20mA (Typ) when VCC is shorted to ground.

9.1.6 Poor Source Qualification

After the adapter is plugged in, the IC starts to detect the input power's current capability.

It turns on VBUS discharging path from VBUS pin to ground for around 100ms during the qualification process. If the V_{BUS} > V_{BUS_UVLO} in the process, and V_{BUS} < V_{BUS_OVP}, the adapter is determined as a good source, so the PG_STAT bit is set to 1.

If the charger detects V_{BUS} > V_{BUS_OVP} during the qualification, it keeps turn-on VBUS discharge current path till the VBUS drops below VBUS OVP threshold. If the qualification fails due to the VBUS OVP or a bad source, the IC sets PG_STAT bit to 0.

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Poor source function also can be disabled by set 0x11<1>=1.

9.2 ADC

The SC8808 integrate 11-bit ADC and provide 2 working mode selection.

When Reg0x1A<6>=1, ADC works at One-shot mode. Host need to set ADC_START bit to 1 to enable one-shot conversion, when ADC conversion is completed, ADC_START is reset to 0.

When Reg0x1A<6>=0, ADC works at Continuous mode, ADC automatically samples voltage and current channel enabled by host control.

Item	Range	Resolution
IIN_ADC	0mA~51175mA	25mA/step，with 2mΩ IBUS resistor
IOTG_ADC	0mA~51175mA	25mA/step，with 2mΩ IBUS resistor
ICHG_ADC	0mA~20470mA	10mA/step，with 5mΩ IBAT resistor
IDCHG_ADC	0mA~20470mA	10mA/step，with 5mΩ IBAT resistor
VBUS_ADC	0mV~81880mV	40mV/step
VBAT_ADC	0mV~81880mV	40mV/step
NTC_ADC	0%~99.9%*VCC	0.0488%*VCC

9.3 Charging mode

9.3.1 Dynamic Power Management

When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device reduces the charge current to regulate the input current to the IINDPM limit or regulate input voltage to VINDPM voltage.

9.3.1.1 Input Current limit setting

The actual input current limit can be set by internal register or external IBUS_SET pin.

a) Internal Register Setting (Reg0x11<7>=0)

- IINDPM is set by Reg0x07<7:0>
- For 2mΩ IBUS sense resistor，IINDPM ranges from 2375mA to 50000mA, 7bit, step=375mA
- Default IINDPM value is set to 50 A

b) External setting: (Reg0x11<7>=1)

- IINDPM is set by IBUS_SET pin voltage, the allowed maximum voltage is 2V
- V_{IBUS_SET} = 20× IBUS_LIM × R_{S1}, Where R_{S1} is IBUS sense resistor, IBUS_LIM is input current limit

9.3.1.2 VINDPM setting

VINDPM function is adopted in case of adapter overload condition. VINDPM voltage is set by VBUS_FB pin.

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VINDPM=Vindpm_REF*(1+Rup/Rdown)

Where，

- Vindpm_REF is set by Reg0x08 and Reg0x09，which ranges from 0.1V-1.123V
- R_{UP} and R_{DOWN} is the resistor divider.

VINDPM voltage must be set at a proper value which usually is lower than adapter voltage to ensure charger working normally.

9.3.2 Charging Profile

Charger can autonomously complete a charging cycle without host involvement according to the register configurations. The default charging configuration is shown as below.

Charging parameters	Registers	Default values
Charging voltage V_{BAT_REF}	Charge Voltage FB: Reg0x03	1.536V
Fast charging current limit	Charge Current: Reg0x00	Internal Reg: 20A for 5mΩ External: set by resistor
Pre-charge current limit I_{PRECHG}	Pre-charge Current: Reg0x01	2A
Trickle charge current I_{BAT_SHORT}	Fixed	2A
Termination current I_{TERM}	Termination Current: Reg0x02	1A
Recharge voltage threshold V_{RECH}	VRECHG: Reg0x10<5:4>	97.6%
VBAT short voltage V_{BAT_SHORT}	Fixed	3.2V
VBAT_Low voltage V_{BAT_LOWV}	VBAT_LOWV: Reg0x10<7:6>	71.4%
IINDPM current I_{INDPM}	IINDPM: Reg0x07h	Internal Reg: 50A for 2mΩ External: set by resistor
VINDPM_FB voltage V_{INDPM_REF}	VINDPM_REF: Reg0x09/0x08	0.612V

9.3.2.1 Fast Charge Current Limit Setting

The actual fast charging current limit is decided by the lower setting of CC charge current (REG0x00) and IBAT_SET pin. The actual fast charge current limit is decided by Reg0x11<6>.

a) Internal Register (Reg0x11<6>=0)

- Fast charge current is set by Reg0x00<7:0>
- For 5mΩ IBAT sense resistor，charge current ranges from 1000mA to 20000mA, step=100mA, offset = 1000mA
- Default IBAT LIMIT value is set to 10A

b) External setting: (Reg0x11<6>=1)

- Fast charge current is set by IBAT_SET pin voltage, the allowed maximum voltage is 2V
- V_{IBAT_SET} = 20× IBAT_LIM × R_{S2}

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Where R_{S2} is IBAT sense resistor, IBAT_LIM is charge current limit. When External setting is selected, fast charge current must be set to above 4A to ensure the pre-charge current is above 0.4A.

9.3.2.2 Pre-Charge Current Limit Setting

The actual pre-charge current limit is decided by REG0x01() or external IBAT SET pin, which is set by Reg0x11<6>

a) Internal Register (Reg0x11<6>=0)

- Pre-charge current is set by Reg0x01<7:0>
- For 5mΩ IBAT sense resistor, pre-charge current ranges from 300mA to 10A
- Default pre-charge current value is set to 2A

b) External setting: (Reg0x11<6>=1)

- Pre-charge current equals to 0.2* Fast charge current
- For 5mΩ IBAT sense resistor, Pre-charge current range from 400mA to 10A

9.3.2.3 Termination Current Limit Setting

The actual termination current limit is decided by REG0x02() or external IBAT SET pin，which is set by Reg0x11<6>

a) Internal Register (Reg0x11<6>=0)

- Termination Current is set by Reg0x02<5:0>
- For 5mΩ IBAT sense resistor，termination current range from 400mA to 6.7A
- Default termination current value is set to 1 A

b) External setting: (Reg0x11<6>=1)

- Termination current= 0.1* Fast charge current
- Range: 400mA~6700mA
- For 5mΩ IBAT sense resistor, When External setting is selected, ICC is suggested to be above 4A

SC8808 supports Li-ion, LiFePO4 and Lead-Acid battery charging profile.

#1 Li-ion and LiFePO4 battery charging profile:

The host can always control the charging parameters through I2C control.

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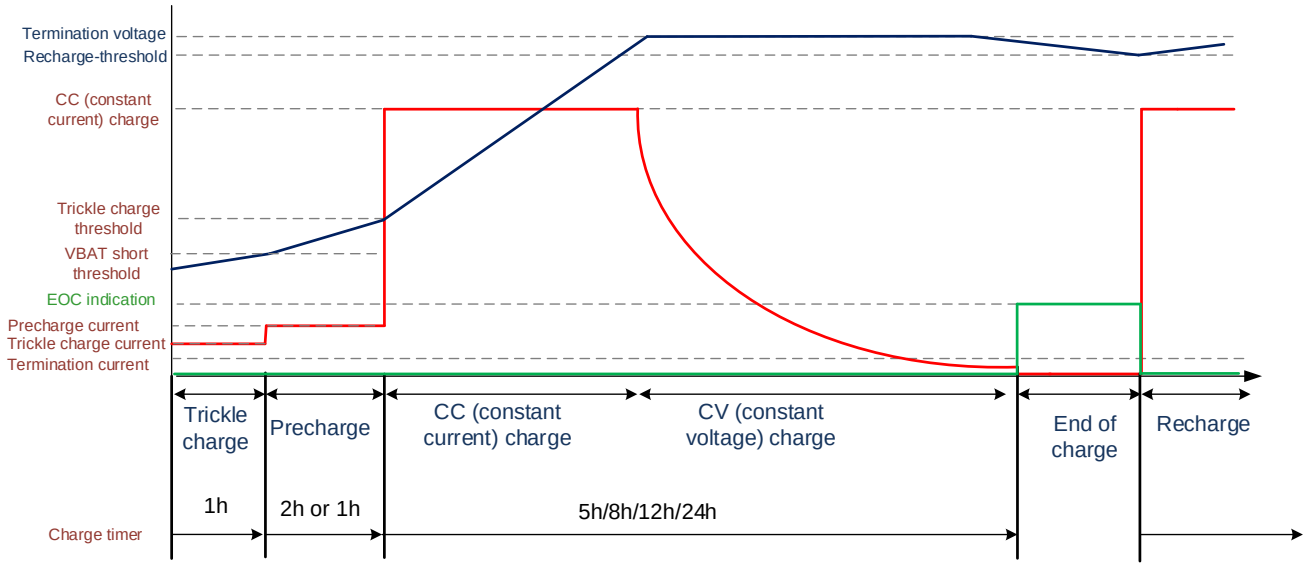

The CHG_STAT bit indicates the charging phases as:

000 – not charging

001 – charge under VBAT short condition (VBAT < VBAT_SHORT)

010 – pre-charge (VBUS_SHORT < VBAT < VBAT_LOWV)

011 – fast charge (CC mode, VBAT > VBAT_LOWV)

100 – taper charge (CV mode)

101 – EOC, charge termination done

110 – float charge (only when EN_float_charging bit (Reg0x11<2>) is set to 1)

111 – Reserved

The charger can automatically terminate the charging cycle when it detects the battery is fully charged.

When the charger detects that VBAT>V_{TERM}, IBAT < I_{TERM}, and it is not in VINDPM / IINDPM / thermal regulation for 500ms, the charger determines the battery is fully charged, so it terminates the charge automatically. This phase is also called End of Charge. In EOC phase, the converter stops switching

The auto-termination function can be disabled by setting EN_TERM = 0(Reg0x11<4>). The change of EN_TERM setting is effective immediately.

#2 Lead-Acid battery charging profile:

The SC8808 adopts float charge for lead-acid battery. When battery voltage reaches CV voltage and charge current is lower than termination current, IC enters float charge phase. In float charge:

- Float charge stat is set to 1 to inform host.
- Safety timer is disabled
- Charge termination is disabled

When EN_Float_charge bit toggeles, or adapter replug-in charge will restart float charge flow again.

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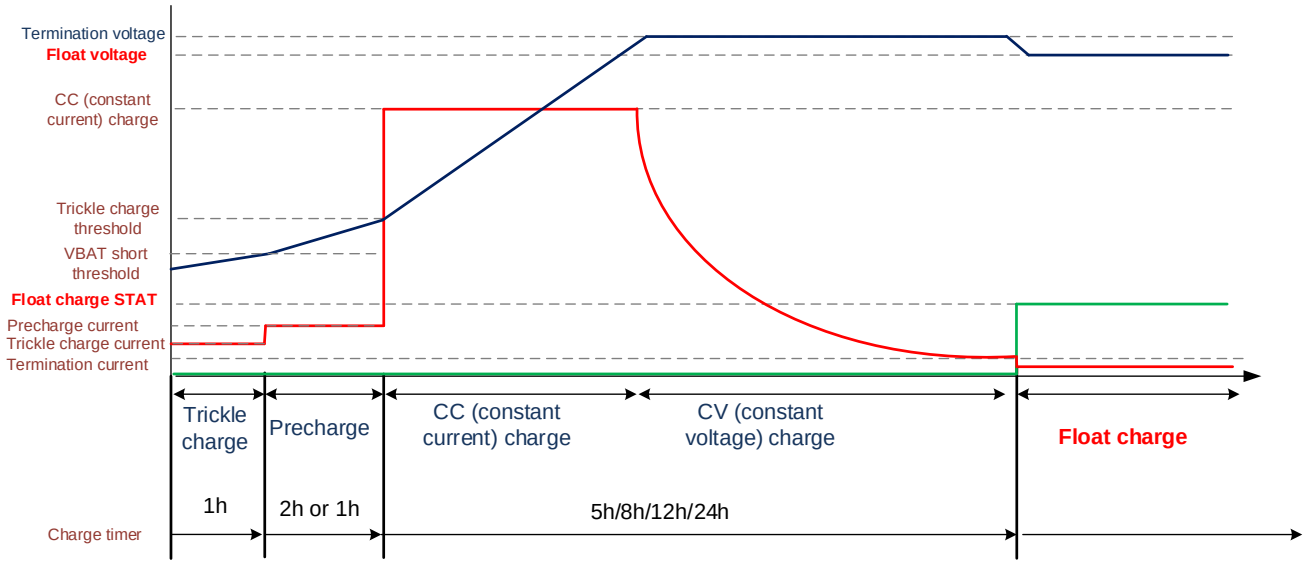

9.3.3 Status Indication

When IC charges the battery in trickle charge/CC charge/CV charge mode, the STAT pin outputs logic high, so the LED connected at STAT pin is turned on, indicating the charging is in process.

After the EOC conditions are met, the STAT pin is high-impedance status, indicating the battery cells are fully charged.

If the battery voltage drops below the recharge threshold V_{RECH}, the STAT pin will be turned on again.

When fault happens，the STAT outputs high and low at 0.5Hz frequency.

The charging status is as follow:

Table 1 STAT pin and working status

STAT status	IC working status
Low	Normal charging (Trickle /Pre-Charge/CC /CV /Recharge)
High-Z	End of charging (EOC)/ charger disable (EN_DCDC=0, CE is pulled down)
0.5Hz blinking	Abnormal charging（VBUS OVP/BAT OVP/Safety timer triggered/ /NTC_HOT/ NTC_COLD

9.3.4 Safety timer

The charger supports safety timer function to prevent extended charging cycle due to abnormal battery conditions.

The safety timer value is shown as below.

Safety timer	Value
Fast charge safety timer (Constant current charge/Constant voltage charge)	Set by CHG_TMR bits (Reg0x15<2>), default value = 12 hrs.
Trickle charge safety timer	Fixed at 1 hr.
Pre-charge safety timer	Set by CHG_TMR bit (Reg0x15<1:0>), 2 hrs. or 1 hrs.

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These timers can be disabled by corresponding register bits. When the timer is enabled or programmed, it restarts to count with the new value at once if it is in the right phase. When EN_TERM=0, Fast charge timer is disabled. If charging stops due to VBAT_OVP fault protection, the active timer will be suspended.

The **fast charge** safety timer gets reset for any of the following events:

1. Toggle DIS_DCDC bit
2. Adapter is re-plugged in
3. EOC state，V_{BAT} falls below V_{RECH}
4. BAT voltage changes from pre-charge to fast charge or vice versa
5. Change of the CHG_TRM bits
6. /CE toggles

The **trickle charge** safety timer gets reset for any of the following events:

1. Toggle DIS_DCDC bit
2. Adapter is re-plugged in
3. BAT voltage changes from trickle charge to pre-charge or vice versa
4. /CE toggles

The **pre-charge** safety timer gets reset for any of the following events:

1. Toggle DIS_DCDC bit
2. Adapter is re-plugged in
3. BAT voltage changes from trickle charge to pre-charge or vice versa, or changes from pre-charge to fast charge or vice versa
4. Change of the PRECHG_TRM bit
5. /CE toggles

9.4 OTG mode

The charger enters into OTG mode with all the following conditions are met:

- EN_OTG bit is set to 1 and DIS_DCDC bit is set to 0
- V_{BAT} >V_{BAT_UVLO}, Battery voltage is valid
- V_{DRV_UVLO} < V_{EXT_VDRV} < V_{DRV_OVP}, driver voltage is valid
- NTC HOT/COLD protection is not triggered

after the above conditions are valid, charger starts and VBUS ramps up to target voltage.

VOTG voltage is set by VBUS_FB pin or Internal register, which is decided by Reg0x16<6>.

a) Set by External VBUS_FB pin (Reg0x16<6>=1)

the output voltage is set by the resistor divider connected at VBUS_FB pin and can be calculated as below.

$$VOUT = V_{FB_REF} \times (1+\frac{R_{UP}}{R_{DOWN}})$$

Where:

V_{FB_REF} is the internal reference voltage 1.123V

R_{UP} and R_{DOWN} are the resistors connected from VBUS to VBUS_FB and to AGND

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If external setting method is not needed, FB pin is not suggested to be float which may cause uncertain output voltage. It is better to connect FB pin to resistor divider to ensure that IC output is under regulation.

b) Set by Internal register VOTG Reg0x05/04 (Reg0x16<6>=0)

OTG_Voltage is decided by Reg0x05/04, ranges from 5V to 48V.

- When Reg0x05<2>=0, OTG offset is 0.54V, OTG voltage ranges from 5V to 21V, voltage step is 20mV
- When Reg0x05<2>=1, OTG offset is 21.05V, OTG voltage ranges from 21.05~48V，voltage step is 50mV

OTG voltage adjustment provides slew rate selection, set by Reg0x16<3:2>:

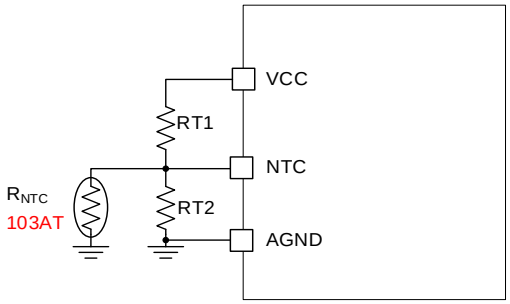
- 00: 0.05mV/μs
- 01: 0.2mV/μs
- 10: 0.5mV/μs(default)
- 11: 1mV/μs

In order to support MFI, OTG output current limit loop entering delay is adopted. After OTG current exceeds setting limit and last for 1ms (default) set by Reg0x16<5:4>, CC loop takes over and output voltage drops to avoid overload

9.5 NTC/JEITA function

9.5.1 JEITA compliance in charging mode

The IC can monitor the battery cell temperature through Negative Temperature Coefficient thermistor (NTC thermistor). The NTC thermistor shall be connected at NTC pin with external divider as shown in below figure.



NTC pin function can be disabled by short to GND.

The IC compares the NTC voltage with internal thresholds, so to decide whether the battery temperature is within a good range. If the temperature is outside the range of T1-T5, the IC stops the charging operation; if the temperature is within T1-T5 range, the charger determines whether to reduce the charging current or voltage as JEITA guideline requires for battery safety.

JEITA is valid only for CC/CV phase

The IC also provides flexible voltage / current settings beyond the JEITA requirements as below:

	T1-T2 (cool)	T2-T3 (normal)	T3-T5 (warm)
JEITA guideline -	< 1/2 * I_{CC}	Normal charge	I_{CHG}

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Charge current			
JEITA guideline - Charge voltage	V_{BAT_REG}	V_{BAT_REG}	< V_{BAT_REG}
Charge current control	JEITA Low Temp Current Setting (Reg0x18<2:1>): 00: Suspend 01: 20% * I_{CC} (default) 10: 40% * I_{CC} 11: 100% * I_{CC}	I_{CC}	JEITA High Temp Current Setting (Reg0x18<4:3>): 00: Suspend 01: 20% * I_{CC} 10: 40% * I_{CC} 11: 100% * I_{CC} (default)
Charge voltage control	V_{BAT_REG}	V_{BAT_REG}	JEITA High Temp Current Setting (Reg0x18<7:5>): 000: Charge Suspend 001: Set CV to 97.6%*CV 010: Set CV to 95.2%*CV（default） 011: Set CV to 93%*CV 100~111: CV unchanged

The host can disable the NTC function by setting TS_DIS = 1(Reg0x19<0>).

The host can disable the Jeita function by setting EN_JEITA = 0(Reg0x18<0>).

Use below equation to calculate the RT1/RT2 resistance when a 103AT NTC thermistor is used as shown in the application circuit.

$$R_{T2} = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - \frac{1}{V_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - 1\right)}$$

$$R_{T1} = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}}$$

The IC provides the comparator with fixed thresholds for T1 and T5. The thresholds for T2 and T3 can be programmed by TS_COOL and TS_WARM bits.

9.5.2 Cold/Hot temperature window in OTG mode

There are three zones for OTG mode: cold, normal and hot. The NTC voltage must be within the normal range for normal operation. If the temperature is outside of the range, the OTG mode is suspended, the converter stops switching. The IC reports the abnormal temperature status by TS_COLD_STAT and TS_HOT_STAT bits for discharging mode. During the fault, the VCC regulator keeps on.

Once the temperature returns within the normal range, the OTG mode is recovered and the fault status bits are cleared.

The thresholds can also be programmed through register bits.

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9.6 IMON function

The IMON function keeps working when DIS_DCDC = 1 but is disabled to save power when /CE is pulled HIGH.

The IC monitors the SNS1P-SNS1N and SNS2P-SNS2N in real time. It can output a proportional voltage at IMON pin to the selected object as shown below, providing a way for MCU to monitor the IC input/output current status.

- When EN_OTG=0, IMON pin monitor the charging mode IBUS/IBAT current
- When EN_OTG=1, IMON pin monitor the discharging mode IBUS/IBAT current

Channel	GAIN	Range	IMON output（RATIO bit=00/01/10/11）
IBUS_MON（charger Version）	30x	V_{SNS1P}.V_{SNS1N}=100mV	3V, internal clamp to ~3.2V
IBAT_MON	30x	V_{SNS2P}.V_{SNS2N}=100mV	3V, internal clamp to ~3.2V

9.7 Soft-start SS pin function

The SC8808 integrates SS pin for soft-start control. The soft-start time is set by the value of the soft-start capacitor connected from SS pin to GND. Inrush current during start-up is alleviated by adjusting the soft-starting time.

The Calculation formula is as follow:

- Tss=Css*Vref/Iss
- Iss=1μA
- Vref is CV loop reference in charging mode or VOTG reference in OTG mode

SS function is both valid for charging mode and discharging mode. The typical soft-start time is decided by design: value of resistor 1nF~100nF is acceptable.

9.8 Dead time selection function

The SC8808 detects RDT pin resistor and decides deadtime setting.

Channel	Dead time
SHORT	40ns
RDT=10kΩ	55ns
RDT=27kΩ	70ns
RDT=51kΩ	85ns
RDT=100kΩ	100ns
RDT=200kΩ	115ns
RDT=510kΩ	130ns
OPEN	145ns

9.9 Frequency and SYNC function

The switching frequency can be set by a resistor between FREQ pin and GND. This pin must be pulled to PGND using a R_{FSW}, do not leave floating.

The frequency calculation formula is decided by design, value of resistor 10k~500kΩ is acceptable.

Besides, the SYNC pin can also be used to synchronize the internal oscillator to an external clock signal among 100kHz~480kHz. When SYNC function is used, the deviation between the frequency set by R_{FREQ} resistor and the external frequency shall not exceed 15%.

When SYNC pin is tied to GND or VCC, switching frequency is decided by FREQ setting resistor

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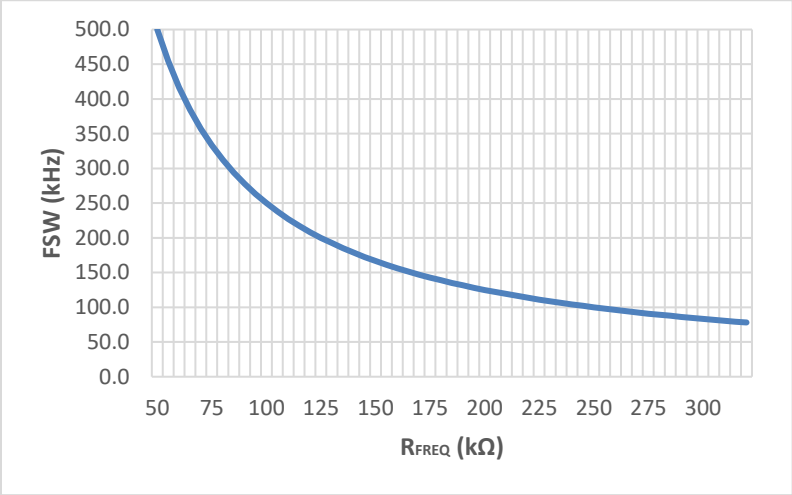
Fsw(kHz)=25000/（R_{FREQ}+10）

R_{FREQ}: Unit kΩ

Fsw：Unit kHz



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9.10 Maximum Power Point Tracking (MPPT)

The SC8808 adopts perturbation & observation method to track solar panel maximum power point. When MPPT function is enabled. Suggestion to enable MPPT algorithm:

- Set VBUS_FB resistor divider to ensure MPPT scan voltage covers panel voltage
- Set MPPT scan range is clamped down to VINDPM_REF_MIN(Reg0x14<1:0>)
- Set IBAT_LIM to proper value, or disable IBAT_ILIM external current limit
- Set IBUS_LIM to proper value, or disable IBUS_ILIM external current limit
- Set IL_MAX_CLP to proper value
- Set Reg0x13/Reg0x14/Reg0x40 according to practical test

The SC8808 provides interfaces in the register, related detail can be referred to register description

9.11 PFM/PWM Mode

In order to improve converter light-load efficiency, IC switches to PFM operation at light load.

- Reg0x16<1>=1 (EN_PFM_CHG), PFM is enabled in charging mode. Otherwise FPWM mode is selected, In most case FPWM mode is not suggested due to possible negative inductor current which may cause backfill and high voltage stress at VBUS input.
- Reg0x16<0>=1 (EN_PFM_OTG), PFM is enabled in OTG mode. Otherwise FPWM mode is selected.

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9.12 Protection

SC8808 supports full protections including input overvoltage protection, overcurrent protection, battery overvoltage protection, battery short and over temperature protection.

9.12.1 VBUS OVP

In charging mode, once the voltage at VBUS pin is detected higher than input overvoltage threshold (82V typ), DCDC stop switching at once, discharging current is pulled down automatically until OVP condition disappear. STAT pin is 0.5Hz blanking to indicate fault, and VBUS_PG_STAT is set to 0, VBUS_OVP_STAT is set to 1. After VBUS OVP disappears，IC restart poor source qualification.

9.12.2 Cycle by Cycle Peak/Valley OCP (IL_MAX_CLP)

SC8808 provides cycle-by-cycle current limit to protect against overcurrent and short circuit conditions for charging and discharging mode. In buck mode, if the valley current detected by CSN-CSP in low-side buck exceed the current limit, the buck low side MOSFET is turned-on until the current falls down to current limit. In boost mode, If the peak current detected by CSP-CSN in low-side boost switch exceed the current limit, the boost switch is turned off for the rest of switching cycle. The current limit is set by internal register(Reg0x12<1:0>), 25A default for 3mΩ sense resistor.

9.12.3 BAT OVP

There are two kind of battery overvoltage protection. VBAT absolute overvoltage protection and VBAT relative overvoltage protection.

1. VBAT absolute overvoltage protection:
   When battery voltage VBAT pin >82V, VBAT absolute over-voltage protection is triggered no matter in charging mode or OTG mode, DCDC stop switching at once, battery discharging current is pulled down automatically till OVP condition disappear
2. VBAT relative overvoltage protection:
   a) In charging mode, when $V_{BAT_FB} > V_{BAT_OVP}$ (104%*ChargeVoltage), the charger stops switching in charging mode. The VBAT_OVP_STAT is set to 1 inform the host. When $V_{BAT_FB} < V_{BAT_OVP}$(102%*ChargeVoltage), the charger recovers switching. VBAT internal discharging current is also turned on VBAT pin automatically under VBAT OVP condition, and is turned off when VBAT OVP fault is removed.
   b) In OTG mode, when $V_{BAT_FB} > V_{BAT_OVP}$ (104%*ChargeVoltage) occurs，OTG DCDC switching can be disabled when Reg0x17<0>is set to 0.

9.12.4 Battery Short

If voltage at VBAT pin falls below 3V during charging, IC will regulate inductor valley current and clamp to 2A to limit charge current. When VBAT<0.7V, Q4 is turned off to avoid inductor current continuous increasing due to low battery voltage.

9.12.5 OTG OVP

If OTG voltage is set by internal register, If OTG output voltage > V_{OTG_OVP} (125%*VOTG) in OTG mode, the converter stops switching at once and sets VOTG_OVP_STAT bit to 1. When OTG output voltage falls below the threshold (120%*VOTG), the status bit is cleared and converter resumes switching.

If OTG voltage is set by external VBUS_FB pin, No OTG OVP protection is applied.

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9.12.6 OTG SHORT

If V_{BUS} < V_{OTG_SHORT}(3.2V) is detected in OTG mode, the converter enters into hiccup mode: it stops switching for 500ms and then restarts switching again. After 4ms switching blanking timer expire, if V_{BUS} < V_{OTG_SHORT} is still detected, and OTG_UVP_STAT is set to 1 to report the output short fault, the IC stops switching for 500ms, and then retries again.

When V_{BUS} > V_{OTG_SHORT}, the fault is removed, and the status bit is read cleared.

9.12.7 Thermal Shutdown

Whenever the junction temperature exceeds the 150°C, SC8808 stops switching and stays off until the junction temperature falls below 130°C. During thermal shut down, VCC LDO is off, IC is reset. When the temperature falls below 130°C, SC8808 restarts with soft start.

9.13 I2C Interface

9.13.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x6C (8-bit address is 0xD8 for write command, 0xD9 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

9.13.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

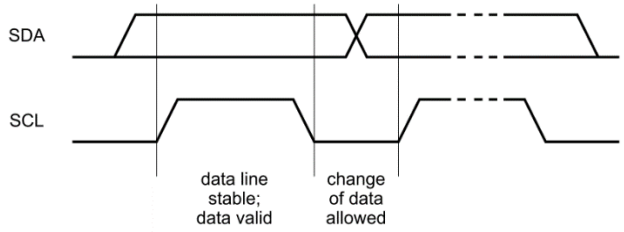

Figure 1 Bit transfer on the I2C bus

9.13.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

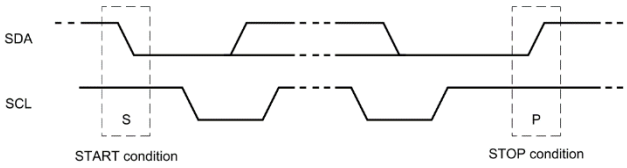

Figure 1 START and STOP conditions

9.13.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal

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interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

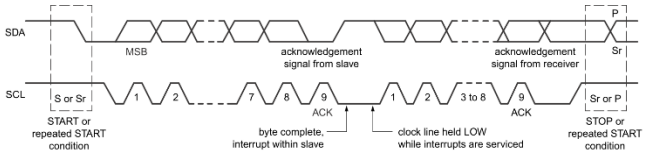

Figure 2 Data transfer on the I2C bus

9.13.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

9.13.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

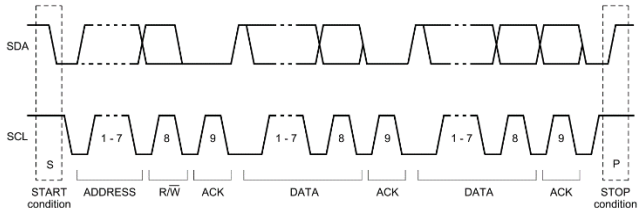

Figure 3 A complete data transfer

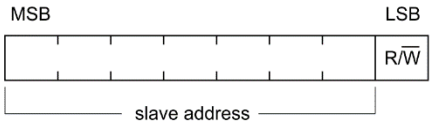

Figure 4 The first byte after the START procedure

9.13.1.6 Single Read and Write

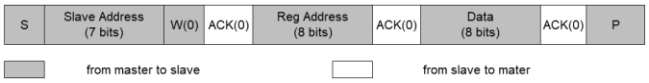

Figure 5 Single Wite

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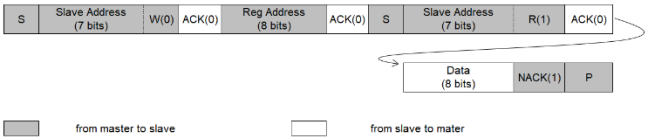

Figure 6 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.13.1.7 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

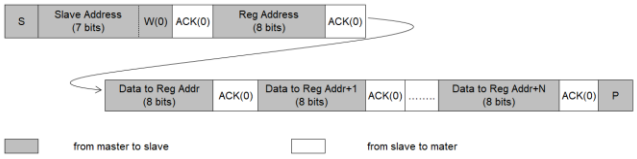

Figure 7 Multi-Write

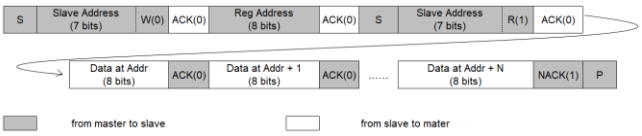

Figure 8 Multi-Read

10 Register Map (address: 0x6C)

ADDR	Name	R/W	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00H	CC CHARGE CURRENT	R/W	10111110	CC CHARGE CURRENT							
0x01H	PRE-CHARGE CURRENT	R/W	x0010000	RESERVED	PRE-CHARGE CURRENT						
0x02H	TERMINATION CURRENT	R/W	xx000110	RESERVED		TERMINATION CURRENT					
0x03H	CHARGE VOLTAGE REF	R/W	xxx10000	RESERVED			CHARGE VOLTAGE REF				
0x04H	OTG VOLTAGE	R/W	01111011	OTG VOLTAGE							
0x05H		R/W	xxxxx000	RESERVED					OTG VOLTAGE		
0x06H	OTG CURRENT	R/W	x0000111	RESERVED	OTG CURRENT						
0x07H	IINDPM CURRENT	R/W	x1111111	RESERVED	IINDPM CURRENT						
0x08H	VINDPM VOLTAGE REF	R/W	00000000	VINDPM VOLTAGE REF							
0x09H		R/W	xxxxxx10	RESERVED					VINDPM VOLTAGE REF		
0x0FH	VOTG OFFSET	R/W	00000000	RESERVED				OTG VOLTAGE OFFSET			
0x10H	CHARGE OPTION0	R/W	11110100	VBAT_LOWV_SEL		VRECH_VTH_SEL		VFLOAT_SEL(2BIT)		DIS_DCDC	REG_RESET
0x11H	CHARGE OPTION1	R/W	11011001	IBUS_SET_SEL	IBAT_SET_SEL	EN_DITHEING	EN_TERM	EN_PRECHARGE_CHARGE	EN_FLOAT_CHARGING	DIS_POOR_SRC_DET	EN_LPM
0x12H	CHARGE OPTION2	R/W	00001100	IBUS_MON_RATIO	RESERVED	IBAT_MON_RATIO	RESERVED	EN_IBUS_MON	EN_IBAT_MON	IL_AVG	
0x13H	MPPT CONTROL0	R/W	00000001	EN_MPPT	MPPT_INITIAL_DELAY	MPPT_FULLSCAN_TIMER		MPPT_PERTUBE_TIMER		MPPT_STEP_SEL	
0x14H	MPPT CONTROL1	R/W	00001110	MPP_ADC_AVG_SEL		MPPSEL	MPPT_POWER_DET_DLY		RESERVED	MPPT_LOW_CLAMP	
0x40H	MPPT CONTROL2	R/W	11110000	RESERVED						MPPT_PETURBTIMER_SCALE	MPPT FULLSCAN
0x15H	CHARGE OPTION3	R/W	00011010	RESERVED			EN_PRE-CHG_TMR	EN_FAST-CHG_TMR	PRE-CHARGETMR_SEL	FASTCHARGETMR_SEL	
0x16H	CHARGE OPTION4	R/W	01101011	EN_OTG	OTG_FB_SEL	LOOP_ENTER_DLY_SEL		OTGSR_SEL		EN_PFM_CHG	EN_PFM_OTG
0x17H	CHARGE OPTION5	R/W	00010101	RESERVED			ADC_FREQ_SEL	EN_VBUS_PD	EN_AUTO_IBAT_DCHG	EN__FORCE_IBAT_DCHG	EN_OTG_DCDC_BATOV
0x18H	JEITA CONTROL0	R/W	01011011	JEITAHIGHTEMP_(TWARM–THOT) VOLTAGESETTING			JEITAHIGHTEMP_(TWARM–THOT) CURRENTSETTING		JEITALOWTEMP_(TCOLD–TCOOL) CURRENTSETTING		EN_JEITA
0x19H	JEITA CONTROL1	R/W	01010100	JEITAT2_SEL		JEITAT3_SEL		OTG_HOT_SEL		OTGCOLD_SEL	TS_DIS
0x1AH	ADC CONTROL	R/W	00000000	ADC_EN	ADC_MODE	ADC_START	EN_ADC_IBUS	EN_ADC_IBAT	EN_ADC_VBUS	EN_ADC_VBAT	EN_ADC_TS
0x20H	CHARGER STATUS0	R	00000000	IBUSREG_STAT	VINDPM_STAT	POWERGOOD STAT	VBUS_PRESE	VBUSOV_STAT	VBATOV_STAT	IL_MAX_CLP_STAT	RESERVED
0x21H	CHARGER STATUS1	R	00000000	CHG_STAT			FASTCHG_TMR_STAT	PRECHG_TMR_STAT	TRICKLE_TMR_STAT	OTG_OVP_STAT	OTG_UVP_STAT

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0x22H	CHARGER STATUS2	R	00000000	TS_COLD_STAT	TS_COOL_STAT	TS_WARM_STAT	TS_HOT_STAT	MPPT_STAT		AUTO_RERVESE_STAT	SYNC_STAT
ADDR	**Name**	**R/W**	**Default**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
0x30H	ADC IBUS	R	00000000	ADC_IBUS							
0x31H		R	00000000	RESERVED						ADC_IBUS	
0x32H	ADC IOTG	R	00000000	ADC_IOTG							
0x33H		R	00000000	RESERVED						ADC_IOTG	
0x34H	ADC ICHG	R	00000000	ADC_ICHG							
0x35H		R	00000000	RESERVED						ADC_ICHG	
0x36H	ADC IDCHG	R	00000000	ADC_IDCHG							
0x37H		R	00000000	RESERVED						ADC_IDCHG	
0x38H	ADC VBUS	R	00000000	ADC_VBUS							
0x39H		R	00000000	RESERVED						ADC_VBUS	
0x3AH	ADC VBAT	R	00000000	ADC_VBAT							
0x3BH		R	00000000	RESERVED						ADC_VBAT	
0x3CH	ADC VNTC	R	00000000	ADC_VNTC							
0x3DH		R	00000000	RESERVED						ADC_VNTC	

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10.1 REG 0x00H: CC CHARGE CURRENT

Bit	Bit Name	Type	Default	Description
7:0	CC CHARGE CURRENT	R/W	10111110	Range: 1000mA – 20000mA for 5mΩ sense resistor Default: 20000mA <100mA: gain> <1000mA: offset>

10.2 REG 0x01H: PRE-CHARGE CURRENT

Bit	Bit Name	Type	Default	Description
7	Reserved	R	0	Reserved
6:0	Pre-Charge Current	R/W	0010000	Range: 400mA – 10000mA for 5mΩ sense resistor Default: 2000mA <100mA: gain> <400mA: offset>

10.3 REG 0x02H: TERMINATION CURRENT

Bit	Bit Name	Type	Default	Description
7:6	Reserved	R	00	Reserved
5:0	Termination Current	R/W	000110	Range:400mA–6700mA for 5mΩ sense resistor Default:1000mA <100mA: gain> <400mA: offset>

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10.4 REG 0x03H: CHARGE VOLTAGE REF

Bit	Bit Name	Type	Default	Description
7:5	Reserved	R	000	Reserved
4:0	Charge Voltage	R/W	10000	Range: 1504mV-1566mV Default: 1536mV <2mV: gain> <1504mV: offset>

10.5 REG 0x04H: OTG VOLTAGE

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	OTG Voltage	R/W	000-11011111	Default: 5000mV Range1: 5000mV–21000mV (when bit10 = 0) <20mV: gain1> <540mV: offset1> Range2: 21050mV–48000mV (when bit10 = 1) <50mV: gain2> <21050mV: offset2>

10.6 REG 0x06H: OTG CURRENT

Bit	Bit Name	Type	Default	Description
7	Reserved	R	0	Reserved
6:0	OTG Current	R/W	0000111	Range:2375mA–50000mA for 2mΩ sense resistor Default: 5000mA <375mA: gain>

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				<2375mA: offset>

10.7 REG 0x07H: IINDPM CURRENT

Bit	Bit Name	Type	Default	Description
7	Reserved	R	0	Reserved
6:0	INDPM Current	R/W	1111111	Range:2375mA–50000mA for 2mΩ sense resistor Default:50000mA <375mA: gain> <2375mA: offset>

10.8 REG 0x08H: VINDPM VOLTAGE REF

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	VINDPM Voltage	R/W	010-00000000	Range:100mV–1123mV Default:612mV <1mV: gain> <100mV: offset>

10.9 REG 0x0FH: VOTG OFFSET

Bit	Bit Name	Type	Default	Description
7:4	Reserved	R	0000	Reserved
3:0	OTG_VOLTAGE_ OFFSET	R/W	0000	OTG_VOLTAGE_OFFSET: 0000: 0mV(default)

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				0001: 50mV 0010: 100mV 0011: 150mV 0100: 200mV 0101: 250mV 0110: 300mV 0111: 350mV 1000: 400mV 1001: -50mV 1010: -100mV 1011: -150mV 1100: -200mV 1101: -250mV 1110: -300mV 1111: -350mV Note: extra offset for OTG voltage offset2(21050mV) in Range2: 21050mV–48000mV (when 0x04[bit10] = 1)

10.10 REG 0x10H: CHARGE OPTION0

Bit	Bit Name	Type	Default	Description
7:6	VBAT_LOWV_SEL	R/W	11	VBAT_LOWV_SEL(2bit) 00: 30% 01: 55% 10: 66.7% 11: 71.4% (Default) Note: Pre-charge to CC charge threshold
5:4	Vrech_Vth_SEL	R/W	11	Vrech_Vth_SEL(2bit) 00: 93%*ChargeVoltage 01: 94.5%*ChargeVoltage 10: 95%*ChargeVoltage 11: 97.5%*ChargeVoltage(default)

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				Note: Recharge threshold, VBAT falling, below VBAT_REG
3:2	Vfloat_SEL	R/W	01	Vfloat_SEL(2bit) 00: 90.5%*ChargeVoltage 01: 93%*ChargeVoltage(default) 10: 94.5%*ChargeVoltage 11: 95%*ChargeVoltage Note: Float charge threshold
1	DIS_DCDC	R/W	0	DIS_DCDC 0: enable DCDC（Default） 1: disable DCDC
0	Reg_Reset	R/W	0	Reg_Reset 0: Normal (default) 1: Reset registers to default values and reset timer

10.11 REG 0x11H: CHARGE OPTION1

Bit	Bit Name	Type	Default	Description
7	IBUS_SET_SEL	R/W	1	IBUS_SET_SEL 0: set by IINDPM Reg Or OTG current 1: SET by IBUS_SET pin(default)
6	IBAT_SET_SEL	R/W	1	IBAT_SET_SEL 0: set by IBAT Reg 1: SET by IBAT_SET pin(default)
5	EN_Ditheing	R/W	0	EN_Ditheing 0: disable(default) 1: enable Note: frequency dithering
4	EN_TERM	R/W	1	EN_TERM 0: Disable termination 1: Enable termination(default)

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3	EN_precharge_charge	R/W	1	EN_precharge_charge 0: disable 1: enable(default) If this bit is set to 0, pre-charge phase is disabled.
2	EN_Float_Charging	R/W	0	EN_Float_Charging 0: disable(default) 1: enable
1	DIS_POOR_SRC_DET	R	0	DIS_POOR_SRC_DET 0: enable poor source detection (Default) 1: disable poor source detection
0	EN_LPM	R/W	1	EN_LPM 0: disable Low power mode 1: enable Low power mode (default) Note: Low power mode is only valid for battery only mode

10.12 REG 0x12H: CHARGE OPTION2

Bit	Bit Name	Type	Default	Description
7	IBUS_MON_RATIO:	R/W	0	IBUS_MON_RATIO: 0: 1x (default) 1: 2x:
6	Reserved	R	0	Reserved
5	IBAT_MON_RATIO:	R/W	0	IBAT_MON_RATIO: 0: 1x (default) 1: 2x
4	Reserved	R	0	Reserved
3	EN_IBUS_MON	R/W	1	EN_IBUS_MON 0: disable

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				1: enable（default） Note: IBUS current monitoring function
2	EN_IBAT_MON	R/W	1	EN_IBAT_MON 0: disable 1: enable（default） Note: IBAT current monitoring function
1:0	IL_AVG	R/W	00	IL_AVG 00: 25A(default) 01: 15A 10: 40A 11: 40A note: Cycle by cycle peak current limit

10.13 REG 0x13H: MPPT CONTROL0

Bit	Bit Name	Type	Default	Description
7	EN_MPPT	R/W	0	EN_MPPT 0: disable(default) 1: enable
6	MPPT_Initial_Delay	R/W	0	MPPT_Initial_Delay 0: 500ms(default) 1: 2s Note: the timer of initial the starting point of MPPT algorithm
5:4	MPPT_Full scan_Timer	R/W	0	MPPT_Full scan_Timer 00: 5min(default) 01: 10min 10: 15min 11: disable Note: if full scan timer expires, new full scan phase restarts. If full scan is not used, set to 11’b to disable this function.
3:2	MPPT_Pertube_Timer	R/W	0	MPPT_Pertube_Timer

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				00: 0.0625s(default) 01: 0.125s 10: 1.25s 11: disable Note: After charger find the MPP, the bit is used to set timer interval of P&O cycle.
1:0	MPPT_Step_SEL	R/W	01	MPPT_Step_SEL 00: 1x Step 01: 2x Step(default) 10: 4x Step 11: 8x Step Note: MPPT full scan sweep and P&O step for VBUS voltage

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10.14 REG 0x14H: MPPT CONTROL1

Bit	Bit Name	Type	Default	Description
7:6	MPP_ADC_AVG_SEL	R	00	MPP_ADC_AVG_SEL 00: disable（Default） 01: 4x times 10: 8x times 11: 16x times Note: Digital average filter can be adopted to ensure ADC sampling data stable, but larger times requires longer response time for MPPT algorithm.
5	MPP SEL	R	0	MPP_SEL 0: MPP is set by IBAT result (Default) 1: MPP is set by VBUS*IBUS result MPPT algorithm is decided by IBAT result, which means MPP is depending on charger's output power. MPPT algorithm is decided by VBUS*IBUS result, which means MPP is depending on charger's input power
4:3	MPPT_Power_DET_DLY	R/W	01	MPPT_Power_DET_DLY 00: 2ms 01: 5ms(default) 10: 10ms 11: 20ms Note: Full scan MPPT phase，time delay of find the maximum power point by decreasing VINDPM step by step
2	Low_Current_Threshlod Trigger_Full_SCAN	R/W	1	Low_Current_Threshlod Trigger_Full_SCAN 0: 40mA 1: 80mA (default) Reg0x40<0>=0, charger detects IBAT charging current to decide whether to initial a new full san sweep. If IBAT is lower than 40mA or 80mA, full scan sweep is triggered.
1:0	MPPT_LOW_CLAMP	R/W	10	MPPT_LOW_CLAMP 00: Vindpm_Ref_Min=0.407V 01: Vindpm_Ref_Min=0.253V

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				10: Vindpm_Ref_Min=0.614V（Default） 11: Vindpm_Ref_Min=0.712V Note: while full scan sweep is initialed and MPPT algorithm seeks the maximum power point by sweep Vindpm_Ref step by step until the value of low clamp. The low clamp must be lower than minimum PV output voltage under all condition.

10.15 REG 0x40H: MPPT CONTROL2

Bit	Bit Name	Type	Default	Description
7:2	Reserved	R	3C	Reserved
1	MPPT PETURB TIMER SCALE	R/W	0	MPPT_PETURB_TIMER SCALE 0: 1x (default) 1: 8x This bit is used to enlarge perturb timer by 8 times.
0	Low_Current_Trigger_Full_Scan_DIS	R/W	0	Low_Current_Trigger_Full_Scan_DIS 0: Enabled (default) 1: Disabled

10.16 REG 0x15H: CHARGE OPTION3

Bit	Bit Name	Type	Default	Description
7:5	Reserved	R	0	Reserved
4	EN_ pre-chg_TMR	R/W	1	Enable pre-charge timer 0: Disabled 1: Enabled (default)
3	EN_ Fast-chg_TMR	R/W	1	Enable fast charge timer 0: Disabled 1: Enabled (default)
2	Pre-charge TMR_SEL	R/W	0	Precharge timer setting

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				0: 2h(default) 1: 1h
1:0	Fast charge TMR_SEL	R/W	10	Fast charge timer setting 00: 5 hrs 01: 8 hrs 10: 12 hrs (default) 11: 24 hrs

10.17 REG 0x16H: CHARGE OPTION4

Bit	Bit Name	Type	Default	Description
7	EN_OTG	R/W	0	EN_OTG 0: charging mode (default) 1: OTG mode
6	OTG_FB_SEL	R/W	1	OTG_FB_SEL 0: OTG voltage is set by internal register 1: OTG voltage is set by external VBUS_FB pin in OTG mode(default)
5:4	loop_enter_dly_sel	R/W	10	loop_enter_dly_sel: 00: 0 01: 500μs 10: 1ms（default） 11: 2ms
3:2	OTG SR_SEL	R/W	10	OTG slew rate selection: 00: 0.05mV/us 01: 0.2mV/us 10: 0.5mV/us(default) 11: 1mV/us
1	EN_PFM_CHG	R/W	1	EN_PFM_CHG 0: disable PFM in forward mode 1: enable PFM in forward mode(default)

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0	EN_PFM_OTG	R/W	1	EN_PFM_OTG 0: disable PFM in OTG mode 1: enable PFM in OTG mode(default)

10.18 REG 0x17H: CHARGE OPTION5

Bit	Bit Name	Type	Default	Description
7:5	Reserved	R	0	Reserved
4	adc_freq_sel	R	1	adc_freq_sel: 0:10k 1:5k（default）
3	EN_VBUS_PD	R/W	0	EN_VBUS_PD 0: Disable(default) 1: Enable pull-down from VBUS
2	EN_AUTO_IBAT_DCHG	R/W	1	EN_AUTO_IBAT_DCHG 0: The charger will NOT apply a discharging current on BAT during battery OVP triggered 1: The charger will apply a discharging current on BAT during battery OVP triggered (default)
1	EN__FORCE_IBAT_DCHG	R/W	0	EN__FORCE_IBAT_DCHG 0: IDEL (default) 1: Force the charger to apply a discharging current on VBAT
0	EN_OTG_DCDC_BATOV	R/W	1	EN_OTG_DCDC_BATOV 0: disable DCDC when BATOVP occurs 1: enable DCDC when BATOVP occurs (default)

10.19 REG 0x18H: JEITA CONTROL0

Bit	Bit Name	Type	Default	Description

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7:5	JEITA High Temp. (TWARM – THOT) Voltage Setting	R/W	010	JEITA High Temp. (TWARM – THOT) Voltage Setting 000: Charge Suspend 001: Set VREG to 97.6%*CV 010: Set VREG to 95.2%*CV（default） 011: Set VREG to 93%*CV 100~111: VREG unchanged
4:3	JEITA High Temp. (TWARM – THOT) Current Setting	R/W	11	JEITA High Temp. (TWARM – THOT) Current Setting 00: Charge Suspend 01: Set ICHG to 20%* ICHG 10: Set ICHG to 40%* ICHG 11: ICHG unchanged (default)
2:1	JEITA Low Temp. (TCOLD – TCOOL) Current Setting	R/W	01	JEITA Low Temp. (TCOLD – TCOOL) Current Setting 00: Charge Suspend 01: Set ICHG to 20%* ICHG (default) 10: Set ICHG to 40%* ICHG 11: ICHG unchanged
0	EN_JEITA	R/W	1	EN_JEITA 0: Jeita is disabled，warm and cool is not valid for protection 1: Jeita is enabled (default)

10.20 REG 0x19H: JEITA CONTROL1

Bit	Bit Name	Type	Default	Description
7:6	JEITA T2_SEL	R/W	01	JEITA T2 comparator voltage rising thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 00: 71.1% (5C) 01: 68.4% (default) (10C) 10: 65.5% (15C) 11: 62.4% (20C)

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5:4	JEITA T3_SEL	R/W	01	JEITA T3 comparator voltage falling thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ. 00: 48.4% (40C) 01: 44.8% (default) (45C) 10: 41.2% (50C) 11: 37.7% (55C)
3:2	OTG _HOT_SEL	R/W	01	OTG Mode TS HOT Temp Threshold 00: 37.7% (55°C) 01: 60°C (default) 10: 65°C 11: Disable
1	OTG COLD_SEL	R/W	0	OTG Mode TS COLD Temp Threshold 0: -10°C (default) 1: -20°C
0	TS_DIS	R/W	0	Ignore the TS feedback, the charger will consider the TS is always good to allow charging and OTG modes, all the four TS status bits will always stay at 0000 to report the normal condition. 0: Not ignore (Default) 1: Ignore

10.21 REG 0x1AH: ADC CONTROL

Bit	Bit Name	Type	Default	Description
7	ADC_EN	R/W	0	ADC_EN 0: disable （default） 1: enable
6	ADC_MODE	R/W	0	0: Continuous mode （default）

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				1: One_shot mode
5	ADC_START	R/W	0	ADC_START 0: ADC conversion done iN one-shot mode（default） 1: Initial One_shot ADC conversion
4	EN_ADC_IBUS	R/W	0	EN_ADC_IBUS 0: disable(default) 1: enable
3	EN_ADC_IBAT	R/W	0	EN_ADC_IBAT 0: disable(default) 1: enable
2	EN_ADC_VBUS	R/W	0	EN_ADC_VBUS 0: disable(default) 1: enable
1	EN_ADC_VBAT	R/W	0	EN_ADC_VBAT 0: disable(default) 1: enable
0	EN_ADC_TS	R/W	0	EN_ADC_TS 0: disable(default) 1: enable

10.22 REG 0x20H: CHARGER STATUS0

Bit	Bit Name	Type	Default	Description
7	IBUSREG_ STAT	R	0	IBUS regulation status bit: 0: IC is not in IBUS regulation in forward mode or OTG mode 1: IC is in IBUS regulation in forward mode or OTG mode
6	VINDPM_STAT	R	0	Input voltage regulation status bit: 0: IC is not in VINDPM during forward mode 1: IC is in VINDPM during forward mode

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5	Power Good STAT	R	0	Power Good Status 0: Not in power good status 1: Power good
4	VBUS_PRESE	R/W	0	VBUS preset status bit: 0: VBUS is not present 1: VBUS is present
3	VBUSOV_STAT	R	0	VBUSOV_STAT 0: no VBUSOV fault 1: is in VBUSOV fault
2	VBATOV_STAT	R	0	VBATOV_STAT 0: no VBATOV fault 1: is in VBATOV fault
1	IL_MAX_CLP_STAT	R	0	IL_MAX_CLP_STAT 0: Peak/Valley current clamp is not triggered 1: Peak/Valley current clamp is triggered
0	Reserved	R	0	Reserved

10.23 REG 0x21H: CHARGER STATUS1

Bit	Bit Name	Type	Default	Description
7:5	CHG_STAT	R	000	Charge phase status bits: 000: Not Charging 001: Trickle charging 010: Pre-Charge 011: Fast charge (CC mode) 100: Taper Charge (CV mode) 101: Charge Termination Done 110: Float charge 111: Reserved
4	FASTCHG_TMR_STAT	R	0	FASTCHG_TMR_STAT

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				Fast charge timer 0: Normal 1: Safety timer expired
3	PRECHG_TMR_STAT	R	0	PRECHG_TMR_STAT Pre-charge timer 0: Normal 1: Safety timer expired
2	Trickle_TMR_STAT	R	0	Trickle_TMR_STAT Trickle-charge timer 0: Normal 1: Safety timer expired
1	OTG_OVP_STAT	R/W	0	OTG over voltage protection status bit: 0: IC is not in OTG_OVP 1: IC is in OTG_OVP
0	OTG_UVP_STAT	R/W	0	OTG under voltage protection status bit: 0: IC is not in OTG_UVP 1: IC is in OTG_UVP

10.24 REG 0x22H: CHARGER STATUS2

Bit	Bit Name	Type	Default	Description
7	TS_COLD_ STAT	R/W	0	JEITA TS_COLD temp status bit: 0: Battery temperature is not in cold range 1: Battery temperature is in cold range
6	TS_COOL_ STAT	R/W	0	TS_COOL temp status bit: 0: Battery temperature is not in cool range 1: Battery temperature is in cool range
5	TS_WARM_ STAT	R/W	0	TS_WARM temp status bit: 0: Battery temperature is not in warm range 1: Battery temperature is in warm range

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4	TS_HOT_ STAT	R/W	0	TS_HOT temp status bit: 0: Battery temperature is not in hot range 1: Battery temperature is in hot range
3:2	MPPT_STAT	R/W	0	00: MPPT is not enabled 01: MPPT is enabled，but not running 10: MPPT is in progress 11: MPPT is found
1	Auto_Rervese_STAT	R/W	0	Auto_Rervese_STAT 0: not in auto reverse mode 1: in auto reverse mode
0	SYNC_STAT	R/W	0	SYNC_STAT 00: Normal mode 01: Frequency is SYNC with external clock mode

10.25 REG 0x30H: ADC IBUS

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_IBUS	R/W	000-00000000	Range: 0mA – 51187mA Default: 0mA <25: gain> <0: offset>

10.26 REG 0x32H: ADC IOTG

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved

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10:0	ADC_IOTG	R/W	000-00000000	Range: 0mA – 51187mA Default: 0mA <25: gain> <0: offset>

10.27 REG 0x34H: ADC_ICHG

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_ICHG	R/W	000-00000000	Range: 0mA – 20475mA Default: 0mA <10: gain> <0: offset>

10.28 REG 0x36H: ADC_IDCHG

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_IDCHG	R/W	000-00000000	Range: 0mA – 20475mA Default: 0mA <10: gain> <0: offset>

10.29 REG 0x38H: ADC_VBUS

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved

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10:0	ADC_VBUS	R/W	000-00000000	Range: 0mV – 81900mV Default: 0mV <40: gain> <0: offset>

10.30 REG 0x3AH: ADC_VBAT

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_VBAT	R/W	000-00000000	Range: 0mV – 81900mV Default: 0mV <40: gain> <0: offset>

10.31 REG 0x3CH: ADC_VNTC

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_VNTC	R/W	000-00000000	Range: 0% – 99.9% Default: 0% <0.05%: gain> <0: offset>

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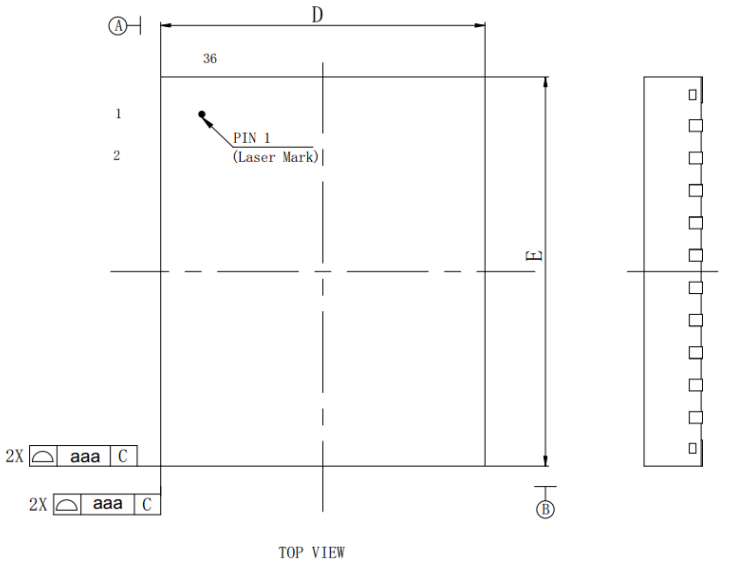
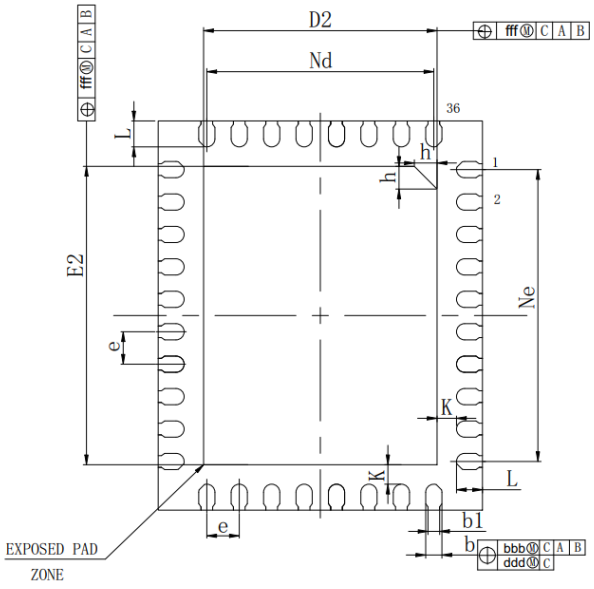
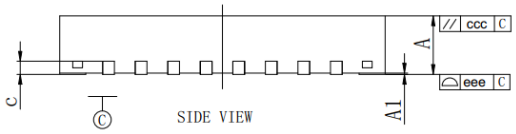
MECHANICAL DATA

QFN 5x6-36







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	4.90	5.00	5.10
E	5.90	6.00	6.10
e		0.50BSC	
D2	3.50	3.60	3.70
E2	4.50	4.60	4.70
Nd		3.50BSC	
Ne		4.50BSC	
L	0.35	0.40	0.45
K		0.30REF	
h	0.30	0.35	0.40
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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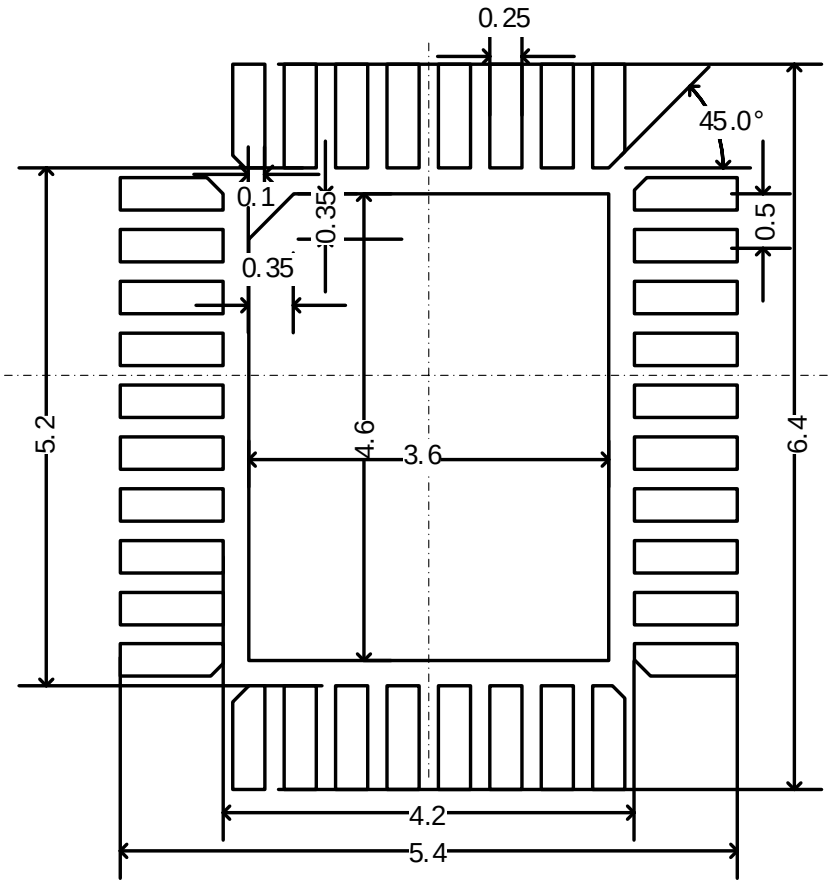
RECOMMENDED FOOTPRINT

Top View



NOTES:

A. All linear dimensions are in millimeters

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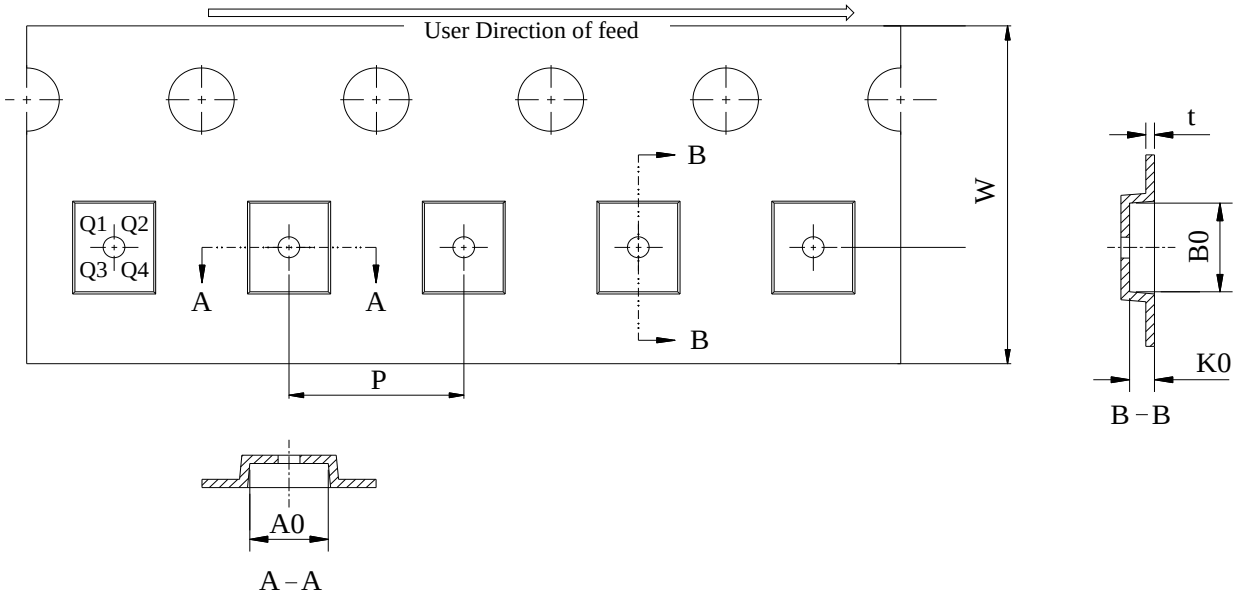
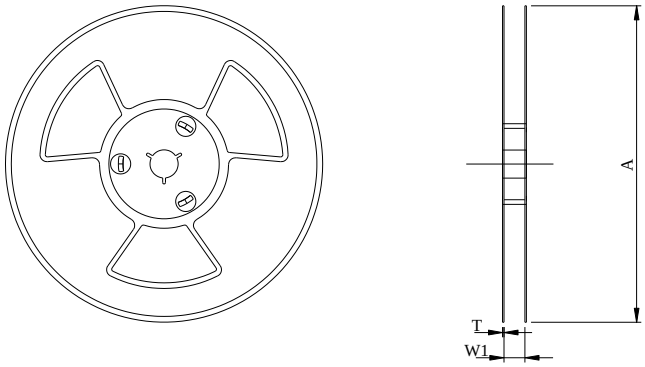
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00+0.20/-0.10	8.00±0.10	5.30±0.10	6.30±0.10	1.20±0.10	0.30±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	329±1	12.8±1	2.0±0.3

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