

SC77208CQ Dual Channel 8-mΩ Smart High Side Driver with Advanced Protections and Diagnostics

1 Descriptions

The SC77208CQ is a fully-protected dual channel smart high side driver qualified in automotive grade. Full diagnostics and high accuracy current sense of each channel enable intelligent control of the load even in harsh conditions. It integrates two 8mΩ MOSFETs in a compact package size with advanced protections of overload protection, dynamic thermal swing shutdown, absolute thermal shutdown. It features intelligent restart control mode in fault events. A multiplexed pin delivers proportional current sense signals or fault indications in both Active Mode and Standby Mode.

2 Features

- Qualified for Automotive Applications.
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C4B
- Dual Channel 8mΩ Smart High-Side Driver with Full Diagnostics.
 - 14-pins, Intelligent Restart Control Mode, Channel Fault Diagnosis, Proportional Load Current Sense Output
- Operating Junction Temperature: -40 to 150°C.
- Wide Operating Voltage from 4 to 28V with Load Dump Withstand Voltage up to 36V.
- Ultra Low Sleep Mode Current < 0.5 μA.
- Input Control, 3.3V and 5V Logic Compatible.
- High Accuracy Current Sense:
 - ±9% @ 10A
 - ±9% @ 2.8A
 - ±18% @ 1A
 - ±35% @ 0.1A
 - ±60% @ 0.02A
- Electrical Transient Disturbance Immunity Certification of ISO7637-2 and ISO16750-2

- Advanced Protections:
 - Short to GND and Overload Protection with Intelligent Restart Control mode
 - Dynamic Thermal Swing Shutdown and Absolute Thermal Shutdown
 - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
 - Loss of GND and Loss of Battery Protection
 - Under Voltage Lockout (UVLO) Protection
- Diagnostics:
 - Overload and Short to Ground Detection in Active Mode
 - Open Load and Short to Battery Detection in Standby Mode

3 Applications

- High Side Power Driver for Sub-module
- Power Switch for Automotive Lamp
- High Side Relays and Solenoids
- General Resistive, Inductive and Capacitive Loads

4 Device Information

ORDER NUMBER	DESCRIPTION	PACKAGE	BODY SIZE
SC77208CQSHER	<ul style="list-style-type: none"> Intelligent Restart Control Mode Channel Fault Diagnosis Output Proportional Load Current Sense Output 	eSSOP-14	5.2mm x 3.9mm x 1.4mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
1.0	2025.05.07		Initial released
1.0.1	2025.07.17	6~9	8.5 Electrical Characteristics 1. "Overload Detection Current@-40°C and 25°C" Updated (Min./Typ./Max.:55A/75A/95A → Min./Typ./Max.:65A/80A/95A) 2. "Overload Detection Current@150°C" Updated (Min./Typ./Max.:45A/65A/85A → Min./Typ./Max.:55A/70A/85A) 3. "Overload Detection Current at High VDS" Updated (Typ.:30A → Typ.:40A) 4. "Overload Detection Current Jump Start Condition" Updated (Typ.:30A → Typ.:40A)
1.0.2	2025.07.29	6~9	8.5 Electrical Characteristics 1. "Accuracy of Current Sense (ICS × KSNS – IOUT) /IOUT × 100" Updated IOUT=0.1A (Min. /Max.: -30%/+30% → Min./Max.: -35%/+35%) IOUT=1A (Min. /Max.: -13.5%/+13.5% → Min./Max.: -18%/+18%)
1.0.3	2025.08.07	6~9	8.5 Electrical Characteristics 1. "Overload Detection Current@-40°C" Updated (Max.:95A → Max.:105A) 2. "Overload Detection Current@150°C" Updated (Min./Typ./Max.:55A/70A/85A → Min./Typ./Max.:60A/75A/90A) 3. "Accuracy of Current Sense (ICS × KSNS – IOUT) /IOUT × 100" Updated IOUT=2.8A (Min. /Max.: -8%/+8% → Min./Max.: -9%/+9%) IOUT=5.5A (Min. /Max.: -8%/+8% → Min./Max.: -9%/+9%) IOUT=10A (Min. /Max.: -8%/+8% → Min./Max.: -9%/+9%) 4. "Output Voltage Drop Limitation at Small Load Currents" Updated (Min.:1mV → Min.:0.3mV) 5. "Fault High Voltage of IS @5V ≤ VS < 7V" Updated (Min.:4.3V → Min.:4.2V)
1.04	2026.3	Update	1. Electrical Characteristics "Power Supply Minimum Operating Voltage" Updated (Min.:2.0V → Max.:3.1V) 2. Update the function description in the datasheet

6 Typical Application Circuit

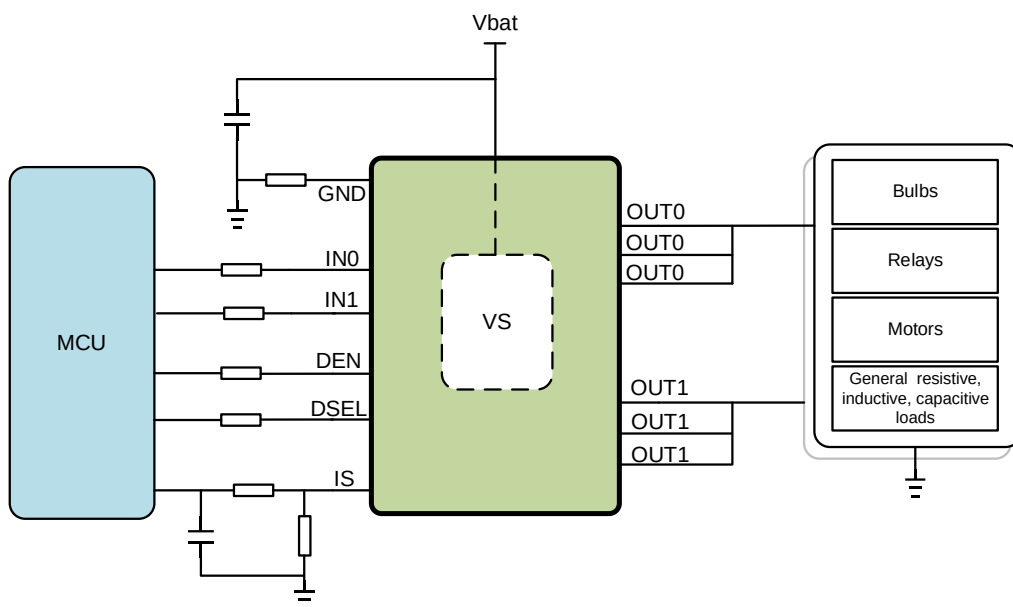


Figure 6-1. Typical Application Circuit

7 Terminal Configuration and Functions

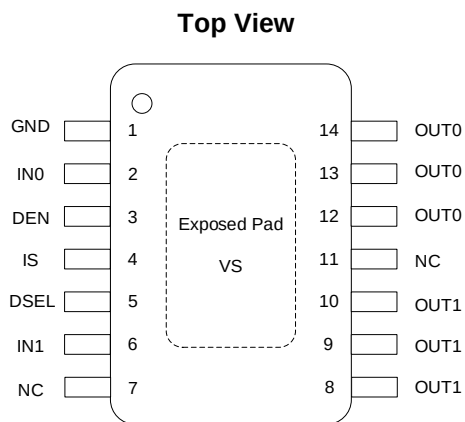


Figure 7-1. Configuration Diagram (Top View)

Table 7-1 Suggested Connections For Unused And Not Connected Pins

NUMBER	TERMINAL NAME	I/O	DESCRIPTION
1	GND	-	Ground connection.
2	IN0	I	Input pin of Channel 0. Active high to turn on Channel 0. If not used: connect to GND pin or to module ground with resistor $R_{IN} = 4.7 \text{ k}\Omega$.
3	DEN	I	Diagnosis enable pin. Active high. If not used: connect to GND pin or to module ground with resistor $R_{DEN} = 4.7 \text{ k}\Omega$.

4	IS	O	Multiplexed sense output. It delivers proportional current sense signals. Besides, fault indications are reported in Active Mode and Standby Mode. If not used: left open.
5	DSEL	I	Diagnosis selection pin. Active high to select Channel 1 to perform diagnosis, low to select Channel 0 to. If not used: connect with a 10kΩ resistor either to GND pin or to module ground.
6	IN1	-	Input pin of Channel 1. Active high to turn on Channel 1. If not used: connect to GND pin or to module ground with resistor $R_{IN} = 4.7\text{ k}\Omega$.
7	NC	-	Not connected.
8	OUT1	O	Output of Channel 1.
9	OUT1	O	Output of Channel 1.
10	OUT1	O	Output of Channel 1.
11	NC	-	Not connected.
12	OUT0	O	Output of Channel 0.
13	OUT0	O	Output of Channel 0.
14	OUT0	O	Output of Channel 0.
Exposed Pad	VS	I	Power supply connection.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	Unit
Voltage Range at Terminals ⁽²⁾	Power Supply Voltage ⁽³⁾	-0.3	36	V
	Reverse Polarity Voltage ⁽⁴⁾	-16		V
	Supply Voltage for Short Circuit Protection		18	V
	Voltage on INx, DEN, DSEL Pins	-0.3	7	V
	Voltage on IS Pin	-2.7	7	V
Current Range at Terminals ⁽²⁾	DC Current on OUTx Pins ⁽⁵⁾		Internally limited	A
	Current on GND Pin	-50 -250 ⁽⁵⁾	50	mA
	Current on INx, DEN, DSEL	-20	20	mA
	Current on IS Pin	-25	30	mA
f _{IN,MAX}	PWM Frequency on INx Pins		2	kHz
T _A	Operating Ambient Temperature Range	-40	125	°C
T _J	Operating Junction Temperature Range	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C
E _{AS}	Inductive Load Switch-off Energy Dissipation, Single Pulse ⁽⁶⁾		65	mJ

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Supply voltage to withstand load dump test for 400ms, according to ISO 16750-2:2010 load dump Test B.
- (4) Reverse polarity condition: t < 60s, reverse current < I_{L,REV}, GND pin 47Ω resistor.
- (5) For limited time range: t < 120s.
- (6) Test condition: VS = 28 V, IL = 2*I_{L,NOM}, T_J = 150°C. FR4 2s2p board, 2 × 70 μm Cu, 2 × 35 μm Cu. 600 mm² thermal pad copper area.

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human Body Model (HBM) ESD Stress Voltage ⁽²⁾	All Pins	-4	4	kV
	Charged Device Model (CDM) ESD Stress Voltage ⁽³⁾	All Pins	-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per AEC-Q100-002. The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
- (3) Level listed above is the passing level per AEC-Q100-011.

8.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V _S	Voltage on VS pin	5		28	V
V _{IH}	Input Logic High on INx, DEN, DSEL Pins	2.1		5.5	V
V _{IL}	Input Logic Low on INx, DEN, DSEL Pins	0		0.8	V
I _{L,NOM}	Nominal DC Load Current		10		A
T _A	Operating Ambient Temperature	-40		125	°C
T _J	Operating Junction Temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		eSSOP-14	UNIT
R _{ΘJA}	Junction to ambient thermal resistance ⁽²⁾	33.3	°C/W
R _{ΘJC(top)}	Junction to case(top) thermal resistance	24.3	°C/W
R _{ΘJC(bottom)}	Junction to Case(Bottom) Thermal Resistance	1.5	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	9.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	3.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	9.3	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated

8.5 Electrical Characteristics

-40°C < T_J < 150°C and 5V < V_S < 28V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY VOLTAGE						
V _{S,NOM}	Normal Operating Voltage		5	13.5	28	V
V _{S,EXT}	Extended Operating Voltage	R _{on} and switching characteristics may vary compared to those in V _{S,NOM} , but protection functions are still operative.	3.1		5	V
V _{S,UVR}	Undervoltage Restart	V _S Rising threshold to exit undervoltage, V _{INx} = 5V	3.1	3.4	4.1	V
V _{S,UVF}	Undervoltage Shutdown	V _S Falling threshold to enter undervoltage, V _{INx} = 5V	2.7	2.9	3.1	V
V _{S,UVhys}	Undervoltage Shutdown Hysteresis	V _{S,UVR} - V _{S,UVF}		0.5		V
V _{S,JS}	Power Supply Voltage Threshold for Overload Threshold Reduction in Case of Short Circuit		18.5	20.5	22.5	V

-V _{S,REV}	Breakdown Voltage between GND and VS Pins in Reverse Battery	I _{GND,REV} = 7 mA, T _J = 150 °C	16			V
t _{DELAY,UVR}	Power Supply Undervoltage Recovery Time	V _{INx} =V _{DEN} =5V	2.5	5	7.5	ms
t _{D,SLEEP}	Blanking time into Sleep Mode	V _S = 13.5 V, V _{OUT} = 0 V, V _{INx} = 0 V, V _{DEN} = 5 V to 0 V	12			ms
V _{S,CLAMP}	Power Supply Clamping Voltage	I _{VS} = 5 mA, T _J = -40°C	42			V
		I _{VS} = 5 mA, T _J = 25°C~125°C	46	48	50	V
OPERATING CURRENT						
I _{S,SLEEP}	Supply Current in Sleep Mode	V _S = 13.5V, V _{OUT} = 0V, V _{INx} = 0V, V _{DEN} = 0V, T _J = 25°C	0.5			μA
		V _S = 13.5V, V _{OUT} = 0V, V _{INx} = 0V, V _{DEN} = 0V, T _J = 125°C	3			μA
I _{GND,STBY}	Supply Current in Standby Mode	V _S = 13.5V, V _{OUT} = 0V, V _{INx} = 0V, V _{DEN} = 5V	3	5	mA	
I _{S,ON}	Supply Current for No Load, No Diagnosis	V _S = 13.5V, I _L = 0A, V _{INx} = 5V, V _{DEN} = 0V	3	5	mA	
I _{GND,ON}	Operating Current in Active Mode(All Channels ON)	V _S = 13.5V, I _L = 5 A, V _{INx} = 5 V, V _{DEN} = 5 V	6			mA
I _{L,OFF}	Output Leakage Current in Sleep Mode	V _S = 13.5V, V _{OUT} = 0V, V _{INx} = 0V, V _{DEN} = 0V, T _J = 25°C	0.5			μA
		V _S = 13.5V, V _{OUT} = 0V, V _{INx} = 0V, V _{DEN} = 0V, T _J = 125°C	3			μA
POWER STAGE						
R _{ON}	ON-state Resistance	V _S =13.5V, I _L = 5A, T _J = 25°C	8			mΩ
		V _S =13.5V, I _L = 5A, T _J = 150°C	14			mΩ
R _{ON,CRANK}	ON-state Resistance in Cranking State	V _S =3.1V, I _L = 2A, T _J = 150°C	20			mΩ
R _{ON,INV}	ON-State Resistance in Inverse Current	V _S =13.5V, I _L = -5A, V _{DEN} =0V, T _J = 25°C	10			mΩ
		V _S =13.5V, I _L = -5A, V _{DEN} =0V, T _J = 150°C	20			mΩ
R _{ON,REV}	ON-State Resistance in Reverse Polarity	V _S =-13.5V, I _L = -5A, V _{DEN} =0V, T _J = 25°C	10			mΩ
		V _S =-13.5V, I _L = -5A, V _{DEN} =0V, T _J = 150°C	33			mΩ
I _{LOVL}	Overload Detection Current	V _S = 5~18 V, T _J = -40°C	65	80	105	A
		V _S = 5~18 V, T _J = 25°C	65	80	95	A
		V _S = 5~18 V, T _J = 150°C	60	75	90	A
I _{LOVL,HVS} ⁽¹⁾	Overload Detection Current at High V _{ds}	V _{ds} > 22V	40			A

I _{LOVL,JS} ⁽¹⁾	Overload Detection Current Jump Start Condition	V _S > V _{S,JS}	40	A
V _{DS,CLP}	Drain to Source Clamp Voltage	I _L = 2A, T _J = -40°C	36	V
		I _L = 2A, T _J = 25°C ~150°C	38 42 46	V
OUTPUT DIODE CHARACTERISTICS				
V _{OUT,F}	Drain Source Diode Voltage	V _{INx} =0, I _L = -5A	0.75 0.85	V
I _{L,REV} ⁽¹⁾	Continuous Reverse Current when Reverse Polarity	t < 60s, V _S = 13.5V, GND pin 47Ω resistor, T _J = 25 °C	7.5	A
I _{L,INV} ⁽¹⁾	Continuous Inverse Current When V _{OUT} > V _S + V _{OUT,F}	t < 60 s, V _S = 13.5 V, T _J = 25°C	7.5	A
LOGIC INPUT (INx, DEN, DSEL)				
V _{IH}	Input Logic High		2.1	V
V _{IL}	Input Logic Low		0.8	V
V _{I,HYS}	Input Logic Hysteresis		200	mV
I _{IH}	High Level Pull-down Current	V _{INx} =2.1V	20	μA
I _{IL}	Low Level Pull-down Current	V _{INx} =0.8V	1 20	μA
DIAGNOSTICS AND PROTECTION				
I _{LOSS,GND}	Output Leakage Current when Loss of Ground	V _S = 13.5 V, V _{INx} = V _{DEN} = 5V	100	μA
V _{OL,OFF}	Open Load Detection Threshold in Standby Mode (V _S -V _{OUT})	V _{INx} = 0 V, V _{DEN} = 5 V	1.5 2 2.5	V
I _{OL,OFF}	Standby Mode Output Sink Current with Open Load	V _S = 13.5 V, V _{OUT} = V _S - 2.5 V, V _{INx} = 0 V, V _{DEN} = 5 V	40	μA
t _{D,OL,IN}	Standby Mode Diagnostic Delay Time from Falling Edge of Input	V _S = 13.5 V, V _{OUT} = 13.5 V, V _{INx} = 5V to 0V, V _{DEN} = 5V	180 250 330	μs
t _{D,OL,VO}	Standby Mode Diagnostic Delay Time from Rising Edge of V _{OUT}	V _S = 13.5 V, V _{OUT} =0 to V _S , V _{INx} = 0 V, V _{DEN} = 5 V	190 240	μs
t _{D,OL,DEN}	Standby Mode Diagnostic Delay Time from Rising Edge of DEN	V _S = 13.5 V, V _{OUT} = V _S , V _{INx} = 0 V, V _{DEN} = 0 to 5 V	200	μs
T _{SD} ⁽¹⁾	Thermal Shutdown Temperature		170	°C
T _R ⁽¹⁾	Thermal Shutdown Reset Temperature		150	°C
T _{SW} ⁽¹⁾	Thermal Swing Shutdown Threshold		60	°C
T _{HYS} ⁽¹⁾	Hysteresis for Resetting the Thermal Shutdown and Swing		15	°C
t _{RTY}	Auto Retry Time after Fault Condition		40 80 110	ms

t _{FAULT,CR}	Counter Reset Delay Time after Fault Condition		40	80	110	ms
t _{DEN,CR}	Minimum DEN Pulse Duration for Counter Reset		50	100	150	μs
n _{RTY}	Automatic Retries in Case of Fault after a Counter Reset		5			
n _{RTY,NT}	Automatic Retries in Case of Fault after the First t _{RTY} Activation		1			
n _{RTY,CYC}	Maximum “Retry” Cycles allowed before Channel Latch OFF		2			
Multiple SENSE Functions						
K _{IS}	Ratio of Current Sense		5450			
I _{L(OL)_4u}	Open Load Output Current at I _{IS} = 4 μA		8	15	25	mA
dk _{IS} /K _{IS}	Accuracy of Current Sense (I _{IS} × K _{IS} – I _L) / I _L × 100	I _L = 0.02A	-60		60	%
		I _L = 0.1A	-35		35	
		I _L = 0.25A	-29.5		29.5	
		I _L = 1A	-18		18	
		I _L = 2.8A	-9		9	
		I _L = 5.5A	-9		9	
		I _L = 10A	-9		9	
V _{DS_SLC}	Output Voltage Drop Limitation at Small Load Currents	V _S =13.5V, V _{DEN} = V _{INx} = 5V, I _L =20mA	0.3	3	10	mV
V _{IS,SAT} ⁽¹⁾	IS Saturation Voltage	V _S = 7V to 18V; R _{IS} = 1.2kΩ; V _{INx} = 5V V _{DEN} = 5V	4.8			V
V _{IS,H}	Fault High Voltage of IS	V _S ≥ 7V	5	5.5	6	V
		5V≤V _S <7V	4.2		6	V
I _{IS,SAT}	IS Saturation Current	V _S = 7V to 18V; R _{IS} = 1.2kΩ; V _{INx} = 5V, V _{DEN} = 5V	4			mA
I _{IS,FAULT}	Fault Current of IS	V _S = 7V to 18V; R _{IS} = 1.2kΩ; V _{INx} = 5V, V _{DEN} = 5 V	4.4	7.5	10	mA
I _{IS,OLOFF}	Sense Open Load in Standby Mode	V _S = 7V to 18V; R _{IS} = 1.2kΩ; V _{INx} = 0V, V _{DEN} = 5 V	2	2.8	3.5	mA
I _{IS,LEAK1}	Leakage Current of IS in Diagnostic Disable State	V _{INx} = 5 V, V _{DEN} = 0 V, V _{IS} = 0 V, I _L = 6 A	0.5			μA
I _{IS,LEAK2}	Leakage Current of IS in Diagnostic Enable State	V _{INx} = 5 V, V _{DEN} = 5 V, V _{IS} = 0 V, I _L = 0 A, T _J = 125°C	1.5			μA

$t_{IS,ON1}$	Current IS Settling Time from DEN Rising Edge	$I_L \geq 1\text{ A}$, $R_{IS} = 1.2\text{ k}\Omega$, $V_{INx} = 5\text{ V}$, $V_{DEN} = 0\text{ to }5\text{ V}$, V_{IS} to 90% of sense value	40	μs
$t_{IS,OFF1}$	Current IS Settling Time from DEN Falling Edge	$I_L \geq 1\text{ A}$, $R_{IS} = 1.2\text{ k}\Omega$, $V_{INx} = 5\text{ V}$, $V_{DEN} = 5\text{ to }0\text{ V}$, V_{IS} to 10% of sense value	20	μs
$t_{IS,FAULT,D}$	Sense Delay Time at Channel Switch ON after Last Fault Condition		500	μs
$t_{IS,ON2}$	Current Sense Settling Time from IN Rising Edge	$I_L \geq 1\text{ A}$, $R_{IS} = 1.2\text{ k}\Omega$, $V_{INx} = 0\text{ to }5\text{ V}$, $V_{DEN} = 5\text{ V}$, V_{IS} to 90% of sense value	110	μs
$t_{IS,OFF2}$	Current Sense Settling Time from IN Falling Edge	$I_L \geq 1\text{ A}$, $R_{IS} = 1.2\text{ k}\Omega$, $V_{INx} = 5\text{ to }0\text{ V}$, $V_{DEN} = 5\text{ V}$, V_{IS} to 10% of sense value	20	μs
$t_{IS,CC}^{(1)}$	Current Sense Settling Time after Channel Change	$I_L \geq 1\text{ A}$, $R_{IS} = 1.2\text{ k}\Omega$, $V_{INx} = 5\text{ V}$, $V_{DEN} = 5\text{ V}$, $V_{DSEL} = 5\text{ to }0\text{ V}$ or $0\text{ to }5\text{ V}$, V_{IS} to 10% of sense value	5 20	μs
Switching Characteristics				
$t_{D,ON}$	Turn-on Delay Time	V_{INx} rising edge to $V_{OUT} = 20\% * V_S$, $V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	25 40 65	μs
$t_{D,OFF}$	Turn-off Delay Time	V_{INx} falling edge to $V_{OUT} = 80\% * V_S$, $V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	25 45 95	μs
t_{ON}	Turn-on Time	V_{INx} rising edge to $V_{OUT} = 90\% * V_S$, $V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	55 65 110	μs
t_{OFF}	Turn-off Time	V_{INx} falling edge to $V_{OUT} = 10\% * V_S$, $V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	30 60 110	μs
dV/dt_{ON}	Turn-on Slew Rate	$V_{OUT} = 20\%$ to 80% , $V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	0.2 0.4 0.6	$\text{V}/\mu\text{s}$
dV/dt_{OFF}	Turn-off Slew Rate	$V_{OUT} = 80\%$ to 20% , $V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	0.2 0.5 0.7	$\text{V}/\mu\text{s}$
t_{skew}	Pulse Skew $t_{D,ON} - t_{D,OFF}$	$V_S = 13.5\text{ V}$, $R_L = 2.6\Omega$, $T_J = 25^\circ\text{C}$	-50 50	μs

(1) Parameter guaranteed by design and characterization; not subject to production test.

8.6 Typical Characteristics

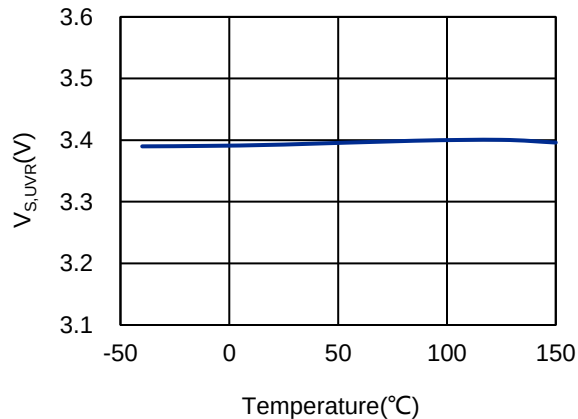


Figure 8-1. V_{S,UVR} vs T_A

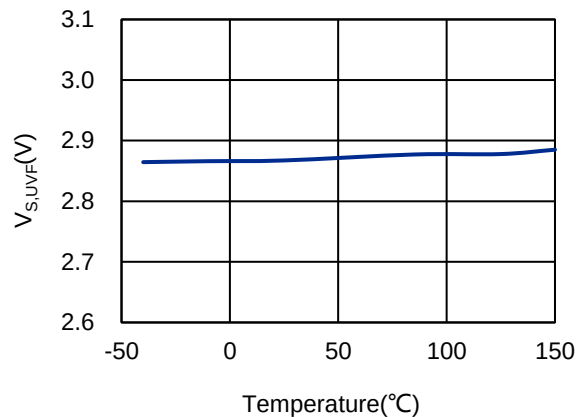


Figure 8-2. V_{S,UVF} vs T_A

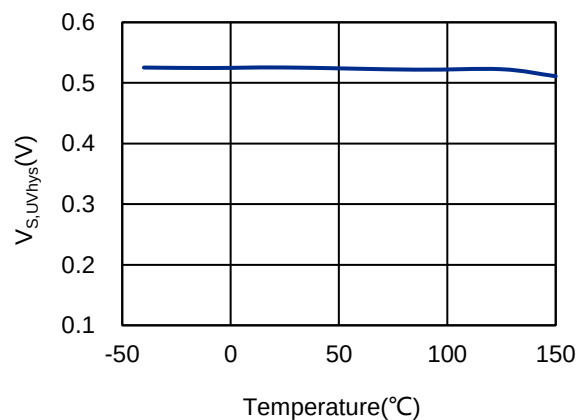


Figure 8-3. V_{S,UVhys} vs T_A

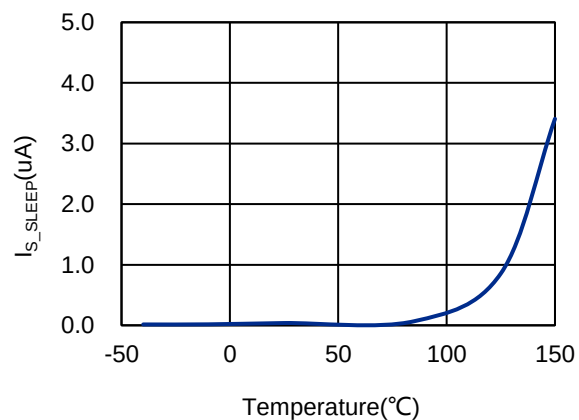


Figure 8-4. I_{S,SLEEP} vs T_A

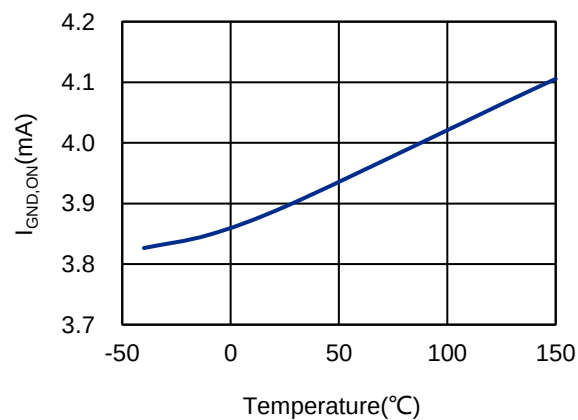


Figure 8-5. I_{GND,ON} vs T_A

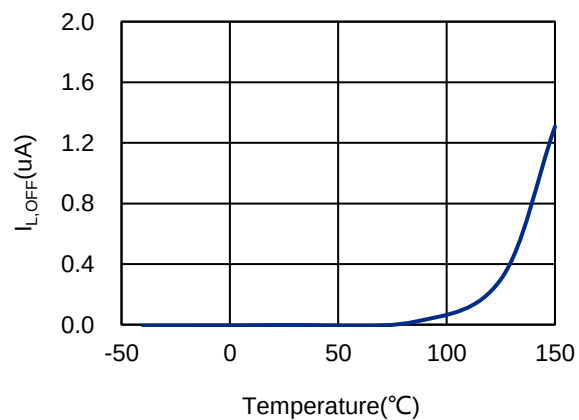


Figure 8-6. I_{L,OFF} vs T_A

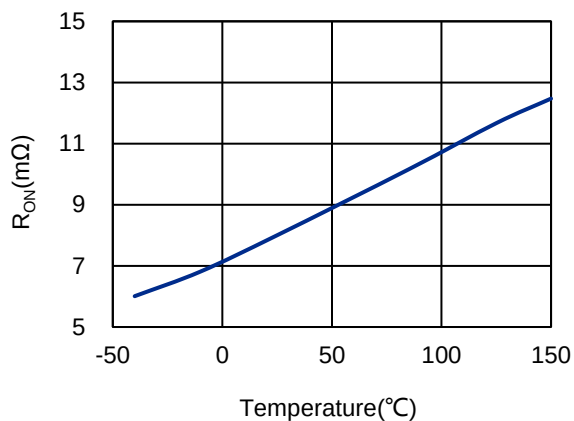


Figure 8-7. R_{ON} vs T_A

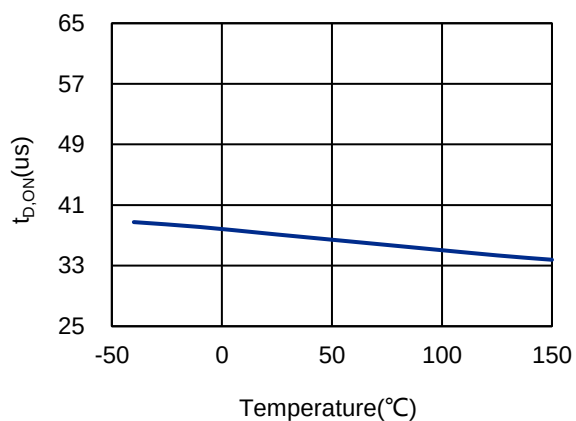


Figure 8-8. t_{D,ON} vs T_A

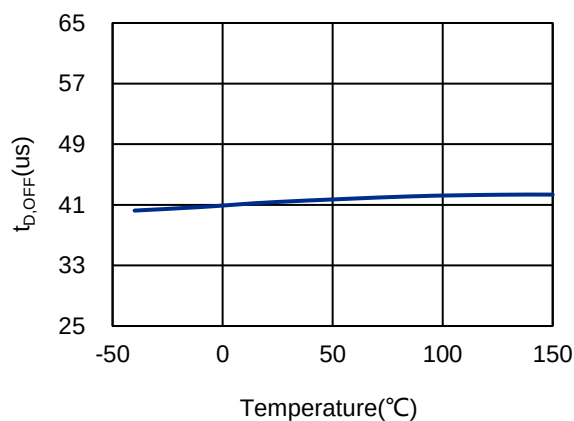


Figure 8-9. t_{D,OFF} vs T_A

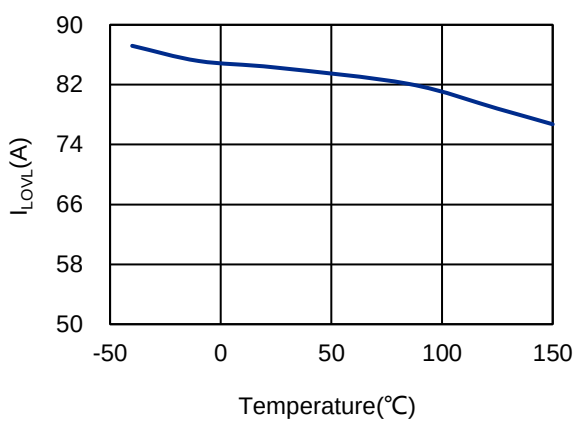


Figure 8-10. I_{LOVL} vs T_A

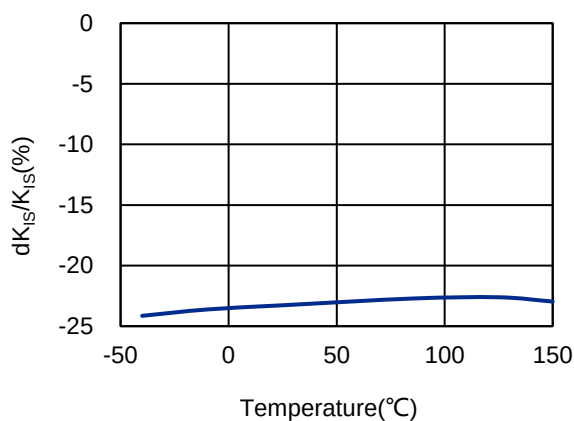


Figure 8-11. dK_{IS} / K_{IS} vs T_A (I_L = 0.01A)

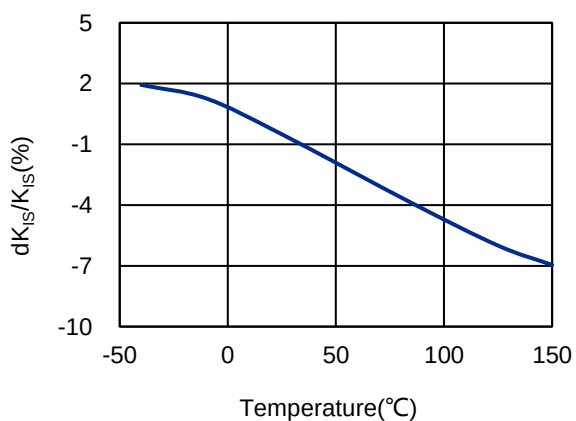


Figure 8-12. dK_{IS} / K_{IS} vs T_A (I_L = 2A)

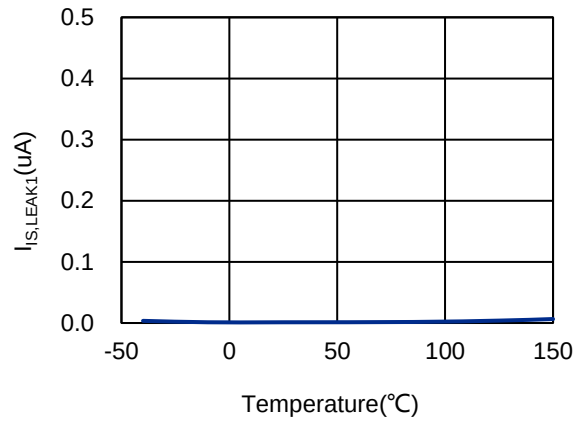


Figure 8-13. $I_{IS,LEAK1}$ VS T_A

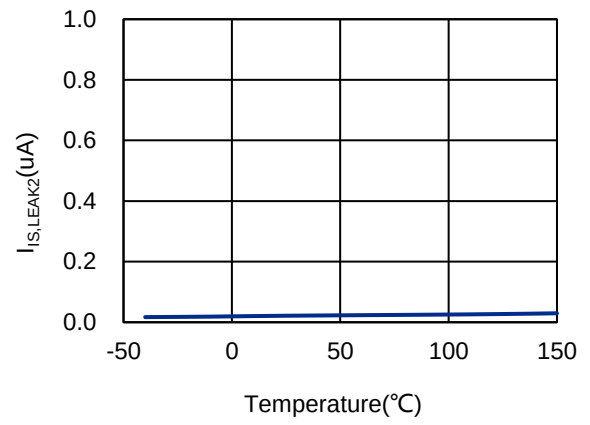


Figure 8-14. $I_{IS,LEAK2}$ VS T_A

9 Functional Block Diagram

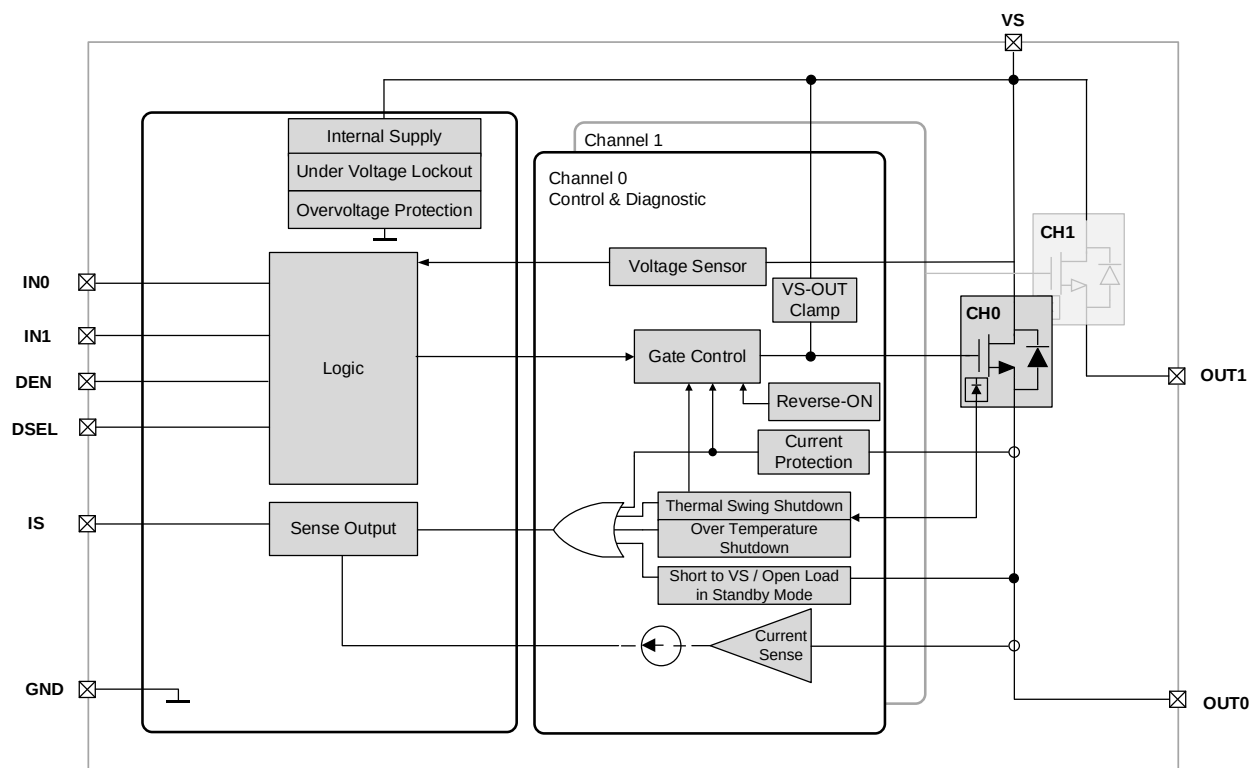


Figure 9-1. Functional Block Diagram

10 Feature Description

10.1 Operating Modes

The device has three operating states called 'Sleep Mode', 'Standby Mode' and 'Active Mode', which are decided by the logic level of INx pin and DEN pin, the operating mode diagram is shown as below.

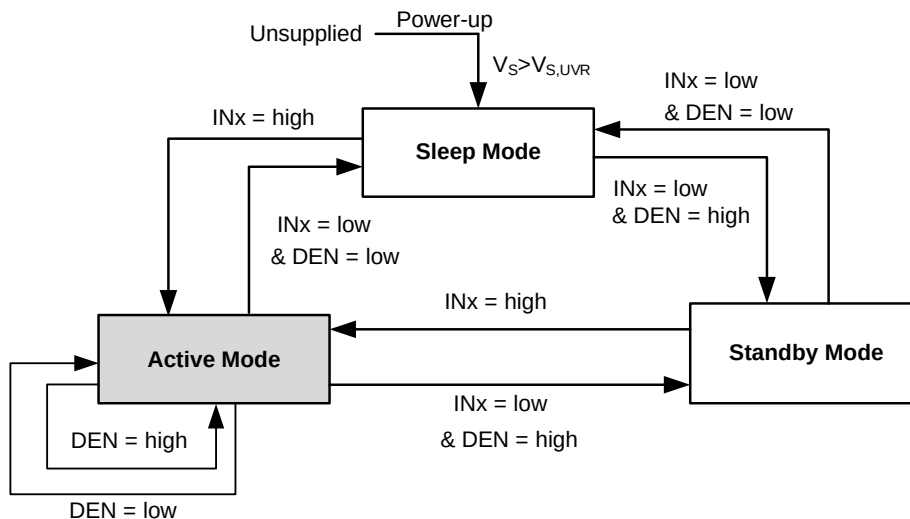


Figure 10-1. Operating Mode Diagram

10.1.1 Sleep Mode

During Sleep Mode, the output channel of the device is turned OFF. Current consumption is minimum (see parameter $I_{S,SLEEP}$). No overtemperature protection, overload protection or diagnostic functions are active in this mode.

10.1.2 Standby Mode

The device operates in Standby Mode when $DEN = \text{high}$ and $INx = \text{low}$. The output channel is OFF. Current consumption is specified as $I_{GND,STBY}$.

10.1.3 Active Mode

When the device is in Active Mode, the output channel is ON if no internal latch occurs. Current consumption is specified as $I_{GND,ON}$ (measured at the GND pin). Overload and overtemperature protections are active. The diagnostic function is active when $DEN = \text{high}$.

10.2 Power Stages

10.2.1 Switching Resistive Loads

When switching resistive loads, the switching time and slew rates are shown in Figure 10-2.

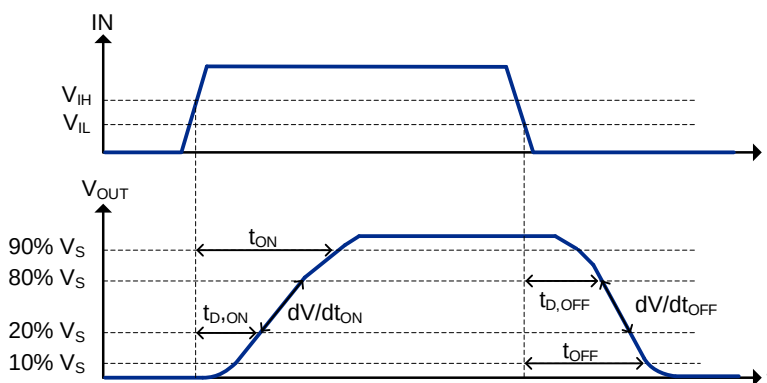


Figure 10-2. Switching a Resistive Load

10.2.2 Switching Inductive Loads

When turning OFF inductive loads with high-side switches, the output voltage V_{OUT} drops to a negative potential, because the inductance tends to maintain the current flow. To prevent the device from damage due to overvoltage, a voltage clamp mechanism is implemented. The clamping mechanism limits the negative output voltage to a safe value. Figure 10-3 shows a concept drawing of implementation.

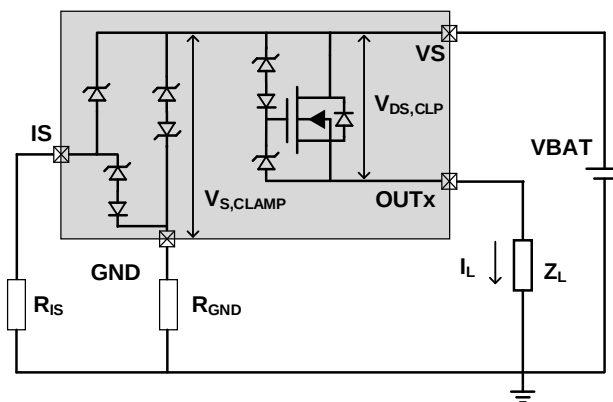


Figure 10-3. Output Clamp Diagram

During switching OFF of inductive loads, all energy stored in the inductive loads must be dissipated in the device. The maximum allowable energy is limited by the component's thermal design. Refer to Chapter 8.1 for the maximum allowable values of E_{AS} (single pulse energy).

10.2.3 Inverse Current Behavior

When $V_{OUT} > V_S$, an inverse current flows into the power MOSFET (see Figure 10-4). When $INx = \text{low}$, the MOSFET channel is turned OFF. In this state, current flows through the body diode, leading to substantial power dissipation and a rise in device temperature. When $INx = \text{high}$, the channel is turned ON, allowing current to flow through the MOSFET channel. The Inverse-ON resistance ($R_{ON,INV}$) of the channel helps reduce power dissipation in the output stage. During inverse current operation, the channel remains in either ON or OFF state.

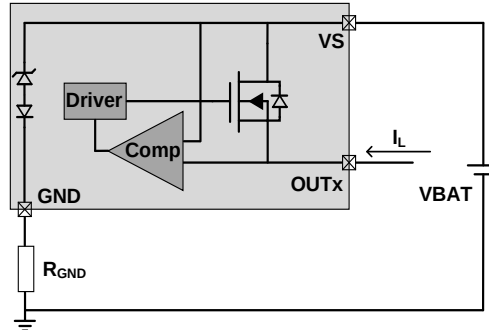


Figure 10-4. Inverse Current Circuitry

10.3 Protection

10.3.1 Overtemperature Protection

To prevent the junction temperature from exceeding the threshold, the device features both absolute thermal shutdown (T_{SD}) and dynamic thermal swing shutdown (T_{SW}) protection mechanisms. Once the temperature exceeds the threshold T_{SD} , or the temperature swing exceeds the threshold T_{SW} , the overheated channel is turned OFF and remains OFF until T_J has reached the "Restart" condition described in Chapter 10.3.7. Figures 10-5 and 10-6 respectively demonstrate these two over-temperature protection mechanisms. $T_{J,REF}$ is the reference temperature used for dynamic temperature protection.

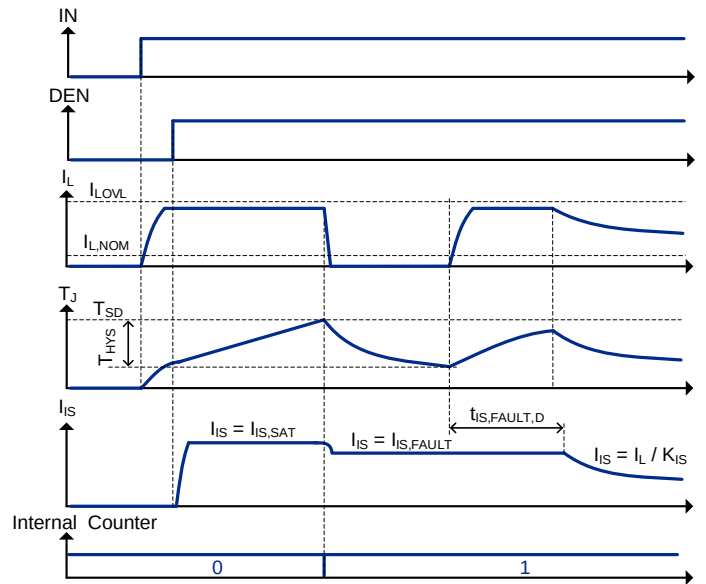


Figure 10-5. Overtemperature Protection (Thermal Shutdown)

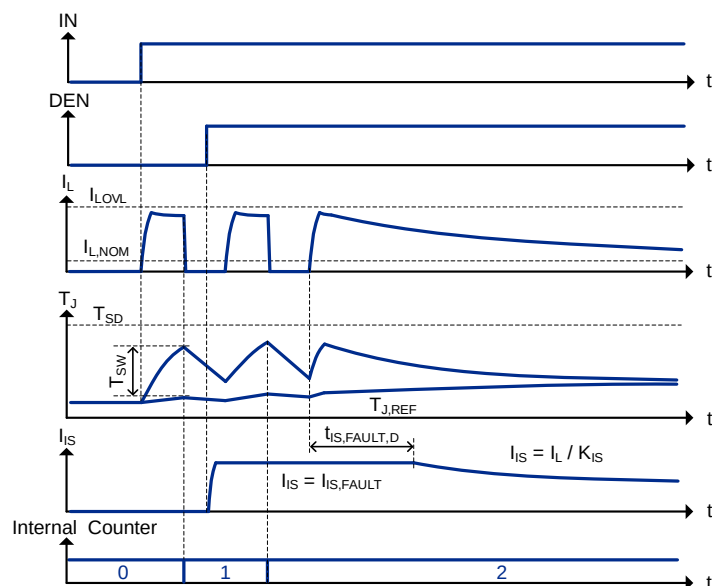


Figure 10-6. Overtemperature Protection (Thermal Swing Shutdown)

10.3.2 Overload Protection

The device features protection against overload and short circuit to ground. Its overload threshold decreases as junction temperature rises: at high temperatures, the overload threshold is reduced to prevent device damage. When the supply voltage V_S exceeds $V_{S,JS}$ (during load dump or jump start), the overload detection current decrease to $I_{LOVL,JS}$ as shown in Figure 10-7.

Once the load current meets or exceeds the applicable overload threshold, the output channel is switched off. The channel is allowed to restart according to the retry strategy described in Chapter 10.3.7.

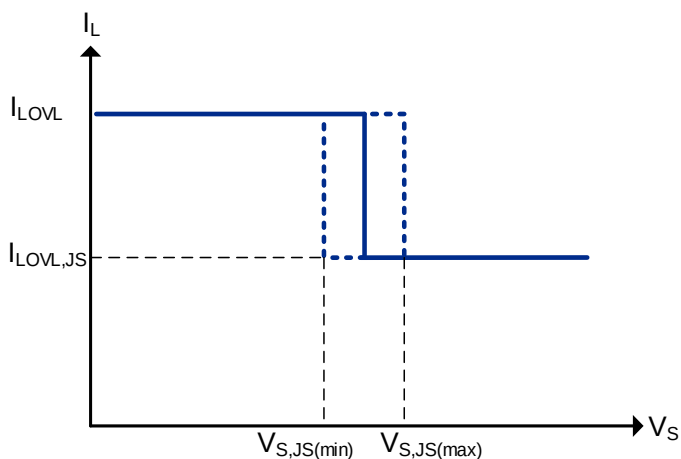


Figure 10-7. Overload Detection Current Variation with VS Voltage

10.3.3 Undervoltage Protection

Undervoltage protection monitors the supply voltage (V_S). If V_S drops below the minimum operating threshold ($V_{S,UVF}$), the output is turned off regardless of the input status. A delay time $t_{DELAY,UVR}$ is required for restart after voltage recovery to prevent undervoltage caused by a short-circuit fault.

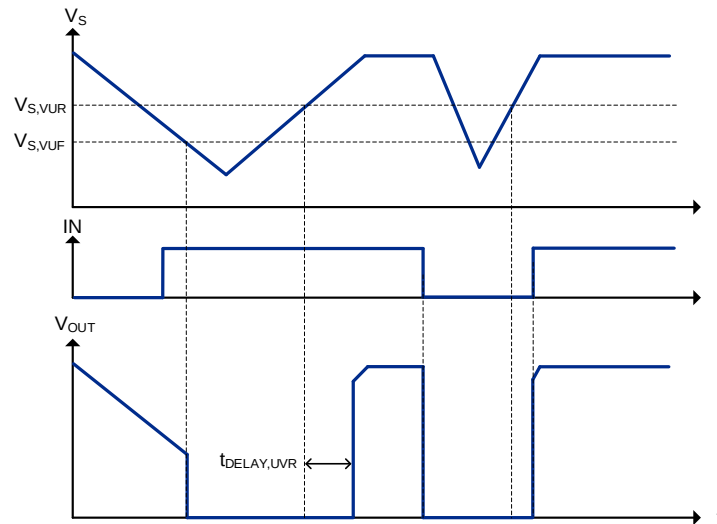


Figure 10-8. VS Undervoltage Protection

10.3.4 Overvoltage Protection

In the case of supply voltage spikes above $V_{S,CLAMP}$, there is a clamp mechanism available for overvoltage protection for the logic circuit and the output channel. The device features overvoltage protection in all operating modes. When overvoltage protection occurs, the power MOSFET remains operational and its output follows the INx pin.

10.3.5 Reverse Battery Protection

In Reverse Battery condition, the output stage is switched ON (see parameter $R_{ON,REV}$) because of Reverse-ON feature which limits the power dissipation in the output stage. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stage must be limited by the connected load. Digital input pins need external resistors for current limiting as well. A typical application circuit of this function is shown in Figure 10-9. A resistor between module ground and GND pin is required to activate Reverse-ON.

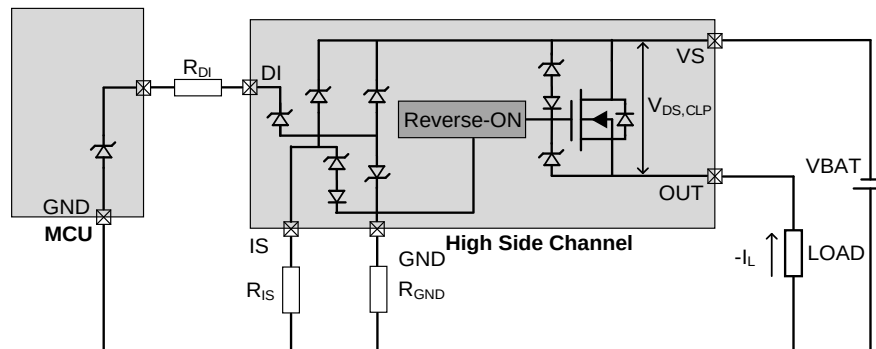


Figure 10-9. Reverse Battery Protection

10.3.6 Loss of Ground Protection

In the event of Loss of Ground, the device automatically switches off the power MOSFET, ensuring no current flows into the load. It is recommended to connect a resistor between any logic pins and the microcontroller to ensure the channel switch OFF.

Note: In case any logic pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.

10.3.7 Intelligent Retry Strategy

The intelligent retry strategy is a protection mechanism designed to ensure device safety and reliability. When a protection event occurs during $INx = \text{high}$, the affected channel is switched off and the internal counter is incremented. The IS pin outputs a fault current $I_{IS, \text{FAULT}}$ in this case if $DEN = \text{high}$.

The channel can be allowed to restart only if the “restart” conditions for the protection mechanisms are fulfilled:

- For overtemperature: $T_J < T_{SD}$ and $T_J - T_{J, \text{REF}} < T_{SW}$ (including hysteresis).
- For overload: $I_L < 50\text{mA}$ and T_J within T_{SD} and T_{SW} ranges (including hysteresis).

The channel is allowed to switch on for n_{RTY} times before switching off. After a time t_{RTY} , if $IN = \text{high}$, the channel is switched on again for $n_{RTY, NT}$ times before switching off again (“retry” cycle). After $n_{RTY, CYC}$ consecutive “retry” cycles, the channel is latched off.

Two ways to reset the internal counter are shown in Figure 10-10, Figure 10-11 and Figure 10-12.

- Reset via IN pin: Pull the IN pin low for a duration exceeding $t_{\text{FAULT, CR}}$ (typical 80ms).
- Forced reset via DEN pin: Keep the $IN = \text{low}$, then apply a pulse to the DEN pin longer than $t_{\text{DEN, CR}}$ (typical 100 μs). The DSEL pin must select the channel that has to be de-latched and keep the same logic value while DEN pin toggles twice (rising edge followed by a falling edge).

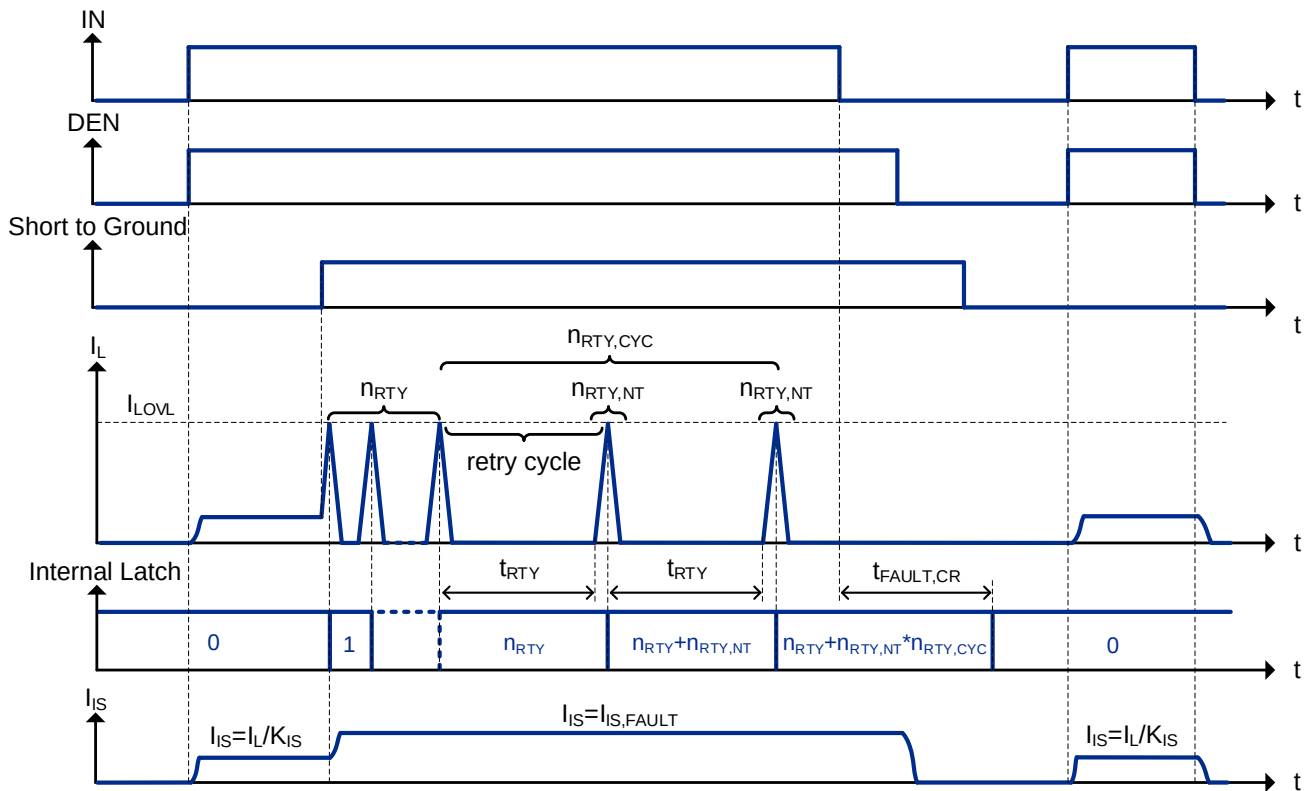


Figure 10-10. Retry Strategy Timing Diagram

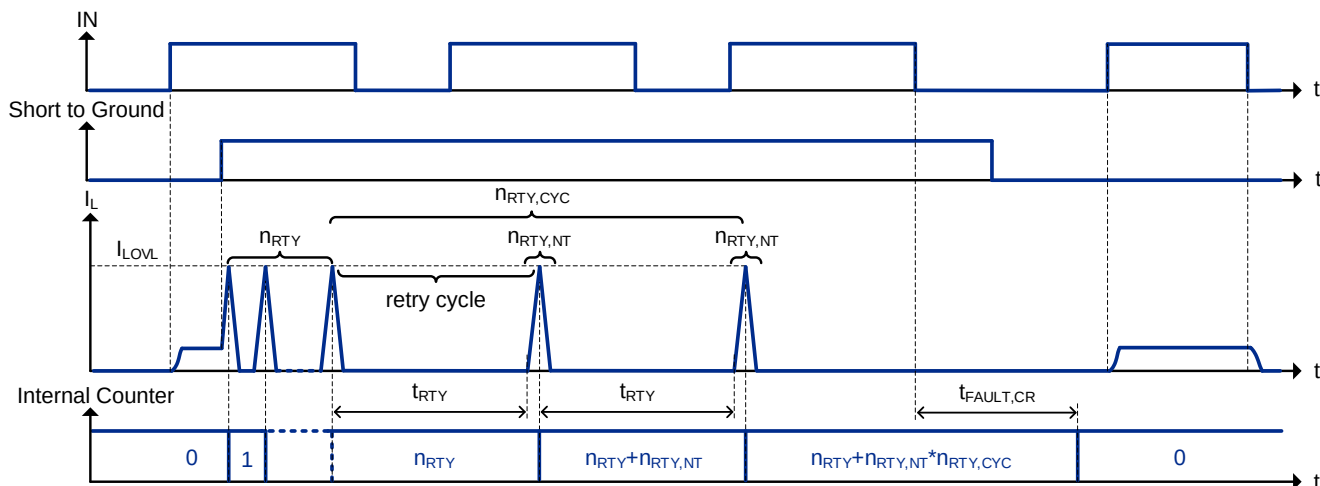


Figure 10-11. Retry Strategy Timing Diagram - Channel operated in PWM

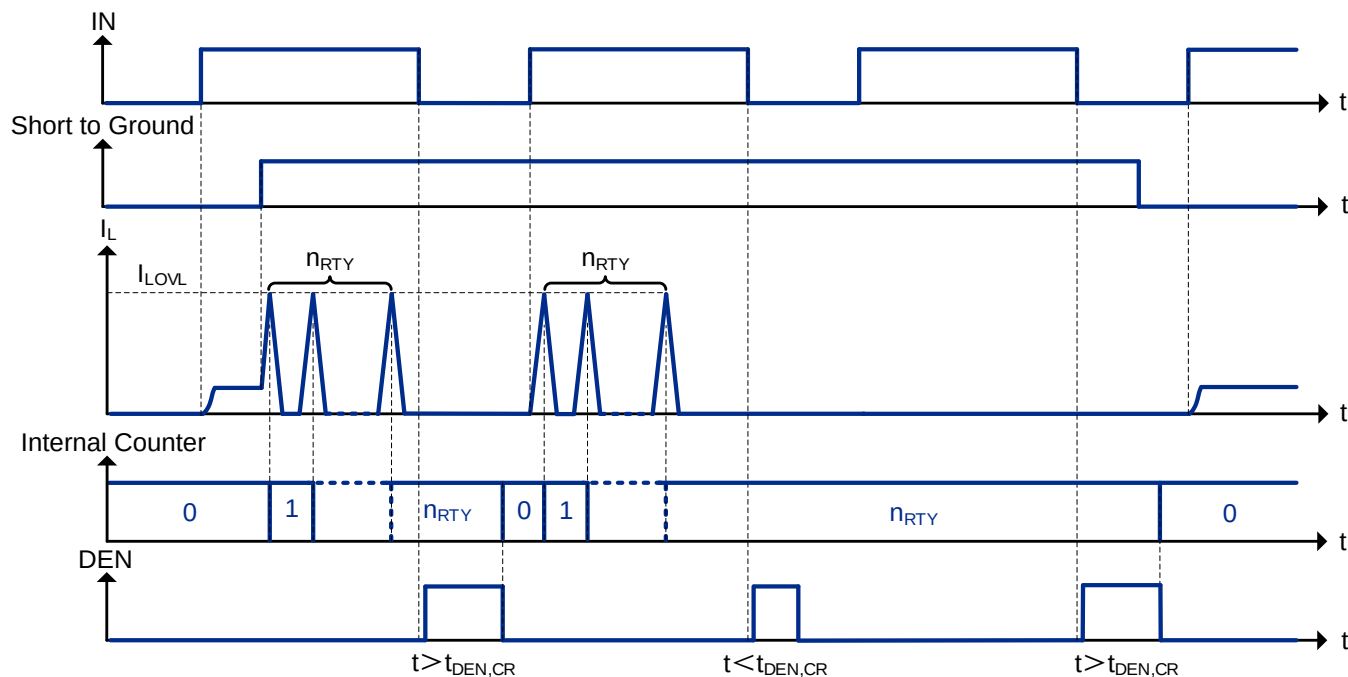


Figure 10-12. Retry Strategy Timing Diagram with Forced Reset

10.4 Diagnosis

The device integrates comprehensive diagnostic capabilities via IS pin, which delivers proportional current sense signals or fault indications when DEN = high and a channel is selected using DSEL pin. When DEN = low, the IS pin enters a high-impedance state. A sense resistor (R_{IS} , typically 1.2k Ω) must be connected between the IS pin and module ground to limit power dissipation. Table 10-1 gives a quick reference to the multiplexed output state of the IS pin during the device operation.

Table 10-1. Sense Signal, Function of Application Condition

Conditions	INx	DEN	OUT	IS
Normal Operation	Low	High	~GND	Z I _{IS,FAULT} if counter > 0
Short Circuit to GND			~GND	Z I _{IS,FAULT} if counter > 0
Overtemperature			Z	I _{IS,FAULT}
Short Circuit to V _S			V _S	I _{IS,OLOFF} I _{IS,FAULT} if counter > 0
Open Load			< V _S - V _{OL,OFF}	Z I _{IS,FAULT} if counter > 0
			> V _S - V _{OL,OFF}	I _{IS,OLOFF} I _{IS,FAULT} if counter > 0
Inverse Current			V _{OUT} > V _S	I _{IS,OLOFF} I _{IS,FAULT} if counter > 0
Normal Operation	High		~V _S	I _{IS} = I _L / K _{IS}
Short Circuit to GND			~GND	I _{IS,FAULT}
Overload			< V _S	I _{IS,FAULT}
Overtemperature			Z	I _{IS,FAULT}
Short Circuit to V _S			V _S	I _{IS} < I _L / K _{IS}
Open Load			~V _S	I _{IS} = I _{IS,LEAK2}
Inverse Current			V _{OUT} > V _S	I _{IS} = I _{IS,LEAK2}
All Conditions	n.a.	Low	n.a.	Z

In case DEN is set to “high”, the Sense for the selected channel is enabled or disabled using DSEL pin. Table 10-2 gives the truth table.

Table 10-2. Diagnostic Truth Table

DEN	DSEL	IS
“Low”	Not Relevant	Z
“High”	“Low”	Sense Output 0
“High”	“High”	Sense Output 1

10.4.1 Diagnosis in Active Mode

Diagnosis in Active Mode is enabled when DEN = high. The channel is selected using DSEL pin, and diagnostic signals are delivered via the IS pin. It includes two functions: proportional current sense and fault indications.

When no faults are present and the drain-source voltage $V_{DS} \leq V_{DS, OLOFF}$, the IS pin outputs an analog current I_{IS} proportional to the load current I_L , following the ratio $K_{IS} = I_L/I_{IS}$. For small load currents, the device activates output voltage limitation ($V_{DS, SLC}$) to enhance the accuracy of K_{IS} . An external RC filter is recommended for the IS pin to reduce signal ripple.

If overtemperature, overload, or short circuit to ground occurs, the value of the internal retry counter will change from its reset state. The IS pin outputs a fault current $I_{IS, FAULT}$ as long as diagnosis is enabled. When DEN=high and the affected channel is selected via the DSEL pin, the IS pin outputs a fault current $I_{IS, FAULT}$. The following 3 situations may occur:

- If the channel is on and the number of retries is lower than " $n_{RTY} + n_{RTY, CYC} * n_{RTY, NT}$ ", $I_{IS, FAULT}$ is provided for a time of $t_{IS, FAULT, D}$ after the channel is allowed to restart, after which $I_{IS} = I_L/K_{IS}$. During a retry cycle the current $I_{IS, FAULT}$ is provided each time the channel diagnosis is checked.
- If the channel is on and the number of retries reach the upper limit " $n_{RTY} + n_{RTY, CYC} * n_{RTY, NT}$ ", the current $I_{IS, FAULT}$ is provided until the internal counter is reset.
- If the channel is off and the internal counter is not in the reset state, the current $I_{IS, FAULT}$ is provided each time the channel diagnosis is checked.

Figure 10-13 shows the relation between I_{IS} and I_L .

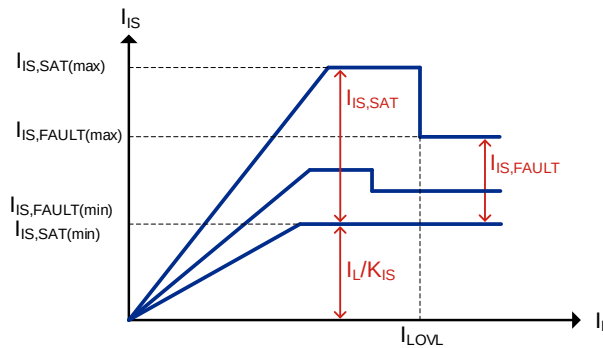


Figure 10-13. Relation Between I_{IS} and I_L

10.4.2 Diagnosis in Standby Mode

Diagnosis is activated in Standby Mode. The channel is selected using DSEL pin, and diagnostic signals are delivered via the IS pin. It includes two functions: open load detection and fault indications.

The device compares the voltage V_{DS} with the threshold voltage $V_{DS, OLOFF}$ to detect load conditions. If open load occurs ($V_{DS} \leq V_{DS, OLOFF}$), the IS pin outputs an open load fault current ($I_{IS, OLOFF}$). To differentiate open load and short circuit to V_S , an external switch and a pull-up resistor are recommended. It is necessary to wait a time $t_{D, OL, IN}$ between the falling edge of the input pin and the sensing at pin IS for Open Load in Standby Mode to allow the internal comparator to settle (see Figure 10-15).

If a fault condition is detected by the device (the internal counter has a value different from the reset value), a current $I_{IS, FAULT}$ is provided by IS pin each time the channel diagnosis is checked also in Standby Mode.

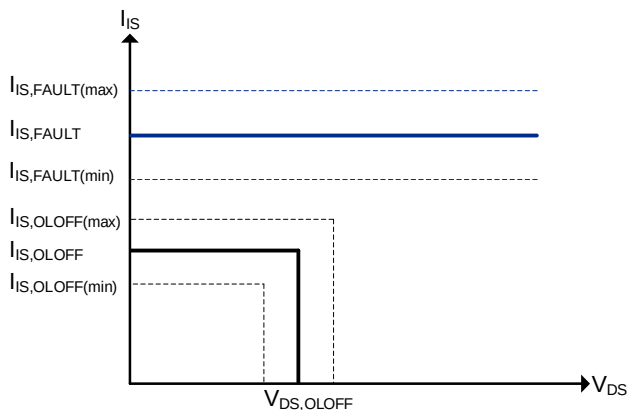


Figure 10-14. Relation Between $I_{IS, OLOFF}$ and $I_{IS, FAULT}$ as Functions of V_{DS}

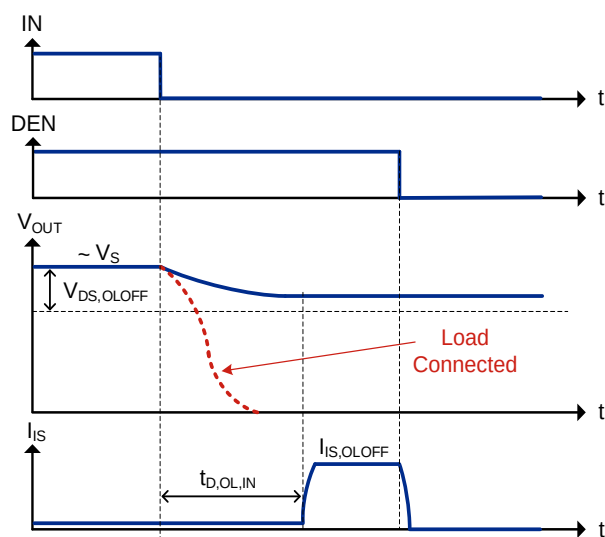


Figure 10-15. Timings for an Open Load Detection

10.4.3 Sense Time

Sense timings of the device define the response characteristics of the IS pin during IN/DEN activation and deactivation, with all parameters are specified under the test conditions given in Section 8.5. Figure 10-16 presents the sense settling and disabling time.

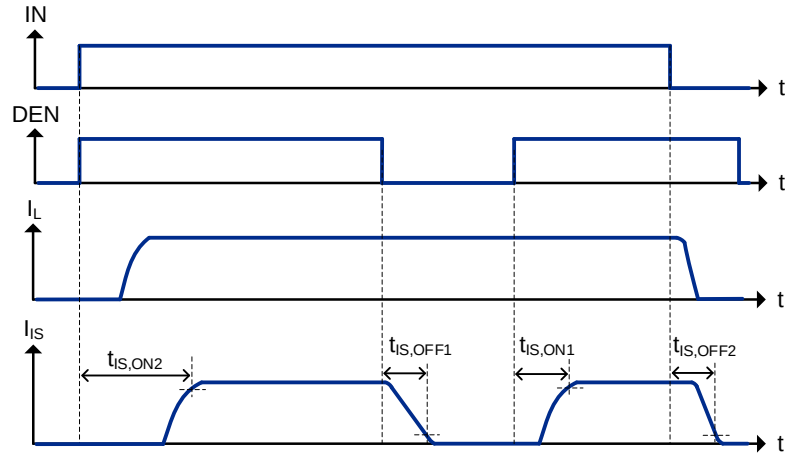


Figure 10-16. Sense Settling and Disabling Time

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This is a very simplified example of an application circuit. The function must be verified in the real application.

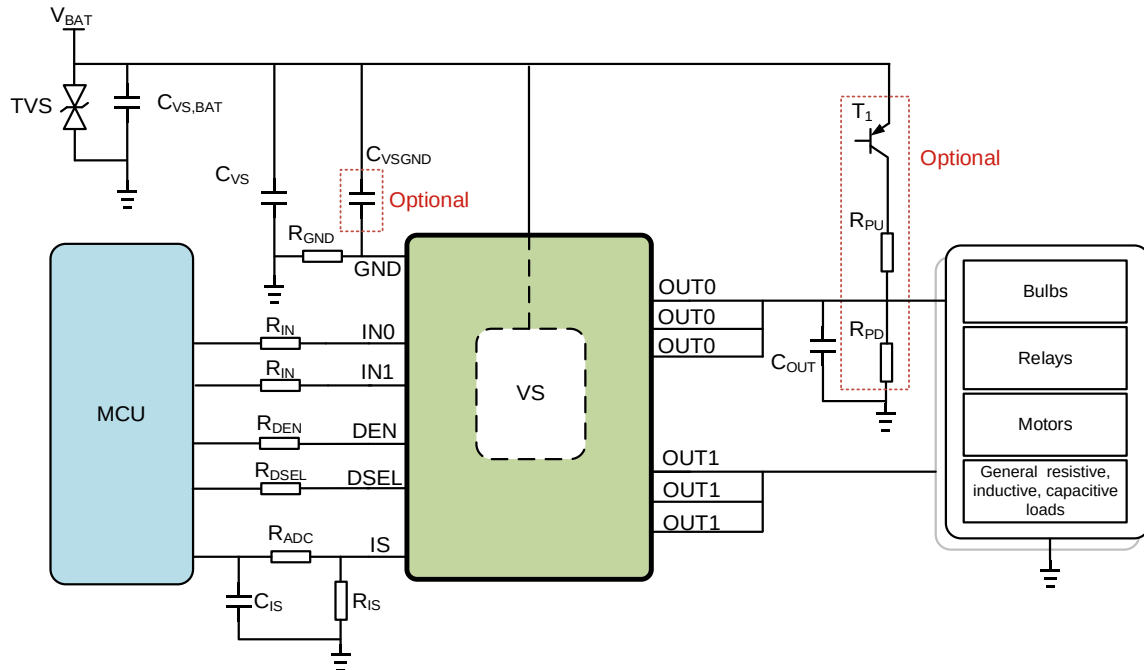


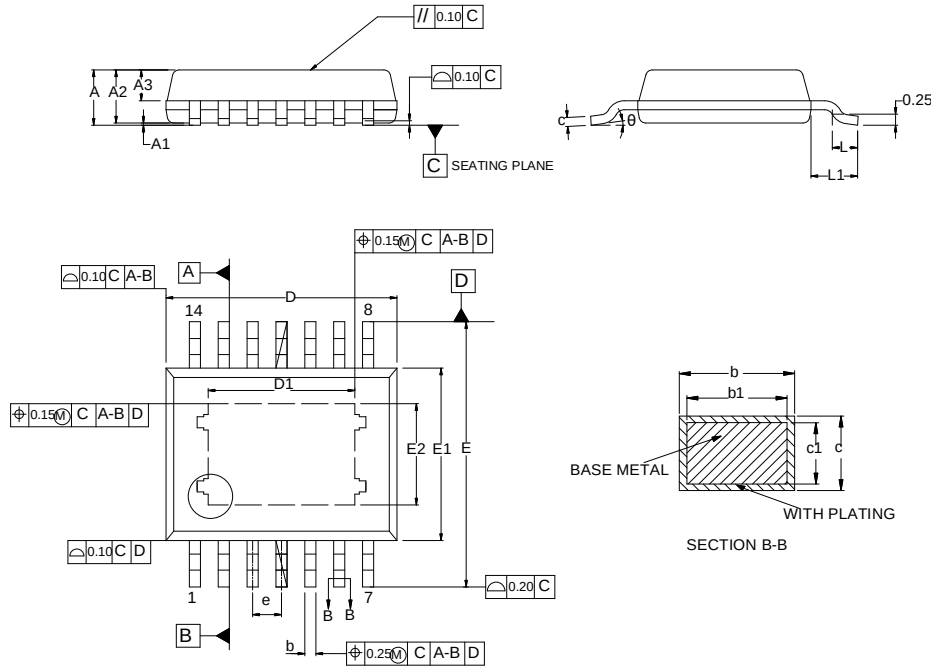
Figure 11-1. Application Diagram

Table 11-1. Suggested Component Values

Reference	Value	Purpose
R _{IN}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{DEN}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{DSEL}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{PD}	47kΩ	Output pull-down Ensure polarization of the device outputs to distinguish between Open Load and Short to VS in Standby Mode
R _{PU}	1.5kΩ	Output pull-up Ensure polarization of the device output during Open Load in Standby Mode
C _{OUT}	10nF	Protection of the device output during ESD events
T ₁	-	Switch the battery voltage for Open Load in Standby Mode
C _{VS}	100nF	Filtering of voltage spikes on the battery line
C _{VSGND}	47nF	Buffer capacitor for fast transient
TVS	33V	Diode transient voltage suppressor diode
C _{VS,BAT}	-	Filtering / buffer capacitor located at V _{BAT} connector
R _{IS}	1.2kΩ	Sense resistor
R _{ADC}	4.7kΩ	Protection of microcontroller ADC input during Overvoltage, Reverse Battery, Loss of Ground
C _{IS}	220pF	Sense signal filtering
R _{GND}	47Ω	Protection in case of Overvoltage and Loss of Battery while driving inductive loads

MECHANICAL DATA

eSSOP-14

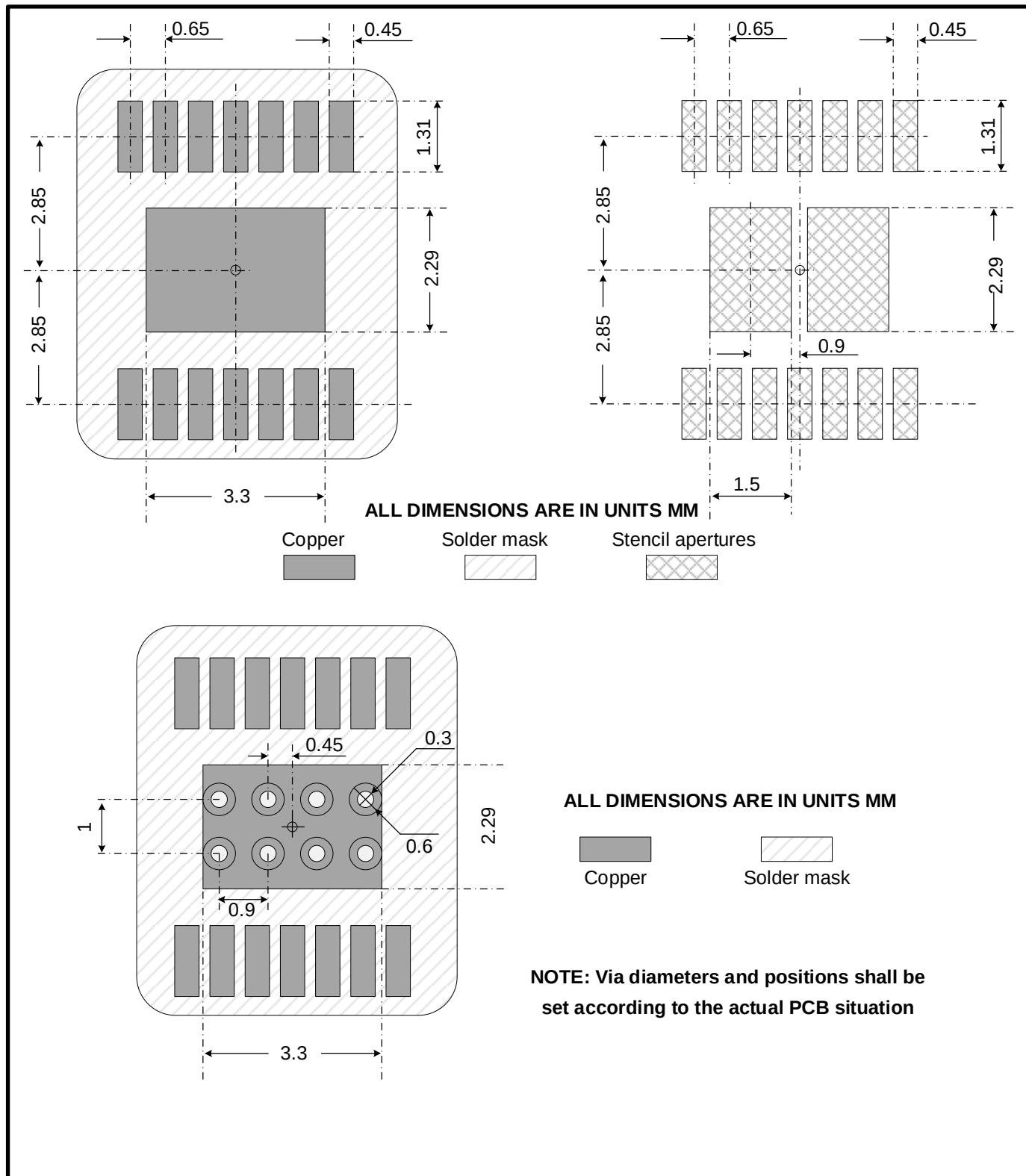


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.40
A1	0.00	—	0.10
A2	1.10	1.20	1.30
A3	0.60	0.70	0.80
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	5.10	5.20	5.30
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.65BSC		
L	0.40	0.57	0.80
L1	1.05REF		
θ	0	—	8°

Size(mm) L/P Size (mm)	E2	D1
98*138	2.29±0.30	3.30±0.30

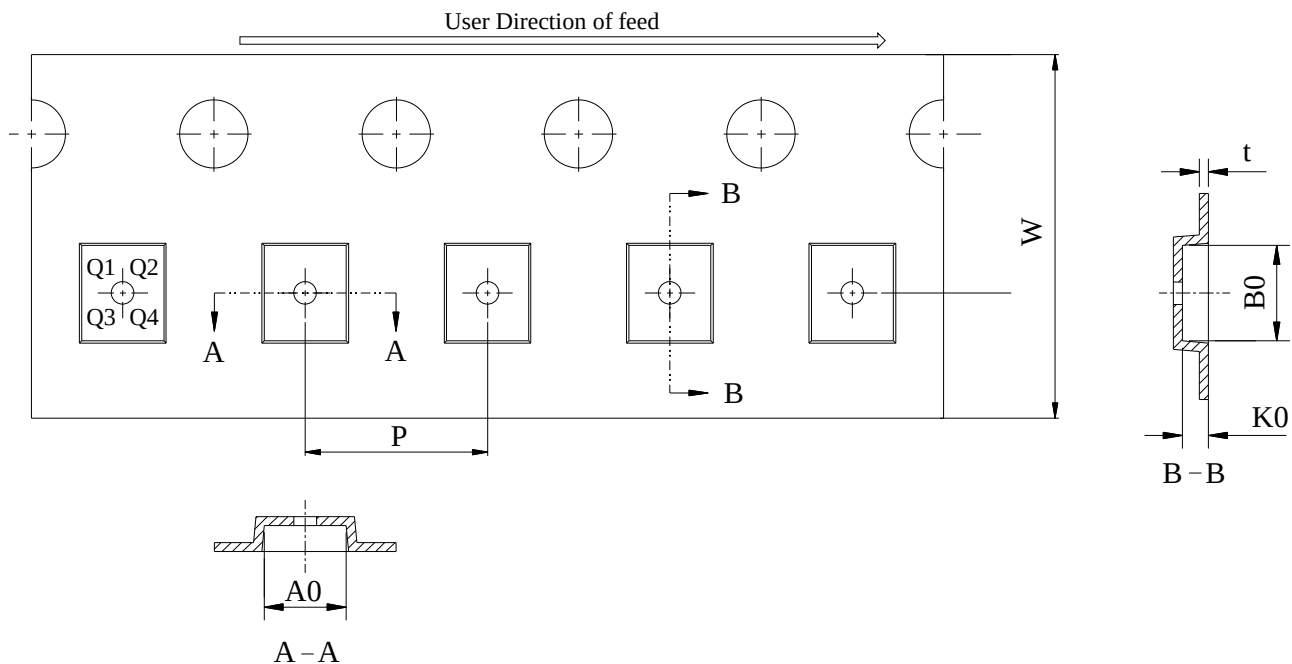
RECOMMENDED FOOTPRINT

eSSOP-14



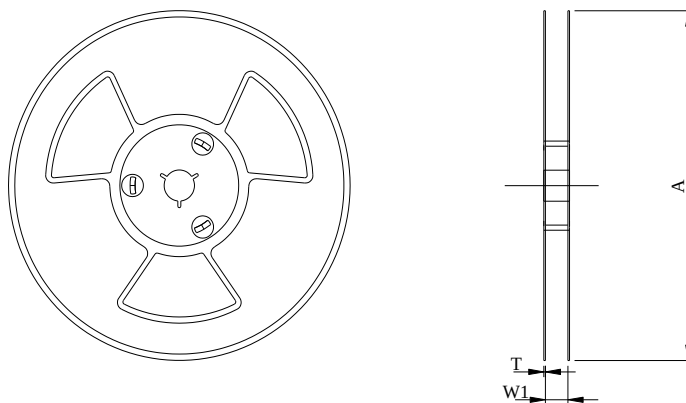
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	$12.00+0.30/-0.1$	8.00 ± 0.10	6.50 ± 0.10	5.50 ± 0.10	1.75 ± 0.10	0.30 ± 0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330 ± 1	$12.4 +1/-0$	2.1 ± 0.3

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