Synchronous, 80V Buck-Boost Controller with I2C

1 Descriptions

SC8708 is a synchronous buck-boost controller, which supports buck mode, boost mode and buck-boost mode. SC8708 has wide input range from 4.5V to 80V and wide output range from 5V to 80V. SC8708 also provides input current and output current monitoring function.

Through I2C interface, user can program the output current limit, output voltage adjustment, and other parameters flexibly. Besides, the output current limit, output voltage and switching frequency could be set by external resistors.

SC8708 supports frequency dithering to meet better EMI performance and integrates synchronization feature to switch under same frequency with external clock.

SC8708 integrates 11-bit ADC to monitor voltage, current. Full protection is supported including input and output over-voltage protection, output over-current protection and over-temperature protection.

SC8708 is available in a 5mm x 6mm QFN-36 Package

2 Features

- Wide Input Range: 4.5V to 80V, 88V sustainable
- High Efficiency Buck-Boost Conversion
- Compliant with PD 3.1
  - Output voltage 5~21V, 20mV/step;
  - Output voltage 21.05~48V, 50mV/step
  - EPR (Extended Power Range) 28V/36V/48V
  - Output Current: 2375mA~50A, 375mA/step for 2mΩ
- I2C interface
- Current limit set by external resistor and register, up to 50A, support 2mΩ (50A) /5mΩ (20A) sense resistor
- Support external supply for driver, up to 10V
- Switching frequency: 80kHz~480kHz and support frequency dithering and frequency synchronization
- Current monitor for input and output current
- Integrated 11-bit high accuracy ADC for current/voltage monitor
- Protection including UVP, OVP, OCP, SCP, OTP
- QFN 5x6-36 Package, 0.5mm pitch

3 Applications

- Docking
- Outdoor Power Station
- Industrial Equipment
- Power Backup
- Medical equipment

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8708QDGR	36 pin QFN	5mm x 6mm x 0.75mm

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5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.1.0	2026/03	4/5/20~22	1. Corrected frequency calculation formula 2. Update Typical Application 3. Increase Application Information & Layout Guide

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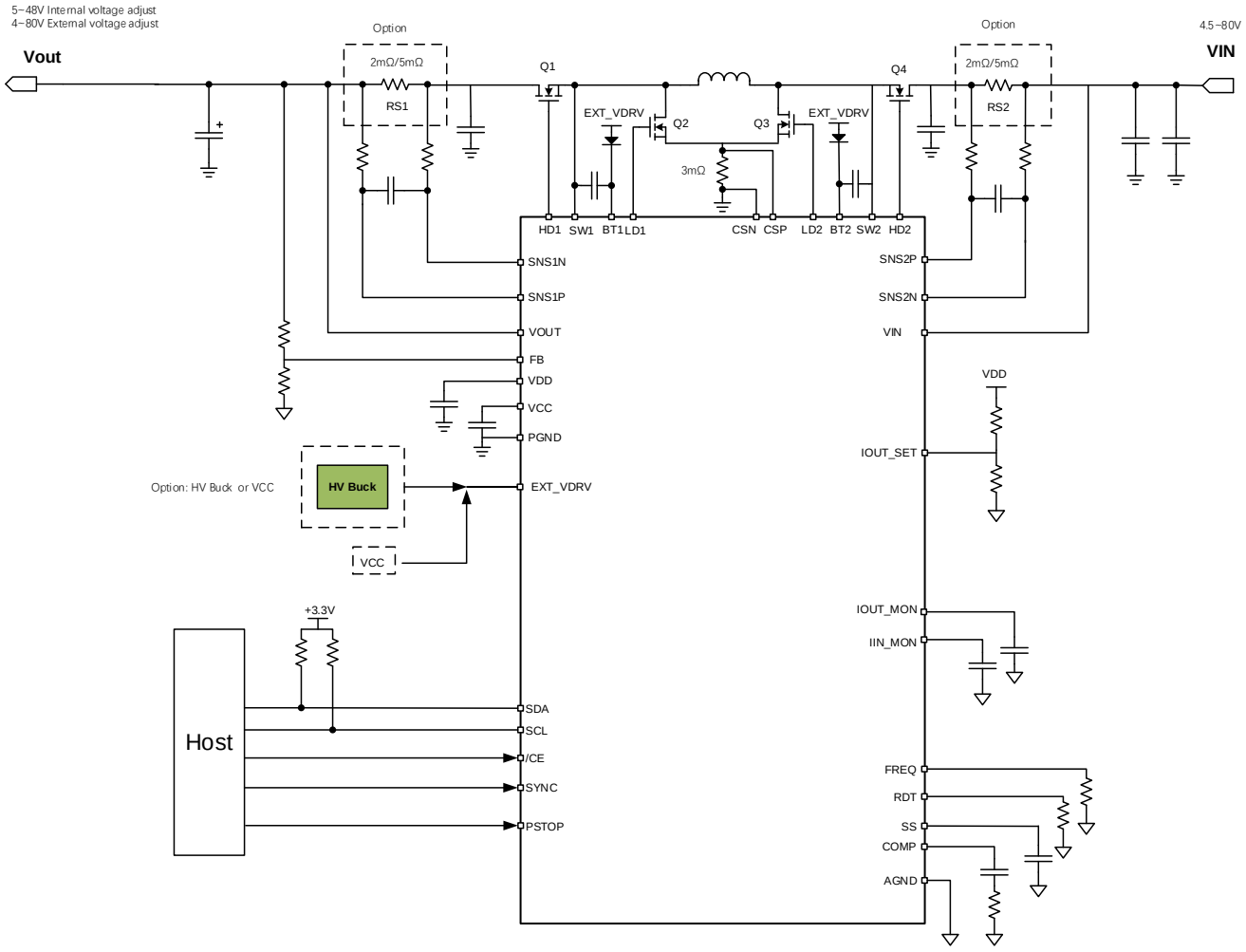
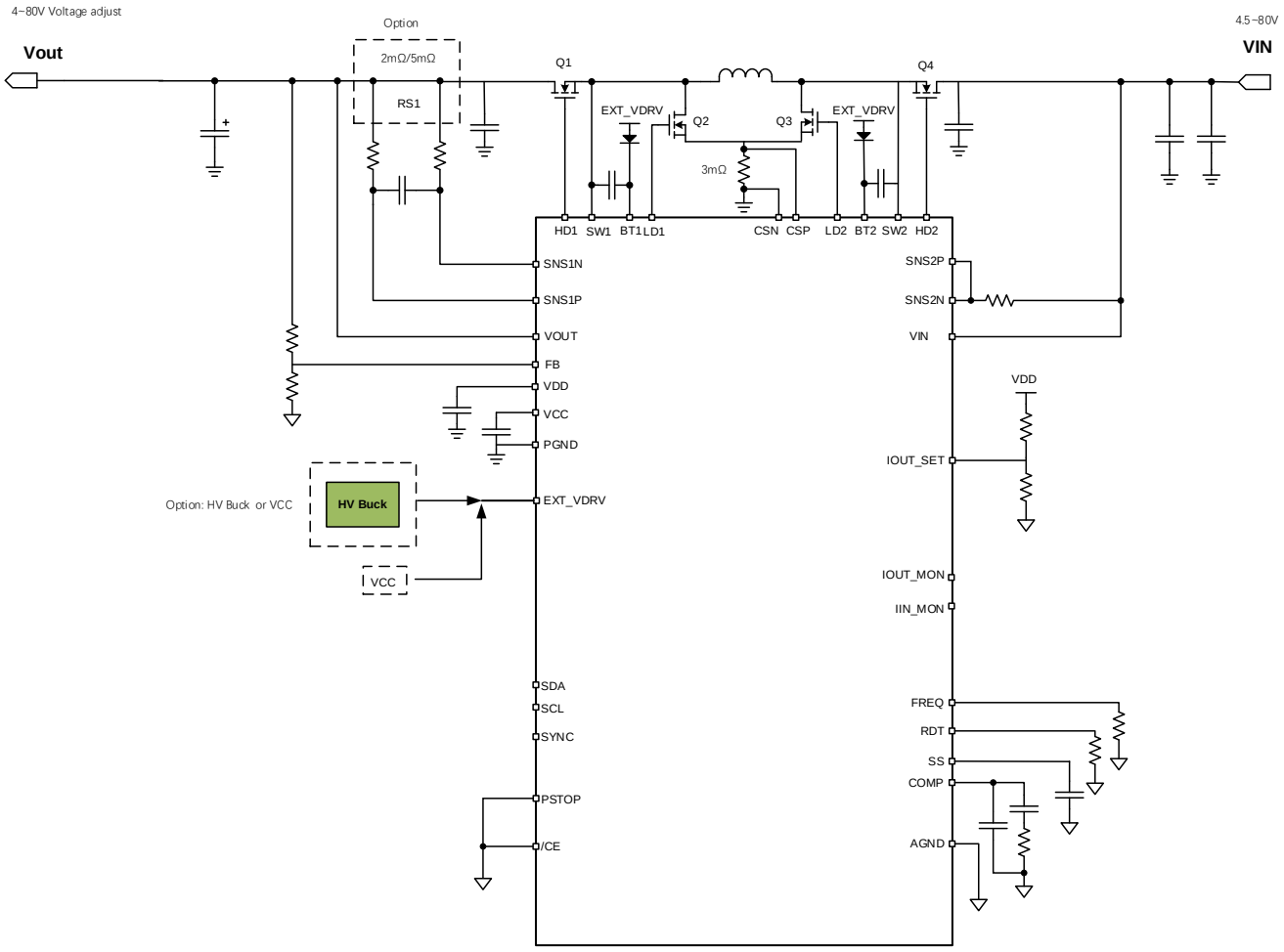
6 Typical Application Circuit



Typical Application with I2C Interface

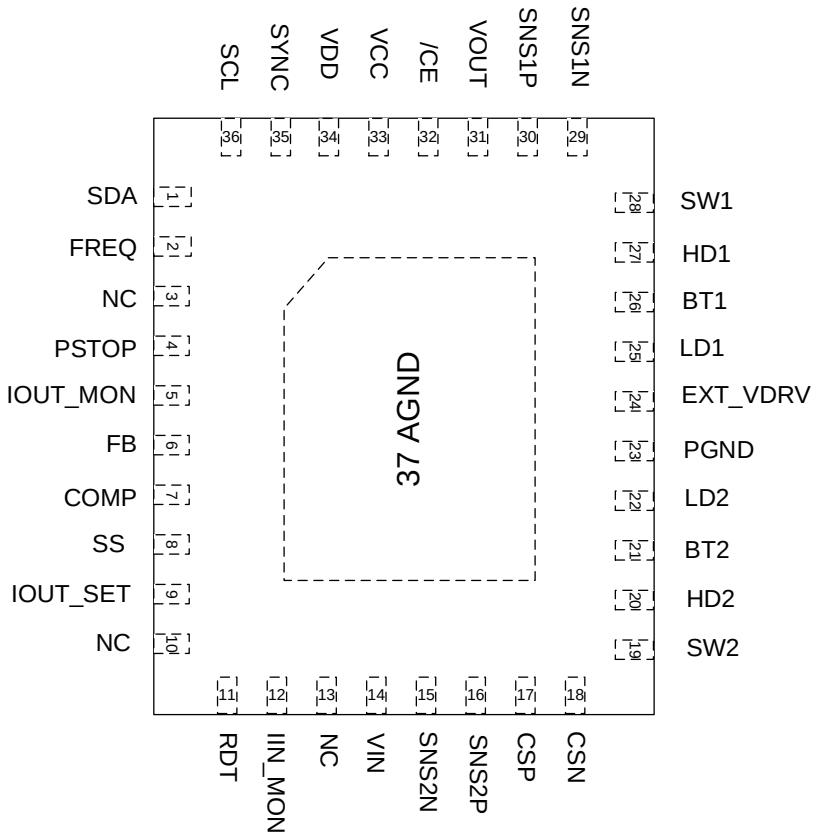


Typical Application Stand Alone

7 Terminal Configuration and Functions

TOP VIEW

QFN 5X6-36



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	SDA	I/O	I2C open-drain data I/O. Connect to data line from the host controller. Connect a 10kΩ pullup resistor according to I2C specifications.
2	FREQ	I	Switching frequency selection pin. Connect a resistor to grand to set switching frequency among 80kHz to 480kHz, the calculation formula is: F_{SW}(kHz) = 25000 / (R_{FREQ}+10) (kΩ)
3	NC	O	Not connected
4	PSTOP	I	Power stop pin. PSTOP is connected to VCC, the IC will stop switching; PSTOP is connected to ground, the IC will rework.
5	IOUT_MON	O	Output current monitoring output pin, connect a capacitor to GND. the calculation formula is: V_{IOUT_MON}=30*(V_{SNS1P}-V_{SNS1N})

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6	FB	I	Feedback input of VOUT, connect to resistor divider from VOUT.
7	COMP	O	Connect RC network with this pin to compensate the control loop.
8	SS	O	Soft-start setting pin. Connect a capacitor to configure soft start time. Typical capacitor value is 10nF
9	IOUT_SET	I	IOUT current limit setting pin. Set IOUT current by connecting a resistor to GND.
10	NC	O	Not connected
11	RDT	O	Dead time setting pin. Connect a resistor to GND to set a proper deadtime.
12	IIN_MON	O	IIN current monitoring input pin, connect a capacitor to GND. the calculation formula is: $V_{IIN_MON}=30*(V_{SNS2P}-V_{SNS2N})$
13	NC	O	Not connected
14	VIN	PWR	Input pin.
15	SNS2N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 5mΩ) on the power path to sense the current.
16	SNS2P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 5mΩ) on the power path to sense the current.
17	CSP	I	Positive input of Inductor current sense node.
18	CSN	I	Negative input of Inductor current sense node.
19	SW2	PWR	Switching node 2. Connect this pin to the inductor
20	HD2	O	Gate driver output to control the external high side power MOSFET(Q4).
21	BT2	PWR	Connect a 100nF capacitor between BT2 pin and SW2 pin to bootstrap a bias voltage for high side MOSFET driver.
22	LD2	O	Gate driver output to control the external low side power MOSFET(Q3).
23	PGND	I/O	Power ground.
24	EXT_VDRV	PWR	Gate driver supply input, Place at least 2.2μF ceramic capacitor near this pin to PGND pin close to the IC. Connect with external supply or connect directly to VCC.
25	LD1	O	Gate driver output to control the external low side power MOSFET(Q2).
26	BT1	PWR	Connect a 100nF capacitor between BT1 pin and SW1 pin to bootstrap a bias voltage for high side MOSFET driver.
27	HD1	O	Gate driver output to control the external high side power MOSFET(Q1).
28	SW1	PWR	Switching node 1. Connect this pin to the inductor
29	SNS1N	I	Negative input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 2mΩ) on the power path to sense the current.

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30	SNS1P	I	Positive input of a current sense amplifier. Connect to one pad of the current sense resistor (typical 2mΩ) on the power path to sense the current.
31	VOUT	PWR	Output pin.
32	/CE	I/O	IC enable pin. This pin is internally pulled low. When this pin is pulled high, IC is disabled. When this pin is pulled high. IC is reset and enter shutdown mode. /CE is also used for hardware rest function.
33	VCC	PWR	Output of an internal 5.25V LDO regulator. Connect a at least 2.2 μF ceramic capacitor from VCC to PGND pin close to the IC
34	VDD	PWR	Used for bias power supply. Connect a at least 2.2 μF ceramic capacitor from VDD to PGND pin close to the IC
35	SYNC	I	Frequency setting and external clock signal input pin, the internal frequency is synchronized to the external clock frequency when external clock signal is applied to this pin.
36	SCL	I	I2C clock input. Connect to clock line from the host controller. Connect a 10kΩ pullup resistor according to I2C specifications.
37	AGND	/	Connect to AGND with PGND.

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8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VOUT, VIN, SNS1N, SNS1P, SNS2N, SNS2P,	-0.3	88	V
	SW1, SW2	-0.3	88	V
	SW1, SW2 (200ns)	-1	88	V
	SW1, SW2 (10ns)	-5	100	V
	BT1-SW1, HD1-SW1, BT2-SW2, HD2-SW2,	-0.3	13.2	V
	BT1, BT2, HD1, HD2	-0.3	90	V
	SYNC, FREQ, /CE, PSTOP, FB, COMP, SS, SDA, SCL, IOUT_MON, IIN_MON, NTC, IOUT_SET, RDT	-0.3	6	V
	LD1, LD2	-0.3	13.2	V
	VCC,	-0.3	6	V
	EXT_VDRV	-0.3	13.2	V
	SNS1P to SNS1N, SNS2P to SNS2N	-0.3	0.3	V
	BT1 to SW1, BT2 to SW2, HD1 to SW1, HD2 to SW2	-0.3	13.2	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
VOUT	VOUT voltage range	3.3		80	V
VIN	VIN voltage range	4.5		80	V
T_A	Operating ambient temperature	-40		105	°C
T_J	Operating junction temperature	-40		125	°C

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R_{S1}	IOUT current sense resistor	2	2	10	mΩ
R_{S2}	IIN current sense resistor	2	5	10	mΩ
R_{S3}	Inductor peak/valley current sense resistor	2	3	5	mΩ
Inductance	L	4.7	10	47	μH
Fsw	Switching frequency	80	200	480	kHz

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8.4 Thermal Information

THERMAL RESISTANCE(1)		QFN-36 (5mmX6mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	33.7	°C/W
θ_{JC}	Junction to case thermal resistance	14.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	10.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

8.5 Electrical Characteristics

T_J= +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
I_{Q_VIN}	Quiescent current into VIN pins	VIN = 80V, DCDC is disabled, I2C enabled，VCC disable，ADC disabled, /CE= Low, Tj<85°C		40		μA
		VIN = VIN, No VOUT; VCC and I2C enabled，VDRV short to VCC, ADC all channel is enabled, /CE= Low, Tj<85°C		1200		μA
		VIN = 80V, /CE=high, in shutdown mode; Tj<85°C		5		μA
POWER SUPPLY						
V_{UVLO_VIN}	VIN under-voltage lockout threshold	VIN rising		4.5	4.7	V
		VIN falling	3.9	4.1		V
V_{CC}	VCC regulation voltage	VIN = 6V~80V	5	5.25	5.5	V
V_{DROP_VCC}	Drop out voltage of VCC regulator	VIN =5V, I_{VCC} = 20mA		100	200	mV
I_{VCC_LIM}	VCC regulator current capability	VIN = 10V, V_{CC} > 3V	70	130		mA
		VIN = 10V, V_{CC} = 1V		20	30	mA
Driver						
$V_{EXT_VDRV_UVLO}$	EXT_VDRV supply voltage to work	Rising edge		4.5	4.7	V
		Falling edge	3.9	4.1		V
$V_{EXT_VDRV_OVP}$	EXT_VDRV overvoltage	Rising edge		13	13.3	V
		Falling edge	12.3	12.6		V
$V_{DRV_ON_Q1_Q4}$	Buck/Boost high side driver turn on resistance	V_{BTx}-V_{SWx}=5.25V，100mA sourcing		0.1	0.2	V
$V_{DRV_OFF_Q1_Q4}$	Buck/Boost high side driver turn off resistance	V_{BTx}-V_{SWx} =5.25V，100mA sinking		0.04	0.15	V

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$I_{DRV_ON_Q1_Q4}$	Buck/Boost high side driver turn on resistance	V_{BTx} - V_{SWx} = 5.25V	1.5	3		A
$I_{DRV_OFF_Q1_Q4}$	Buck/Boost high side driver turn off resistance	V_{BTx} - V_{SWx} = 5.25V	1.5	3		A
$V_{BTx_REFRESH_TH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST1}-V_{SW1} when low side refresh pulse is requested	2.5	3.2	3.7	V
	Rising edge			3.4	3.8	V
$V_{DRV_ON_Q2_Q3}$	Buck/Boost low side driver turn on resistance	100mA sourcing		0.1	0.2	V
$V_{DRV_OFF_Q2_Q3}$	Buck/Boost low side driver turn off resistance	100mA sinking		0.05	0.15	V
$I_{DRV_ON_Q2_Q3}$	Buck/Boost low side driver turn on resistance	V_{EXT_DRV} = 5.25V	1.3	3		A
$I_{DRV_OFF_Q2_Q3}$	Buck/Boost low side driver turn off resistance	V_{EXT_DRV} = 5.25V	2	3		A
SWITCHING FREQUENCY						
F_{SW}	Switching frequency	R_{FREQ}= 52kΩ		400		kHz
		R_{FREQ}= 62.5kΩ		345		kHz
		R_{FREQ}= 115kΩ		200		kHz
		R_{FREQ}= 240kΩ		100		kHz
SYNC	SYNC pin threshold	Input high voltage threshold	1.3			V
		Input low voltage threshold			0.4	V
t_{SYNC_MIN}	Minimum external clock pulse width		100			ns
DEAD TIME SETTING						
t_{DT}	Dead time setting	R_{DT}= 0kΩ		40		ns
		R_{DT}= 10kΩ		55		ns
		R_{DT}= 27kΩ		70		ns
		R_{DT}= 51kΩ		85		ns
		R_{DT}= 100kΩ		100		ns
		R_{DT}= 200kΩ		115		ns
		R_{DT}= 510kΩ		130		ns
		R_{DT}= float		145		ns
CURRENT MONITOR						
V_{IOUT_MON}	Suggested IMON output voltage range		0		3	V
G_{IMON_IOUT}	IOUT current sensing ratio	V_{IOUT_MON} / $V_{SNS1P-SNS1N}$, R_{SNS1} = 2mΩ		30		V/V

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$V_{IMON_IOUT_ACC}$	IOUT current monitor accuracy in charging mode	VSNS1P-SNS1N=40mV IOUT = 20A, R_{SNS1} = 2mΩ	-3		3	%
		VSNS1P-SNS1N=20mV	-10		10	%
G_{IIN_MON}	IIN current sensing ratio	V_{IIN_MON} / $V_{SNS2P-SNS2N}$, R_{SNS2} = 5mΩ		30		V/V
$V_{IMON_IIN_ACC}$	IIN current monitor accuracy in charging mode	IIN = 20A, R_{SNS2} = 5mΩ	-1		1	%
		IIN = 10A, R_{SNS2} = 5mΩ	-2		2	%
		IIN = 1A, R_{SNS2} = 5mΩ	-20		20	%
REGULATION						
$V_{OUT_REG_INT}$	VOUT regulation accuracy	VOUT=5V setting	-3		3	%
		VOUT=20V setting	-2		2	%
		VOUT=28V setting	-3		3	%
		VOUT=48V setting	-2		2	%
$V_{OUT_EXT_FB}$	Output feedback reference voltage		1.112	1.123	1.134	V
I_{OUT_INT}	IOUT regulation accuracy	R_{SNS1}= 2mΩ，IOUT= 10A setting Set by reg	-3		3	%
		R_{SNS1}= 2mΩ，IOUT= 5A setting Set by reg	-6		6	%
I_{OUT_EXT}	IOUT regulation accuracy	R_{SNS1}= 2mΩ，IOUT= 10A setting Set by ext	-5		5	%
		R_{SNS1}= 2mΩ，IOUT= 5A setting Set by ext	-10		10	%
Protections						
$V_{OUT_ABS_OVP}$	VOUT abs OVP threshold	VOUT rising		82		V
		VOUT falling	78	80		V
$V_{IN_ABS_OVP}$	VIN abs OVP threshold	VIN rising	80	82	84	V
		VIN falling	78	80	82	V
V_{OUT_OVP}	VOUT OVP threshold, Output voltage set by Internal register	VOUT rising, as percentage of the regulation target, to stop switching	120	125	130	%
		VOUT falling, as percentage of the regulation target, to recover	115	120	125	%
V_{OUT_SHORT}	VOUT short threshold	VOUT falling, to stop switching	3	3.2	3.4	V
		VOUT rising, to recover	3.4	3.6	3.8	V
I_{VALLEY_CLP}	Cycle by cycle peak/valley current limit	3mΩ sense resistor		40		A
		3mΩ sense resistor		25		A
		3mΩ sense resistor		15		A
R_{OUT_DIS}	Discharging current at VOUT pin when VOUT OVP happens			7	12	kΩ
R_{IN_DIS}	Discharging current at VIN pin when VIN OVP happens			5	8	kΩ

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ADC					
ADC Frequency	Frequency of polling all ADC channels			900	Hz
ADC_VOUT	VOUT voltage reading	Range	0	81.9	V
		LSB		40	mV
ADC_VIN	VIN voltage reading	Range	0	81.9	V
		LSB		20	mV
ADC_IOUT	Input current reading, 2mΩ	Range	0	51187.5	mA
		LSB		25	mA
ADC_IIN	VIN input current reading, 5mΩ	Range	0	20.475	A
		LSB		10	mA
ADC_Error	Accuracy of ADC_IOUT		-8	8	LSB
I2C INTERFACE AND IO LOGIC					
V_{IL}	SCL, SDA input low voltage			0.4	V
V_{IH}	SCL, SDA input high voltage		1.2		V
f_{SCL}	I2C clock frequency			400	kHz
T_{dgl_I2C}	Deglitch time for I2C signal			50	ns
I_{SINK_SDA}	SDA pin sink current	V_{SDA} = 0.4V	70	100	mA
/CE IO LOGIC					
$R_{/CE}$	/CE pull down resistance			2.4	MΩ
V_{IL}	/CE input low voltage			0.4	V
V_{IH}	/CE input high voltage		1.2		V
t_{dgl_CE}	Deglitch time for /CE pin	Falling		5	μs
		Rising		5	μs
THERMAL REGULATION AND SHUTDOWN					
T_{SD}	Thermal shutdown temperature	Temperature rising, 150°C setting		150	°C
		Thermal shutdown hysteresis		20	°C
t_{SD}	Thermal shutdown deglitch time	Temperature rising		1	μs
		Temperature falling		1	μs

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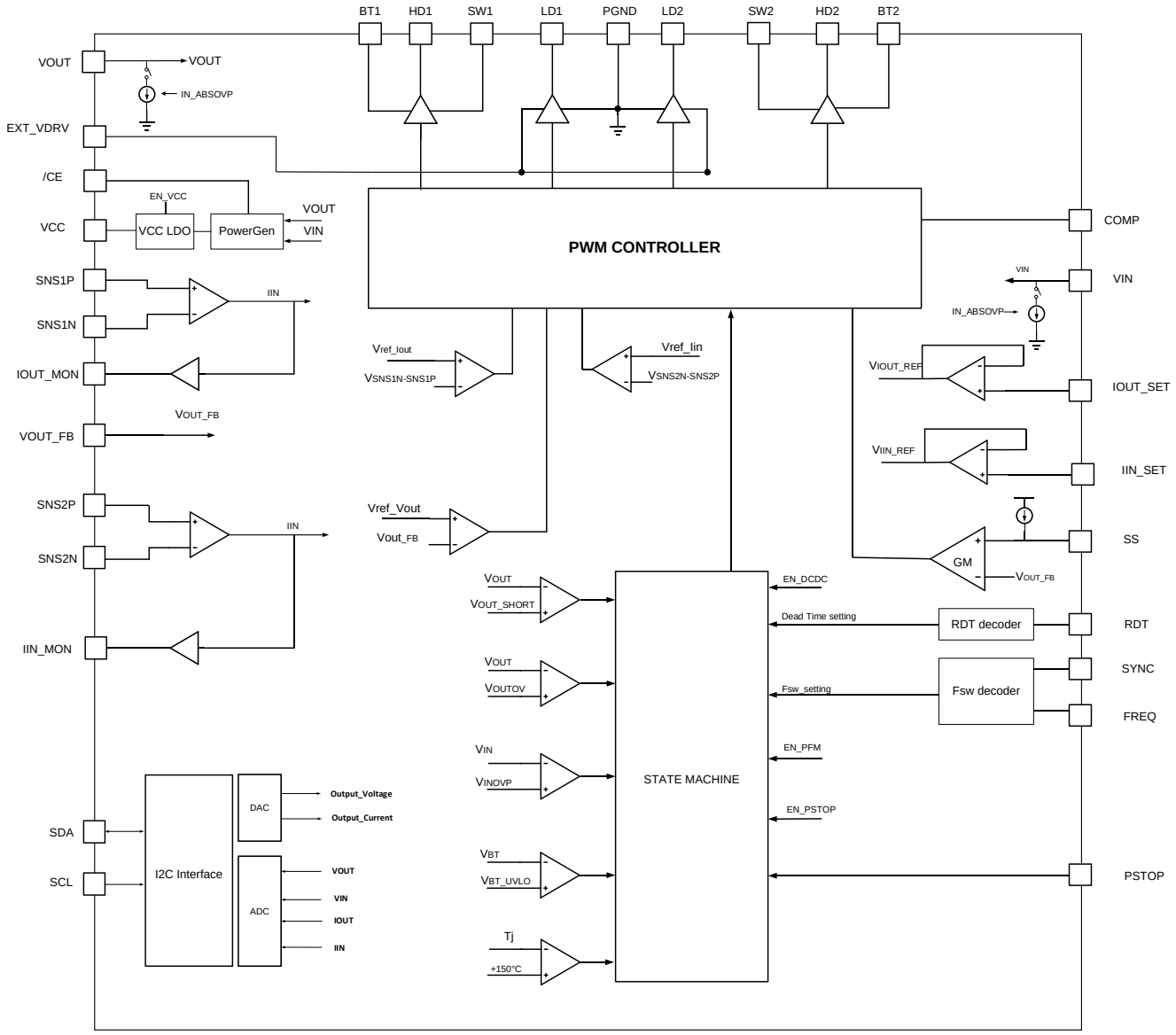
9 Function Block



10 Feature Description

10.1 POR

The IC is powered up when VIN > VIN_UVLO, and the I2C register becomes accessible to the host. The internal bias circuit of the IC is powered by VOUT or VIN pin.

10.1.1 Chip Enable and Shutdown Mode

The device adopts /CE pin as hardware IC enable pin. When the /CE pin is connected to logic HIGH, the IC is disabled and all the I2C registers is reset. Thus, /CE pin can be used as hardware reset function. Do not keep /CE pin float, an external pull-up or pull-down resistor is needed to establish a robust control logic.

When /CE is pulled down, IC consumes lower quiescent current from VIN pin by turning off most of block. VCC LDO is not activated.

10.1.2 Standby Mode

The device enters standby mode by set Reg0x10<1>=1. When IC enters standby mode, controller stop switching.

10.1.3 VCC regulator power up

VCC regulator provides operation current to the internal circuit of the IC, driver circuit can be powered by VCC or EXT_DRV. When VOUT and VIN are both higher than>7.7V, VCC is powered by the lower one of VOUT and VIN to minimize power consumption.

The VCC regulator can provide 130mA load capability, but its current limit is fold-back to 20mA(typ) when VCC is shorted to ground.

10.1.4 PSTOP

SC8708 also has power stop function by PSTOP pin. When PSTOP is connected to VCC, the IC will stop switching; and when PSTOP is connected to ground, the IC will rework. This function can be canceled by set Reg0x19<0>=1.

10.2 Output Voltage Setting

The SC8708's DCDC switching is enabled with all the following conditions are met:

- VIN >VIN_UVLO input voltage is valid
- $V_{DRV_UVLO} < V_{EXT_VDRV} < V_{DRV_OVP}$

after the above conditions are valid, converter starts and VOUT ramps up to target voltage.

VOUT voltage is set by VOUT_FB pin or internal register.

a) Set by External VOUT_FB pin (default)

The output voltage is set by the resistor divider connected at VOUT_FB pin and can be calculated as below.

$$VOUT = V_{FB_REF} \times (1+\frac{R_{UP}}{R_{DOWN}})$$

Where:

V_{FB_REF} is the internal reference voltage 1.123V.

R_{UP} and R_{DOWN} are the resistors connected from VOUT to FB and to AGND.

If external setting method is not needed, FB pin is not suggested to be float which may cause uncertain output voltage. It is better to connect FB pin to resistor divider to ensure that IC output is under regulation.

b) Set by Internal register VOUT Reg0x05/04

Output voltage is decided by Reg0x05/04, ranges from 5V to 48V.

- When Reg0x05<2>=0, VOUT voltage ranges from 5V to 21V, voltage step is 20mV
- When Reg0x05<2>=1, VOUT voltage ranges from 21.05 to 48V，voltage step is 50mV

Output voltage adjustment provides slew rate selection, set by Reg0x16<3:2>:

- 00: 0.05mV/μs
- 01: 0.2mV/μs
- 10: 0.5mV/μs(default)
- 11: 1mV/μs

10.3 Current Limit Setting

In order to support MFI, CC loop enter delay is adopted. After Output current exceeds setting limit and last for 1ms default set by Reg0x16<5:4>, CC loop takes over and output voltage drops to avoid overload.

10.3.1 Output Current limit setting

The actual output current limit can be set by Internal register or External IOUT_SET pin.

a) External setting: (Reg0x11<7>=1) (default)

$$I_{OUT_LIM} = \frac{V_{OUT_SET}}{20 \times R_{S2}}$$

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Where V_{IOUT_SET} is the voltage of IOUT_SET pin, R_{S2} is IOUT sense resistor, and I_{OUT_LIM} is input current limit.

b) Internal Register Setting (Reg0x11<7>=0)

- For 2m Ω , IOUT Range: 2375mA-50A, 7bit, step=375mA
- Default IOUT value is set to 5A

10.4 Frequency and SYNC function

The switching frequency can be set by a resistor between FREQ pin and GND. This pin must be pulled to PGND using a R_{FSW}, do not leave floating.

The frequency calculation formula is decided by design, value of resistor 10k~500kΩ is acceptable.

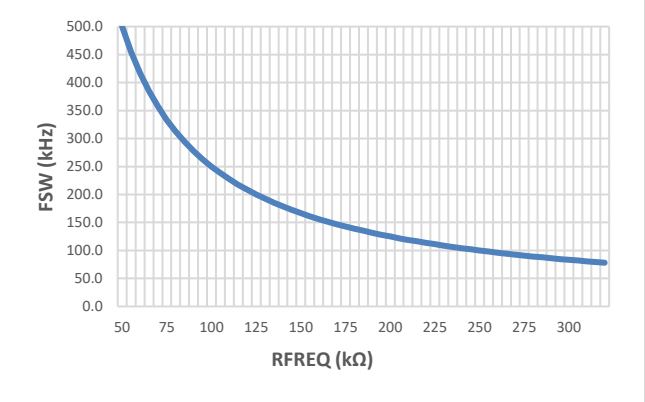
Besides, the SYNC pin can also be used to synchronize the internal oscillator to an external clock signal among 100kHz~480kHz. When SYNC function is used, the deviation between the frequency set by R_{FREQ} resistor and the external frequency shall not exceed 15%.

When SYNC pin is tied to GND or VCC, switching frequency is decided by FREQ setting resistor

Fsw(kHz)=25000 / (R_{FREQ}+10)

R_{FREQ}: Unit kΩ

Fsw: Unit kHz



10.5 Dead time selection function

The SC8708 detects RDT pin resistor and decides deadtime setting.

Configuration	Dead time
SHORT	40ns
RDT=10kΩ	55ns
RDT=27kΩ	70ns
RDT=51kΩ	85ns
RDT=100kΩ	100ns
RDT=200kΩ	115ns
RDT=510kΩ	130ns
OPEN	145ns

10.6 Soft-start SS pin function

The SC8708 integrates SS pin for soft-start control. The soft-start time is set by the value of the soft-start capacitor connected from SS to GND. Inrush current during start-up is alleviated by adjusting the soft-starting time.

The Calculation formula is as follow:

- Tss=Css*Vref/Iss
- Iss=1μA
- Vref is CV loop reference in VOUT reference

SS function is both valid for charging mode and discharging mode. The typical soft-start time is decided by design: value of resistor 1nF~100nF is acceptable.

10.7 IMON function

The IMON function keeps working when DIS_DCDC = 1 but is disabled to save power when /CE is pulled HIGH.

The IC monitors the SNS1P-SNS1N and SNS2P-SNS2N in real time. It can output a proportional voltage at IMON pin to the selected object as shown below, providing a way for MCU to monitor the IC input/output status.

Channel	GAIN	Range	IMON output（RATIO bit=00/01/10/11）
IOUT_MON	30x	V_{SNS1P-} V_{SNS1N}=100mV	3V, internal clamp to ~3.2V
IIN_MON	30x	V_{SNS2P-} V_{SNS2N}=100mV	3V, internal clamp to ~3.2V

10.8 PFM/PWM Mode

In order to improve converter light-load efficiency, IC switches to PFM operation at light load.

- Reg0x16<0>=1 (EN_PFM), PFM is enabled. Otherwise FPWM mode is selected.

10.9 ADC

The SC8708's ADC provide 2 working mode:

1) One-shot mode(default): Reg0x3B[6]=1, ADC_START=1 to enable one-shot conversion
2) Continuous mode

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Item	Range	Resolution
IOUT_ADC	0mA~51175mA	25mA/step，2mΩ
IIN_ADC	0mA~20470mA	10mA/step, 5mΩ
VOUT_ADC	0mV~81880mV	40mV/step
VIN_ADC	0mV~81880mV	40mV/step

10.10 Protection

SC8708 supports full protections including input overvoltage protection, overcurrent protection, and over temperature protection.

10.10.1 Cycle by Cycle Peak/Valley OCP

SC8708 provides cycle-by-cycle current limit to protect against overcurrent and short circuit conditions for charging and discharging mode. In buck mode, if the valley current detected by CSN-CSP in low-side buck exceed the current limit, the buck low side MOSFET is turned-on until the current falls down to current limit. In boost mode, If the peak current detected by CSP-CSN in low-side boost switch exceed the current limit, the boost switch is turned off for the rest of switching cycle. The current limit is set by internal register, 25A default for 3mΩ sense resistor.

10.10.2 VIN Absolute OVP

When input voltage VIN pin >82V, VIN absolute over-voltage protection is triggered, DCDC stop switching at once, Internal discharging current is pulled down automatically till OVP condition disappear

10.10.3 VOUT Relative OVP

If VOUT voltage is set by internal register, If output voltage > V_{OUT_OVP} (125%*VOUT), the DCDC stops switching at once and sets VOUT_OVP_STAT bit to 1. When output voltage falls below the threshold (120%*VOUT), the status bit is cleared and converter resumes switching.

If VOUT voltage is set by external VOUT_FB pin, No VOUT OVP protection is applied.

10.10.4 VOUT Absolute OVP

If VOUT_FB is short to ground, once the voltage at VOUT pin is detected higher than input overvoltage threshold (82V typ), DCDC stop switching at once, 10mA discharging current and is pulled down and VOUT_OVP_STAT is set to 1automatically until OVP condition disappear.

10.10.5 VOUT SHORT

If VOUT < $VOUT_{_SHORT}$(3.2V) is detected, the converter enters into hiccup mode: it stops switching for 500ms and VOUT_UVP_STAT is set to 1 to report the output short fault. Then IC restarts switching again. After 4ms switching blanking timer expire, if VOUT < $VOUT_{_SHORT}$ is still detected, and, the IC stops switching for 500ms, and then retries again.

When VOUT > $VOUT_{_SHORT}$, the fault is removed, and the status bit is read cleared.

10.10.6 Thermal Shutdown

Whenever the junction temperature exceeds the 150°C, IC stops switching and stays off until the junction temperature falls below 130°C. During thermal shut down, VCC LDO is off, IC is reset. When the temperature falls below 130°C, SC8708 restarts with soft start.

10.11 I2C Interface

10.11.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x6C (8-bit address is 0xD8 for write command, 0xD9 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

10.11.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

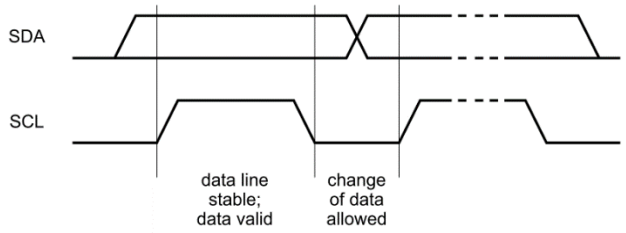

Figure 1 Bit transfer on the I2C bus

10.11.1.2 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to

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HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

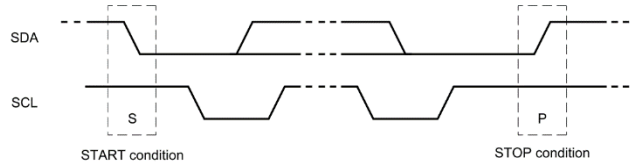

Figure 2 START and STOP conditions

10.11.1.3 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

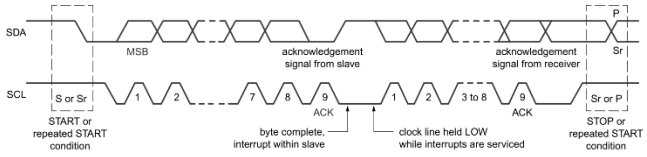

Figure 3 Data transfer on the I2C bus

10.11.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

10.11.1.5 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

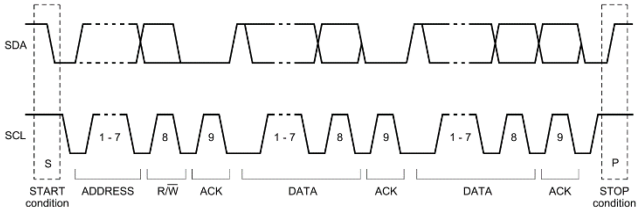

Figure 4 A complete data transfer

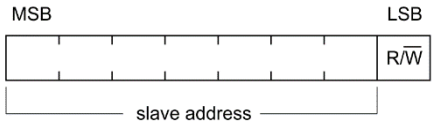

Figure 5 The first byte after the START procedure

10.11.1.6 Single Read and Write

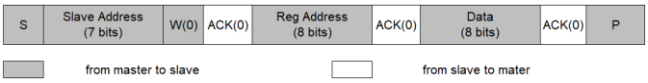

Figure 6 Single Wite

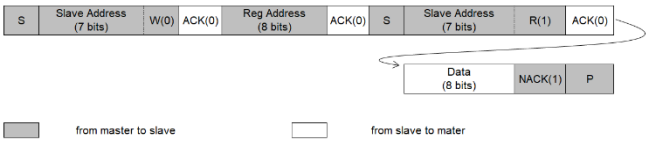

Figure 7 Single Read

If the register address is not defined, the IC send back NACK and go back to the idle state.

10.11.1.7 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

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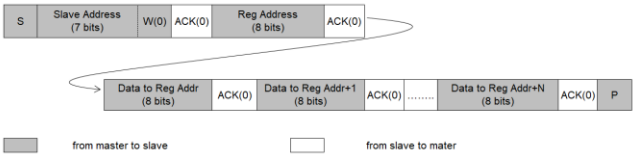

Figure 8 Multi-Write

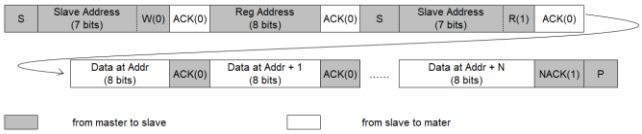

Figure 9 Multi-Read

11 Application Information

11.1 HV Buck Voltage

The voltage of a typical HV buck is set to not exceed 10V.

If the layout, especially the layout traces related to the driver, are too long, it is necessary to consider the damage to the chip caused by voltage spikes, and the output voltage of the external HV Buck can be adjusted down to 8V.

11.2 COMP Network

For comp to ground, generally using 10k + 10nF can meet most requirements.

If you need to speed up the loop, you can increase R and decrease C; conversely, if you want to slow down the loop, decrease R and increase C, while trying to keep the RC product constant during this process.

Additionally, when the current is very large or external voltage regulation is used, connect a capacitor of 100 pF or more in parallel to ground on comp.

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12 Layout Guide

12.1 Schematic Diagram Suggestions:

1. A 330nF resistor must be connected between BT1 and SW1 & BT2 and SW2, and a diode must be connected from VCC to BT1. The diode is a fast recovery diode with sufficient voltage withstand capability.
2. EXT VDRV/VCC/VIN/OUT pins must each be connected to at least 1uF MLCC
3. The COMP pin is connected to RC, with typical values of 10k/10nF, in parallel with 100pF, and the ground is connected to AGND
4. IBAT_MON/IBUS_MON/IBAT_SET/IBUS_SET pin components are grounded to AGND
5. FB voltage divider resistor is grounded to AGND
6. DT/FREO/RDT Ground Connected to AGND
7. AGND and PGND must be connected at a single point.

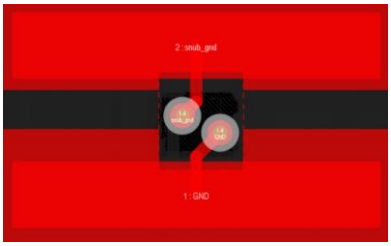
12.2 CSP/CSN

CSP/CSN pin is the chip sampling inductor current.

The chip uses peak/valley current mode, so it has relatively high requirements for inductor current sampling and should follow the following principles

12.2.1 Kelvin Sense

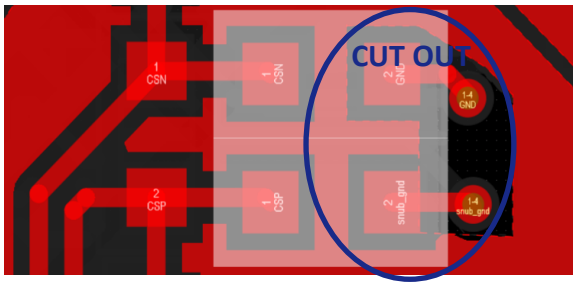
The sampling point of CSP/CSN is placed in the middle of the sense resistor.



CSP/CSN traces should be routed to avoid other high-frequency interference signals (such as drive signals, SW signals) as much as possible

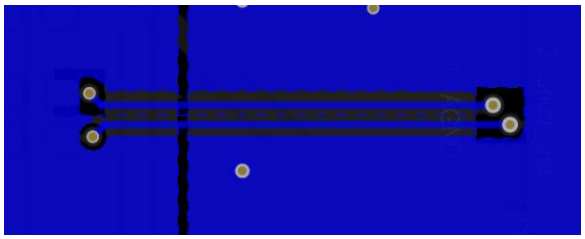
12.2.2 Copper Cut out

When laying copper, be careful not to cover the GND of the sampled differential traces (which also includes the subsequent filtering resistors and capacitors), and add a single cut out for separation on each layer.



12.2.3 Traces short

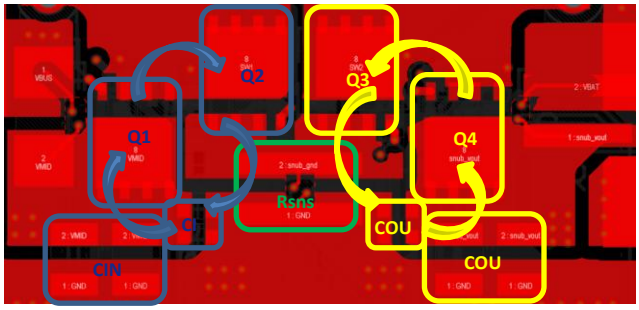
If the current is very large, the traces of CSP/CSN should be connected to the sampling resistor and the chip with the shortest possible length.



12.3 Power Trace

1, The hot loop formed by the input power path Cin→Q1→Q2→Sense resistor should be kept as small as possible.

2, The hot loop formed by the output power path Cout→Q3→Q4→Sense resistor should be as small as possible.



12.4 SNS1P/SNS1N/SW1

SNS1N-SW1 is used for Q1 ZCD detection, and it is recommended that the trace be routed as close as possible to the Drain-source sampling of Q1.

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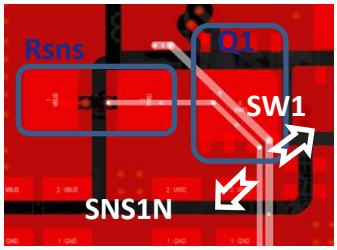
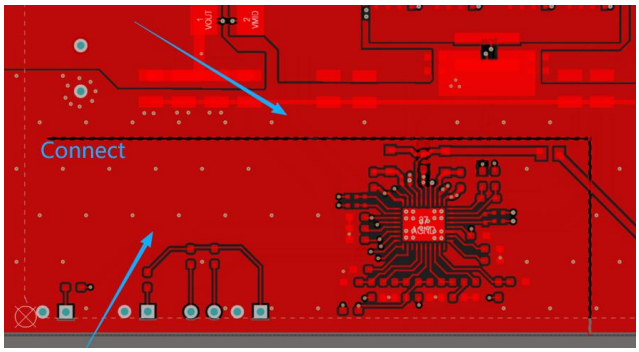
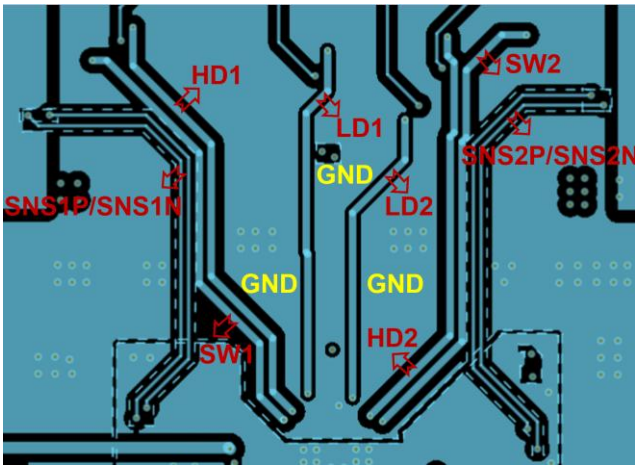


Differential traces of SNS1P-SNS1N-SW1.



12.5 Drive Trace



When driving high-power transistors, check if the driving power supply traces (HS/LD/SW/BOOT/VDRIVE, etc.) are wide enough, and it is recommended to be greater than 20 mils.

The driving traces HS and SW are parallel, LS and GND are parallel, and HS and LS should be avoided being parallel as much as possible to prevent interference.

The LD trace and the SW of the MOS should also avoid overlapping on the upper and lower layers to reduce the interference of SW on LD.

The BT capacitor should be placed as close as possible to the chip and directly connected to the SW-BT pin of the chip nearby.

12.6 AGND/PGND

The VCC capacitor is connected to AGND.

The AGND and PGND of the chip pins cannot be directly connected; instead, they require separate copper pours for each and should be separated on each layer.

The connection between AGND and PGND should be near the ground of the input or output capacitor, which can effectively avoid the impact caused by PGND fluctuations.

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13 Register Map (Address: 0x6C, 7bit)

ADDR	Name	R/W	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04H	VOLTAGE	R/W	01111011	VOLTAGE							
0x05H		R/W	xxxxx000	RESERVED					VOLTAGE		
0x06H	CURRENT	R/W	x0000111	RESERVED	CURRENT						
0x0FH	VOLTAGE OFFSET	R/W	00000000	RESERVED				VOLTAGE OFFSET			
0x10H	OPTION0	R/W	11110100	RESERVED						DIS_DCDC	REG_RESET
0x11H	OPTION1	R/W	11011001	IOUT_SET_SEL	RESERVED	EN_DITHERING	RESERVED				EN_LPM
0x12H	OPTION2	R/W	00001100	IOUT_MON_RATIO	RESERVED	IIN_MON_RATIO	RESERVED	EN_IOUT_MON	EN_IIN_MON	IL_AVG	
0x16H	OPTION3	R/W	01101011	RESERVED	FB_SEL	CC LOOP_ENTER_DLY_SEL		SR_SEL		RESERVED	EN_PFM
0x17H	OPTION4	R/W	00010101	RESERVED			ADC_FREQ_SEL	EN_VOUT_PD	EN_AUTO_IIN_DCHG	RESERVED	EN_VINOV
0x19H	JEITA CONTROL1	R/W	01010100	RESERVED							EN_PSTOP
0x1AH	ADC CONTROL	R/W	00000000	ADC_EN	ADC_MODE	ADC_START	EN_ADC_IOUTT	EN_ADC_IIN	EN_ADC_VOUT	EN_ADC_VIN	RESERVED
0x20H	STATUS0	R	00000000	IOUTREG_STAT	RESERVED			VOUTOV_STAT	VINOV_STAT	IL_MAX_CLP_STAT	RESERVED
0x21H	STATUS1	R	00000000	RESERVED						OVP_STAT	UVP_STAT
0x22H	STATUS2	R	00000000	RESERVED							SYNC_STAT
0x32H	ADC IOUT	R	00000000	ADC_IOUT							
0x33H		R	00000000	RESERVED					ADC_IOUT		
0x36H	ADC IIN	R	00000000	ADC_ IIN							
0x37H		R	00000000	RESERVED					ADC_ IIN		
0x38H	ADC VOUT	R	00000000	ADC_ VOUT							
0x39H		R	00000000	RESERVED					ADC_ VOUT		
0x3AH	ADC VIN	R	00000000	ADC_VIN							
0x3BH		R	00000000	RESERVED					ADC_VIN		

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13.1 REG 0x04H: VOLTAGE

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	OTG Voltage	R/W	000-01111011	Default:5000mV Range1:5000mV–21000mV (BIT 10=0) <20: gain> <540: offset> Range2:21050mV–48000mV (BIT 10=1) <50: gain> <21050: offset>

13.2 REG 0x06H: CURRENT

Bit	Bit Name	Type	Default	Description
7	Reserved	R	0	Reserved
6:0	OTG Current	R/W	0000111	Range:2375mA–50000mA Default:5000mA <375: gain> <2375: offset>

13.3 REG 0x0FH: VOLTAGE OFFSET

Bit	Bit Name	Type	Default	Description
7:4	Reserved	R	0000	Reserved
3:0	VOLTAGE_OFFSET	R/W	0000	VOLTAGE_OFFSET: 0000: 0mV(default) 0001: 50mV

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				0010: 100mV 0011: 150mV 0100: 200mV 0101: 250mV 0110: 300mV 0111: 350mV 1000: 400mV 1001: -50mV 1010: -100mV 1011: -150mV 1100: -200mV 1101: -250mV 1110: -300mV 1111: -350mV

13.4 REG 0x10H: OPTION0

Bit	Bit Name	Type	Default	Description
7:2	Reserved	R/W	000011	Reserved
1	DIS_DCDC	R/W	0	DIS_DCDC 0: enable DCDC (Default) 1: disable DCDC
0	Reg_Reset	R/W	0	Reg_Reset 0: Normal (default) 1: Reset registers to default values and reset timer

13.5 REG 0x11H: OPTION1

Bit	Bit Name	Type	Default	Description
7	IOUT_SET_SEL	R/W	1	IOUT_SET_SEL

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				0: set by OTG current 1: SET by IOUT_SET pin(default)
6	Reserved	R	0	Reserved
5	EN_Dithering	R/W	0	EN_Dithering 0: disable(default) 1: enable
4:1	Reserved	R	0	Reserved
0	EN_LPM	R/W	1	EN_LPM 0: disable 1: enable(default)

13.6 REG 0x12H: OPTION2

Bit	Bit Name	Type	Default	Description
7	IOUT_MON_RATIO:	R/W	0	IOUT_MON_RATIO: 0: 1x (default) 1: 2x:
6	Reserved	R	0	Reserved
5	IIN_MON_RATIO:	R/W	0	IIN_MON_RATIO: 0: 1x (default) 1: 2x
4	Reserved	R	0	Reserved
3	EN_IOUT_MON	R/W	1	EN_IOUT_MON 0: disable 1: enable (default)
2	EN_IIN_MON	R/W	1	EN_IIN_MON 0: disable

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				1: enable （default）
1:0	IL_AVG	R/W	00	IL_AVG 00: 25A(default) 01: 15A 10: 40A 11: 40A

13.7 REG 0x16H: OPTION3

Bit	Bit Name	Type	Default	Description
7	Reserved	R/W	1	Reserved
6	FB_SEL	R/W	1	FB_SEL 0: Voltage is set by internal register 1: Voltage is set by external FB pin (default)
5:4	CC Loop_Enter_Dly_Sel	R/W	10	CC Loop_Enter_Dly_Sel: 00: 0 01: 500us 10: 1ms （default） 11: 2ms
3:2	SR_SEL	R/W	10	Slew rate selection: 00: 0.05mV/us 01: 0.2mV/us 10: 0.5mV/us(default) 11: 1mV/us
1	Reserved	R/W	1	Reserved
0	EN_PFM	R/W	1	EN_PFM 0: disable PFM 1: enable PFM (default)

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13.8 REG 0x17H: OPTION4

Bit	Bit Name	Type	Default	Description
7:5	Reserved	R	0	Reserved
4	ADC_freq_sel	R	1	ADC_freq_sel: 0:10k 1:5k（default）
3	EN_VOUT_PD	R/W	0	EN_VOUT_PD 0: Disable(default) 1: Enable pull-down from VOUT
2	EN_AUTO_IIN_DCHG	R/W	1	EN_AUTO_IIN_DCHG 0: The DCDC will NOT apply a discharging current on VIN during VIN OVP triggered 1: The DCDC will apply a discharging current on VIN during VIN OVP triggered (default)
1	Reserved	R/W	0	Reserved
0	EN_VINOV	R/W	1	EN_VINOV 0: disable DCDC when VINOVP occurs 1: enable DCDC when VINOVP occurs (default)

13.9 REG 0x19H: JEITA CONTROL1

Bit	Bit Name	Type	Default	Description
7:1	Reserved	R/W	01	Reserved
0	EN_PSTOP	R/W	0	0: Enable PSTOP function (Default) 1: Disable PSTOP function

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13.10 REG 0x1AH: ADC CONTROL

Bit	Bit Name	Type	Default	Description
7	ADC_EN	R/W	0	ADC_EN 0: disable （default） 1: enable
6	ADC_MODE	R/W	0	0: Continuous mode（default） 1: One_shot mode
5	ADC_START	R/W	0	ADC_START 0: ADC conversion done in one-shot mode（default） 1: Initial One_shot ADC conversion
4	EN_ADC_IOUT	R/W	0	EN_ADC_IOUT 0: disable(default) 1: enable
3	EN_ADC_IIN	R/W	0	EN_ADC_IIN 0: disable(default) 1: enable
2	EN_ADC_VOUT	R/W	0	EN_ADC_VOUT 0: disable(default) 1: enable
1	EN_ADC_VIN	R/W	0	EN_ADC_VIN 0: disable(default) 1: enable
0	Reserved	R/W	0	Reserved

13.11 REG 0x20H: STATUS0

Bit	Bit Name	Type	Default	Description

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7	IOUTREG_ STAT	R	0	IOUT regulation status bit: 0: IC is not in IOUT regulation 1: IC is in IOUT regulation
6:4	Reserved	R	0	Reserved
3	VOUTOV_STAT	R	0	VOUTOV_STAT 0: no in VOUTOV fault 1: is in VOUTOV fault
2	VINOV_STAT	R	0	VINOV_STAT 0: no VINOV fault 1: is in VINOV fault
1	IL_MAX_CLP_STAT	R	0	IL_MAX_CLP_STAT 0: Peak/Valley current clamp is not triggered 1: Peak/Valley current clamp is triggered
0	Reserved	R	0	Reserved

13.12 REG 0x21H: STATUS1

Bit	Bit Name	Type	Default	Description
7:2	Reserved	R	000	Reserved
1	OVP_STAT	R/W	0	Over voltage protection status bit: 0: IC is not in OVP 1: IC is in OVP
0	UVP_STAT	R/W	0	Under voltage protection status bit: 0: IC is not in UVP 1: IC is in UVP

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13.13 REG 0x22H: STATUS2

Bit	Bit Name	Type	Default	Description
7:1	Reserved	R/W	0	Reserved
0	SYNC_STAT	R/W	0	SYNC_STAT 00: Normal mode 01: Frequency is SYNC with external clock mode

13.14 REG 0x32H: ADC IOUT

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_IOUT	R/W	000-00000000	Range: 0mA – 51187mA Default: 0mA <25: gain> <0: offset>

13.15 REG 0x36H: ADC_IIN

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_IIN	R/W	000-00000000	Range: 0mA – 20475mA Default: 0mA <10: gain> <0: offset>

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13.16 REG 0x38H: ADC_VOUT

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_VOUT	R/W	000-00000000	Range: 0mV – 81900mV Default: 0mV <40: gain> <0: offset>

13.17 REG 0x3AH: ADC_VIN

Bit	Bit Name	Type	Default	Description
15:11	Reserved	R	00000	Reserved
10:0	ADC_VIN	R/W	000-00000000	Range: 0mV – 81900mV Default: 0mV <40: gain> <0: offset>

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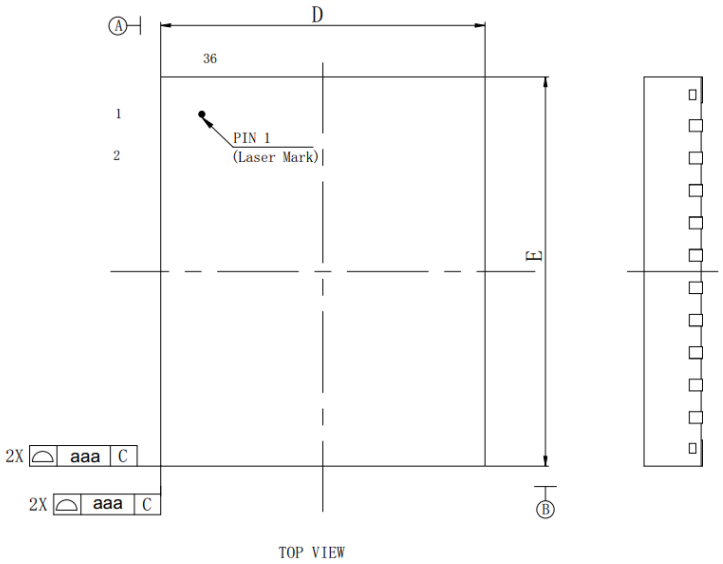
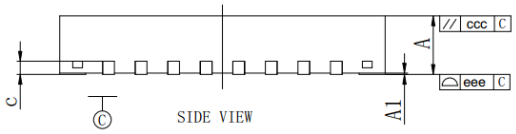
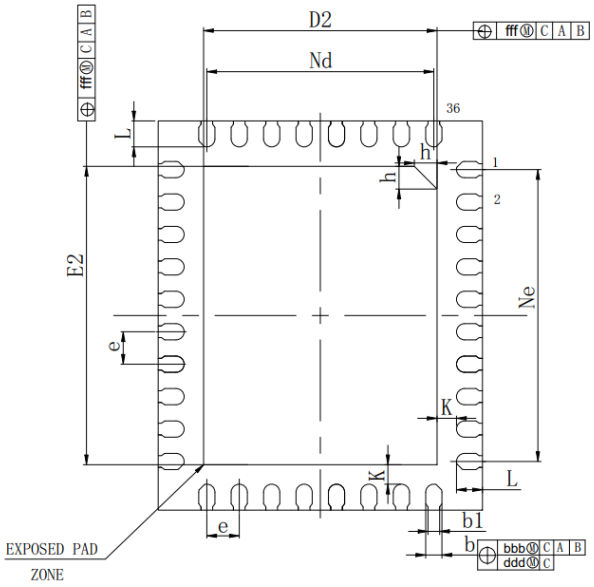
MECHANICAL DATA

QFN 5x6-36







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.203REF	
D	4.90	5.00	5.10
E	5.90	6.00	6.10
e		0.50BSC	
D2	3.50	3.60	3.70
E2	4.50	4.60	4.70
Nd		3.50BSC	
Ne		4.50BSC	
L	0.35	0.40	0.45
K		0.30REF	
h	0.30	0.35	0.40
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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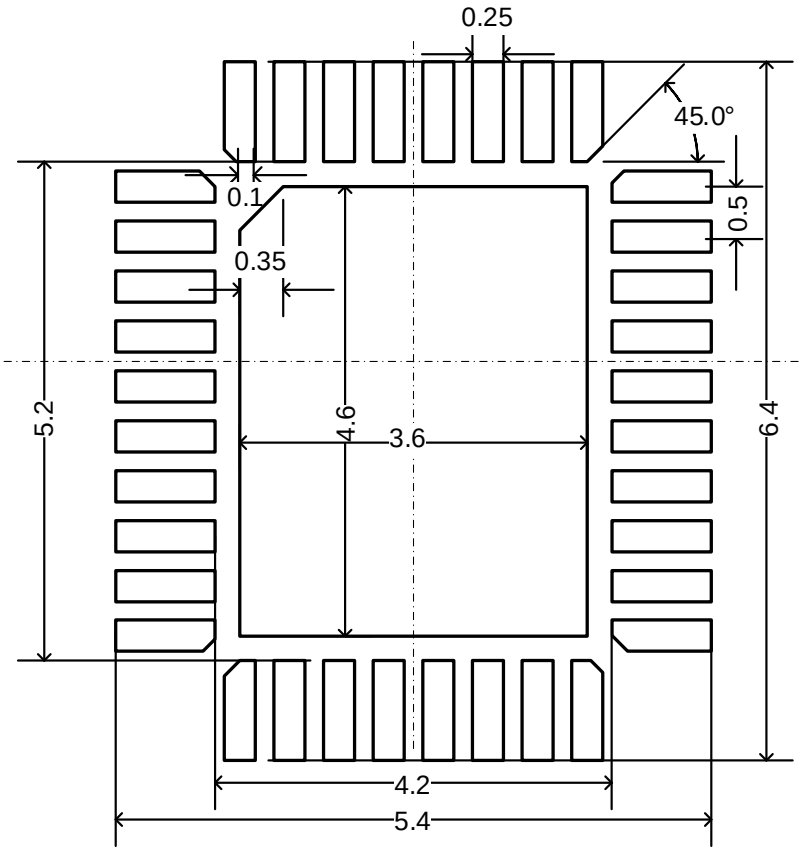
RECOMMENDED FOOTPRINT



NOTES:

A. All linear dimensions are in millimeters

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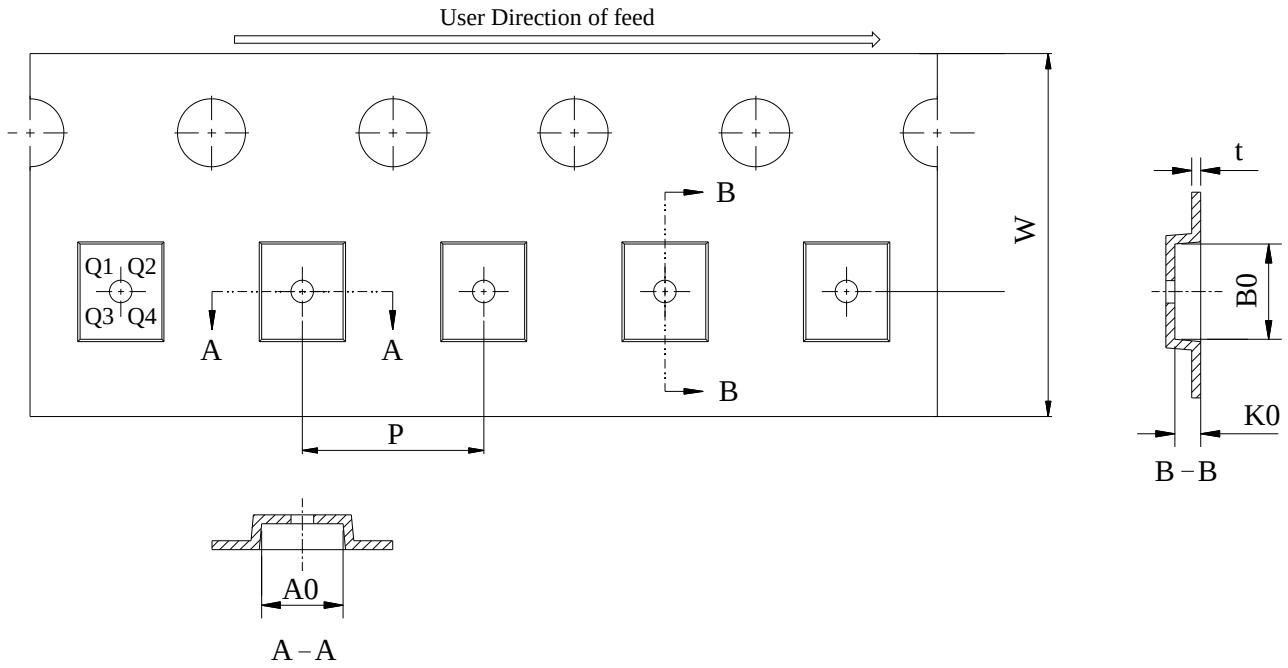
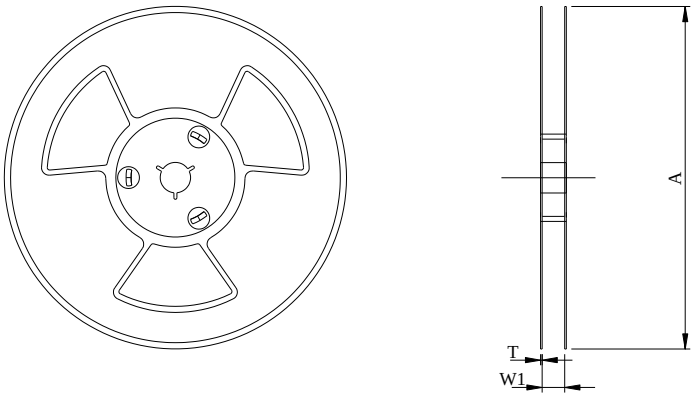
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12±0.2	8±0.1	5.3±0.1	6.3±0.1	1.2±0.1	0.3±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	329±1	12.4^{+2}_{0}	2.0±0.3

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