



SC77101Q Single Channel 90-mΩ Smart High Side Driver with Advanced Protections and Diagnostics

1 Descriptions

The SC77101Q device is a fully-protected single channel smart high-side switch, with an integrated 90-mΩ NMOS power FET. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. External adjustable current limit improves reliability of the whole system by limiting the inrush or overload current.

2 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: - 40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C4B
- Functional Safety Capable
 - Documentation Available to Aid Functional Safety System Design
- Single-Channel 90-mΩ Smart High-Side Switch with Full Diagnostics
 - Version A: Open-Drain Status Output
 - Version B: Current Sense Analog Output
- Wide Operating Voltage 4V to 40 V
- Ultralow Standby Current < 500 nA
- Operating Junction Temperature: - 40 to 150°C
- Input control: 3.3-V and 5-V Logic Compatible
- High Accuracy Current Sense:
 - Error <±25 mA at 500 mA
 - Error <±4 mA at 5 mA
- Adjustable Current Limit with External Resistor: Accuracy ±20% when >500-mA Load
- Protections:
 - Short-to-GND Protection by Current Limit (Internal or External)
 - Thermal Shutdown and Thermal Swing with Self-recovery
- Inductive Load Negative Voltage Clamp with Optimized Slew Rate
- Loss of GND and Loss of Battery Protection
- Undervoltage Lockout (UVLO) Protection
- Diagnostics:
 - On-state and Off-state: Output Open and Short-to-battery Detection
 - Overload and Short-to-ground Detection and Current Limit
 - Thermal Shutdown / Thermal Swing Detection

3 Applications

- High Side Power Switch for Sub-module
- Power Switch for Low-wattage Lamp
- High Side Relays and Solenoids
- General Resistive, Inductive and Capacitive Loads



4 Device Information

ORDER NUMBER	DIAGNOSTIC TYPE	PACKAGE	BODY SIZE
SC77101AQSTER	Open Drain Status Output	eTSSOP-14	4.40mm x 5.00 mm x 1.2mm
SC77101BQSTER	Current Sense & Diagnostic	eTSSOP-14	4.40mm x 5.00 mm x 1.2mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
1.0	2023.5.18	New	Initial Version.
1.3.0	2023.9.10	Page 1	Change from "100 mΩ NMOS power FETs" to "90 mΩ NMOS power FETs"
1.3.5	2024.2.9	Page 20	Add Tape & Reel Information
1.3.6	2024.3.5	Page 7, 8, 9	Update parameter limit.
1.3.7	2025.4.30	Page 19, 20	Add Layout chapter



6 Typical Application Circuit

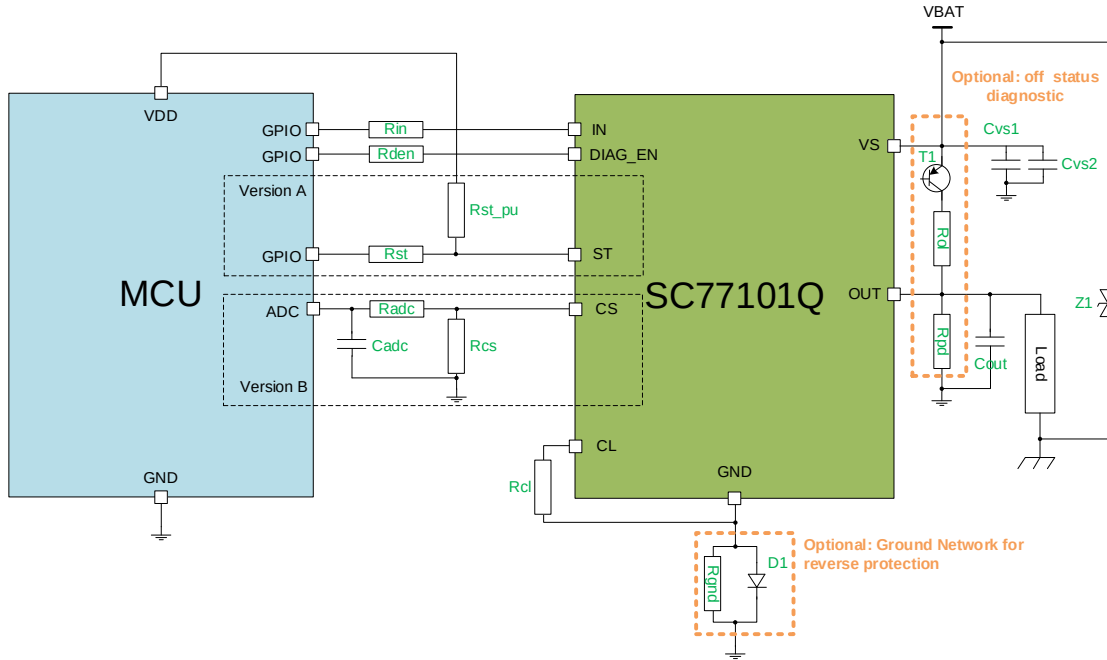


Figure 6-1. Typical Application Circuit

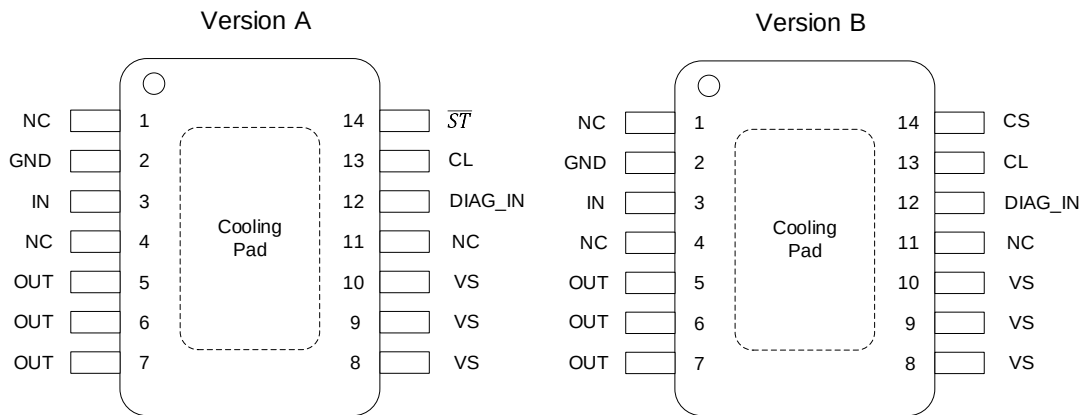
NAME	USED OR NOT		VALUE	DESCRIPTION
	VER. A	VER. B		
Rin	Y	Y	10kΩ	Current limit resistor, protection of micro-controller for overvoltage.
Rden	Y	Y	10kΩ	Current limit resistor, protection of micro-controller for overvoltage.
Rst	Y	N	10kΩ	Current limit resistor, protection of micro-controller for overvoltage.
Rst_pu	Y	N	10kΩ	Pull up resistor for open drain output ST.
Radc	N	Y	10kΩ	Current limit resistor, protection of micro-controller for overvoltage and also used as RC filter of CS signal.
Cadc	N	Y	1nF	Used as RC filter of CS signal. A time constant (Radc * Cadc) longer than 10 μs is recommended.
Rcs	N	Y	Configurable	Current sense resistor for current sensing. Keep it floating if it is not used.
Rcl	Y	Y	Configurable	Current limit resistor used for external current limit setting. Connect it to GND if no external current limit is used.
Rgnd	O	O	1kΩ	Used for reverse protection.
D1	O	O	VF<0.3V	Used for reverse protection.
T1	O	O	—	Switch for Open Load in OFF status diagnostic.
Rol	O	O	1.5kΩ	To enable Open Load detection in OFF diagnosis.
Rpd	O	O	47kΩ	Used to distinguish between Open Load and Short to VS in OFF Diagnosis.
Cvs1	Y	Y	100nF	Filtering of voltage spikes on the battery line.
Cvs2	Y	Y	1uF	Filtering of voltage spikes on the battery line.
Cout	Y	Y	10nF	Protection of output for ESD & EMC.
Z1	Y	Y	36 V TVS Diode	Transient Voltage Suppressor diode.

Note: Y – Yes; N – No; O – Optional



7 Terminal Configuration and Functions

TOP VIEW



NUMBER	TERMINAL		I/O	DESCRIPTION
	NAME VER. A	NAME VER. B		
1	N.C.	N.C.	—	Not connected.
2	GND	GND	—	Ground pin.
3	IN	IN	I	Input signal for channel on/off control.
4	N.C.	N.C.	—	Not connected.
5	OUT	OUT	O	High side output, connected to load.
6	OUT	OUT	O	Same as pin 5.
7	OUT	OUT	O	Same as pin 5.
8	VS	VS	I	Power supply, connected to 12V.
9	VS	VS	I	Same as pin 8.
10	VS	VS	I	Same as pin 9.
11	N.C.	N.C.	—	Not connected.
12	DIAG_EN	DIAG_EN	I	Enable signal (high active) for diagnostic function. Connect to device GND if not used.
W13	CL	CL	O	Programmable pin for current limit value. Connect to device GND if external current limit is not used.
14	$\overline{ST}$	CS	O	For version A, open-drain diagnostic status output (low active). Leave floating if not used. For version B, current sense output. Leave floating if not used.
Cooling Pad	—	—	—	Cooling pad. Connect to device GND or leave floating.



8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	Supply voltage ⁽³⁾⁽⁴⁾	-0.3 -18	48	V
	Voltage on IN and DIAG_EN pin	-0.3	7	V
	Voltage on $\overline{ST}$ and CL pin	-0.3	7	V
	Voltage on CS pin	-2.7	7	V
Current range at terminals ⁽²⁾	DC current on OUT pin		Internally limited	A
	Current on GND pin	-50 -250 ⁽⁵⁾	20	mA
	Current on IN and DIAG_EN pin	-30	2	mA
	Current on $\overline{ST}$ pin	-30	10	mA
	Current on CL and CS pin	-2	30	mA
f _{IN,MAX}	PWM frequency on IN pin		2	KHz
T _A	Operating ambient temperature range	-40	125	°C
T _J	Operating junction temperature range	-40	150	°C
T _{STG}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Supply voltage to withstand 48V load dump test for 400ms, according to ISO 16750-2:2010 Test B
- (4) Reverse polarity condition: t < 60 s, reverse current < I_{OUT,REV1}, GND pin 1-kΩ resistor in parallel with diode.
- (5) For limited time range: t < 120s

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	VS, OUT, GND	-5	5	kV
		All other pins	-4	4	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾		-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per AEC-Q100-002. The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
- (3) Level listed above is the passing level per AEC-Q100-011.



8.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V _S	Voltage on VS pin	5	13.5	28	V
	Voltage on IN and DIAG_EN pin	0		5	V
	Voltage on $\overline{ST}$ pin	0		5	V
I _{OUT,NOM}	Nominal DC load current	0		4	A
T _A	Operating ambient temperature	-40		125	°C
T _J	Operating junction temperature	-40		150	°C



8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		eTSSOP14 (4.4mm x 5.0mm)	UNIT
R _{ΘJA}	Junction to ambient thermal resistance ⁽²⁾	41	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	25	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

(2) The thermal data is based on JESD 51-7 & JESD 51-5. The copper pad is soldered to the thermal land pattern

8.5 Electrical Characteristics

-40°C < T_J < 150°C and 5V < V_S < 40V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{S,NOM}	Nominal operating voltage		5	13.5	40	V
V _{S,EXT}	Extended operating voltage	R _{DS(on)} value increase maximum 20%, compared to 5V, see R _{DS(on)} parameter	3.5		5	V
V _{S,UVR}	Undervoltage restart	V _S rises up from 0V, the device would turn on when V _S > V _{S,UVR}	3.5	3.7	4	V
V _{S,UVF}	Undervoltage shutdown	V _S falls down from 13.5V, the device would shutdown when V _S < V _{S,UVF}	3	3.2	3.5	V
V _{S,UVhys}	Undervoltage shutdown, hysteresis			0.5		V
OPERATING CURRENT						
I _{GND,NOM}	Nominal operating current	V _{IN} =5V, V _{DIAG_EN} =0V, without load			5	mA
		V _{IN} =5V, V _{DIAG_EN} =0V, with 10Ω load			10	mA
I _{VS,SLP}	Current @sleep mode ⁽¹⁾	V _S =13.5V, V _{IN} =V _{DIAG_EN} = V _{CS} = V _{CL} = V _{OUTPUT} =0V, T _J =25°C			0.5	uA
		V _S =13.5V, V _{IN} =V _{DIAG_EN} = V _{CS} = V _{CL} = V _{OUTPUT} =0V, T _J =85°C			0.5	uA
		V _S =13.5V, V _{IN} =V _{DIAG_EN} = V _{CS} = V _{CL} = V _{OUTPUT} =0V, T _J =125°C			5	uA
I _{VS,STBY}	Current @standby mode with diagnostic enable	V _{IN} =0V, V _{DIAG_EN} =5V			1.2	mA
t _{OFF,DEG}	Standby mode deglitch time	IN from high to low, the device enters into standby mode, if deglitch time > t _{OFF,DEG}		12.5		ms
I _{OFF}	Output leakage current @ off-state	V _S =13.5V, V _{IN} =V _{OUTPUT} =0V, T _J =25°C			0.5	uA
		V _S =13.5V, V _{IN} =V _{OUTPUT} =0V, T _J =125°C			3	uA
POWER STAGE						
R _{DS,ON}	Output resistance @ on-state	V _S >5V, T _J =25°C, I _{OUT} =1A		88	100	mΩ
		V _S >5V, T _J =150°C, I _{OUT} =1A			166	mΩ



		$V_S=3.5V, T_J=25^{\circ}C, I_{OUT}=1A$	120	mΩ
$I_{LIM,INT}$	Internal current limit		6 12	A
$I_{LIM,TSD}$	Current limit during thermal shutdown	Internal current limit under thermal cycling condition	5	A
		External current limit under thermal cycling condition	50%	$I_{LIM,EXT}$
$V_{DS,CLP}$	Drain to source internal clamp voltage		42 47 52	V
OUTPUT DIODE CHARACTERISTICS				
$V_{OUT,F}$	Drain to source diode voltage	$V_{IN}=0, I_{OUT}=-0.2A$	0.7	V
$I_{OUT,REV}$	Continuous reverse current when reverse polarity	$t < 60s, V_S = 13.5V, GND$ pin 1-kΩ resistor in parallel with diode. $T_J = 25^{\circ}C$	4	A
LOGIC INPUT				
$V_{IN,H}$	High-level voltage for IN and DIAG_EN		2	V
$V_{IN,L}$	Low-level voltage for IN and DIAG_EN		0.8	V
$V_{IN,HYS}$	Hysteresis voltage for IN and DIAG_EN		130	mV
$R_{IN,PD}$	Pull down resistor for IN		150	kΩ
R_{DIAG_PD}	Pull down resistor for DIAG_EN		150	kΩ
DIAGNOSTICS				
$I_{OUT,BGND}$	Output leakage current when loss of ground		100	μA
$V_{OL,OFF}$	Open load detection threshold @off-state	$V_{IN} = 0V$, When $V_S - V_{OUT} < V_{OL,OFF}$, duration longer than $t_{OL,OFF}$. Open load detected	1.4 1.8 2.6	V
$I_{OL,OFF}$	Off-state output sink current with open load	$V_{IN} = 0V, V_S = V_{OUT} = 13.5V, T_J = 125^{\circ}C$	55	μA
$t_{OL,OFF}$	Open load detection-threshold deglitch time @off state	$V_{IN} = 0V$, When $V_S - V_{OUT} < V_{OL,OFF}$, duration longer than $t_{OL,OFF}$. Open load detected	600	μs
$I_{OL,ON}$	Open load detection threshold @on-state	$V_{IN} = 5V$, When $I_{OUT} < I_{OL,ON}$, duration longer than $t_{OL,ON}$. Open load detected, version A only	2 6 16	mA
$t_{OL,ON}$	Open load detection-threshold deglitch time @on state	$V_{IN} = 5V$, When $I_{OUT} < I_{OL,ON}$, duration longer than $t_{OL,ON}$. Open load detected, version A only	700	μs
$V_{ST,LOW}$	Low-level voltage for $\overline{ST}$	$I_{ST}=2mA$, version A only	0.4	V
T_{SD}	Thermal shutdown threshold		170	$^{\circ}C$
$T_{SD,RST}$	Thermal shutdown reset temperature		155	$^{\circ}C$
T_{SW}	Thermal swing shutdown threshold		60	$^{\circ}C$



T_{HYS}	Hysteresis for resetting the thermal shutdown and swing		10	°C
CURRENT SENSE (VERSION B ONLY) AND CURRENT LIMIT				
K_{CS}	Ratio of current sense		500	
K_{CL}	Ratio of current limit		2000	
dK_{CS}/K_{CS}	Accuracy of current sense ($I_{CS} \times K_{CS} - I_{OUT}$) / $I_{OUT} \times 100$	$I_{OUT} \geq 5mA$	-80 80	%
		$I_{OUT} \geq 25mA$	-10 10	
		$I_{OUT} \geq 50mA$	-7 7	
		$I_{OUT} \geq 500mA$ ($T_j \leq 125^\circ C$)	-5 5	
dK_{CL}/K_{CL}	Accuracy of current limit ⁽²⁾⁽³⁾ ($I_{CL} \times K_{CL} - I_{OUT}$) / $I_{OUT} \times 100$	$I_{LIM} \geq 0.5A$	-20 20	%
$V_{CS,LIN}$	Linear voltage range of CS	$V_S \geq 5V$	0 4	V
$I_{OUT,LIN}$	Linear output current range	$V_S \geq 5V, V_{CS,LIN} \leq 4V$	0 4	A
$V_{CS,H}$	Fault high voltage of CS	$V_S \geq 7V$	4.5 5 5.25	V
		$V_S \geq 5V$	Min($V_S - 0.8, 4.3$) 4.9	V
$I_{CS,H}$	Fault current of CS	$V_S \geq 7V, V_{CS} = 4.3V$	9	mA
$V_{CL,TH}$	Internal current limit threshold voltage		1.233	V
$I_{CS,LEAK}$	Leakage current of CS @diagnostic disable state	$V_{IN}=5V, R_{LOAD}=10\Omega, V_{DIAG_EN}=0V, T_j=125^\circ C$	1	uA
		$V_{IN}=0V, R_{LOAD}=10\Omega, V_{DIAG_EN}=0V, T_j=125^\circ C$	1	uA
$t_{CS,OFF1}$	CS settling time from DIAG_EN falling edge	$V_{IN} = 5V, I_{OUT} \geq 5mA, V_{DIAG_EN}$ from 5 to 0 V. V_{CS} to 10% of sense value	10	us
$t_{CS,ON1}$	CS settling time from DIAG_EN rising edge	$V_{IN} = 5V, I_{OUT} \geq 5mA, V_{DIAG_EN}$ from 0 to 5 V. V_{CS} to 90% of sense value	10	us
$t_{CS,OFF2}$	CS settling time from IN falling edge	$V_{DIAG_EN} = 5V, I_{OUT} \geq 5mA, V_{IN}$ from 5 to 0 V. V_{CS} to 10% of sense value	100	us
$t_{CS,ON2}$	CS settling time from IN rising edge	$V_S = 13.5V, V_{DIAG_EN}=5V, I_{OUT} \geq 100mA, V_{IN}$ from 0 to 5 V. V_{CS} to 90% of sense value	150	us
Switching Characteristics ($V_S=13.5V, R_{LOAD}=10\Omega$)				
$t_{D,ON}$	Turn-on delay time	IN rising edge to $V_{OUT}=10\%$, $V_{DIAG_EN}=5V, I_{OUT}=1A$	20 60	us
$t_{D,OFF}$	Turn-off delay time	IN falling edge to $V_{OUT}=90\%$, $V_{DIAG_EN}=5V, I_{OUT}=1A$	40 90	us
dV/dt_{ON}	Turn-on slew rate	V_{OUT} from 10% to 90%, $V_{DIAG_EN}=5V, I_{OUT}=1A$	0.1 0.5	V/us
dV/dt_{OFF}	Turn-off slew rate	V_{OUT} from 90% to 10%, $V_{DIAG_EN}=5V, I_{OUT}=1A$	0.1 0.5	V/us



$t_{D,mismatch}$	The mismatch time between turn on and turn off	$V_S = 13.5V, I_{OUT}=1A.$ $t_{D,mismatch} = t_{D,rise} - t_{D,fall}$ $t_{D,rise}$ is the IN rising edge to $V_{OUT} = 90\%$. $t_{D,fall}$ is the IN falling edge to $V_{OUT} = 10\%$.	-85	25	us
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- (1) The current includes the leakage current at output stage.
- (2) The accuracy of external current limit is only applicable to overload conditions that is over 50% greater than the current limit setting.
- (3) The external current limit is recommended to be set higher than 0.5A.

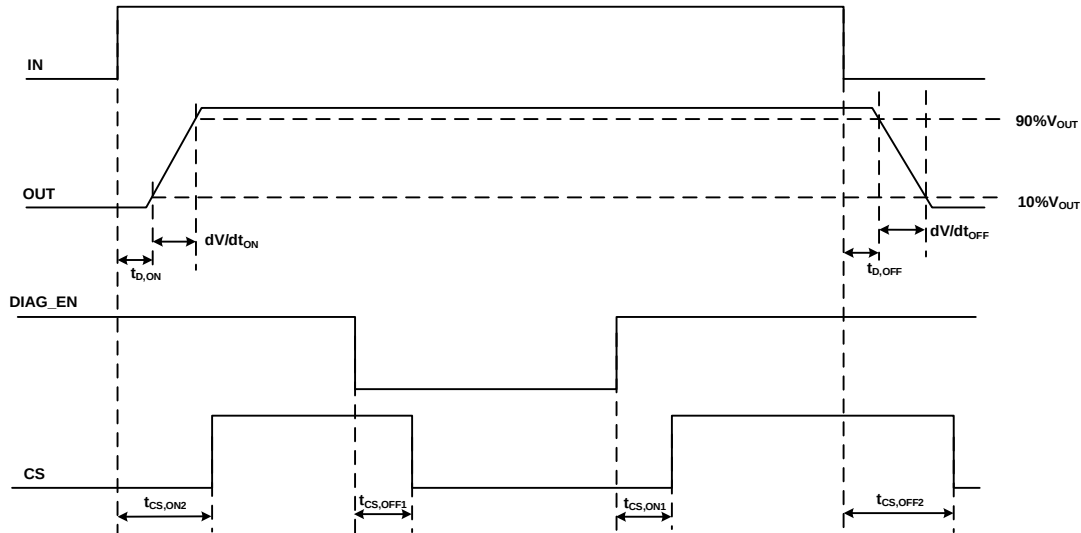


Figure 8-1. Switching Characteristics

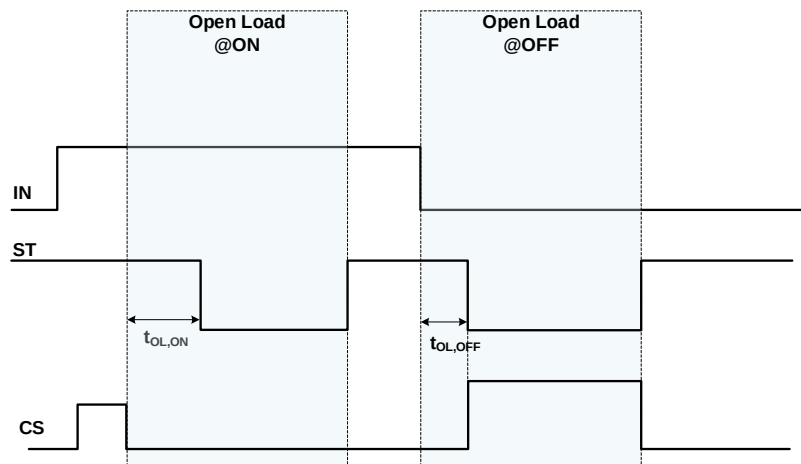


Figure 8-2. Open-Load Blanking Time Characteristics



8.6 Typical Characteristics

All the following data are based on the mean value of the three lots samples, $V_S=13.5V$ if not specified.

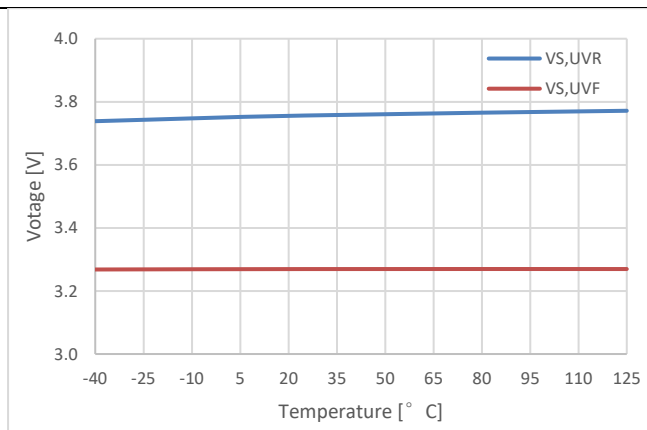


Figure 8-3. $V_{S,UVR}$ & $V_{S,UVF}$

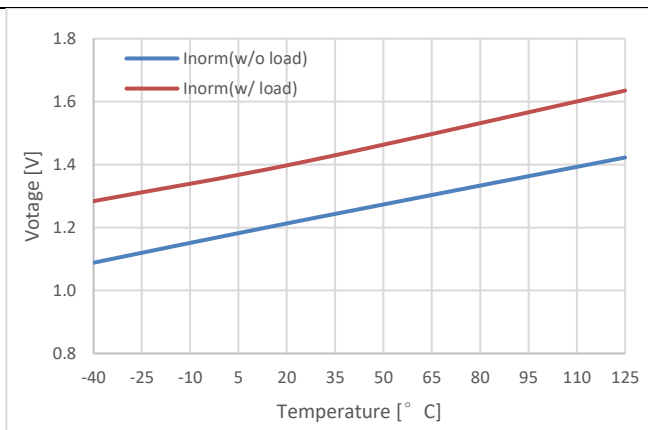


Figure 8-4. I_{norm} w/ and w/o load

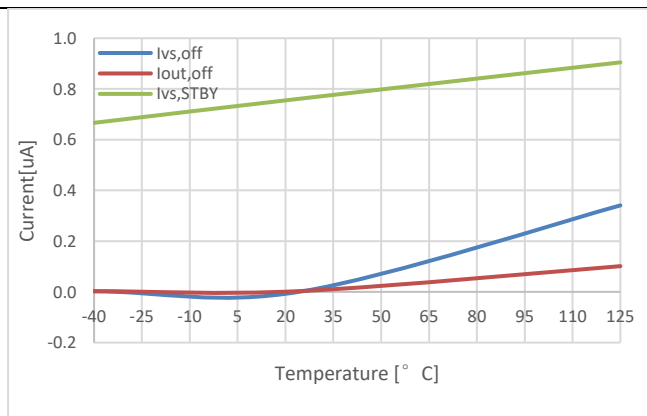


Figure 8-5. $I_{vs,off}$, $I_{out,off}$ & $I_{vs,STBY}$

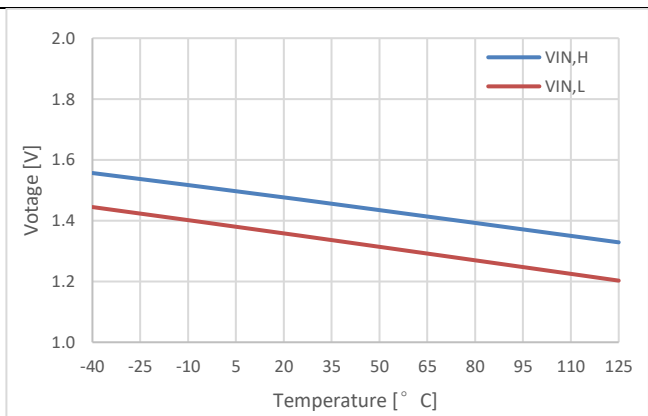


Figure 8-6. $V_{IN,H}$ & $V_{IN,L}$

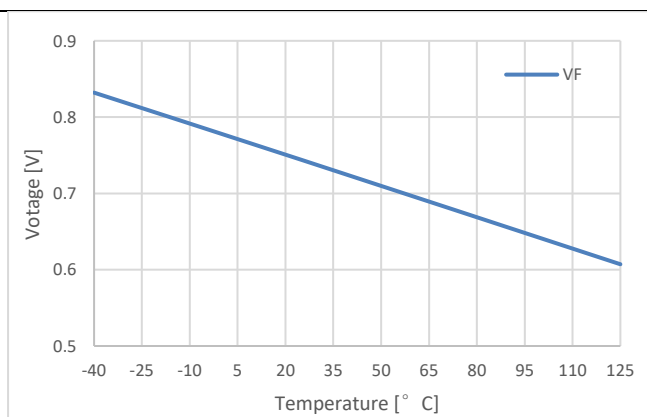


Figure 8-7. V_F

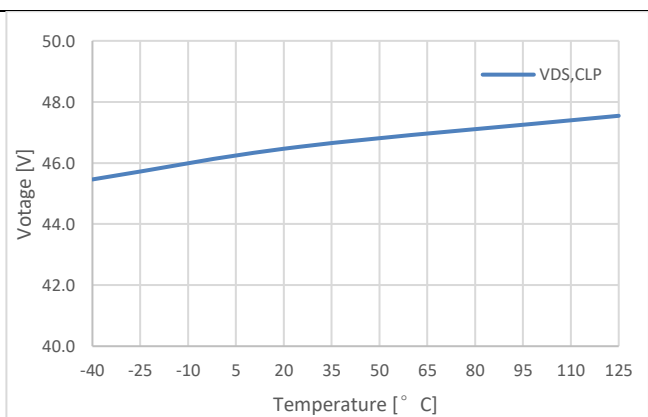
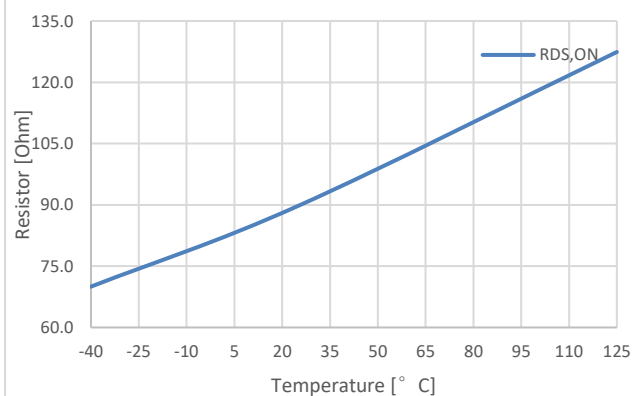
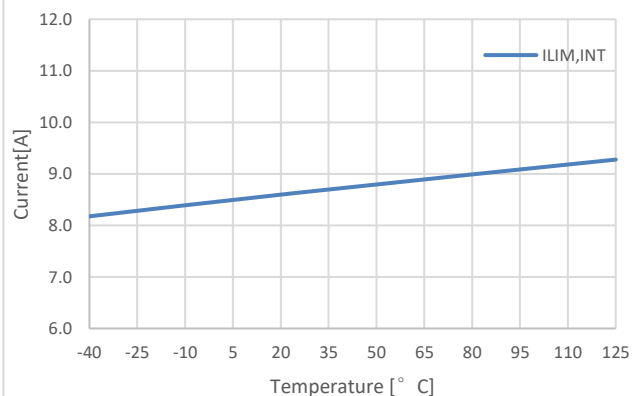
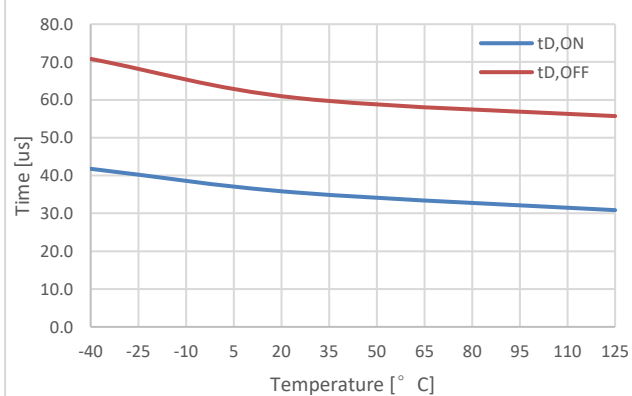
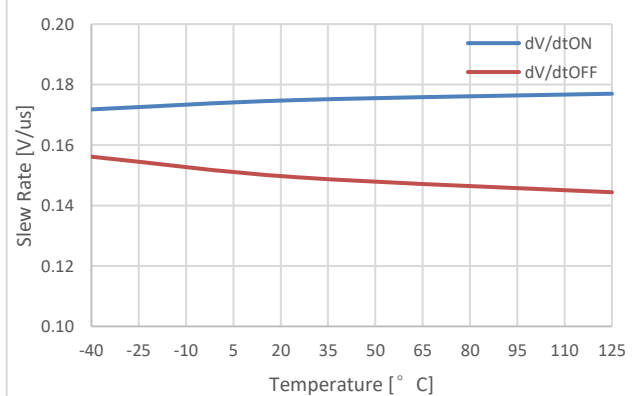
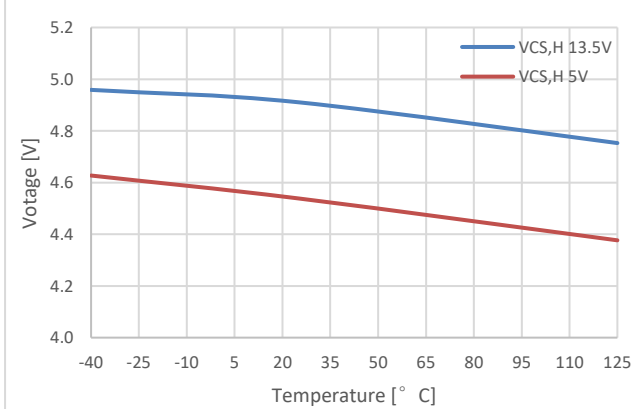
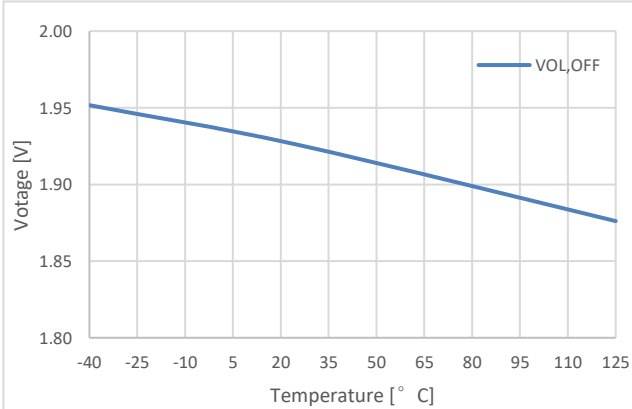


Figure 8-8. $V_{DS,CLP}$

Figure 8-9. $R_{DS,ON}$ Figure 8-10. $I_{LIM,INT}$ Figure 8-11. $t_{D,ON}$ & $t_{D,OFF}$ Figure 8-12. dV/dt_{ON} & dV/dt_{OFF} Figure 8-13. $V_{CS,H}$ @ $V_S = 5V$ & $V_S = 13.5V$ Figure 8-14. $V_{O,OFF}$

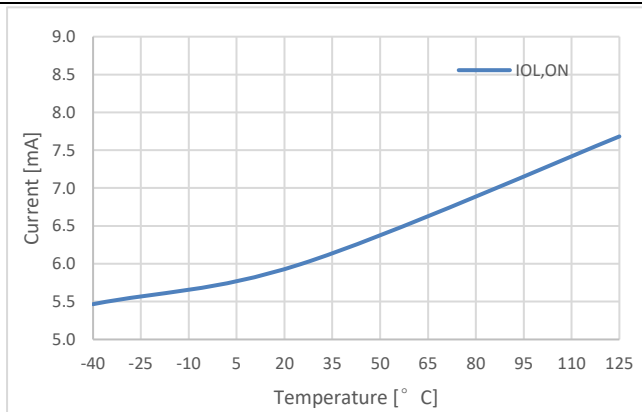


Figure 8-15. IOL,ON

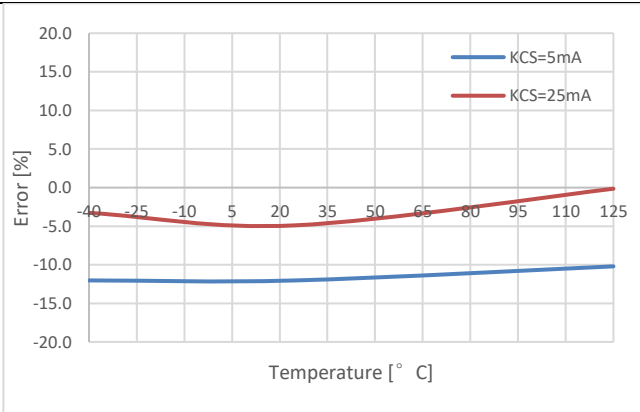


Figure 8-16. KCS accuracy @ IOUT=5mA & 25mA

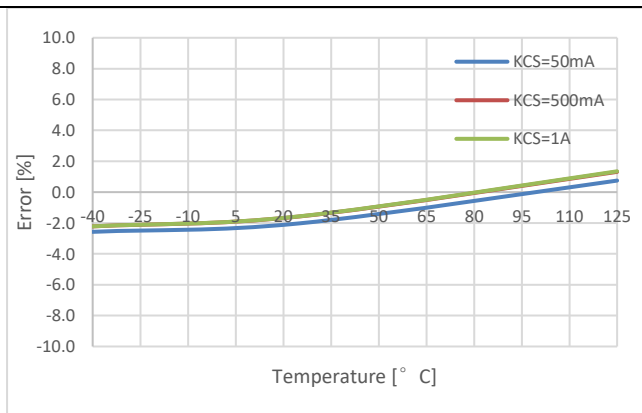


Figure 8-17. KCS accuracy @ IOUT=50mA & 500mA & 1A

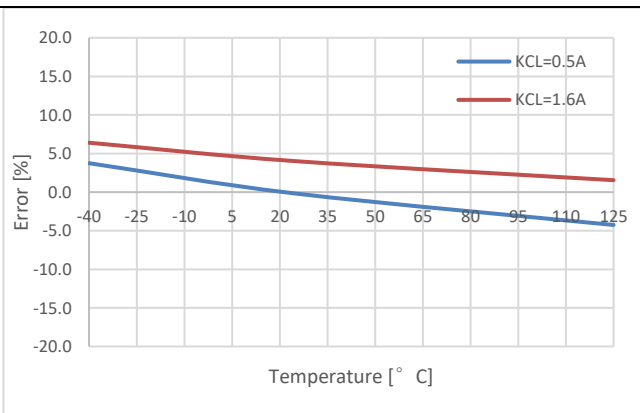


Figure 8-18. KCL accuracy @ ILIM=0.5A & 1.6A



9 Functional Block Diagram

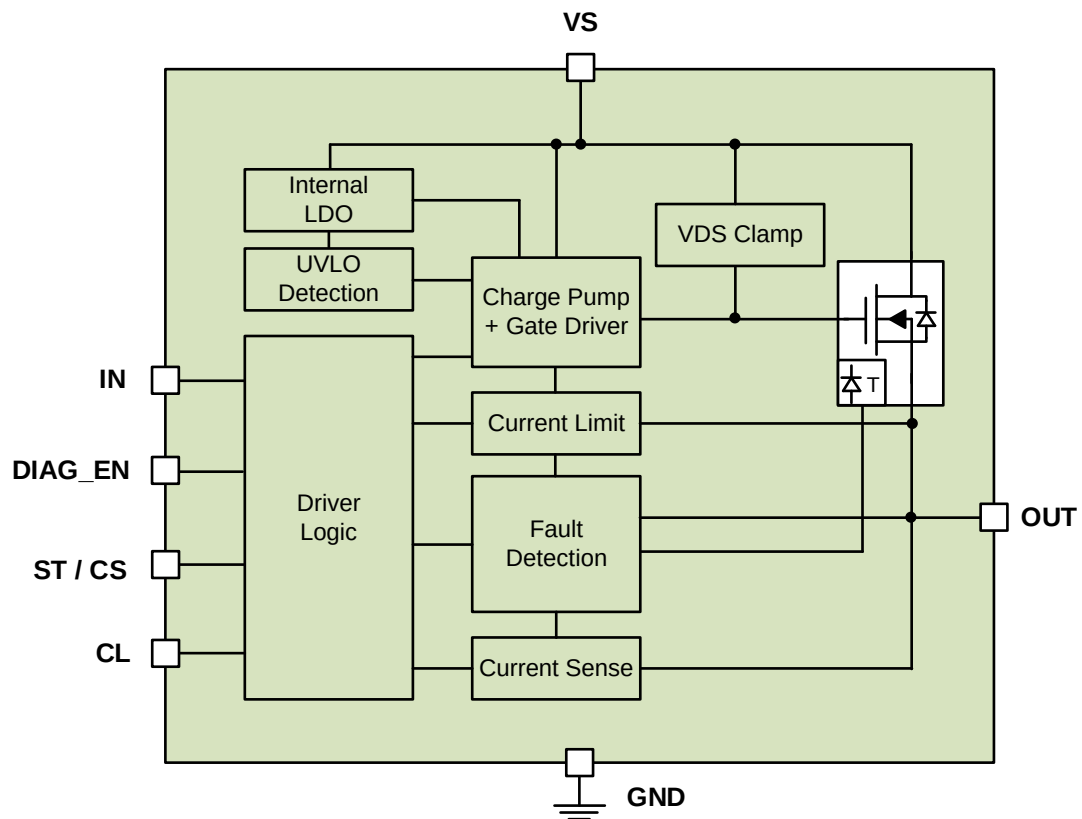


Figure 9-1. Functional Block Diagram



10 Feature Description

10.1 Working Modes

There are three working modes in the device: normal mode, standby mode (with diagnostic) and sleep mode (without diagnostic). Figure 10-1 shows a work-mode state-machine state diagram.

If an off-state power saving is required in the system, the standby current is less than 500 nA with DIAG_EN low. If an off-state diagnostic is required in the system, the typical standby current is around 1 mA with DIAG_EN high. Note that to enter standby or sleep mode requires IN low and $t > t_{OFF,DEG}$. $t_{OFF,DEG}$ is the standby-mode deglitch time, which is used to avoid false triggering.

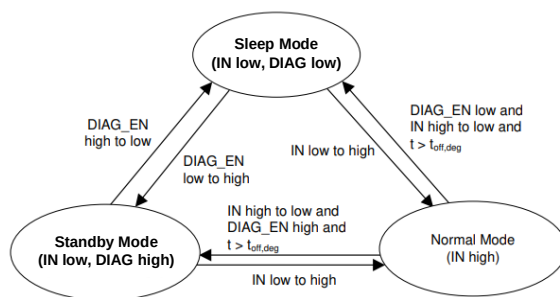


Figure 10-1 Working Mode State Machine

10.2 Current Sense

The high-accuracy real-time current-sense function is implemented for version B. An internal current mirror is used to source 1 / K_{CS} of the load current, flowing out to the external resistor between the CS pin and GND, and reflected as voltage on the CS pin. K_{CS} is the ratio of the current at output stage and the sensing current at CS pin. It is a constant value across the temperature and supply voltage. Each device was internally calibrated while in production, so post-calibration by users is not required in most cases.

To ensure the CS voltage is within the linear region, an appropriate R_{CS} is need to be calculated as below:

$$R_{CS} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS}}{I_{OUT}} \times K_{CS} \quad (1)$$

When the IC is in a fault condition, the CS pin would perform as a diagnostic report pin. For example, if current limit, thermal shutdown/swing, open load, or short to battery in the off-state occurs, the voltage of CS pin would be pulled up to $V_{CS,H}$. Please check Figure 10-2 for details.

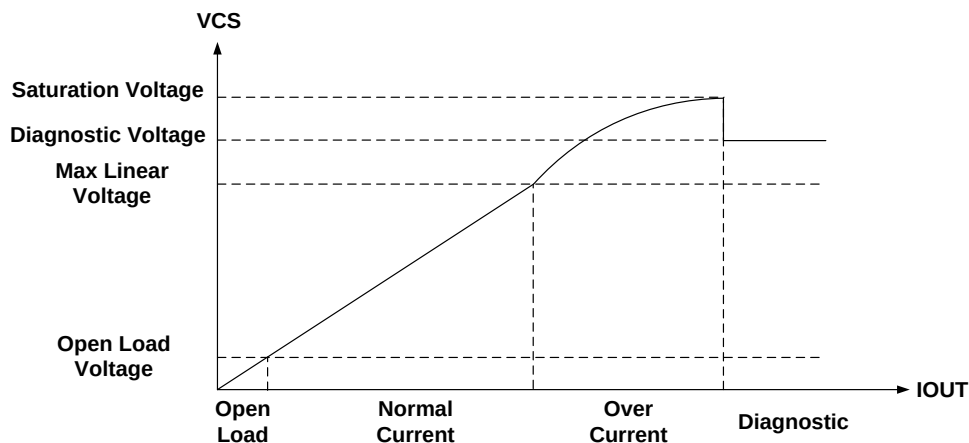


Figure 10-2 VCS in different working mode



10.3 Programmable Current Limit

A high-accuracy current limit is integrated internally, which offers protection from overstressing to the load and integrated power FET. If the current limit occurs, the IC would hold the current at the set value, and pulls up the CS pin to diagnostic voltage $V_{CS,H}$. And IC support two current-limit thresholds as below:

External programmable current limit -- An external resistor is used set the I_{CL} limit at CL pin, which is proportional to I_{OUT} with K_{CL} factor. When I_{OUT} exceed the CL current set by the external resistor, a closed loop steps in immediately. V_{GS} voltage regulates accordingly, leading to the V_{DS} voltage regulation.

Internal current limit -- The internal current limit is fixed and typically 12 A. To connect CL pin directly to device GND would trigger the internal current limit for large-current applications.

Both the internal current limit (I_{LIM_NOM}) and external programmable current limit are always active when V_S is powered and IN is high. The lower one (of I_{LIM_NOM} and the external programmable current limit) is applied as the actual current limit. Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the CL pin must be connected with device GND.

To use the current limit in the application, an appropriate R_{CL} is need to be calculated as below:

$$R_{CL} = \frac{V_{CL,TH}}{I_{CL}} = \frac{V_{CL,TH}}{I_{OUT}} \times K_{CL} \quad (2)$$

10.4 Inductive-Load Switching-Off Clamp

If an inductive load is driven by HSD, when the load is switch on, the current through the inductor increases with a constant time given by the values of the inductance and the resistance of the load:

$$i = \frac{V_S}{R} (1 - e^{-\frac{t}{\tau}}) \quad (3)$$

$$\tau = \frac{L}{R} \quad (4)$$

And the energy stored in the inductor is calculated as below:

$$E_{LOAD} = \frac{1}{2} \cdot L \cdot \left(\frac{V_S}{R}\right)^2 \quad (5)$$

When the load is switched off, due to the inductance, the load current tempts to continue to flow in the same direction which causes the load voltage to be pulled down to negative. To protect the power FET to be breakdown in this situation, an internally clamping $V_{DS,CLP}$ between the drain and source is implemented, and the power FET is turned on for inductance-energy dissipation during the current-decay period (T_{DECAY}). Please check the graphic diagram in Figure 10-3.

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET may break down if the voltage is not clamped during the current-decay period. To protect the power FET in this situation, internally clamp the drain-to-source voltage, namely $V_{DS,CLP}$, the clamp diode between the drain and gate.

$$V_{DS,CLP} = V_S - V_{OUT} = V_S - R \cdot i(t) - L \cdot \frac{di(t)}{dt} \quad (6)$$

Solve equation 6,

$$i(t) = \frac{V_S}{R} \cdot e^{-\frac{t}{\tau}} + \frac{V_S - V_{DS,CLP}}{V_{DS,CLP}} \cdot (1 - e^{-\frac{t}{\tau}}) \quad (7)$$

Solve equation 7 with $i(t)=0$,

$$t_{DECAY} = \tau \cdot \ln\left(\frac{V_{DS,CLP}}{V_{DS,CLP} - V_S}\right) \quad (8)$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductance-energy dissipation. The total dissipated energy E_{HSD} is calculated as below:

$$E_{HSD} = \int_0^{t_{DECAY}} V_{DS,CLP} \cdot i(t) dt$$



$$= V_{DS,CLP} \cdot t_{DECAY} \left(\frac{V_S - V_{DS,CLP}}{R} \right) - \tau \frac{V_{DS,CLP}^2}{R} \left(e^{-\frac{t_{DECAY}}{\tau}} - 1 \right) \quad (9)$$

With approximation of $R \approx 0$, then

$$t_{DECAY} = \frac{LI_L}{V_{DS,CLP} - V_S} \quad (10)$$

$$E_{HSD} = \frac{1}{2} LI_L^2 \cdot \left(\frac{V_{DS,CLP}}{V_{DS,CLP} - V_S} \right) \quad (11)$$

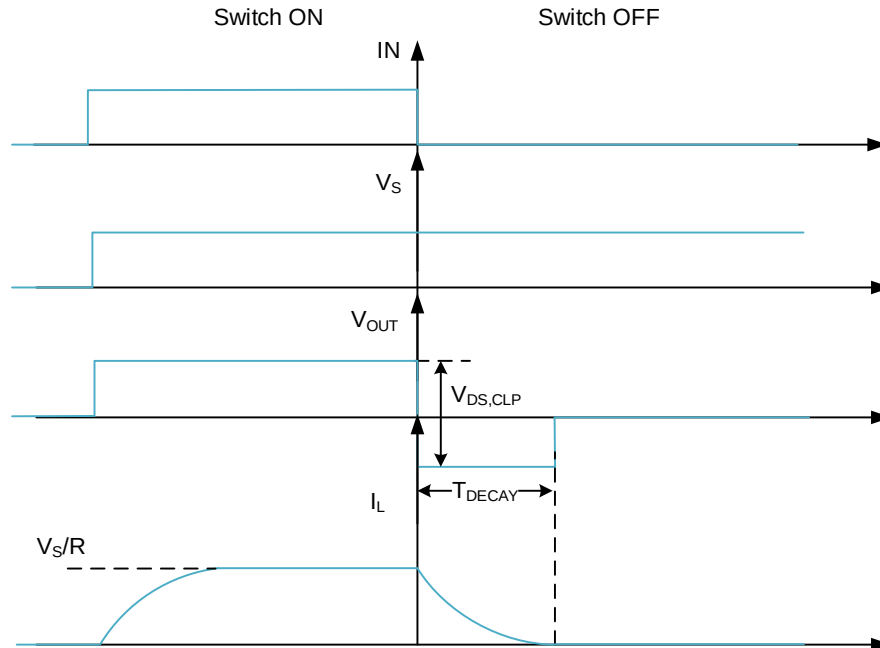


Figure 10-3 Inductive Load Switching-ON/OFF Diagram

10.5 Protections and Diagnostics

10.5.1 Fault Truth Table

Table 10-1 shows the fault table of OUT, CS, ST pin signal under different fault conditions.

Table 10-1. Fault Table

Application Conditions	IN	Diag_EN	Vout	CS	ST
Normal Operation	H	H	$\approx V_S$	I_L / K	H
Vs: Under-voltage	H	H	≈ 0	Hiz	Hiz
Vout: Short to GND	H	H	0	Vcs,h	L
Vout: Short to Vs	H	H	Vs	≈ 0	L(deglitch)
Vout: Open Load	H	H	$\approx V_S$	≈ 0	L(deglitch)
Overcurrent	H	H	$< V_S$	Vcs,h	L
Overtemperature	H	H	≈ 0	Vcs,h	L
Normal Operation	L	H	≈ 0	$< I_{off}$	H
Vs: Under-voltage	L	H	≈ 0	Hiz	Hiz
Vout: Short to GND	L	H	0	0	H
Vout: Short to Vs	L	H	$\approx V_S$	Vcs,h (deglitch)	L(deglitch)
Vout: Open Load	L	H	$> V_S - V_{ol,off}$	Vcs,h (deglitch)	L(deglitch)
Overtemperature	L	H	≈ 0	Vcs,h	L
All condition	X	L		0	Hiz



10.5.2 Short-to-GND and Overload Detection

When Power FET is ON, the short-to-GND fault is reported with low voltage on ST (version A) or $V_{CS,H}$ on CS (version B), when a current limit is triggered. The lower one of the internal and external set values is applied for the actual current limit.

The fault would be auto recovered when the fault condition is cleared. If it is not cleared for certain time, the current limit would further trigger the thermal shutdown to protect the power FET.

10.5.3 Open-Load Detection

When Power FET is ON, if the current is lower than 6mA, IC would report the open load fault with low voltage on ST for version A. For version B, this fault would not report directly. The user could detect the voltage of CS pin and judge accordingly.

When Power FET is OFF, if $V_S - V_{OUT} < V_{OL,OFF}$, the open load fault would be reported with low voltage on ST (version A) or $V_{CS,H}$ on CS (version B).

The fault would be auto recovered when the fault condition is cleared.

10.5.4 Short-to-Battery Detection

When Power FET is ON, the IC would report the fault with low voltage on ST for version A. For version B, this fault would not report directly. The user could detect the voltage of CS pin and judge accordingly.

When Power FET is OFF, the short to battery would lead to $V_{OUT} - V_S < V_{OUT,F}$, which would report the low voltage on ST (version A) or $V_{CS,H}$ on CS (version B).

The fault would be auto recovered when the fault condition is cleared.

10.5.5 Thermal Shutdown Protection

There are two different thermal shutdown mechanism implemented in the IC: the dynamic protection and static protection.

For the dynamic thermal protection, the IC would shut down the power FET when the temperature of the power FET is increasing sharply with $\Delta T = T_{DMOS} - T_{LOGIC} > T_{SW}$. The fault would be reported with low voltage on ST (version A) or $V_{CS,H}$ on CS (version B).

The fault would be auto recovered when $\Delta T = T_{DMOS} - T_{LOGIC} < T_{SW} - T_{HYS}$.

For the static thermal protection, the IC would shut down the power FET when the temperature of the power FET $T > T_{SD}$. The fault would be reported with low voltage on ST (version A) or $V_{CS,H}$ on CS (version B).

The fault would be auto recovered when $T < T_{SD} - T_{HYS}$.

10.5.6 UVLO Protection

The IC would shut down the power FET when $V_S < V_{S,UVF}$.

The fault would be auto recovered when $V_S > V_{S,UVR}$.

10.5.7 Loss of GND Protection

The IC would shut down the power FET when loss of GND occurs.

The fault would be auto recovered when the GND connection is back to normal.

10.5.8 Loss of Power Supply Protection

The IC would shut down the power FET when loss of supply occurs.

The fault would be auto recovered when the supply connection is back to normal.



11 Layout

11.1 Layout Guidelines

To prevent the device from triggering thermal protection, it is critical to maintain the junction temperature (T_J) below 150°C. High output currents can lead to substantial power dissipation. While the eTSSOP package offers superior thermal impedance characteristics, the effectiveness of heat dissipation heavily relies on the printed circuit board (PCB) design. Optimized PCB layouts significantly enhance heat transfer efficiency, which is vital for ensuring long-term operational stability of the device.

Maximize Copper Coverage: The primary heat dissipation path from the device to the ambient environment depends on the PCB's copper layers, especially in applications without additional heat sinks. Maximizing copper coverage in the area directly beneath the package is crucial for improving substrate thermal conductivity, particularly when no heat dissipation structures are implemented on the opposite side of the board.

Optimize Thermal Via Configuration: Dense arrays of thermal vias positioned directly under the device's ground pad enhance vertical Thermal conductivity. A full-board via distribution is recommended to achieve optimal Thermal transfer performance.

Via Processing Specifications: All thermal vias must undergo plating closure or be plugged and capped on both sides to ensure complete metallization. Post-processing solder coverage must meet a minimum of 85% to eliminate solder void risks and maintain electrical reliability as well as thermal conduction efficiency.

11.2 Layout Example

11.2.1 Without a GND Network

For optimized heat dissipation in designs without GND network, establish a direct connection between the cooling pad and the PCB's ground copper layer .

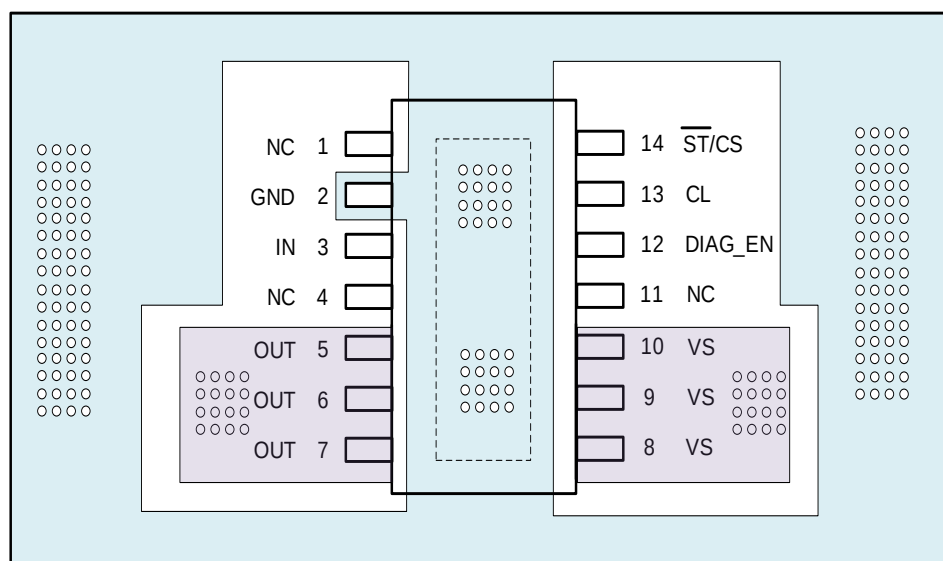


Figure 11-1 Layout Example 1 (Without a GND Network)

11.2.2 With a GND Network

When a GND network is present, connect the cooling pad to the PCB ground copper layer via a single trace.

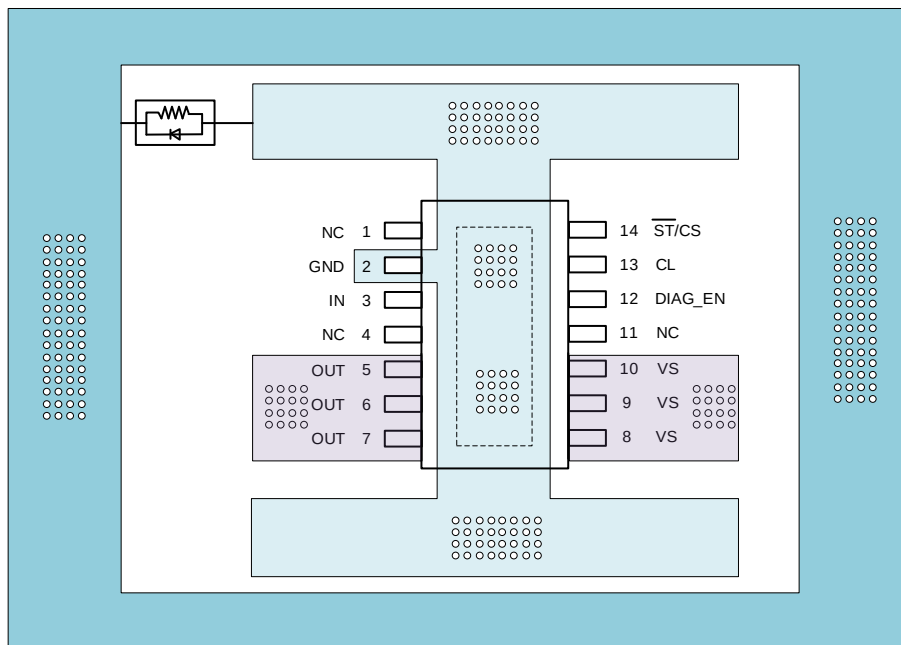


Figure 11-2 Layout Example 2 (With a GND Network)

11.3 Thermal Considerations

The device incorporates thermal shutdown circuitry to prevent excessive junction temperature. To maintain continuous normal operation, ensure the junction temperature remains below the TSD activation threshold. Upon exceeding this threshold, the output turns off. Normal operation resumes only after the junction temperature cools below the TSD deactivation point, at which time the output turns on.

To calculate the power dissipated by the device, use the following formula:

$$P_T = I_{OUT}^2 \cdot R_{DS(on)} + V_S \cdot I_{nom} \quad (12)$$

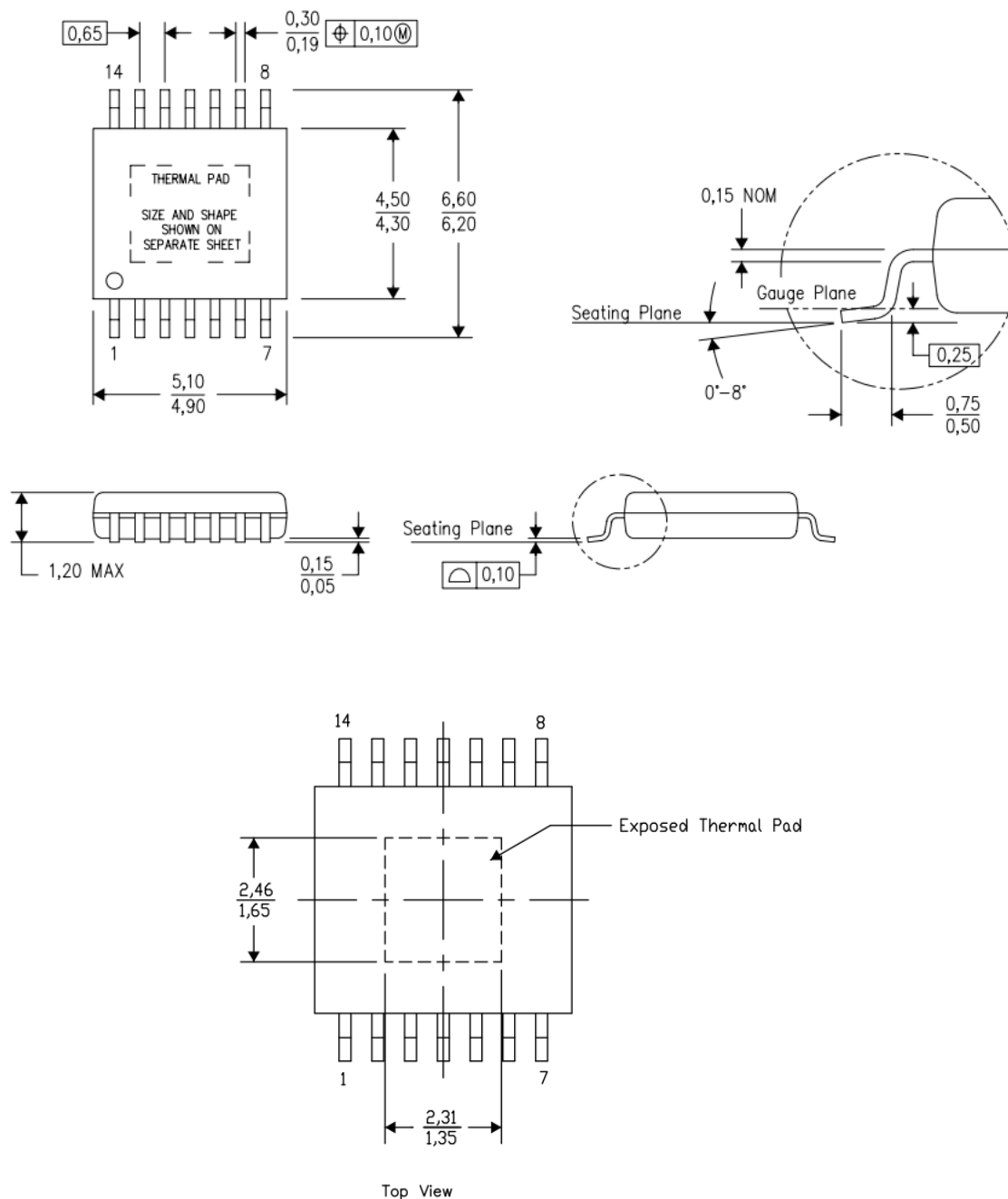
Following the determination of power dissipation, the junction temperature can be calculated using the ambient temperature and the device's thermal impedance with the formula:

$$T_J = T_A + R_{\theta JA} \cdot P_T \quad (13)$$



MECHANICAL DATA

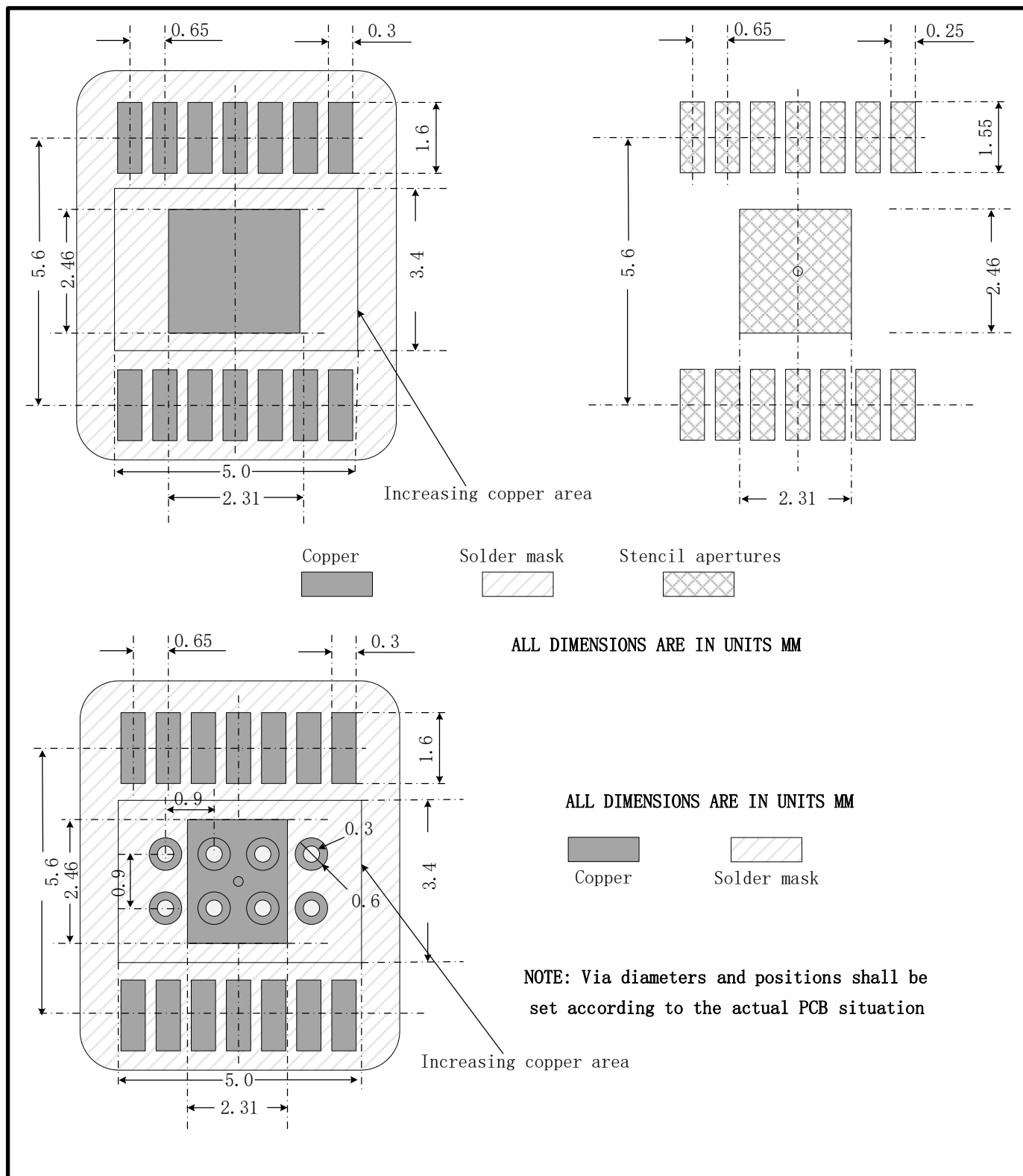
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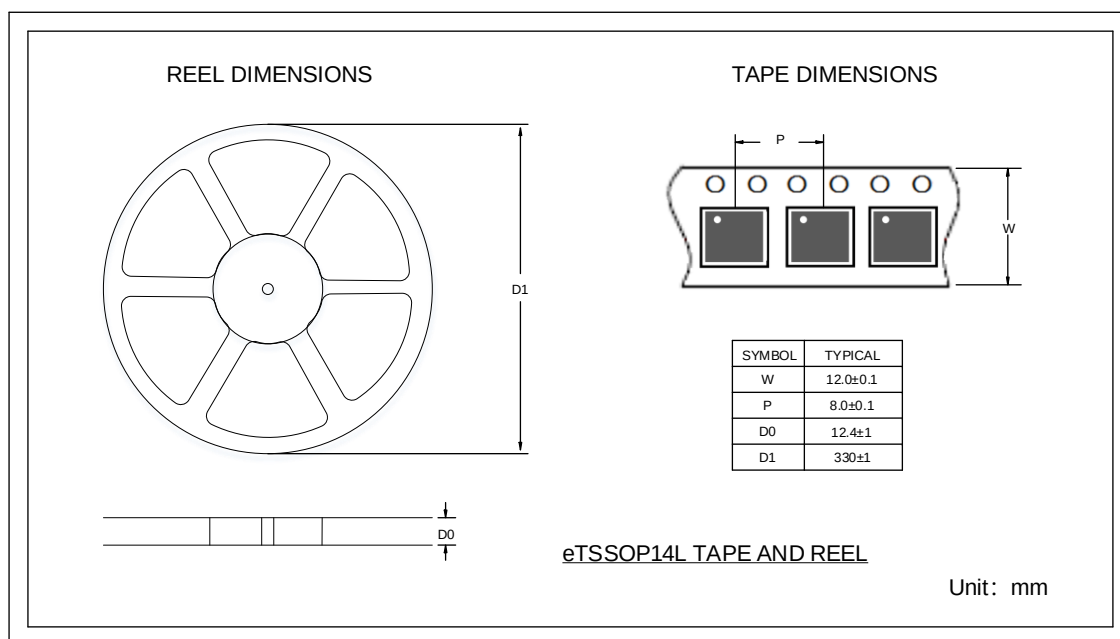
PACKAGE PADS AND STENCIL DATA

eTSSOP-14





TAPE AND REEL INFORMATION





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