

SC8724 High Efficiency, Synchronous, 22V Buck-Boost Converter with Four Integrated MOSFET

1 Description

SC8724 is a synchronous 4-switch buck-boost converter with four integrated switches. It provides excellent power efficiency and voltage regulation no matter whether the output voltage is higher, lower, or equal to the input voltage. SC8724 supports a very wide input and output voltage range. It can support applications from 2.7V to 22V input range and 3V to 22V output range and provides up to 10A average inductor current limit.

SC8724 employs average current-mode control. The output voltage is adjusted by a divider resistor network on the FB pin. The switching mode (PSM/FPWM) and the switching frequency can be adjusted by the external setting. The device also provides a programmable output current limit which supports flexible design for different applications.

SC8724 supports internal current limit, input under-voltage protection, output over-voltage protection, output short protection, FB short circuit protection, and over-temperature protection to ensure safety under different abnormal conditions.

The IC is in a 25-pin 4x4 QFN package.

3 Applications

- Wall Adapter
- Power Bank with Quick Charge
- USB Type C Hub
- Wireless Charger
- Industry Power Supplies

2 Features

- High-Efficiency Buck-Boost Conversion
- Few External Components
- Integrated Low $R_{DS(ON)}$ Switches
- Wide VIN Range: 2.7 V to 22 V
- Wide VOUT Range: 3V to 22V
- Fixed 5.1V VOUT with FB tied to GND
- Up to 10A Inductor Current Limit
- 250k/500k/800k/1MHz Adjustable Switching Frequency
- Adjustable Output Current Limit
- Forced PWM Mode/ PSM Mode Selectable
- EN control and Programmable UVLO
- Internal Soft Start
- Absolute Input and Output Over Voltage Protection
- Output Short Protection with Hiccup Mode
- Thermal Shutdown Protection
- Under Voltage Protection
- Over Voltage Protection
- QFN-25 FC 4 x 4 Package

4 Device Information

Part Number	Package	Dimension
SC8724QFER	25 pin QFN	4.0mm x 4.0mm x 0.75mm

5 Typical Application Circuit

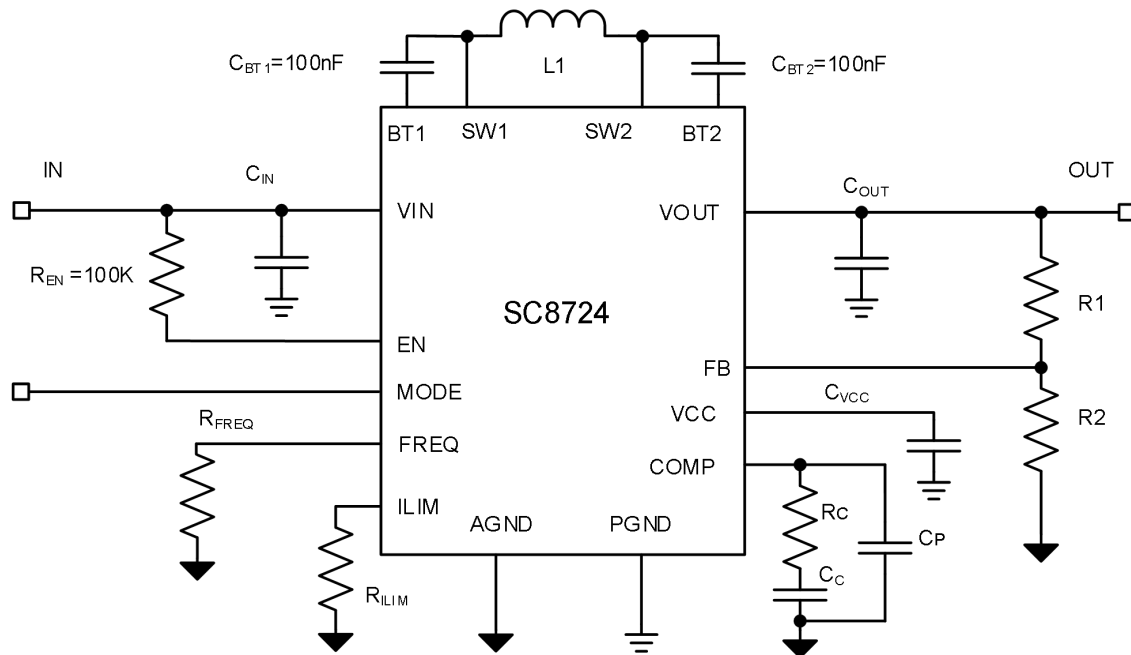
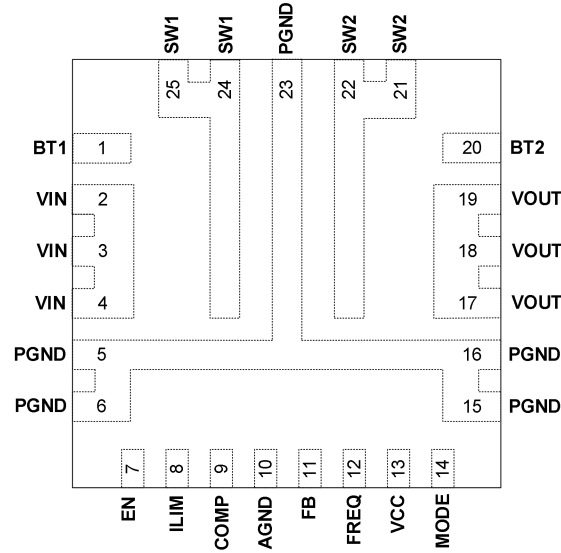


Figure1. Typical application circuit

6 Terminal Configuration and Functions

Top View



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	BT1	PWR	Connect a 100nF ceramic capacitor between the BT1 pin and SW1 pin to provide the boosted bias voltage for the high side gate driver of Q1.
2,3,4	VIN	PWR	The power input node of the converter.
5,6,15,16,23	PGND	PWR	Power ground. The user shall connect PGND and AGND on PCB.
7	EN	I	Enable logic input. Logic high level enables the device and logic low level disables the device. Using a 100k resistor in serial with EN pin when the EN pin is tied to VIN.
8	ILIM	I	Connect a resistor to set the current limit value of the output current.
9	COMP	I	Connect an RC network to compensate for the control loop.
10	AGND	I/O	Analog ground. The user shall connect PGND and AGND on PCB.
11	FB	I	Feedback node of VOUT output voltage. Set the VOUT output voltage by the resistor divider connected to this pin. The output voltage is configured for fixed 5.1V with the FB pin connected to GND.
12	FREQ	I	Set the typical switching frequency of the device. FREQ pin ties to AGND: 250kHz FREQ pin keeps floating: 500kHz $R_{FREQ} = 75k\Omega$: 800kHz $R_{FREQ} = 220\ k\Omega$: 1MHZ The switching frequency is locked during the device is enabled.
13	VCC	PWR	The output of an internal regulator. Connect a 1 μ F ceramic capacitor from VCC to the PGND pin close to the IC. The regulator supplies internal gate drivers.
14	MODE	I	Mode selection pin. Logic high level sets the device in forced PWM mode; logic low level or floating sets the device in PSM mode. Connect to PGND to extend thermal performance if PSM



			mode is used.
17,18,19	VOUT	PWR	The power output node of the converter. Output voltage feedback node when FB short to ground is detected.
20	BT2	PWR	Connect a 100nF ceramic capacitor between the BT2 pin and SW2 pin to provide the boosted bias voltage for the high side gate driver of Q4.
21,22	SW2	PWR	Switching Node 2. Connect to the inductor. Connect a 100nF ceramic capacitor between the BT2 pin and SW2 pin to provide the boosted bias voltage for the high side gate driver.
24,25	SW1	PWR	Switching Node 1. Connect to the inductor. Connect a 100nF ceramic capacitor between the BT1 pin and SW1 pin to provide the boosted bias voltage for the high side gate driver.

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	MODE, ILIM, COMP, FB, FREQ, VCC	-0.3	6	V
	VIN, VOUT, SW1, SW2, EN	-0.3	25	V
	SW1, SW2 for less than 10ns	-4	27	V
	BT1 to SW1, BT2 to SW2	-0.3	6	V
T _J	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the network ground terminal.

6.2 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		QFN-25 (4mmX4mm)	UNIT
θ _{JA}	Junction to ambient thermal resistance	42	°C/W
θ _{JC}	Junction to case resistance	10	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

6.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-1.5	1.5	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

		MIN	MAX	UNIT
VIN	VIN voltage range	2.7	22	V
VOUT	VOUT voltage range	3	22	V
L	Inductance for L1, Fsw=250kHz	3.3		μH
	Inductance for L1, Fsw=500kHz/800kHz/1MHz	2.2		μH

6.5 Electrical Characteristics

T_J = 25°C and V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY VOLTAGE							
V _{IN}	Operating voltage		2.7		22	V	
V _{UVLO}	VIN under-voltage lockout threshold	Rising edge	2.45	2.55	2.65	V	
		Hysteresis	180			mV	
V _{INOVP}	Absolute OVP threshold for VIN	Rising edge	22.5	23	24	V	
		Hysteresis	1.2			V	
I _Q	Quiescent current into VIN	VIN = 8V, VOUT = 5V EN = H, non-switching	1.5			mA	
I _{SHUTDOWN}	Shutdown current VIN	VIN = 8V, EN = L	6			8	μA
VCC, DRIVER AND POWER SWITCH							
V _{CC}	VCC regulation voltage	VIN = 9V	5			V	
		VIN= 5V, ICC = 30mA	4			V	
I _{VCC_LIM}	VCC current limit	VIN = 9V, VCC = 4V	80	100		mA	
R _{DSon_HS}	High side MOS Q1 on resistance	VIN=12V	17			mΩ	
	High side MOS Q4 on resistance	VIN=12V	17			mΩ	
R _{DSon_LS}	Low side MOS Q2 on resistance	VIN=12V	21			mΩ	
	Low side MOS Q3 on resistance	VIN=12V	21			mΩ	
OUTPUT							
V _{OUT}	Output voltage range		3	22		V	
V _{FB}	FB reference voltage	FPWM mode	1.188	1.2	1.212	V	
V _{FB_OVP}	FB OVP threshold, over FB target	Rising edge	108	110	112	%	
		Hysteresis	7			%	
V _{OUT_ABSOVP}	Absolute OVP threshold for VOUT	Rising edge	22.5	23	24	V	
		Hysteresis	1			V	
V _{SHORT}	The short circuit detection threshold	Falling edge	2.1	2.3	2.5	V	
		Hysteresis	0.2			V	
T _{Hiccup_on}	On period of Hiccup Mode	Output short circuit detected	20			ms	
T _{Hiccup_off}	Off period of Hiccup Mode	Output short circuit detected	400			ms	
CURRENT LIMIT							
I _{LIM}	Max average inductor current limit	VO=5V	8	10	13	A	
I _{OC}	Output current limit	VOUT=5V, RILIM=22k	2.4	2.7	3	A	
		VOUT=5V, RILIM=18k	3	3.3	3.6	A	
ERROR AMPLIFIER							
G _{mEA}	Error amplifier gm		0.16			mS	
R _{OUT}	Error amplifier output resistance		20			MΩ	
I _{COMP}	COMP sink and source current		35			μA	

I _{BIAS_FB}	FB pin input bias current	FB in regulation	50			nA
LOGIC CONTROL						
V _{EN}	EN control logic threshold	Rising edge	1.1	1.2	1.3	V
		Hysteresis	0.2			V
V _{MODE_L}	MODE logic low voltage		0.4			V
V _{MODE_H}	MODE logic high voltage		1.4			V
Frequency						
F _{sw}	Switching frequency	FREQ pin ties to AGND	200	250	330	kHz
		FREQ pin keeps floating	420	500	580	kHz
		R _{FREQ} = 75kΩ	700	800	900	kHz
		R _{FREQ} = 220kΩ	850	1000	1150	kHz
SOFTSTART						
t _{SS}	Internal soft-start time	From 10% to 90% V _{OUT}	10			ms
THERMAL SHUTDOWN						
T _{SD}	Thermal shutdown temperature		150			°C
	Thermal shutdown hysteresis		20			°C

8 Feature Description

8.1 Enable and Programmable UVLO

The SC8724 has an enable control pin EN: pulling it high enables the IC and pulling it low disables the IC. Connect EN to VIN for automatic startup.

EN pin can also be reused for VIN under-voltage protection. Connecting the center tap of the divider resistors between VIN and GND programs the VIN under-voltage threshold and restart voltage, as shown in Figure. 2

The VIN under-voltage threshold can be calculated as the following equation.

$$V_{IN_LOW} = 1V \times \left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

When the input voltage is higher than the startup threshold, the device goes back to normal operation.

$$V_{IN_HIGH} = 1.2V \times \left(1 + \frac{R_{IN1}}{R_{IN2}}\right)$$

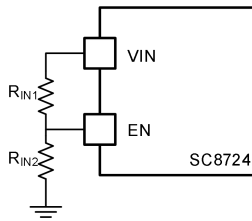


Figure 2 UVLO Threshold Programming

8.2 Soft Start

The IC implements a soft start feature to prevent inrush current during startup. After the IC is enabled, it ramps up the internal reference voltage by 10ms. The output voltage follows the reference, so it starts up slowly. Meantime, the IC ramps up the current limits during the startup.

8.3 Output Voltage Setting

The SC8724 can be configured for fixed 5.1V output with FB pin connected to GND. The output voltage can also be configured for customized values by using external feedback resistors and can be calculated as below.

$$V_{OUT} = V_{FB_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

Where:

V_{FB_REF} is the internal reference voltage of 1.2V. R_{UP} is the resistor connected from VOUT to FB and R_{DOWN} is the resistor connected from FB to AGND.

8.4 Constant Current Mode

SC8724 operates either in CV (constant voltage) mode or CC (constant current) mode and automatically changes from CV to CC smoothly. In CV mode, SC8724 regulates the output voltage. As long as the output current limit threshold is reached, SC8724 enters CC mode, and the output voltage drops while the output current is clamped at the setting values.

The output current limit can be set by the resistors connected ILIM pin to the ground by the following equation.

$$I_{LIM_OUT} = \frac{60000}{R_{ILIM}}$$

Where R_{ILIM} is the value of the current configuration resistor.

If the current limiting function is not needed, please short the ILIM pin to ground

8.5 FPWM/PSM Operation

The IC supports two operation modes: FPWM mode and PSM mode.

In FPWM mode, the IC always works with a constant switching frequency for the whole load range. This helps achieve the best output voltage performance, but the efficiency is low at light load conditions because of the high switching loss.

In PSM mode, the IC still works with constant switching frequency under heavy load conditions, but under light load conditions, it changes to pulse-skip operation to reduce the switching loss. The efficiency can be improved under light load conditions while the output voltage ripple will be a little larger compared with PWM operation.

The device adopts a MODE pin to configure the switching mode. Logic high level sets the device in forced PWM mode; logic low level or floating sets the device in PSM mode. Connect to PGND to extend thermal performance if PSM mode is used.

The below figure shows the output voltage behavior of PSM mode.

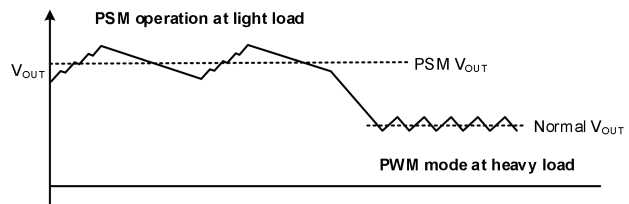


Figure 3 PSM operation

8.6 Switching Frequency

The SC8724 provides four switching frequency selection of 250kHz/ 500kHz/ 800kHz/ 1MHz. The switching frequency is configured by an R_{FREQ} resistor from the FREQ pin to GND. The typical switching frequency configuration is shown in the following table:

Table 1 Switching frequency configuration

Recommended R_{FREQ}	Typical FSW
0Ω (Tie to GND)	250kHz
Floating	500kHz
75kΩ	800kHz
220kΩ	1MHz

8.7 VCC Driver

The IC integrates a VCC regulator to generate the driving voltage for the internal driver circuit.

The VCC is supplied by VIN or VOUT and is clamped to 5V. Connect a 1μF ceramic capacitor from VCC to the PGND pin close to the IC.

8.8 Protections

8.8.1 Over Voltage Protection

The IC supports 3 mechanisms for overvoltage protection.

The first is once the IC detects the VIN voltage is higher than 23V(Typ.), it stops switching until the voltage drops below the threshold.

The second is once the IC detects the output voltage exceeds 110% of the setting target, the IC stops switching until the output voltage drops below 103% of the set target. This feature reduces output voltage overshoot during a line or a load transient.

The third is once the IC detects the VOUT voltage is higher than 23V(Typ.), the IC stops switching until the voltage drops below the threshold. This protection protects the device from damage even if the FB feedback connection is improperly configured.

8.8.2 Inductor Current Limitation

The IC implements internal current limits. Once the IC detects the inductor current is higher than the target, it reduces the switching duty cycle and keeps the inductor current from increasing. The typical internal average current limit is 10A.

8.8.3 Output Short Circuit Protection

The device integrates a hiccup mode which is triggered once the output voltage is lower than 2.3V. In hiccup mode, SC8724 periodically stops switching for 400ms and then tries to restart with output current increases to the current limit of 20ms. This protection mode is especially useful when the output is dead-short to the ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit condition is removed, SC8724 exits hiccup mode and goes back to normal operation.

8.8.4 Over Temperature Protection

Once SC8724 detects the chip junction temperature exceeds 150°C, the device goes into thermal shutdown and stops switching. When the junction temperature falls below the typical 130°C, the IC resumes operation.

9 Application Information

9.1 Input and Output Capacitor Selection

Since MLCC ceramic capacitor has good high-frequency filtering and low ESR, X5R or X7R capacitors are recommended for input and output capacitors. Typically, two 22 μF ceramic input capacitors and three 22 μF ceramic output capacitors work for most applications. The input/output capacitors should be placed as close to VIN / VOUT pins as soon as possible, and they should be also near the PGND pins or thermal pad.

Capacitors' derating effect under DC bias should be taken into account when selecting the capacitors. Ceramic capacitor normally loses their most capacitance at the rated voltage, so leave a margin on voltage rating to ensure adequate effective capacitance. For example, if the highest operating voltage is 12V, select a 16V or 25V capacitor.

Besides this, a high-value electrolytic capacitor or tantalum capacitor is recommended to place in parallel with the ceramic capacitors at the output to improve the load transient response.

9.2 Inductor Selection

Because the selection of the inductor affects the loop stability and the power efficiency, the inductor is one of the most important components for the DCDC design.

The IC can work with inductors between 2.2 μH to 10 μH range for most applications. A higher value is suggested to keep the inductor current ripple $\leq 30\%$ of the DC.

Compared with a high-value inductor in the same package size, a lower value inductor normally has smaller DC resistance (DCR) and means lower conduction power loss. The DCR power loss can be calculated roughly as

$$PL_{DC} = IL^2 \cdot DCR$$

IL is the effective value of the inductor current.

However, besides DCR, the core loss or AC loss of an inductor also affects the power efficiency a lot. The low-value inductor causes a large inductor current ripple, thus high core loss or AC loss, so it is not always the low-value inductor that supports the higher efficiency.

Since the core loss is related to the inductor material type, and normally the inductor vendors don't provide the core loss data, it is very difficult to suggest what inductor value can result in higher efficiency.

For applications where efficiency or thermal dissipation is very important, it is highly suggested that the user chooses

the inductor in a larger package size for lower DCR, and also tests the efficiency with different inductor values, to find the best combination to achieve the highest efficiency.

The saturation current is another important parameter when selecting the inductor. The inductance can decrease from 20% to 35% when the current approaches saturation level, so the user should make sure the saturation current is higher than the inductor peak current during the operation.

The inductor peak current can be calculated by the below formula.

$$IL_{peak} = IIN + \frac{VIN \cdot (VOUT - VIN \cdot \eta)}{2 \cdot fsw \cdot L \cdot VOUT} \quad (VOUT \geq VIN)$$

$$IL_{peak} = IOUT + \frac{VOUT \cdot (VIN - VOUT)}{2 \cdot fsw \cdot L \cdot VIN \cdot \eta} \quad (VOUT < VIN)$$

η is the power conversion efficiency. Users can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting an inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the output current.

9.3 Loop Compensation Design

The device adopts an average current mode control scheme with an external compensation circuit.

The purpose of loop compensation is to ensure stable work within the rated range. The voltage loop requires external compensation and the output of the error amplifier is connected to the COMP pin. Connect the RC compensation network from the COMP pin to the ground to avoid voltage loop oscillations.

The different operation modes of the SC8724 use the same compensation network, and the boost has one extra right half-plane zero frequency, so the boost is easier to oscillate. From the point of view of loop stability, choose one of the worst of both to compensate, which is the boost mode.

The simplified boost voltage loop with a TYPE_II compensation network is moded by the following equation:

$$H(s) = \frac{V_{REF} \times G_m \times R_O \times \frac{R_{LOAD} \times (1-D)}{0.02}}{V_{OUT} \times \frac{(1 + \frac{s}{2\pi f_{ESRZ}})(1 - \frac{s}{2\pi f_{RHPZ}})(1 + \frac{s}{2\pi f_{COMZ}})}{(1 + \frac{s}{2\pi f_P})(1 + \frac{s}{2\pi f_{COMP1}})(1 + \frac{s}{2\pi f_{COMP2}})}}$$

Which

R_{LOAD} is the output impedance.

D is the duty cycle in boost mode.

R_O is the output impedance of the error amplifier that is 100MΩ.

$$f_P = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}}$$

$$f_{ESRZ} = \frac{1}{2\pi \times R_{C_{OUT}} \times C_{OUT}}$$

$$f_{RHPZ} = \frac{R_{LOAD} \times (1-D)^2}{2\pi \times L}$$

And the following is the zero and pole frequency of TYPE_II compensation

$$f_{COMZ} = \frac{1}{2\pi \times R_C \times C_C}$$

$$f_{COMP1} = \frac{1}{2\pi \times R_C \times C_P}$$

$$f_{COMP2} = \frac{1}{2\pi \times R_O \times C_C}$$

In general, loop compensation is calculated in the following steps:

Step 1, set the crossing frequency, f_c . For stability reasons, f_c must be less than 1/6 of the f_{RHPZ} , and less than 1/10 of the switching frequency. The higher the f_c , the faster the dynamic response of the load and the more sensitive it is to other noise on boards.

Step 2, set compensation parameters.

$$R_C = \frac{2\pi \times f_c \times C_{out}}{G_m \times \frac{V_{REF}}{V_{OUT}} \times \frac{(1-D)}{0.02}}$$

$$C_C = \frac{R_{LOAD} \times C_{OUT}}{R_C}$$

Step 3, compensate ESR zero frequency. If the output has only ceramic capacitors, C_P can be omitted

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

To ensure the stability of transients, the low-frequency gain after the design is recommended to be greater than 10dB, and the phase margin is greater than 45°.

9.4 Snubber Circuit

The RC snubber circuits at SWx nodes as shown below can be used to suppress the switching spike to improve the EMC performance. A typical snubber circuit is composed of

a 2.2Ω resistor and 1nF capacitor. The user can reduce the resistance and increase the capacitance further to improve the EMC. However, because it often causes higher switching loss and results in lower efficiency, it is suggested not to add snubber circuits unless necessary.

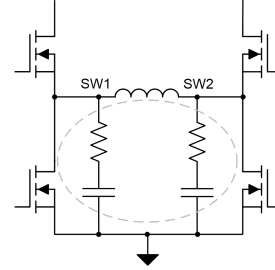


Figure 4 Snubber circuit at SWx nodes

9.5 PCB Layout

9.5.1 Layout guide

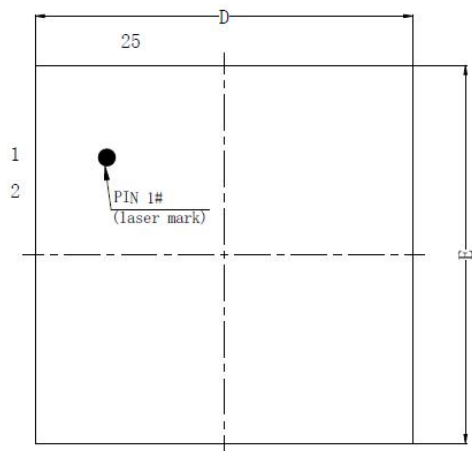
The PCB layout especially at the high switching frequency can affect the performance of the device seriously, such as efficiency, stability, noise, etc. Proper layout of the components to minimize high-frequency current path loop is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. Here is a PCB layout priority list for proper layout.

1. The input capacitors should be placed close to VIN and PGND pins, and the connection traces should be as short as possible. Since the trace will carry a high current, wide copper is suggested. Similarly, the output capacitors should be placed close to VOUT and PGND pins, and keep the trace as wide and short as possible. It is suggested to put the input and output capacitors on the contrary layer to the IC, so the trace to the PGND pad can be in the shortest way. Place sufficient vias to connect VIN or VOUT pins to the capacitors. It is recommended that all components and all power conversions be placed on the same PCB layer.
2. Put the inductor close to the SW1 and SW2 pins. Keep the SW1 and SW2 traces wide because they carry a high current during operation.
3. The bootstrap capacitors should be placed close to SW1 and BT1 or SW2 and BT2. To further reduce EMI radiation, a typical 2~15Ω resistor is recommended in series with the bootstrap capacitor to limit the turn-on slew rate of the high-side MOSFET.
4. Use RC snubbers for SW1 and SW2 to further reduce switching voltage spikes and improve EMI radiation performance. The RC snubbers should be put close to the SWx and PGND pin.
5. The VCC capacitor should be placed close to the VCC and PGND pin.
6. Other components such as the FB divider resistors, RC compensation network, etc should be kept away from the switching nodes SW1 and SW2.
7. Other signal traces should not block the ground return, and the power ground should be kept as wide and complete as possible.

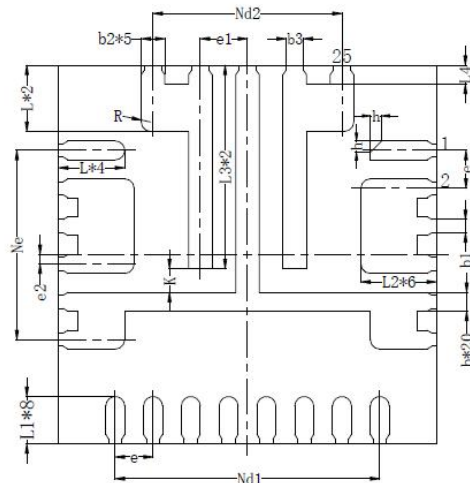
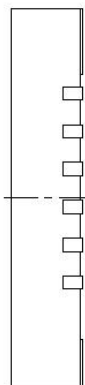
8. Use DC or GND shielding to reduce noise contamination.

MECHANICAL DATA

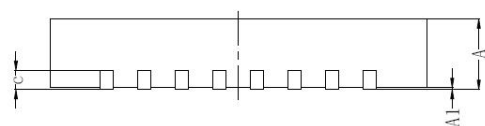
QFN-25 (4x4x0.75)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
b2	0.20	0.25	0.30
b3	0.18REF		
c	0.203REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40BSC		
e1	0.50BSC		
e2	0.10BSC		
Nd1	2.80BSC		
Nd2	2.00BSC		
Ne	2.00BSC		
L	0.65	0.70	0.75
L1	0.45	0.50	0.55
L2	0.75	0.80	0.85
L3	2.10	2.15	2.20
L4	0.15	0.20	0.25
h	0.07	0.12	0.17
R	0.05	0.10	0.15
K	0.25REF		

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