SC71220AQ, SC71420AQ, 16V/1.2A, High-Performance ASIL B Dual/Quad Channels High Side Switch for Automotive Camera Module

1 Descriptions

The SC71220AQ/SC71420AQ is a high-performance dual/quad channels high side switch for automotive camera modules which can deliver up to 1.2A load per channel. Each output channel is individually protected from short-to-battery, short-to-ground, and overcurrent conditions. The device operates from a 3V to 16V input supply. A back-to-back MOSFET configuration achieves up to 28V short-to-battery protection.

The device provides an enable input and I2C interface to read the diagnostic status of the device. An on-board ADC enables reading of the current through each switch. The ASIL B and ASIL D-compliant versions include support for reading an additional seven diagnostic measurements through the ADC, ensuring high-fault coverage.

The device includes overtemperature shutdown and overcurrent limiting on each output channel separately. All devices are designed to operate from -40°C to +125°C ambient temperature.

The device communicates to the MCU via the I2C interface. The device supports up to 8 addresses setting by ADDR pin and factory.

As a functional safety device, SC71220AQ/SC71420AQ is an ASIL B compliant part, providing well-developed monitoring and diagnostics with an internal ADC. Related safety documents are also provided to aid functional safety design.

The SC71220AQ/SC71420AQ is available in 20-pin 4mm X 4mm QFN package.

2 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range: -40°C to 125 °C
- Small Solution:
  - Up to Four 1.2A Protection Switches
  - 3V to 16V Input Supply Range
  - 3V to 5.5V Device Supply
  - 28V Short-to-Battery Protection with Back-to-Back MOSFET
  - 220mΩ On-State Channel Resistance
  - Adjustable Current Limit (up to 1.44A)
  - Parallel Multiple Channels for Higher Current
  - Selectable I2C Addresses
- High Precision:
  - +/- 9% Current-Limit Accuracy
  - 6μA Shutdown Current
- Functional Safety:
  - Integrated 8-bit ADC to Report Channel Output Voltage, Current and Supply Voltage
  - Input OV/UV and Output OV/UV Diagnostics
  - Open Load and Short-to-Battery/GND Diagnostics
  - ASIL B Compliant
  - Documents available to support ISO26262 design
  - Failure modes effects and diagnostic analysis
  - Safety manual

3 Applications

- Power-over-Coax for Radar and Camera Modules in Infotainment and ADAS System.

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4 Device Information

PART NUMBER	OUTPUTS	FUNCTION SAFETY	I2C ADDRESS(ADDR=0)	PACKAGE	BODY SIZE
SC71420AQQDLR	4	ASIL B	0x28	20 pin QFN	4mm x 4mm x 0.75mm
SC71420BQQDLR	4	ASIL B	0x2A	20 pin QFN	4mm x 4mm x 0.75mm
SC71420CQQDLR	4	QM	0x2A	20 pin QFN	4mm x 4mm x 0.75mm
SC71420QQDLR	4	QM	0x28	20 pin QFN	4mm x 4mm x 0.75mm
SC71220AQQDLR	2	ASIL B	0x28	20 pin QFN	4mm x 4mm x 0.75mm

*Notes: *For variants with different options, please contact us.*

5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.1.0	2025/10	NA	1.Release version
V1.1.1	2025/12	21,22	1.Update register description clerical error
V1.1.2	2026/4	23	1.Update Register Maps
V1.1.3	2026/4	18,20,23	1.Update Register Maps
V1.1.4	2026/4	13	1.Update Feature Description
V1.1.5	2026/7	19	1.Update Register Maps
V1.1.6	2026/7	9	1.Update Electrical Characteristics

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6 Typical Application Circuits

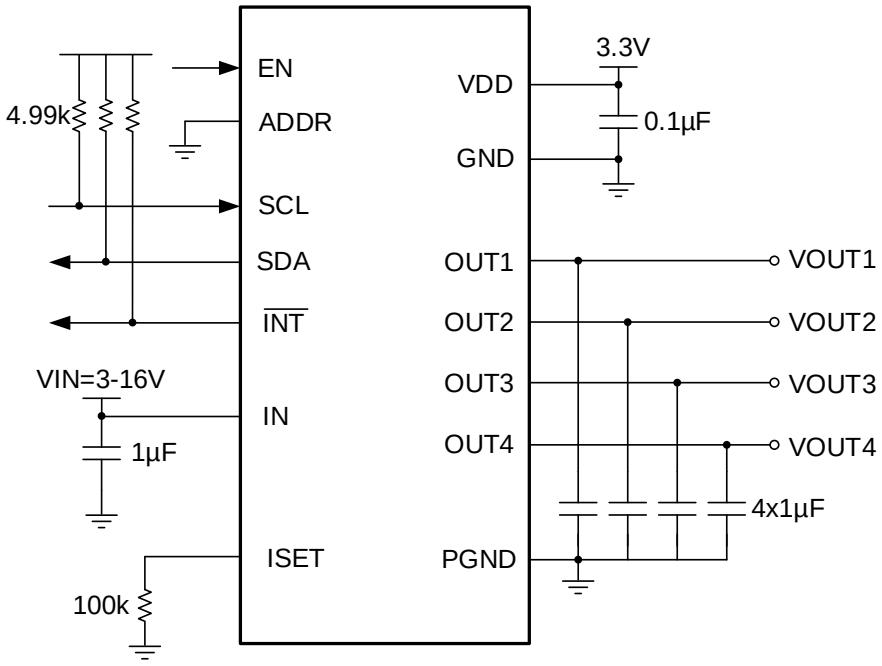

Figure 6-1. Typical Application Circuit of SC71420XQ

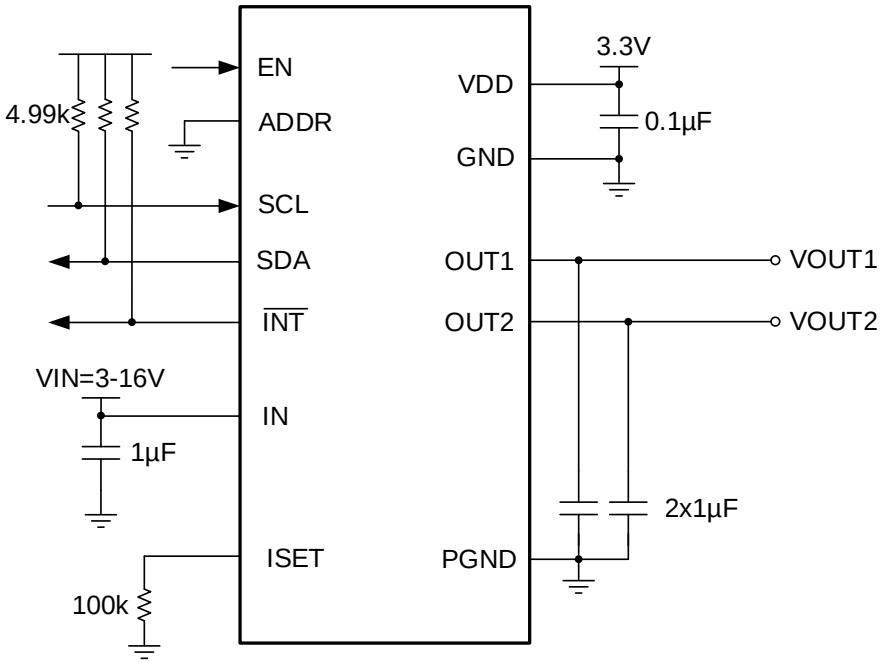

Figure 6-2. Typical Application Circuit of SC71220AQ

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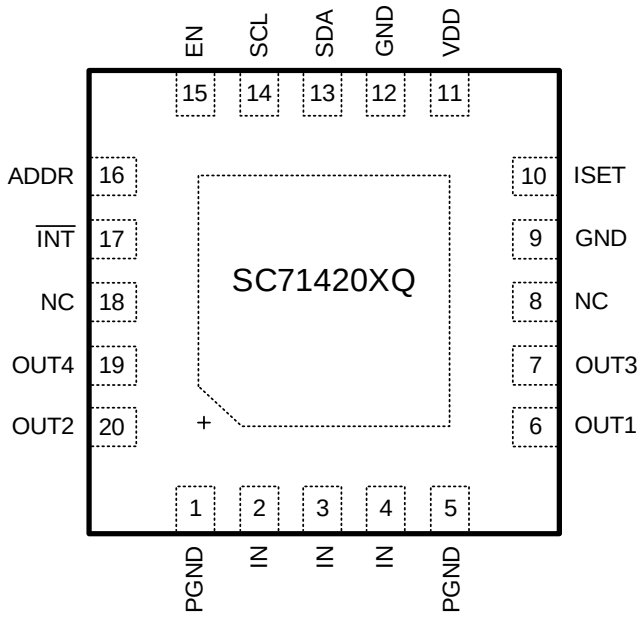
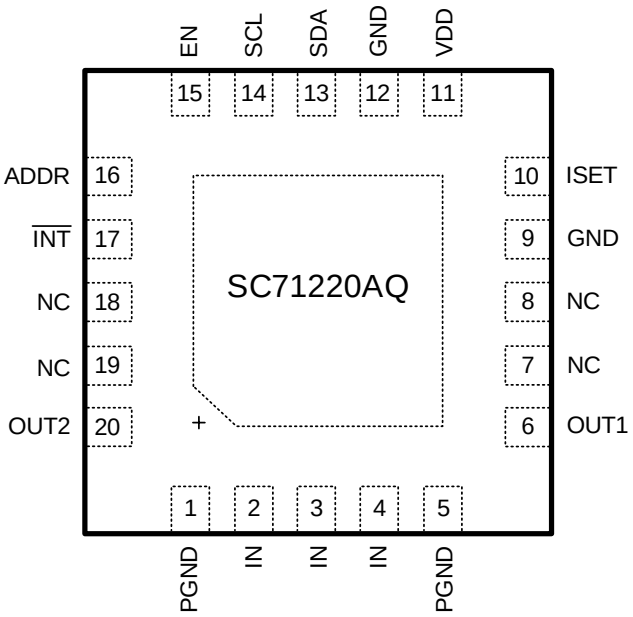
7 Terminal Configuration and Functions

TOP VIEW



TOP VIEW



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TERMINAL		NAME	I/O	DESCRIPTION
SC71420XQ	SC71220AQ			
NUMBER				
1, 5	1, 5	PGND	-	Power Ground. Connect GND and PGND together to the exposed pad (EP).
2, 3, 4	2, 3, 4	IN	I	Input Power Supply. Connect to the output of the DC-DC converter feeding the cameras.
6	6	OUT1	O	Protected Camera Supply Output 1. Connect a 1μF or larger ceramic capacitor from OUT1 to PGND.
7	-	OUT3	O	Protected Camera Supply Output 3. Connect a 1μF or larger ceramic capacitor from OUT3 to PGND.
8, 18	7, 8, 18, 19	NC	-	Not Connected. Leave unconnected or connect to ground.
9, 12	9, 12	GND	-	Analog Ground.
10	10	ISET	O	Connect a resistor from ISET to GND to set the per-channel current limit.
11	11	VDD	I	Device Input Supply. Connect a 100nF or larger ceramic capacitor from VDD to GND.
13	13	SDA	I/O	Data of I2C interface.
14	14	SCL	I	I2C Clock Input.
15	15	EN	I	Active-High Enable Input. Drive EN high for normal operation. On the rising edge, the enabled channels (in the CONFIG register) enter soft-start and on the falling edge, the channels turn off.
16	16	ADDR	-	I2C Address Select. Connect to ground or VDD to select between two different I2C addresses
17	17	INT	-	Active-Low, Open-Drain Interrupt Output. External pullup resistor required, if used.
19	-	OUT4	O	Protected Camera Supply Output 4. Connect a 1μF or larger ceramic capacitor from OUT4 to PGND.
20	20	OUT2	O	Protected Camera Supply Output 2. Connect a 1μF or larger ceramic capacitor from OUT2 to PGND.
-	-	EP	-	Exposed Pad. Connect EP to multiple ground planes with a grid of via for effective thermal dissipation.

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8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C ~ 150°C (unless otherwise noted). (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	IN to PGND	-0.3	20	V
	OUTx to IN	-20	28	V
	OUTx to PGND	-0.3	28	V
	VDD to GND	-0.3	6	V
	All other pins	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage (3), all pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
IN	Input voltage range for cameras	3		16	V
VDD	Input voltage range for device		3.3		V
C_{OUTX}	Output Capacitor		1		μF
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE		QFN20 (4mm x 4mm)	UNIT
$R_{\Theta JA}$	Junction to ambient thermal resistance (SC71420AQ EVM) (1)	24	°C/W

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$R_{\Theta JA}$	Junction to ambient thermal resistance (JESD 51-7) (2)	41	°C/W
$R_{\Theta JC}$	Junction to case resistance (2)	2	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance (2)	9.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (2)	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (2)	9.3	°C/W

(1) Measured on SC71420AQ EVM. 4-layer, 2oz Cu per top and bottom layer and 1oz Cu per inner layer.

(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{DD}=5V, V_{IN}=12V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATE CONDITION						
V_{DD}	Supply Voltage Range			3.3		V
I_{SHDN}	Shutdown Supply Current	V_{EN} = 0V, TA = +25°C		6	20	μA
I_{VDD}	Supply Current	V_{EN} = 5V		0.5		mA
V_{UVLO}	V_{DD} Undervoltage Lockout	Falling	2.5	2.7	2.9	V
V_{UVHYS}	V_{DD} Undervoltage Hysteresis			150		mV
V_{OVLO}	V_{DD} Overvoltage Lockout	Rising	5.5	5.7	5.9	V
V_{OVHYS}	V_{DD} Overvoltage Hysteresis			300		mV
$T_{SD1/2/3/4}$	Thermal shutdown temperature	T_J rising		173		°C
$T_{SD_HYS1/2/3/4}$	Thermal shutdown hysteresis			15		°C
$T_{WR1/2/3/4}$	Thermal warning temperature	T_J rising		150		°C
$T_{WR_HYS1/2/3/4}$	Thermal warning hysteresis			15		°C
SWITCH						
V_{IN}	Input Voltage Range		3.0		16	V
V_{INUVLO}	Input Undervoltage Lockout	Falling	2.5	2.7	2.9	V
V_{INUVH}	Input Under-voltage Lockout Hysteresis			140		mV
V_{INOV}	Input Overvoltage Lockout	Rising	15.5	16.2	17.0	V
V_{INOVH}	Input Overvoltage Hysteresis			0.4		V
I_{IN}	Input Current	V_{EN} = 0V, TA = +25°C		0.1		μA
		All switches enabled, no load		2.0		mA
$R_{ON1/2/3/4}$	On-Resistance			220	400	mΩ
$T_{URAMP1/2/3/4}$	Soft-Start Ramp Time	Option1, 0mA to I_{LIM}		0.5		ms
		Option2, 0mA to I_{LIM}		1		ms
		Option3, 0mA to I_{LIM}		2		ms

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		Option4, 0mA to I_{LIM}		4		ms
$T_{DRAMP1/2/3/4}$	Soft-Shutdown Ramp Time	Option1, from full-on ILIM value to high impedance, any condition that turns off a channel		0.25		ms
		Option2, from full-on ILIM value to high impedance, any condition that turns off a channel		0.5		ms
		Option3, from full-on ILIM value to high impedance, any condition that turns off a channel		1		ms
		Option4, from full-on ILIM value to high impedance, any condition that turns off a channel		2		ms
V_{OUTOV}	Output Overvoltage Threshold	V_{OUT} - V_{IN}, V_{OUT} rising, output disabled	0.10	0.15	0.22	V
V_{OUTOVH}	Output Overvoltage Hysteresis			50		mV
V_{OUTOV_DT}	Output Overvoltage Filter Time	For short to VBAT detection		3		µs
$V_{OUTUV1/2/3/4}$	Output Undervoltage Threshold	V_{IN} – V_{OUT}, V_{OUT} falling	0.55	0.7	0.85	V
$V_{OUTUVH1/2/3/4}$	Output Undervoltage Hysteresis			50		mV
V_{OUTUV_DT}	Output Undervoltage Filter Time			8		µs
CURRENT LIMIT						
I_{OUT}	IOUT Operating Range		72		1498	mA
$I_{LIM_DEFAULT1/2/3/4}$	ILIM Default Current	ISET out of operating range	1200	1498	1600	mA
I_{SET_PULL}	ISET Pullup Current	VISET = 1.25V	4.6	5	5.4	µA
I_{LIM_SET}	Forward Current Limit	R_{ISET} = 25kΩ	136	150	187	mA
		R_{ISET} = 50kΩ	273	300	327	
		R_{ISET} = 100kΩ	546	600	654	
		R_{ISET} = 150kΩ	819	900	981	
		R_{ISET} = 200kΩ	1092	1200	1308	
$V_{HSCG1/2/3/4}$	Hard Short-Detection Comparator Threshold		1.8	1.9	2.0	V
t_{HSC_DT}	Hard Short-Detection Time			1		ms
t_{SSC_DT}	Soft Shorted Output-Detection Time			10		ms
t_{SC_RETRY}	Shorted Output-Retry Time			250		ms
ANALOG						
R_{VIN}	V_{IN} Divide Ratio		-5%	14	+5%	V/V
R_{VDD}	V_{DD} Divide Ratio		-2%	5	+2%	V/V
R_{VISET}	V_{ISET} Divide Ratio		-2%	1	+2%	V/V
R_{VOUT}	V_{OUT} Divide Ratio	V_{IN} - V_{OUT} = 200mV, excluding ADC error	-5%	14	+5%	V/V
LSB-V_{IN}	V_{IN} Voltage LSB			70		mV
LSB-V_{DD}	V_{DD} Voltage LSB			24.78		mV

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LSB-V_{ISET}	V_{ISET} Voltage LSB			5		mV
LSB-V_{OUT}	V_{OUT} Voltage LSB			70		mV
LSB-I_{OUT}	Output-Current LSB	From 0 to 90% of VO1, no load		6		mA
ADC						
V_{DD_ADC}	Normal Supply Voltage	ADC accuracy is ensured	2.8	3.3	5.5	V
	ADC Resolution			8		Bits
INL	Integral Nonlinearity(1)		-1.5		+1.5	LSB
DNL	Differential Nonlinearity(1)		-1		+1	LSB
V_{ADC_REF}	Reference		1.254	1.28	1.306	V
SENSING ACCURACY (including ADC error)						
ACC-V_{IN}	V_{IN} Reading Accuracy		-3%		3%	ΔV/V
ACC-V_{OUT}	V_{OUT} Reading Accuracy		-3%		3%	ΔV/V
ACC-I_{OUT}	Current Reading Accuracy	I_{OUT} = 1200mA	-5%		5%	ΔI/I
		I_{OUT}= 132mA	-9%		9%	ΔI/I
		I_{OUT}= 30mA	-2		2	LSB
DIGITAL OUTPUT (INT)						
V_{INT_L}	Digital Output Low Level	V_{DD} = 3.0V, I_{SINK} = -2mA			0.2	V
I_{INT_LK}	Digital Output leakage	ERR, SDA = VDD = 5.5V			1	μA
DIGITAL INPUTS (EN, SDA, SCL, ADDR)						
V_{EN_H}	Input High Level	Rising	1.3			V
V_{EN_L}	Input Low Level	Falling			0.4	V
V_{EN_HYS}	Hysteresis			0.1		V
I_{EN_PU}	EN Pulldown Current	V_{EN} = 5.0V		1		μA
I_{ADDR_PU}	ADDR Pulldown Current	V_{ADDR} = 5.0V		3		μA
I2C INTERFACE						
V_{IH_IIC}	Input logic high for I2C		1.3			V
V_{IL_IIC}	Input logic low for I2C				0.4	V
f_{SCL}	Clock Frequency				1	MHz
t_{HIGH} (1)	SCL High Time		260			ns
t_{LOW} (1)	SCL Low Time		350			ns
t_{SU_DAT} (1)	Data Setup Time		50			ns
t_{HD_DAT} (1)	Data Hold Time		0			ns
t_{SU_STA} (1)	Setup Time for (Repeated) Start Condition		260			ns
t_{HD_STA} (1)	Hold Time for (Repeated) Start Condition		260			ns
t_{SU_STO} (1)	Setup Time for Stop Condition		260			ns
t_{SP} (1)	Pulse Width of Suppressed Spike			50		ns

(1) Guarantee by Design; not production tested.

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8.6 Typical Characteristics

V_{IN}=12V, V_{DD}=3.3V, T_A=25°C, unless otherwise noted.

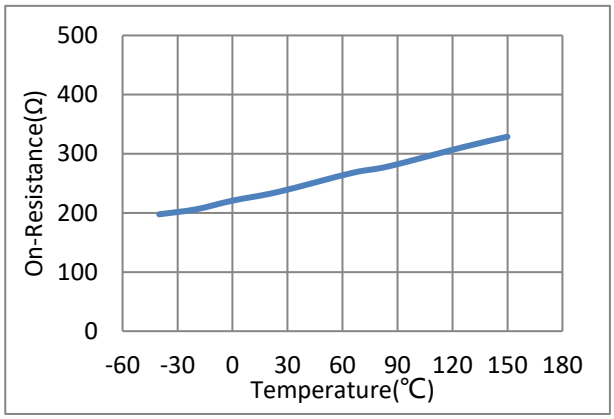

Figure 8-1. ON-Resistance

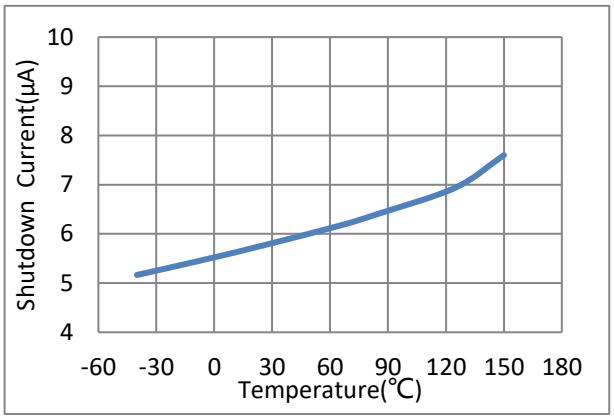

Figure 8-2. Shutdown Supply Current

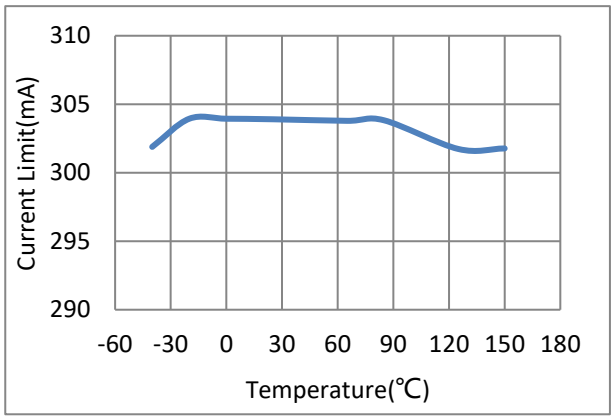

Figure 8-3. Current Limit(I_{LIM_SET} =300mA)

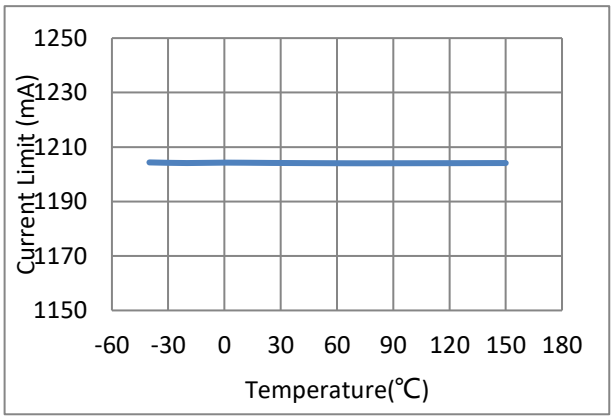

Figure 8-4. Current Limit(I_{LIM_SET} =1200mA)

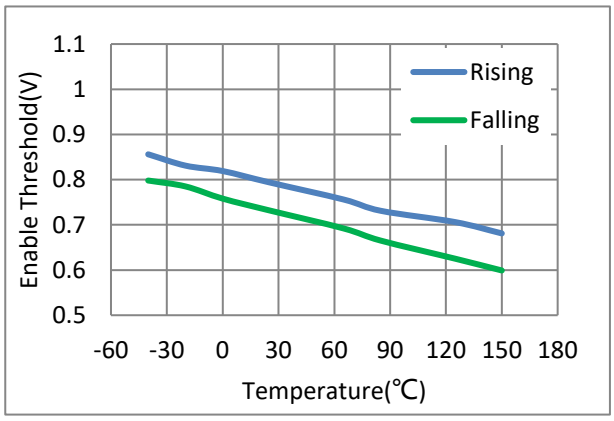

Figure 8-5 Enable Threshold

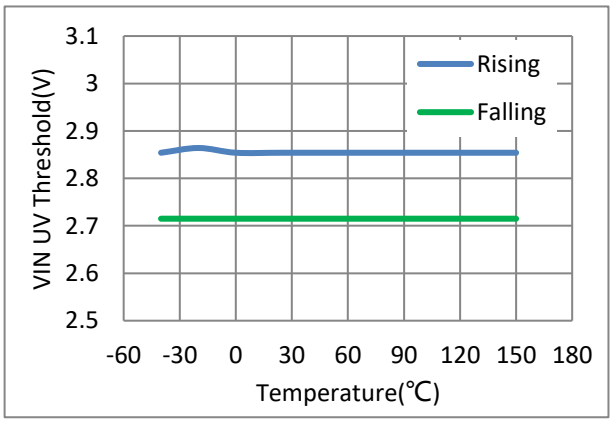

Figure 8-6 VIN UV Threshold

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8.7 Typical Performance Characteristics

V_{IN}=12V, V_{DD}=3.3V, OUT1-OUT4 no load, T_A=25°C, unless otherwise noted.

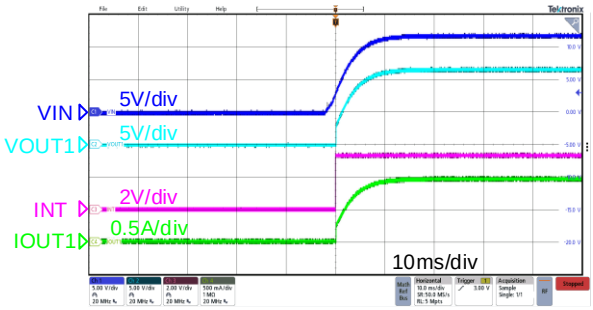

Figure 8-7. V_{IN} ON, OUT1=12Ω

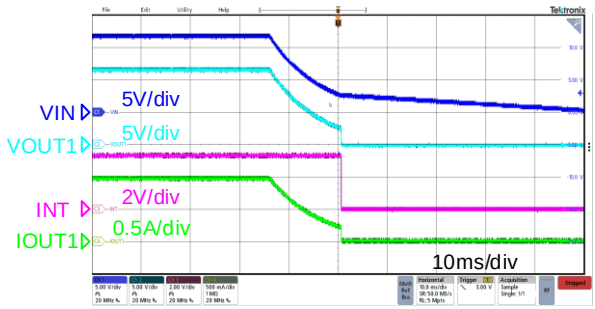

Figure 8-8. V_{IN} OFF, OUT1=12Ω

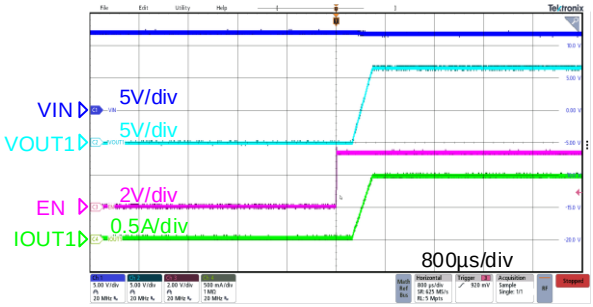

Figure 8-9. EN ON, OUT1=12Ω

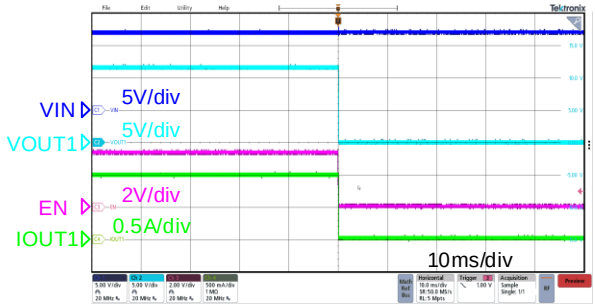

Figure 8-10. EN OFF, OUT1=12Ω

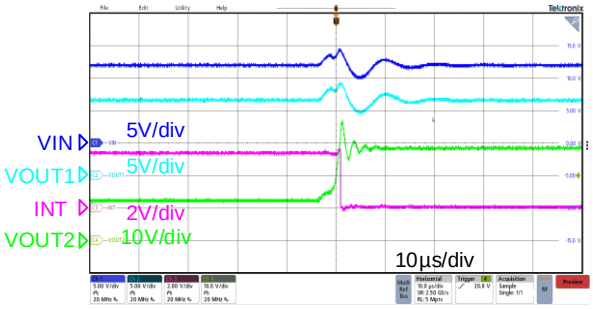

Figure 8-11. OUT1=12Ω, OUT2 Short to 28V Battery

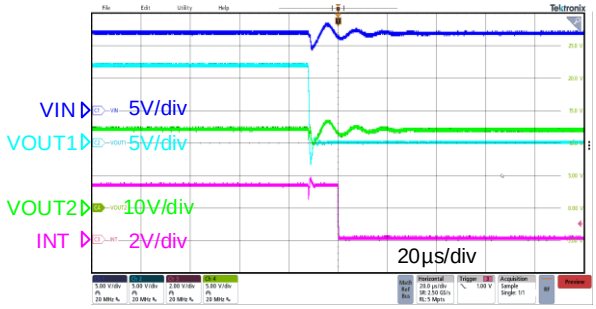

Figure 8-12. OUT1 Short to Ground

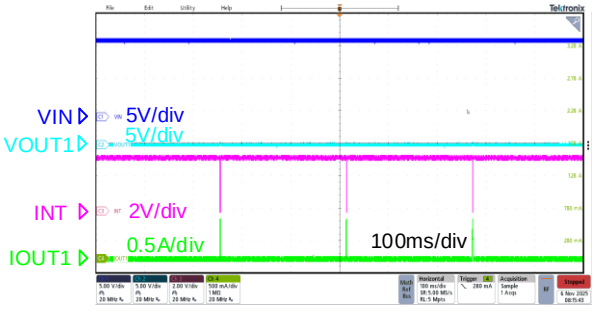

Figure 8-13. OUT1 Short to Ground Steady State

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9 Functional Block Diagram

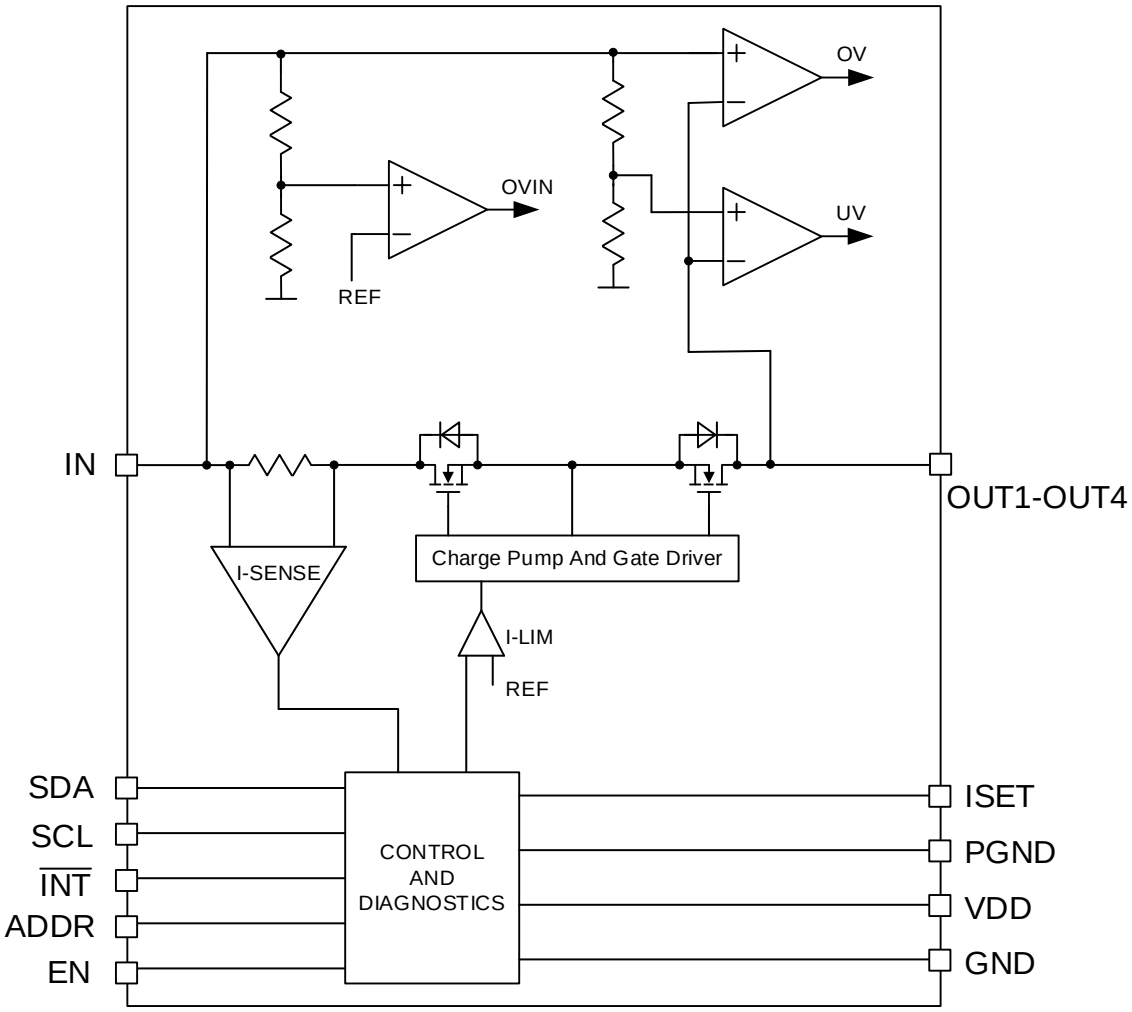

Figure 9-1. Function Block

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10 Feature Description

10.1 Overview

The SC71220AQ/SC71420AQ is a high-performance dual/quad channels high side switch for automotive camera modules which can deliver up to 1.2A load per channel. The input supply voltage range is from 3V to 16V, while the output can tolerate up to 28V (VOUT – VIN). Each output

has an accurate current limit of ±9% to protect the input power supply from overload and short-circuit conditions. In a short-to-battery on the output, the switch opens to prevent back feeding of the battery to the input supply. The internal 8-bit ADC enables reading of the current from each output digitally, simplifying system design.

The ICs can be configured and the status read for each channel through the I2C interface. Individual channels can also be turned on/off through I2C.The ICs are ASIL B compliant, without additional software diagnostics. The internal 8-bit ADC is capable of reading the current and output voltage across each output, along with the voltages of the input supplies and external power rails.

The ICs include overtemperature shutdown and overcurrent limiting separately on each channel. All devices are designed to operate from -40°C to +125°C ambient temperature.

10.2 Enable Control Input (EN)

The EN input activates the device from the low-power shutdown state. The I2C interface to the device is active when VDD is present, even with the EN pin low.

When the EN input goes high, channels with CONFIG.EN[4:1] bits set are enabled. If the EN pin is toggled low, the STAT1-5 faults continue to hold last value and are cleared after reading. If the EN pin is toggled low, the ADC registers continue to hold the last value (they are not cleared after reading). The EN pin should be high for the diagnostics (STAT1-5, and ADC) to update.

10.3 Interrupt Output ($\overline{\text{INT}}$)

The ICs feature an open-drain fault-interrupt output that asserts when any unmasked fault status bit is set. After a fault clears, the clearing of the corresponding status bit depends on CLR bit setting. Connect a pullup resistor from $\overline{\text{INT}}$ to the system I/O supply. The pullup resistance should normally be ≥ 2kΩ to ensure that device can pull down to the specified voltage level

10.4 Soft-Start/Soft-Shutdown

The ICs include a selectable soft-start from 0.5ms to 4ms. Soft-start time limits startup inrush current by ramping the output current from 0mA to ILIM value set by the ILIM registers. The ICs also include a selectable soft-shutdown to minimize inductive ringing on the output channels. When disabled or faulted, the current ramps down from ILIM to 0A in 0.25ms, selectable up to 1ms depending on option selected. This prevents false fault detection caused by inductive ringing that may result from the sudden change in current.

The default value of soft-start/soft-shutdown time is 0.5ms/0.25ms, and it can be configured by OTP.

10.5 Setting the Current Limit

Several factors determine the minimum current-limit setting for proper operation. Each output acts as a current source during the power-up phase. This means that each switch is in current limit, which is a high-power dissipation state. To protect the FETs, they can only be in current limit for a specific amount of time. It is important that the output capacitance is fully charged before this time expires.

The current limit per channel can be set based on the formula in Equation 1

$$ILIM = 600\text{mA} \times \frac{R_{ISET}}{100k\Omega} \quad (1)$$

Note: (valid between 100mA and 1200mA)

Two or more channels can be connected in parallel to supply higher current (two, three, or four times ILIM per channel). When paralleling channels, about 10% margin should be provided for mismatch between individual channel current limits.

10.6 ADC Operation

The 8-bit ADC can be used for diagnostics of the system. There are three different mux settings that allow switch current, switch voltage, and other system voltages to be read through the on-board ADC.

See Table 10-1 for ADC mux settings and Figure 10-1 for an ADC flow diagram.

Table 10-1 ADC Mux Settings

MUX SETTING	DESCRIPTION
00	ADC1–ADC4 readings contain the output current through OUT1–OUT4, respectively.

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	The current can be calculated as: IOUT1–IOUT4 = ADC1–ADC4 x 6mA
01	ADC1–ADC4 readings contain the voltage at the output of the switches of OUT1–OUT4, respectively. The output voltage can be calculated as: VOUT1–VOUT4 = ADC1–ADC4 x 70mV
10	ADC1–ADC4 contain the following voltage readings: ADC1 = VIN (70mV/count) ADC2 = VDD (23.75mV/count) ADC3 = VISET (5mV/count) ADC4 = Unused

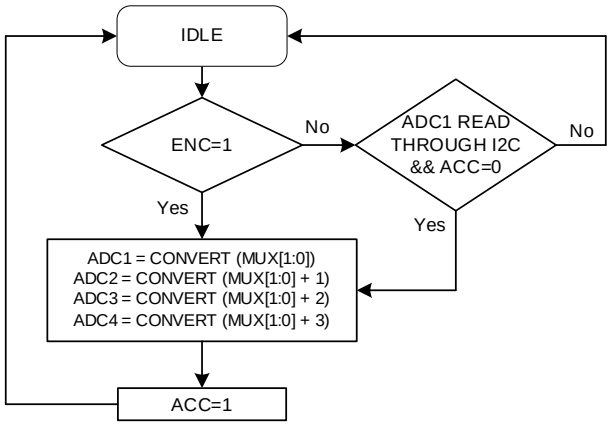

Figure 10-1. ADC Flow Diagram

10.7 Current-Limit/Short-Circuit Protection

The ICs feature current limit that protects the device and remote camera module against short-circuit and overload conditions at the outputs. In the event of a short-circuit or overload condition, the current is limited to the current set by RISET. When a channel has been in current limit for 10ms (1ms when the output voltage is < 2V), the channel turns off to prevent excessive power dissipation. The channel is reenabled after 250ms, entering soft-start.

10.8 Short-to-Battery Protection

The ICs feature a differential overvoltage comparator to detect a short-to-battery condition and prevent back feeding to the input supply. The input voltage is also monitored to provide a redundant path for detection.

If a short-to-battery event occurs before an output is enabled, the output does not turn on, regardless of the enable status.

A short-to-battery condition is detected by the differential OV comparator if the part is enabled.

If the short-to-battery event occurs after an output has been enabled, the reverse-blocking FET is forced off, regardless

of the enable state. The other FET remains enabled; if the short is temporary, the output remains operational, without

having to go through soft-start. After the 100µs(typ) timeout, if the OV fault is not present, the reverse-blocking FET is reenabled.

10.9 Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds +165°C (typ) at a specific output switch, the output switch is turned off, allowing the IC to cool. All other output channels remain enabled. The thermal sensor allows the output channel to turn on again after the junction temperature cools by 15°C

10.10 Automatic Built-in Self Test(ABSIT) Process

The ICs designed a ABIST flow for internal comparator. The input and output overvoltage/undervoltage comparators, thermal warning/shutdown comparators, internal bandgap overvoltage/undervoltage comparators can be tested by using the following procedure:

1. Set EN pin = Low

2. Set CONFIG.EN[4:1] = ‘0’

3. Set EN pin = High

4. IN voltage > IN UV threshold

5. Set MASK.OVTST = ‘1’

6. Read STAT1-5 registers and verify that the corresponding bits are set to ‘1’.

7. Set MASK.OVTST = ‘0

If the IC pass the ABIST flow, the corresponding bit in STAT1-5 will be set to 1. If one of comparator failed the ABIST flow, the corresponding bit in STAT1-5 will be set to 0. Read STAT1-5 to check ABIST result.

Note: Overvoltage and undervoltage conditions on OUT, IN, and VDD cannot be detected while the comparator diagnostic is enabled.

10.11 Packet Error Code (PEC)

In order to increase fault coverage on the I2C interface an optional PEC byte is supported. If PEC is enabled and the

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IC receives an I2C packet with the incorrect PEC byte, the packet is ignored and the IIC_CRC_ERR bit in the STAT1 register is set. This follows the SMBus implementation which The PEC calculation does not include ACK, NACK, START, STOP, nor Repeated START bits. This means that the PEC is computed over the entire message from the first START condition. The ICs supports read and write packets, single byte. For write packets, if PEC is enabled but the master does not provide a valid PEC byte, the PEC byte will be NACK'd and the write data will be ignored. For read packets, the ICs will compute the PEC and return it as the last byte in the message.

calculated the PEC byte using a CRC-8 polynomial of $x^8 + x^2 + x + 1$.

Note: The PEC function can only be configured by OTP Option.

10.12 OTP Check

In order to increase fault coverage，the ICs feature OTP CRC check on OTP storage content. When VDD is high，OTP CRC check starts，if the IC fail the effuse CRC check，the OTP_CRC_DET bit in the STAT5 register is set and the INT will be pulled low.

10.13 Fault Detection

The status registers contain information on the device's status. Table 10-2 details the different faults and information bits within the status registers.

Table 10-2 Status Registers (Faults and Information Bits)

STATUS BIT	DIAGNOSTIC COVERAGE
ISET	When '1' indicates the ISET pin does not have the expected resistance range connected to it. This can be a short-to ground, open, or incorrect resistance value.
UVIN	When '1' indicates that voltage connected to the IN pin is below 2.7V. The outputs are forced off in this condition.
OVIN	When '1' indicates that voltage connected to the IN pin is above 16.5V. The outputs are forced off in this condition
UVDD	When '1' indicates that voltage connected to the VDD pin is below 2.7V. The outputs are forced off in this condition.
OVDD	When '1' indicates that voltage connected to the VDD pin is above 5.7V. The outputs are forced off in this condition.
TS[4:1]	When any of these are '1', the associated channel(s) are in thermal shutdown. The channel remains off until the temperature drops below the thermal-shutdown hysteresis temperature.
TW[4:1]	When any of these are '1', the associated channel(s) are still on, until the temperature reach the thermal shutdown value.
OC[4:1]	When any of these are '1', the associated channel(s) have been in current limit and a shorted output has been detected. The channel(s) off immediately; the real-time status changes back to '0' during the hiccup phase. While the short is present, the associated OC[4:1] bit(s) toggle, but the associated UV[4:1] bit(s) remain '1', indicating the output is not in regulation.

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UV[4:1]	When any of these are '1', the associated channel(s) output are in undervoltage.
OV[4:1]	When any of these are '1', the associated channel(s) output is higher than the input voltage. This can occur if there is a short-to-battery condition, or a transient condition due to abrupt input voltage or output current changes. This fault information should be debounced in software to prevent a false fault detection. In a real fault condition, these bit(s) are '1' for the entire time the fault is present.
ABIST_ERR	The outputs are still on in this condition.
IIC_CRC_ERR	This Bit is only valid when I2C communication PEC is enabled by OTP. When '1' indicates that error happened in the I2C communication. The outputs are still on in this condition.
OTP_CRC_DET	When '1' indicates that the storage content of OTP has changed. The outputs are still on in this condition.

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11 Layout Guide

The PCB layout is critical to get the optimal performance and thermal dissipation. **Figure 11-1** shows a recommended layout.

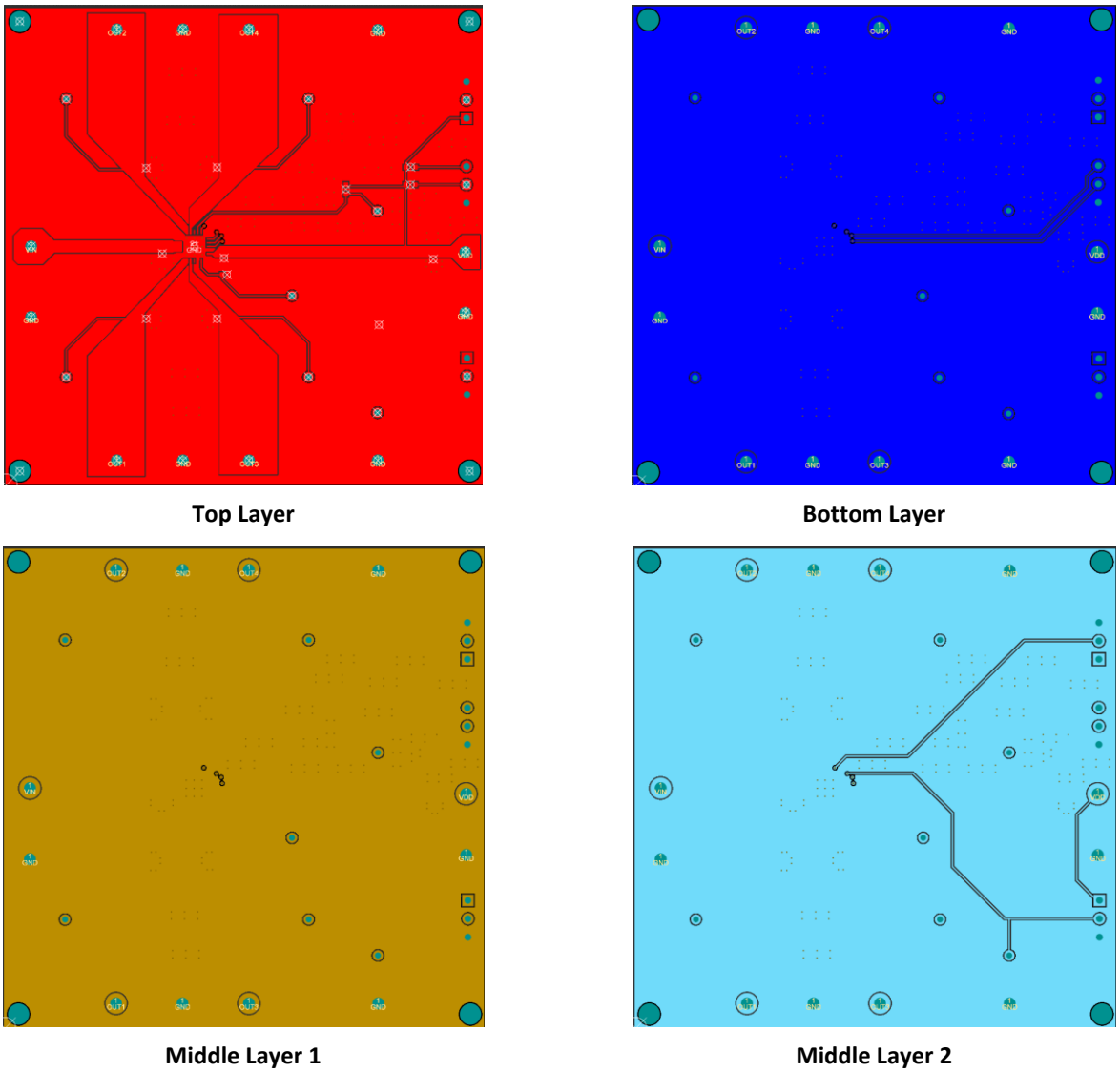
1. The 0.1μF ~ 4.7μF capacitors connected at VDD pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.

2. The 1μF ~ 4.7μF capacitors connected at OUTx and IN pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.

3. To enhance the thermal dissipation capability of the IC, place via under the Thermal PAD

4. Place PGND vias close to PGND pin and under the IC's body.

5.Connect a large ground plane to GND on all layers. Add vias near GND if there are several ground planes on different layers.



Top Layer

Bottom Layer

Middle Layer 1

Middle Layer 2

Figure 11-1 Layout Example

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12 Register Maps

Table12-1 SC71420AQ Register Maps

Addr	Name	Type	D7	D6	D5	D4	D3	D2	D1	D0
0x00	MASK[7:0]	RW	OVTST	ACCM	TSM	VDDM	VINM	OCM	OVM	UVM
0x01	CONFIG[7:0]	RW	MUX[1:0]		ENC	CLR	EN4	EN3	EN2	EN1
0x02	ID[7:0]	RW	RESERVED							
0x03	STAT1[7:0]	R	ABIST_ERR	IIC_CRC_ERR	ISET	ACC	OVIN	UVIN	OVDD	UVDD
0x04	STAT2[7:0]	R	TS2	OC2	OV2	UV2	TS1	OC1	OV1	UV1
0x05	STAT3[7:0]	R	TS4	OC4	OV4	UV4	TS3	OC3	OV3	UV3
0x06	ADC1[7:0]	R	DATA_ADC1[7:0]							
0x07	ADC2[7:0]	R	DATA_ADC2[7:0]							
0x08	ADC3[7:0]	R	DATA_ADC3[7:0]							
0x09	ADC4[7:0]	R	DATA_ADC4[7:0]							
0x0B	MASK2[7:0]	RW	TW4M	TW3M	TW2M	TW1M	Reserved	Reserved	ABIST_ERR_Mask	IIC_CRC_ERR_MASK
0x1A	START_SLEW[7:0]	RW	SS_RAMP4[1:0]		SS_RAMP3[1:0]		SS_RAMP2[1:0]		SS_RAMP1[1:0]	
0x1B	SHDN_SLEW[7:0]	RW	SSD_RAMP4[1:0]		SSD_RAMP3[1:0]		SSD_RAMP2[1:0]		SSD_RAMP1[1:0]	
0x27	STAT4[7:0]	R	TW4	TW3	TW2	TW1	Reserved	Reserved	Reserved	Reserved
0x28	STAT5[7:0]	R	BG_OV	BG_UV	INT_REG_OV	INT_REG_UV	Reserved	Reserved	Reserved	OTP_CRC_DET

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MASK (0x00)

Bit	Type	Bit Name	Default	Description
7	R/W	OVTST	0b	The EN pin must be low to run the diagnostics. The OVIN and OV[4:1] bits in the status registers are set to '1'. 0x0: OV Comparators function normally; 0x1: OV comparator diagnostics enable.
6	R/W	ACCM	1b	ADC Conversion Complete Mask. 0x0: ADC conversion complete, mapped to INT pin 0x1: Mask ADC conversion complete
5	R/W	TSM	0b	Thermal Shutdown Mask. 0x0: Thermal-shutdown faults TS[4:1], TLIM_SERV mapped to INT pin; 0x1: Mask thermal-shutdown faults.
4	R/W	VDDM	0b	VDD Fault Mask. 0x0: OVDD and UVDD mapped to INT pin; 0x1: Mask OVDD and UVDD fault.
3	R/W	VINM	0b	VIN fault mask. 0x0: OVIN and UVIN mapped to INT pin; 0x1: Mask OVIN fault.
2	R/W	OCM	0b	Overcurrent Mask. 0x0: Overcurrent faults OC[4:1] mapped to INT pin; 0x1: Mask short-to-ground fault.
1	R/W	OVM	0b	Overvoltage Mask. 0x0: Overvoltage faults OV[4:1] mapped to INT pin; 0x1: Mask short-to-battery fault.
0	R/W	UVM	0b	Undervoltage Mask (ALL channels). 0x0: Undervoltage faults UV[4:1] mapped to INT pin; 0x1: Mask UV fault.

CONFIG (0x01)

Bit	Type	Bit Name	Default	Description
7:6	R/W	MUX	00b	ADC Mux Select. 00: ADC1-ADC4 registers contain current reading of each Output; 01: ADC1-ADC4 registers contain the output voltages of each output; 10: ADC1-ADC2 registers contain the output voltages of VIN, VDD; 11: Reserved.
5	R/W	ENC	0b	Enable Continuous ADC Reading. 0x0: ADC conversion cycle started by reading ADC1 register; ADC1-ADC4 registers updated sequentially; 0x1: ADC continuously updates ADC1-ADC4 registers. First conversion is started when EN pin toggles high. A new conversion is started after ADC1 is read
4	R/W	CLR	1b	Clear Faults on Read. 0x0: INT pin state and fault registers latch until read through I2C(except internal bandgap and regulator fault); 0x1: INT pin reflects the real-time fault status. Status register fault bits latch until read through I2C.
3	R/W	EN4	1b	Individual Enable Control. 0x0: Disabled; 0x1: Enable OUT4 when EN pin is high.
2	R/W	EN3	1b	Individual Enable Control. 0x0: Disabled; 0x1: Enable OUT3 when EN pin is high.

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1	R/W	EN2	1b	Individual Enable Control. 0x0: Disabled; 0x1: Enable OUT2 when EN pin is high.
0	R/W	EN1	1b	Individual Enable Control. 0x0: Disabled; 0x1: Enable OUT1 when EN pin is high.

ID (0x02)

Bit	Type	Bit Name	Default	Description
7:0	R	Reserved	0	Reserved

STAT1 (0x03)

Bit	Type	Bit Name	Default	Description
7	R	ABIST_ERR	0b	Error Flag for Built-in self-test. 0x0: normal operation; 0x1: OV BIST, UV BIST, EFUSE BIST, or VBG check failed.
6	R	IIC_CRC_ERR	0b	IIC_CRC check error indicator. 0x0: CRC check passed; 0x1: CRC check failed.
5	R1C	ISET	0b	ISET Diagnostics Status. 0 = ISET within operating range; 1 = ISET pin open or shorted.
4	R	ACC	0b	ADC Conversion Complete. 0: Bit is reset reading ADC1_LEGACY; the latest completed ADC readings are always available at ADC1-ADC4 registers; 1: ADC conversions are completed.
3	R1C	OVIN	0b	Input overvoltage. 0: VIN < OVIN threshold; 1: VIN > OVIN threshold.
2	R1C	UVIN	0b	Input undervoltage. 0: VIN > UVIN threshold; 1: VIN < UVIN threshold.
1	R1C	OVDD	0b	VDD overvoltage. 0: VDD < OVDD threshold; 1: VDD > OVDD threshold.
0	R1C	UVDD	0b	VDD undervoltage. 0: VDD > UVDD threshold; 1: VDD < UVDD threshold (switches turned off).

STAT2 (0x04)

Bit	Type	Bit Name	Default	Description
7	R1C	TS2	0b	Thermal Shutdown on OUT2: Each channel has its own thermal sensor. 0 = No fault; 1 = Thermal shutdown occurred on OUT2.
6	R1C	OC2	0b	Overcurrent on OUT2: Hard-short or Soft-short conditions detected. The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time, If fault latching is not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. 0 = No overcurrent present; 1 = Hard-short or Soft-short conditions detected.
5	R1C	OV2	0b	Overvoltage on OUT2. 0 = Output voltage < OV threshold; 1 = Output voltage > OV threshold.
4	R1C	UV2	0b	Undervoltage on OUT2. 0 = Output voltage > UV threshold; 1 = Output voltage < UV threshold.
3	R1C	TS1	0b	Thermal Shutdown on OUT1. 0 = No fault; 1 = Thermal shutdown occurred on OUT1.
2	R1C	OC1	0b	Overcurrent on OUT1: Hard-short or Soft-short conditions detected.

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				0 = No overcurrent present; 1 = Hard-short or Soft-short conditions detected.
1	R1C	OV1	0b	Undervoltage on OUT1. 0 = Output voltage > UV threshold; 1 = Output voltage < UV threshold overvoltage.
0	R1C	UV1	0b	Undervoltage on OUT1. 0 = Output voltage > UV threshold; 1 = Output voltage < UV threshold.

STAT3 (0x05)

Bit	Type	Bit Name	Default	Description
7	R1C	TS4	0b	Thermal Shutdown on OUT4: Each channel has its own thermal sensor. 0 = No fault; 1 = Thermal shutdown occurred on OUT4.
6	R1C	OC4	0b	Overcurrent on OUT4: Hard-short or Soft-short conditions detected. The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time, If fault latching is not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. 0 = No overcurrent present; 1 = Hard-short or Soft-short conditions detected.
5	R1C	OV4	0b	Overvoltage on OUT4. 0 = Output voltage < OV threshold; 1 = Output voltage > OV threshold.
4	R1C	UV4	0b	Undervoltage on OUT4. 0 = Output voltage > UV threshold; 1 = Output voltage < UV threshold.
3	R1C	TS3	0b	Thermal Shutdown on OUT3. 0 = No fault; 1 = Thermal shutdown occurred on OUT3.
2	R1C	OC3	0b	Overcurrent on OUT3: Hard-short or Soft-short conditions detected. 0 = No overcurrent present; 1 = Hard-short or Soft-short conditions detected.
1	R1C	OV3	0b	Undervoltage on OUT3. 0 = Output voltage > UV threshold; 1 = Output voltage < UV threshold overvoltage.
0	R1C	UV3	0b	Undervoltage on OUT3. 0 = Output voltage > UV threshold; 1 = Output voltage < UV threshold.

ADC1 (0x06)

Bit	Type	Bit Name	Default	Description
7:0	R	DATA_ADC1[7:0]	0x00	ADC1 Reading. See MUX[1:0] settings in CONFIG register. ADC Readings Registers: 00 = ADC1–ADC4 contain current readings of each output ADC1–ADC4 readings contain the output current through OUT1–OUT4, respectively. The current can be calculated as: IOUT1–IOUT4 = ADC1–ADC4 x 6mA 01 = ADC1–ADC4 contain output-voltage readings of each output ADC1–ADC4 readings contain the voltage at the output of the switches of OUT1–OUT4, respectively. The output voltage can be calculated as: VOUT1–VOUT4 = ADC1–ADC4 x 70mV 10 = ADC1–ADC3 contain VIN, VDD, VISET ADC1–ADC4 contain the following voltage readings: ADC1 = VIN (70mV/count) ADC2 = VDD (24.78mV/count) ADC3 = VISET (5mV/count) ADC4 = Unused

ADC2 (0x07)

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Bit	Type	Bit Name	Default	Description
7:0	R	DATA_ADC2[7:0]	0x00	ADC2 Reading. See MUX[1:0] settings in CONFIG register. ADC Readings Registers: 00 = ADC1–ADC4 contain current readings of each output ADC1–ADC4 readings contain the output current through OUT1–OUT4, respectively. The current can be calculated as: IOUT1–IOUT4 = ADC1–ADC4 x 6mA 01 = ADC1–ADC4 contain output-voltage readings of each output ADC1–ADC4 readings contain the voltage at the output of the switches of OUT1–OUT4, respectively. The output voltage can be calculated as: VOUT1–VOUT4 = ADC1–ADC4 x 70mV 10 = ADC1–ADC3 contain VIN, VDD, VISET ADC1–ADC4 contain the following voltage readings: ADC1 = VIN (70mV/count) ADC2 = VDD (24.78mV/count) ADC3 = VISET (5mV/count) ADC4 = Unused

ADC3 (0x08)

Bit	Type	Bit Name	Default	Description
7:0	R	DATA_ADC3[7:0]	0x00	ADC3 Reading. See MUX[1:0] settings in CONFIG register. ADC Readings Registers: 00 = ADC1–ADC4 contain current readings of each output ADC1–ADC4 readings contain the output current through OUT1–OUT4, respectively. The current can be calculated as: IOUT1–IOUT4 = ADC1–ADC4 x 6mA 01 = ADC1–ADC4 contain output-voltage readings of each output ADC1–ADC4 readings contain the voltage at the output of the switches of OUT1–OUT4, respectively. The output voltage can be calculated as: VOUT1–VOUT4 = ADC1–ADC4 x 70mV 10 = ADC1–ADC3 contain VIN, VDD, VISET ADC1–ADC4 contain the following voltage readings: ADC1 = VIN (70mV/count) ADC2 = VDD (24.78mV/count) ADC3 = VISET (5mV/count) ADC4 = Unused

ADC4 (0x09)

Bit	Type	Bit Name	Default	Description
7:0	R	DATA_ADC4[7:0]	0x00	ADC4 Reading. See MUX[1:0] settings in CONFIG register. ADC Readings Registers: 00 = ADC1–ADC4 contain current readings of each output ADC1–ADC4 readings contain the output current through OUT1–OUT4, respectively. The current can be calculated as: IOUT1–IOUT4 = ADC1–ADC4 x 6mA 01 = ADC1–ADC4 contain output-voltage readings of each output ADC1–ADC4 readings contain the voltage at the output of the switches of OUT1–OUT4, respectively. The output voltage can be calculated as: VOUT1–VOUT4 = ADC1–ADC4 x 70mV 10 = ADC1–ADC3 contain VIN, VDD, VISET ADC1–ADC4 contain the following voltage readings: ADC1 = VIN (70mV/count) ADC2 = VDD (24.78mV/count) ADC3 = VISET (5mV/count) ADC4 = Unused

MASK2 (0x0B)

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Bit	Type	Bit Name	Default	Description
7	R/W	TW4M	1b	Thermal Warning Mask OUT4: 0 = Thermal Warning faults UV4 mapped to INT pin 1 = Masks UV4 from INT
6	R/W	TW3M	1b	Thermal Warning Mask OUT3: 0 = Thermal Warning faults UV4 mapped to INT pin 1 = Masks UV3 from INT
5	R/W	TW2M	1b	Thermal Warning Mask OUT2: 0 = Thermal Warning faults UV4 mapped to INT pin 1 = Masks UV2 from INT
4	R/W	TW1M	1b	Thermal Warning Mask OUT1: 0 = Thermal Warning faults UV4 mapped to INT pin 1 = Masks UV1 from INT
3	R	Reserved	0b	Reserved
2	R	Reserved	0b	Reserved
1	R/W	ABIST_ERR_Mask	0b	ABIST_ERR_Mask: 0 = ABIST_ERR mapped to INT pin 1 = Masks ABIST_ERR from INT
0	R/W	IIC_CRC_ERR_MASK	0b	IIC CRC Error Mask: 0 = IIC CRC faults mapped to INT pin 1 = Masks IIC CRC faults from INT

START_SLEW (0x1A)

Bit	Type	Bit Name	Default	Description
7:6	R/W	SS_RAMP4[1:0]	0b	Soft-start current ramp rate OUT4 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms
5:4	R/W	SS_RAMP3[1:0]	0b	Soft-start current ramp rate OUT3 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms
3:2	R/W	SS_RAMP2[1:0]	0b	Soft-start current ramp rate OUT2 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms
1:0	R/W	SS_RAMP1[1:0]	0b	Soft-start current ramp rate OUT1 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms

SHDN_SLEW (0x1B)

Bit	Type	Bit Name	Default	Description
7:6	R/W	SSD_RAMP4[1:0]	0b	Soft-shutdown current ramp rate OUT4 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms
5:4	R/W	SSD_RAMP3[1:0]	0b	Soft-shutdown current ramp rate OUT3 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms
3:2	R/W	SSD_RAMP2[1:0]	0b	Soft-shutdown current ramp rate OUT2 0x00: 0.5ms 0x01: 1ms 0x10: 2ms 0x11: 4ms
1:0	R/W	SSD_RAMP1[1:0]	0b	Soft-shutdown current ramp rate OUT1 0x00: 0.5ms 0x01: 1ms

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				0x10: 2ms 0x11: 4ms

STAT4 (0x27)

Bit	Type	Bit Name	Default	Description
7	R1C	TW4	0b	Thermal Warning on OUT4: 0 = No fault 1 = Thermal warning occurred on OUT4
6	R1C	TW3	0b	Thermal Warning on OUT3: 0 = No fault 1 = Thermal warning occurred on OUT3
5	R1C	TW2	0b	Thermal Warning on OUT2: 0 = No fault 1 = Thermal warning occurred on OUT2
4	R1C	TW1	0b	Thermal Warning on OUT1: 0 = No fault 1 = Thermal warning occurred on OUT1
3	R	Reserved	0b	Reserved
2	R	Reserved	0b	Reserved
1	R	Reserved	0b	Reserved
0	R	Reserved	0b	Reserved

STAT5 (0x28)

Bit	Type	Bit Name	Default	Description
7	R	BG_OV	0b	Bandgap OV Error Flag for Internal Bandgap OV Overvoltage on Internal Bandgap: 0 = Bandgap voltage < OV threshold 1 = Bandgap voltage > OV threshold
6	R	BG_UV	0b	Bandgap UV Error Flag for Internal Bandgap UV Overvoltage on Internal Bandgap: 0 = Bandgap voltage > UV threshold 1 = Bandgap voltage < UV threshold
5	R	INT_REG_OV	0b	Internal Regulator OV Error Flag for Internal Regulator OV Overvoltage on Internal Regulator: 0 = Regulator voltage < OV threshold 1 = Regulator voltage > OV threshold
4	R	INT_REG_UV	0b	Internal Regulator UV Error Flag for Internal Regulator UV Overvoltage on Internal Regulator: 0 = Regulator voltage > UV threshold 1 = Regulator voltage < UV threshold
3	R	Reserved	0b	Reserved
2	R	Reserved	0b	Reserved
1	R	Reserved	0b	Reserved
0	R	OTP_CRC_DET	0b	OTP Error Detected 0x0: no error detected 0x1: OTP storage error detected

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13 Configuration Table

Table14-1 OTP Description

OTP Items	Description	Value
START_SLEW	Soft-start current ramp rate	00b: 0.5ms(default) 01b: 1ms 10b: 2ms 11b: 4ms
SHDN_SLEW	Soft-shutdown current ramp rate	00b: 0.25ms(default) 01b: 0.5ms 10b: 1ms 11b: 2ms
I2C_ADDRESS	Configures the I2C address	0: ADDR=0, address = 0x28, ADDR=1, address=0x29 1: ADDR=0, address = 0x2A, ADDR=1, address=0x2B 2: ADDR=0, address = 0x2C, ADDR=1, address=0x2D 3: ADDR=0, address = 0x2E, ADDR=1, address=0x2F

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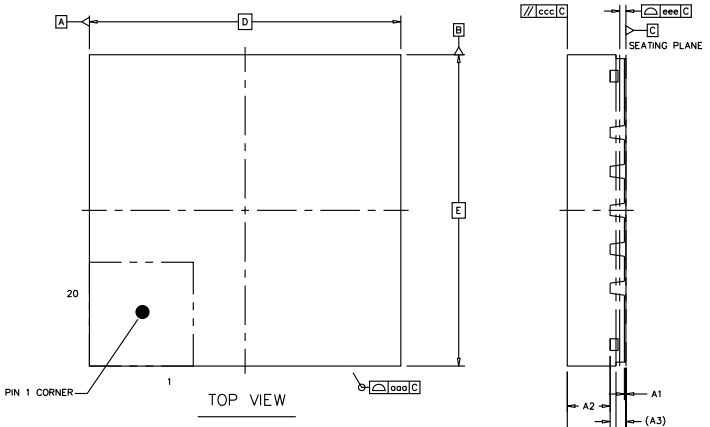
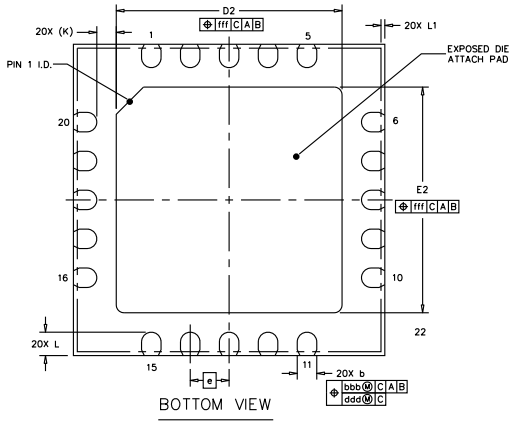
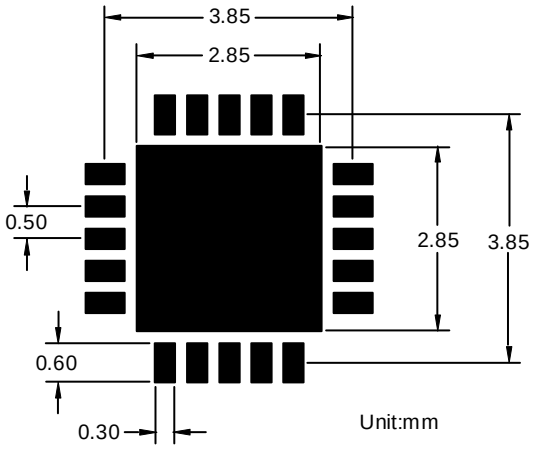
MCHANICAL DATA



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	2.8	2.9	3
	Y	E2	2.8	2.9	3
LEAD LENGTH		L	0.2	0.3	0.4
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	



Unit:mm



Land Pattern

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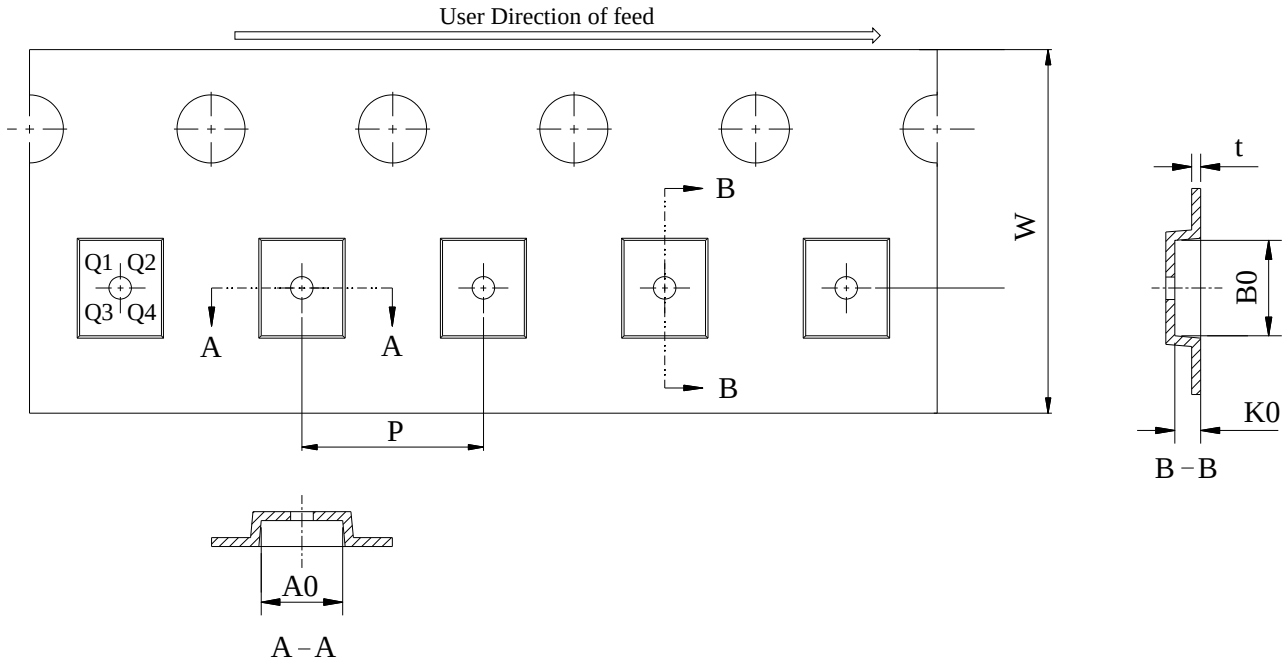
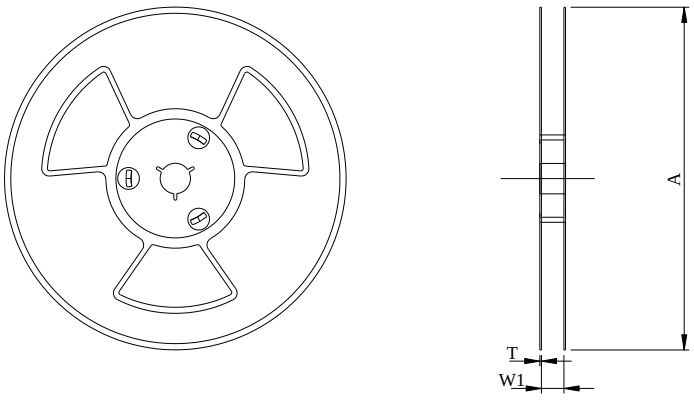
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 ±0.30	8.00±0.10	4.30±0.10	4.30±0.10	1.10±0.10	0.25±0.02	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	12.4 +1/-0	2. 6+1/-0

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