



SC81530Q 36V/3A, Buck Converter with USB Charging Port Supporting CDP and Type-C DFP Mode, AEC-Q100 Qualified

1 Descriptions

SC81530Q is a USB Type-C and BC1.2 charging port controller that includes a synchronous step-down converter. It integrates a single USB current-limit switch and achieves 3A of output current across a wide input supply range, with excellent load and line regulation.

SC81530Q integrates current-limited USB switch, which supports CDP mode for BC1.2, USB Type-C DFP mode and Type-A mode(CC1=100kΩ). SC81530Q also integrates high bandwidth analog switches for DP and DM pass-through.

Fault condition protections include hiccup current limiting, output over-voltage protection (OVP), DP/DM/CC1/CC2 short-to-battery protection, and thermal shutdown.

The SC81530Q is available in 22-pin 4mm x 4mm Wettable packages.

2 Applications

- Automotive USB Type-C Charging Ports
- Automotive Charging Downstream Ports
- Automotive Head Unit

3 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature Grade 1: T_A range: -40°C to 125 °C
- Passes Apple MFI certification test
- USB-IF Type-C certificated
- Integrates synchronous Buck converter:
 - Wide 3.9V to 36V continuous operating input range, 40V ABS voltage
 - Adjustable switching frequency from 200kHz to 2.2MHz
 - Spread Spectrum option
 - Synchronize to external clock
 - Integrates 52.5mΩ/30.5mΩ switching power FETs
 - Selectable Forced PWM Operation and Automatic PFM/FPWM operation
- Integrates multiple protocols:
 - Supports BC1.2 CDP mode
 - Supports USB Type-C DFP mode
 - Integrates 1000MHz bandwidth USB2.0 data switch with OVP
 - Accurate USB switch current limit for Type C & Type A
 - Integrates 23mΩ RDS(ON) USB switch
 - 145°C Internal Load-Shedding entry temperature
- Line drop compensation
- Independent USB on/off control
- Hiccup current limit for Buck and USB switch
- USB_OUT, DP/DM, CC1/CC2 Pins short to battery protection
- EN shutdown discharge function
- Fault indication for USB OCP, OVP(USB_IN), OTP, USB_OUT/DP/DM/CC1/CC2 short to battery,
- ±8kV IEC 61000-4-2 contact discharge ESD rating for CC1/CC2/DP/DM pins
- ±15kV IEC 61000-4-2 air discharge ESD rating for CC1/CC2/DP/DM pin



4 Device Information

ORDER NUMBER	VERSION	MODE IN LIGHT LOAD	FUNCTION OF PIN2	PACKAGE
SC81530QQFLR	CDP	Auto PFM	FLT	4mm x 4mm x 0.9mm
SC81530AQQFLR	CDP	Forced PWM	FLT	4mm x 4mm x 0.9mm
SC81533QQFLR*	CDP	Auto PFM	POL	4mm x 4mm x 0.9mm

*Notes: POL means Type-C plug polarity indicator. Contact Southchip for more information.

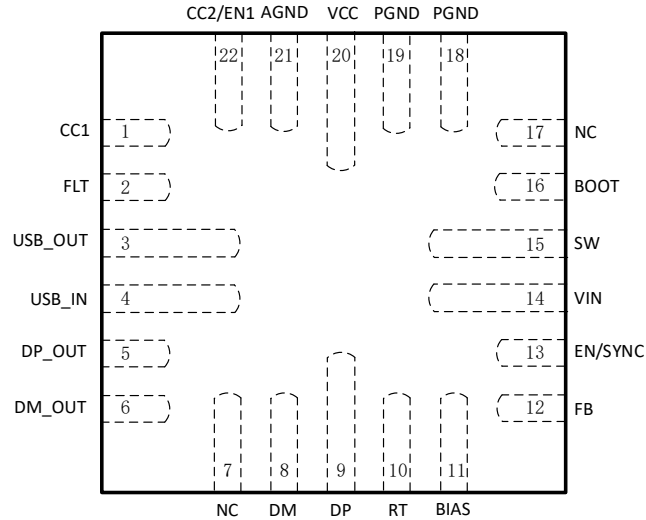
5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.0.5	2025/12	Page3 Page31	The recommended value for the CC capacitor has been changed from 220nF to 2.2nF
V1.0.4	2025/4	Page6	Revise certain descriptions
V1.0.3	2024/11	Page26	Revise certain descriptions
V1.0.2	2024/1	Page6	Add the application description





7 Terminal Configuration and Functions



Terminal		I/O	DESCRIPTION
NUMBER	NAME		
1	CC1	O	Type-C configure channel 1. It also supports VCONN output.
2	FLT	O	This pin indicates USB switch OCP, USB_IN/V _{OUT} OVP, DP/DM/CC1/CC2 short to battery, and thermal shutdown. FLT is an open drain under normal conditions. FLT is pulled low during any of aforementioned fault conditions.
3	USB_OUT	O	USB bus voltage output.
4	USB_IN	I	USB bus voltage input.
5	DP_OUT	O	DP data line. Connect to USB host controller.
6	DM_OUT	O	DM data line. Connect to USB host controller.
7	NC	-	This pin could be left floating or connected to FB pin.
8	DM	I	DM is the input/output used to handshake with portable devices.
9	DP	I	DP is the input/output used to handshake with portable devices.
10	RT	I	Connect this pin to ground through a resistor to set switching frequency between 200 kHz and 2200 kHz.
11	BIAS	O	Internal power supply pin.
12	FB	I	Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
13	EN/SYNC	I	Apply an external CLK on this pin to sync the switching frequency to the external clock.
14	VIN	I	Input power supply for the IC.
15	SW	O	Switching node pin of the buck side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
16	BOOT	O	Connect a 100nF capacitor between BOOT and SW to provide bias voltage for MOSFET drive on Buck controller.
17	NC	-	Can be floating or connected to USB_IN pin.



18, 19	PGND	-	Power Ground.
20	VCC	O	Internal 5V LDO regulator output. Decouple with a 4.7 μ F capacitor.
21	AGND	-	Analog Ground.
22	CC2	O	Type-C configure channel 2. It also supports VCONN output.
	EN1	I	When CC1 is connected to ground via a 100k Ω resistor, the SC81530Q works in Type-A mode. In Type-A mode, this pin functions as EN1. Pull EN1 high to enable the USB switch. Float EN1 or pull it low to disable the USB switch. Apply a middle-level voltage (0.9 to 1.5V) to EN1 to force the chip to enter client mode.



8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C ~ 150°C (unless otherwise noted). ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VIN, EN/SYNC, SW	-0.3	40	V
	BOOT	-0.3	45.5	V
	USB_IN, USB_OUT	-0.3	24	V
	CC1, CC2, DP, DM, BIAS	-0.3	18	V
	Others	-0.3	5.5	V
Power supply transient voltage ramp	VIN		2	V/μs
T _J	IC operating junction temperature range	-40	150	°C
T _{stg}	IC storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Thermal Information

THERMAL RESISTANCE		QFN-22 (4mm x4mm)	UNIT
Θ _{JA}	Junction to ambient thermal resistance (SC81530QEVM) ⁽¹⁾	34	°C/W
Θ _{JA}	Junction to ambient thermal resistance (JESD 51-7) ⁽²⁾	45	°C/W
Θ _{JC(top)}	Junction to case (top) resistance ⁽²⁾	5	°C/W

(1) Measured on SC81530QEVM. 4-layer, 2-oz Cu per top and bottom layer and 1-oz Cu per inner layer, evaluation board.

(2) Measured on JE5D51-7, 4-layer PCB;

8.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human Body Model (HBM) ⁽²⁾	-2	2	kV
	Charged Device Model (CDM) ⁽³⁾	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

**8.4 Recommended Operating Conditions**

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	3.4		36	V
V_{USB_IN}	Output voltage range	3.3		20	V
L	Inductance	2.2	4.7	22	μ H
F_{SW}	Buck switching frequency range	200		2200	kHz
T_J	Operating junction temperature	-40		150	$^{\circ}$ C
T_A	Operating ambient temperature range	-40		125	$^{\circ}$ C



8.5 Electrical Characteristic

$T_J = -40^{\circ}\text{C}$ to 150°C , $V_{IN} = 12\text{V}$ and $V_{EN} = 5\text{V}$. Typical value is tested at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{IN}	Input voltage range		3.4		36	V
V _{IN_UVLO}	V _{IN} rising threshold		3.7	3.9		V
	V _{IN} falling threshold		3.3	3.5		V
I _Q	Overall quiescent current	CC1 connected to ground with a 5.1kΩ resistor, V _{FB} pull high	820	950		μA
I _{SD}	Shutdown current into the V _{IN} pin	IC disabled, V _{EN} =0V		18		μA
V _{CC}	V _{CC} regulator voltage		4.8	5	5.2	V
V _{CC_LIM}	Internal LDO limit		70			mA
EN/SYNC						
V _{EN_H}	EN input level to start switching	Rising threshold	1.21	1.28	1.35	V
V _{EN_L}	EN input level to stop switching	Falling threshold	0.94	1	1.06	V
t _B	Blanking of EN after rising or falling edges		50			μs
t _{SYNC_EDGE}	Enable sync signal hold time after edge for edge recognition		120			ns
V _{EN_SYNC}	Edge height necessary to sync using EN/SYNC pin		4.5			V
POWER MOSFET						
R _{DS(ON)_HS}	High side switch on resistance		52	90		mΩ
R _{DS(ON)_LS}	Low side switch on resistance		31	55		mΩ
V _{BOOT_UVLO}	Voltage on BOOT pin compared to SW which will turn off high-side switch		2.4			V
OUTPUT DISCHARGE						
I _{DIS_OVP}	Output discharge current when V _{OUT} OVP happened		0.3	0.4	0.7	mA
REFERENCE VOLTAGE						
V _{FB}	Feedback voltage	V _{OUT} =5.15V	794	806	818	mV
OSCILATOR						
f _{ADJ}	Minimum adjustable frequency by RT or SYNC	RT = 66.5 kΩ	0.18	0.2	0.22	MHz
	Adjustable frequency by RT or SYNC	RT = 32.4 kΩ	0.36	0.4	0.44	MHz
	Maximum adjustable frequency by RT or SYNC	RT = 5.2 kΩ	1.98	2.2	2.42	MHz
f _{Mod}	Spread Spectrum Modulation Frequency		1/256			F _{SW}
f _{SS}	Frequency spread spectrum span		6			%
TIMING						
t _{ON_MAX}	Maximum HS switch on time		8			μs



t_{ON_MIN}	Minimum HS switch on time		150	ns
t_{OFF_MIN}	Minimum LS switch on time		150	ns
t_{SS}	Soft-start time	Output from 10% to 90%, $V_{OUT}=5.15V$	2.9	ms
HICCUP				
V_{HICCUP}	Hiccup Voltage Threshold		40	%
t_{HIC_ON}	On time of hiccup mode		38	ms
t_{HIC_OFF}	Off time of hiccup mode		460	ms
CURRENT LIMIT				
I_{PEAK}	High-side peak current limit		6.4 7.7 9	A
I_{VALLEY}	Low-side valley current limit		4.2 5.6 6.7	A
I_{LSNEG}	Low-side negative current limit		-3	A
OVP Protection				
V_{OVP1}	Output OVP		117 120 123	%
V_{OVP1_R}	Output OVP recovery		107 110 113	%
t_{FAULT_OVP}	OVP deglitch to assert fault pin		1	ms
$t_{FAULT_OVP_Recovery1}$	OVP deglitch to de-assert fault pin		1	ms
USB SWITCH				
V_{USB_UVR}	Under-voltage lockout rising threshold		4.3 4.5	V
V_{USB_UVHYS}	Under-voltage lockout threshold hysteresis		150	mV
V_{EN1_H}	EN1 logic high input	Turn on the USB switch	2	V
V_{EN1_M}	Enter client mode		0.9 1.5	V
V_{EN1_L}	EN1 logic low input	Turn off the USB switch	0.4	V
$R_{DS(ON)_SW}$	Switch on resistance		23 46	m Ω
$R_{DIS_USB_IN}$	Input discharge resistance	$V_{OUT}=12V$	550	Ω
		$V_{OUT}=5.15V$	230	Ω
I_{LIMIT}	USB Switch current limit	Type-C mode	3.1 3.55 3.9	A
	USB Switch current limit	Type-A Mode	2.4 2.85 3.3	A
t_{HICP_DEG}	Deglitch time before hiccup mode		2	ms
t_{HICP_ON}	V_{BUS} enter hiccup hold time		2	ms
t_{HICP_OFF}	Hiccup mode off time		2	S
t_{USB_SS}	USB_OUT soft-start time	$V_{BUS}=5.15V$, from 10% to 90%	0.4	ms
t_{FLT_DEG}	Fault deglitch time		2	ms
$V_{OV_DM_DP}$	DM, DP pins OVP rising		3.8 4 4.2	V
$V_{OV_DM_DP_HYS}$	DM, DP pins OVP rising hysteresis		200	mV
G_{ADJ_SINK}	Line drop compensation gain		2	$\mu A/A$
V_{FLT_L}	FLT output low voltage		0.05	V



CDP MODE						
V _{DM_SRC}	DM CDP output voltage	V _{DP} = 0.6V, DM_Sink = 0μA	0.6	0.65	0.7	V
		V _{DP} = 0.6V, DM to GND = 22.5Ω	20			mV
V _{DAT_REF}	DP rising lower window threshold for V _{DM_SRC}		0.3	0.35	0.4	V
V _{LGC_SRC}	DP rising upper window threshold for V _{DM_SRC}		0.85	0.9	0.95	V
t _{DM_SRC_DEGH}	V _{DM_SRC} on/off deglitch time		10			ms
R _{ON_DP/DM}	DP/DM on resistance	V _{DP_OUT} = 0V	4			Ω
		V _{DP_OUT} = 2.4V	5.1			Ω
R _{ON_MAT}	DP/DM on resistance matching		10		60	mΩ
C _{DP}	DP to DP_OUT capacitance		10			pF
f _{BW}	3dB bandwidth of analog data switch		1000			MHz
USB TYPE-C 5V @ 3A MODE – CC1, CC2						
R _A	CC resistor to disable Type-C mode		100			kΩ
I _{PLL}	CC pull-up current to detect Type-A mode		10			μA
R _{p_80uA}	CC Rp pull up 80μA capability		80			μA
R _{p_180uA}	CC Rp pull up 180μA capability		180			μA
R _{p_330uA}	CC Rp pull up 330μA capability		330			μA
V _{CC_RD}	CC voltage with 5.1kΩ R _D	CC pin connected to 5.1kΩ pull-down resistor	1.3	1.68	2.0	V
V _{OPEN}	CC detach threshold		2.7			V
t _{CC_DEBOUNCE}	CC voltage falling debounce timer		150			ms
t _{PD_DEBOUNCE}	CC voltage rising debounce timer		10			ms
I _{VCONN_OCP}	VCONN over current threshold		39			mA
V _{CCOVP_TH}	CC OVP rising threshold		5.7	6	6.3	V
V _{CCOVP_HYST}	CC OVP hysteresis		0.26			V
THERMAL SHUTDOWN ⁽¹⁾						
T _{SD}	Thermal shutdown threshold		165			°C
T _{SD_HYS}	Thermal shutdown hysteresis		20			°C

(1) Guarantee by Design



8.6 Typical Characteristics

$V_{IN}=13.5V$, $V_{BUS}=5.15V$, $L=4.7\mu H$, $F_{SW}=400kHz$, mode=PFM with spread spectrum, CC1 connected to ground with a $5.1k\Omega$ resistor, $C_{OUT}=100\mu F/35V$, $T_A=25^\circ C$, unless otherwise noted.

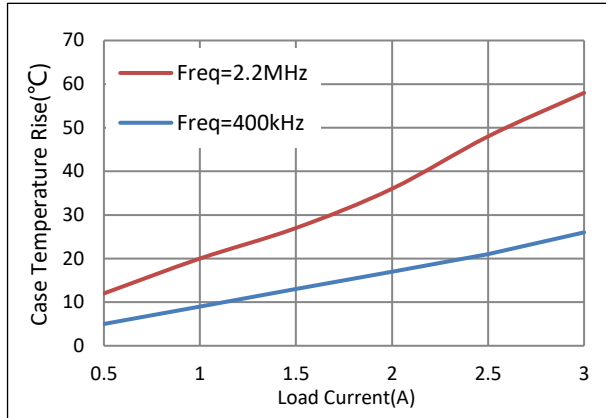


Figure 8-1. Case Temperature Rise

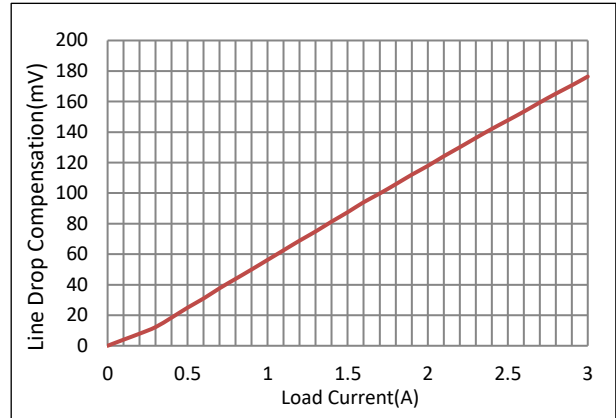


Figure 8-2. Line Drop Compensation

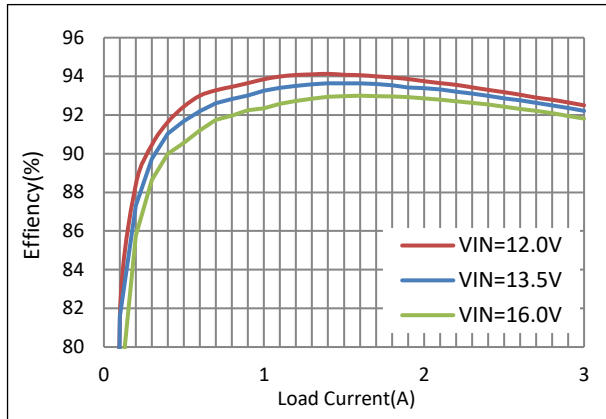


Figure 8-3. Efficiency, PFM, $F_{SW}=400kHz$, measured on USB_OUT, $C_{OUT}=4*22\mu F$ DCR=15mR

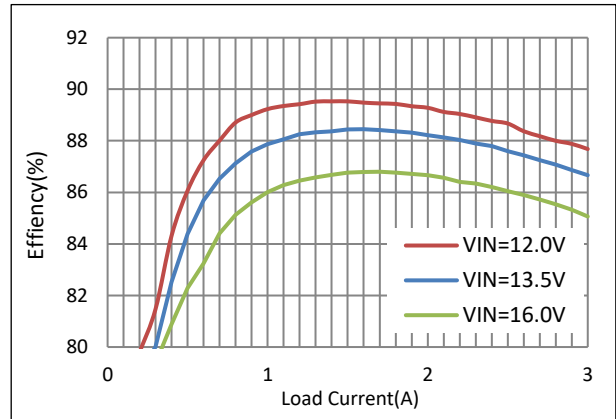


Figure 8-4. Efficiency, PFM, $F_{SW}=2.2MHz$, measured on USB_OUT, $C_{OUT}=2*22\mu F$ DCR=6mR

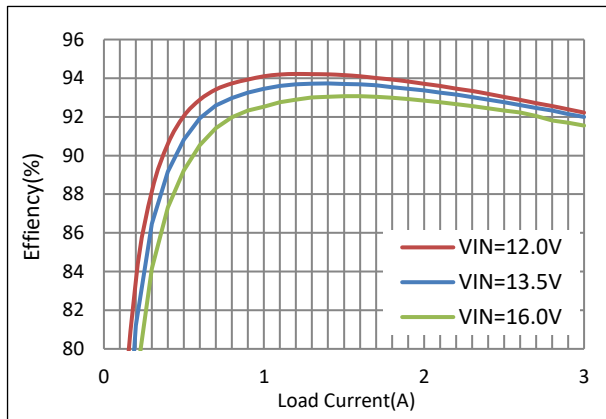


Figure 8-5. Efficiency, FPWM, $F_{SW}=400kHz$, measured on USB_OUT, $C_{OUT}=4*22\mu F$ DCR=15mR

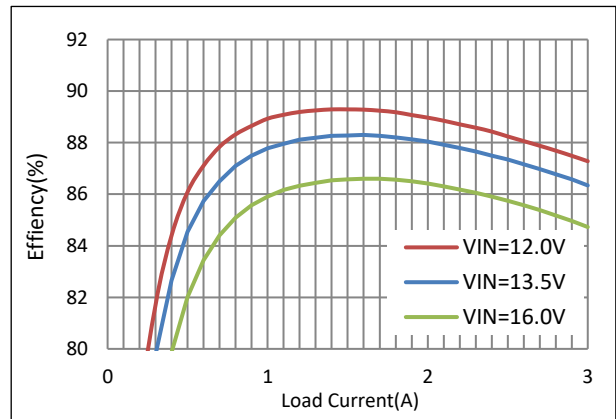


Figure 8-6. Efficiency, FPWM, $F_{SW}=2.2MHz$, measured on USB_OUT, $C_{OUT}=2*22\mu F$ DCR=6mR

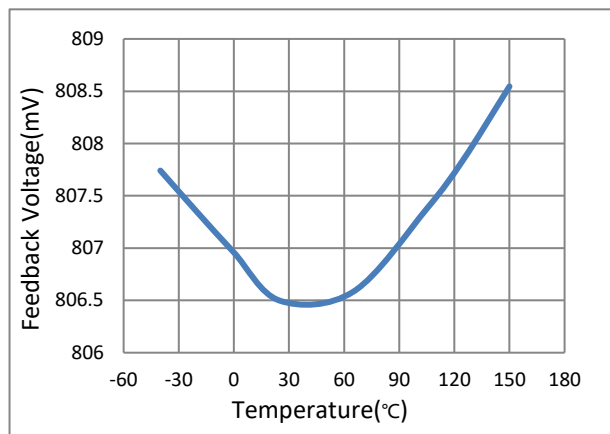


Figure 8-7. Feedback Voltage

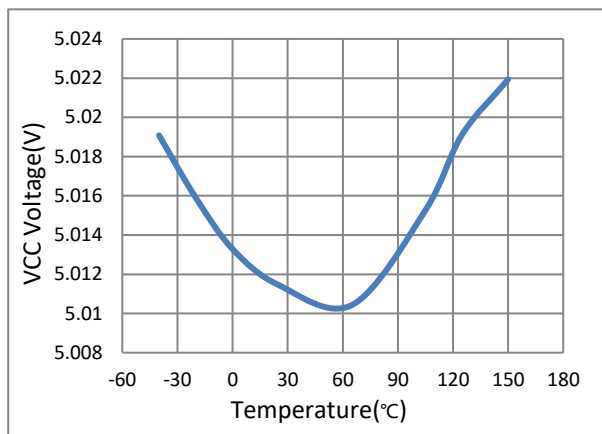


Figure 8-8. VCC Voltage

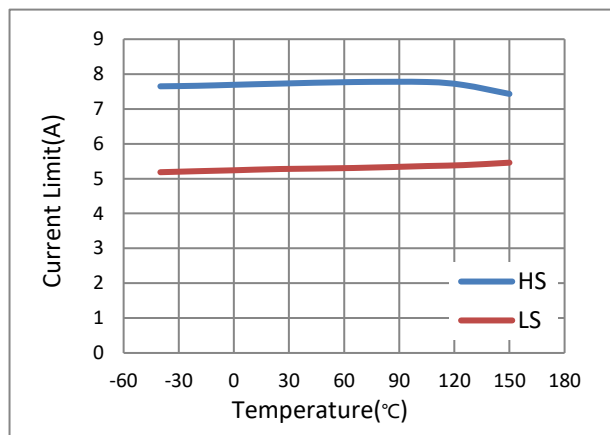


Figure 8-9. High-side and Low-side Current Limits

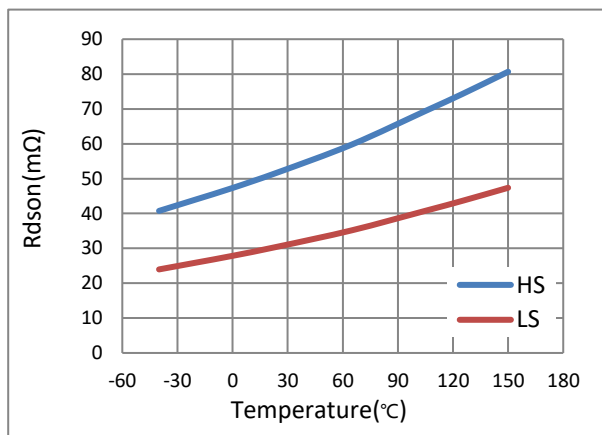


Figure 8-10. High-side and Low-side on resistor

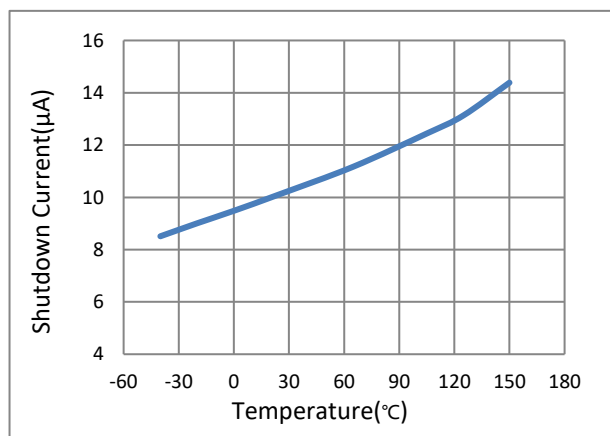


Figure 8-11. Shutdown Current

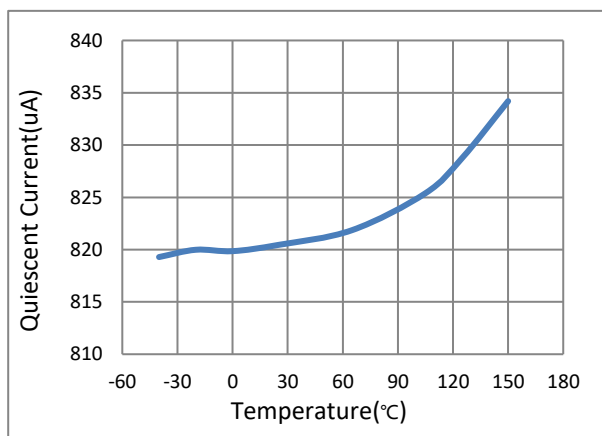


Figure 8-12. Non-Switching Input Supply Current

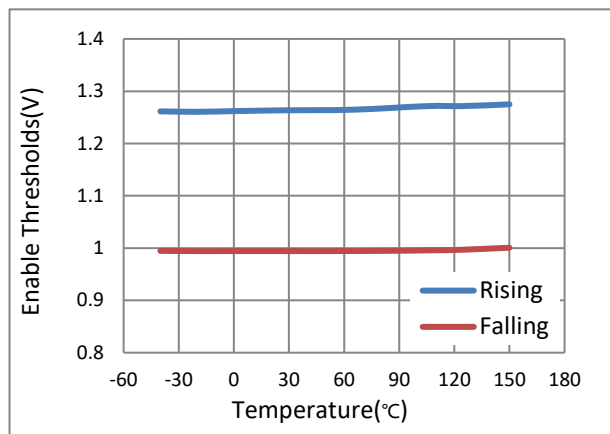


Figure 8-13. Enable Thresholds

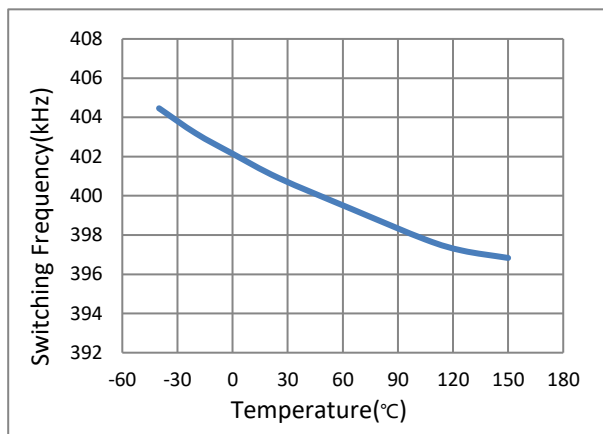


Figure 8-14. Switching Frequency

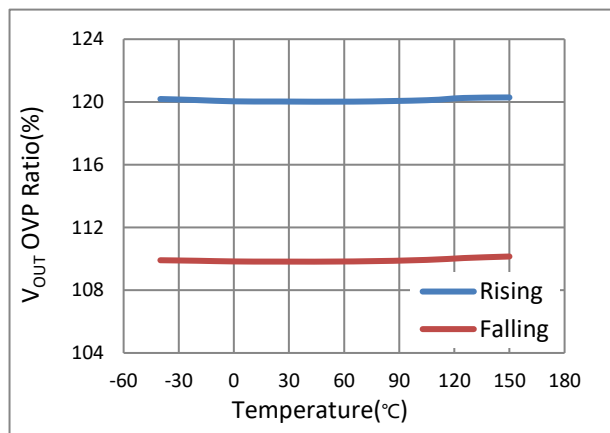


Figure 8-15. Output Over Voltage Protection Ratio

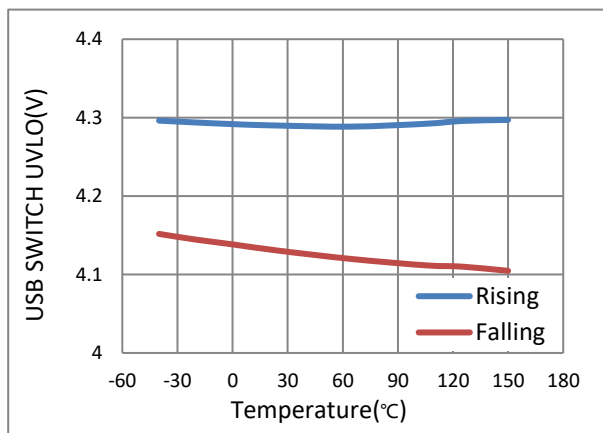


Figure 8-16. USB_SWITCH UVLO

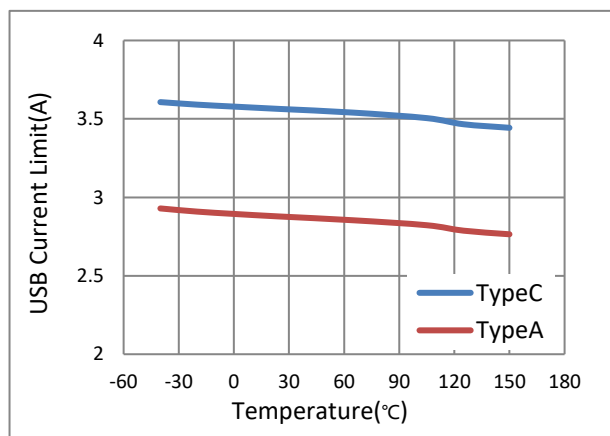


Figure 8-17. USB_SWITCH Current Limit

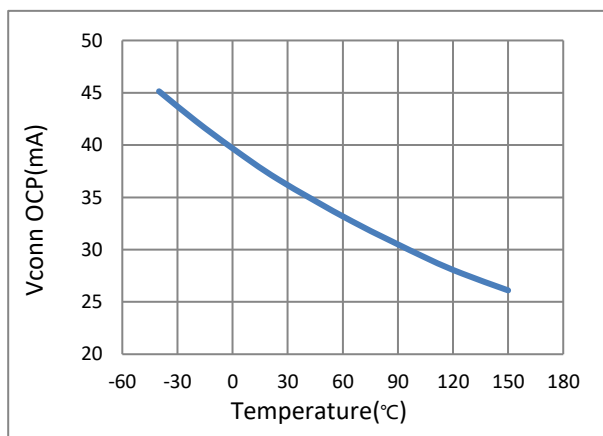


Figure 8-18. Vconn Over Current Protection

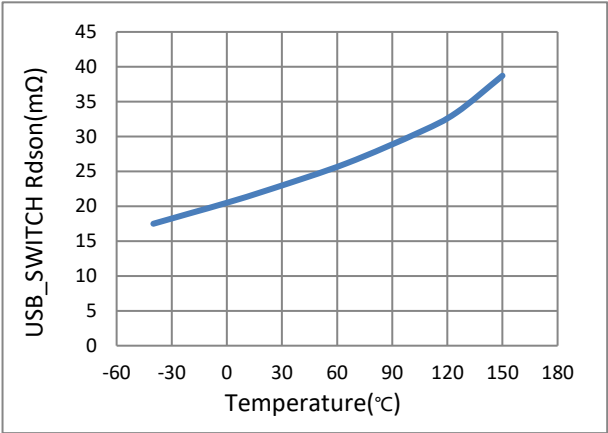


Figure 8-19. USB_SWITCH On Resistor



8.7 Typical Performance Characteristics

$V_{IN}=13.5V$, $V_{BUS}=5.15V$, $L=4.7\mu H$, $F_{SW}=400kHz$, mode=PFM with spread spectrum, CC1 connected to ground with a 5.1k Ω resistor, $C_{OUT}=100\mu F/35V$, $T_A=25^\circ C$, unless otherwise noted.

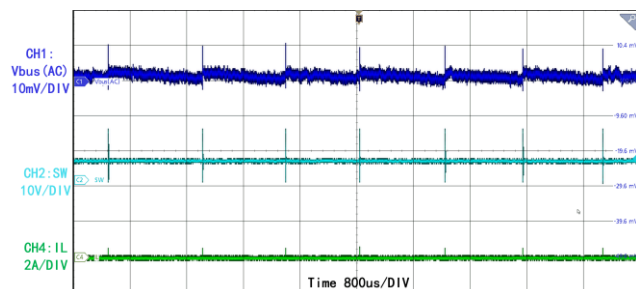


Figure 8-20. Steady State $I_{OUT} = 0A$

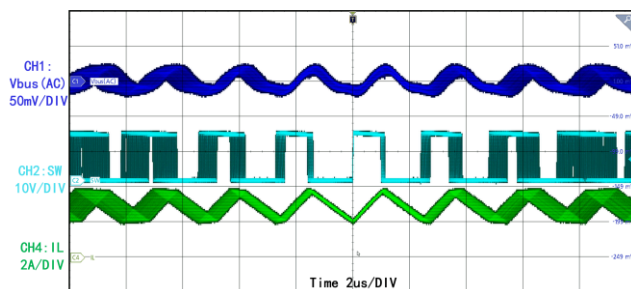


Figure 8-21. Steady State $I_{OUT} = 3A$

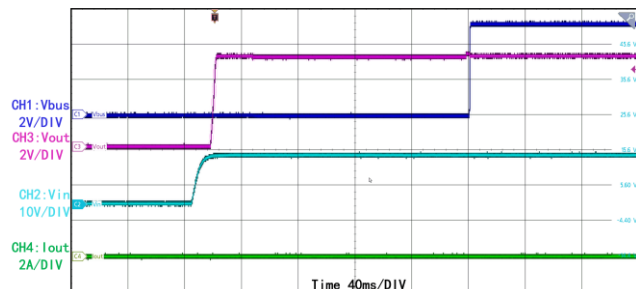


Figure 8-22. Start up through V_{IN} ; $I_{OUT} = 0A$

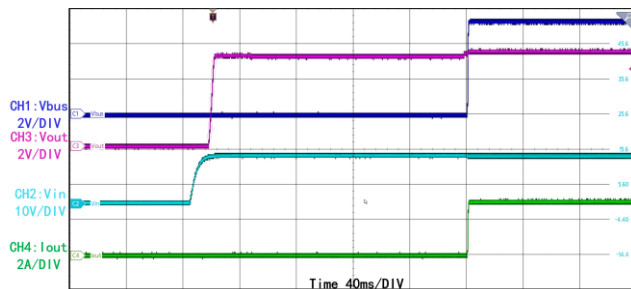


Figure 8-23. Start up through V_{IN} ; $I_{OUT} = 3A$

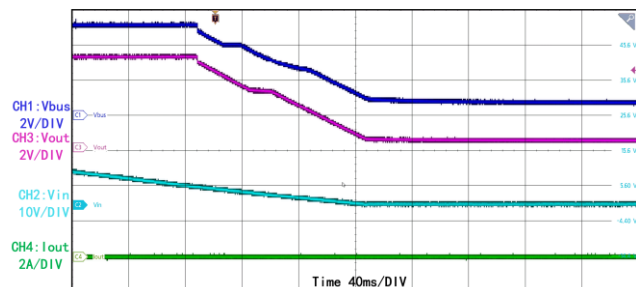


Figure 8-24. Shut down through V_{IN} ; $I_{OUT} = 0A$

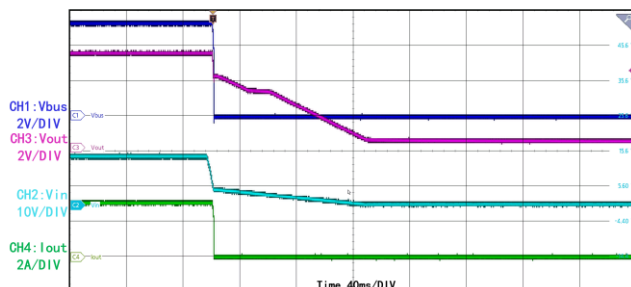


Figure 8-25. Shut down through V_{IN} ; $I_{OUT} = 3A$



$V_{IN}=13.5V$, $V_{BUS}=5.15V$, $L=4.7\mu H$, $F_{SW}=400kHz$, mode=PFM with spread spectrum, CC1 connected to ground with a 5.1k Ω resistor, $C_{OUT}=100\mu F/35V$, $T_A=25^\circ C$, unless otherwise noted.

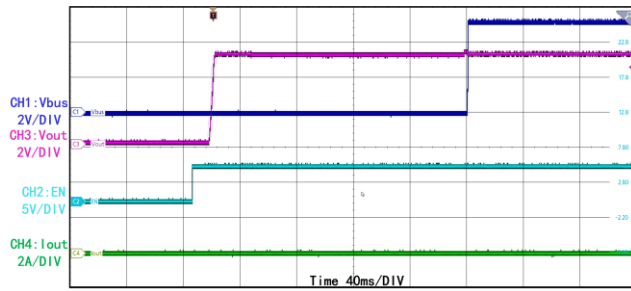


Figure 8-26. Start up through EN; $I_{OUT} = 0A$

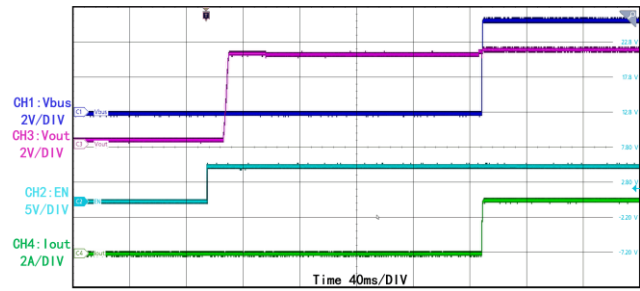


Figure 8-27. Start up through EN; $I_{OUT} = 3A$

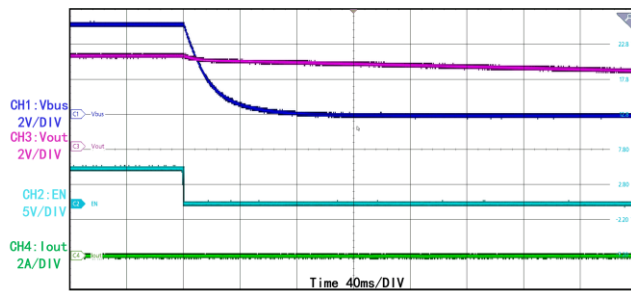


Figure 8-28. Shut down through EN; $I_{OUT} = 0A$

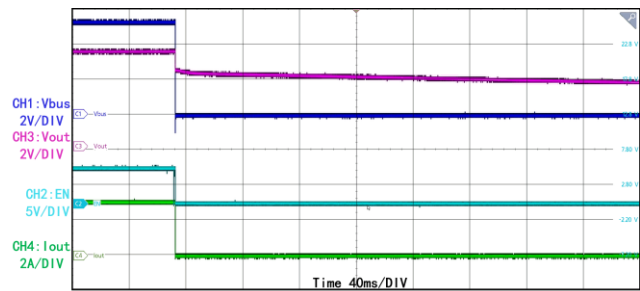


Figure 8-29. Shut down through EN; $I_{OUT} = 3A$

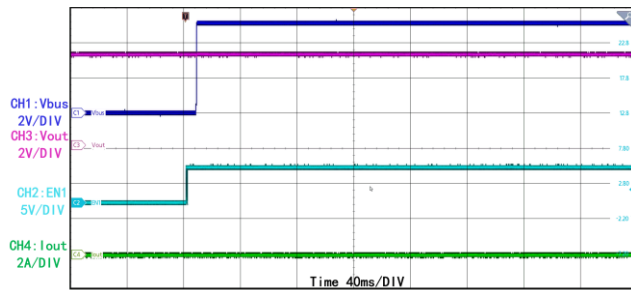


Figure 8-30. Start up through EN1; $I_{OUT} = 0A$; Type-A mode

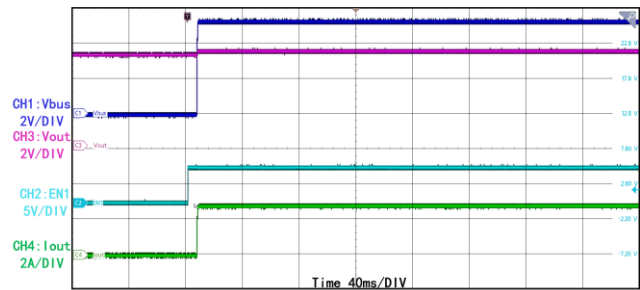


Figure 8-31. Start up through EN1; $I_{OUT} = 2.8A$; Type-A mode



$V_{IN}=13.5V$, $V_{BUS}=5.15V$, $L=4.7\mu H$, $F_{SW}=400kHz$, mode=PFM with spread spectrum, CC1 connected to ground with a 5.1k Ω resistor, $C_{OUT}=100\mu F/35V$, $T_A=25^\circ C$, unless otherwise noted.

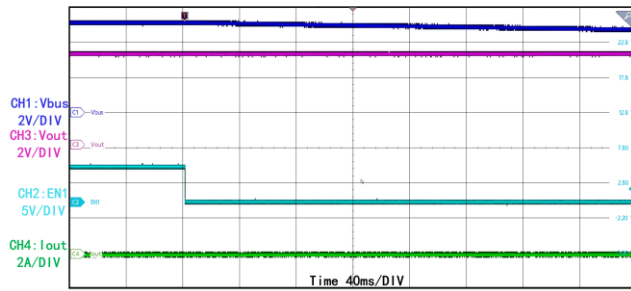


Figure 8-32. Shut down through EN1; $I_{OUT} = 0A$

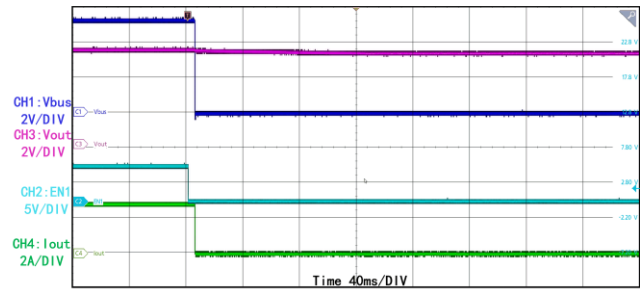


Figure 8-33. Shut down through EN1; $I_{OUT} = 2.8A$

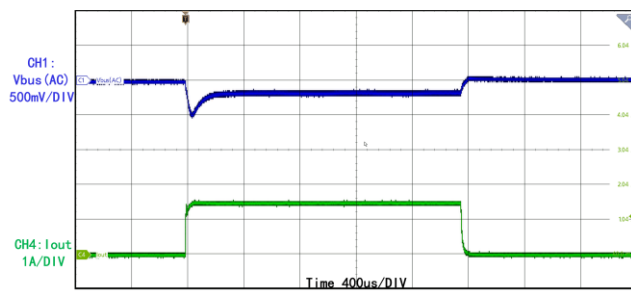


Figure 8-34. Load transient I_{OUT} : 0A->1.5A->0A

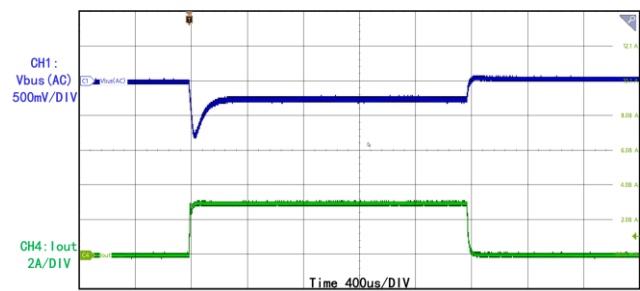


Figure 8-35. Load transient I_{OUT} : 0A->3A->0A

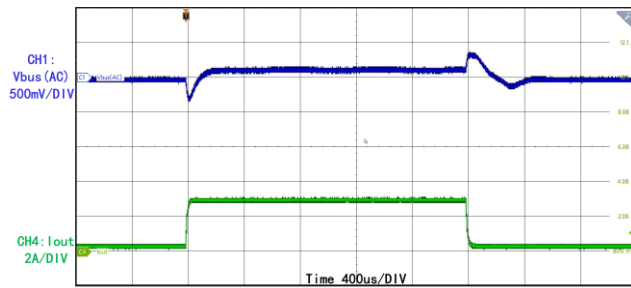


Figure 8-36. Load transient I_{OUT} : 0.3A->3A->0.3A

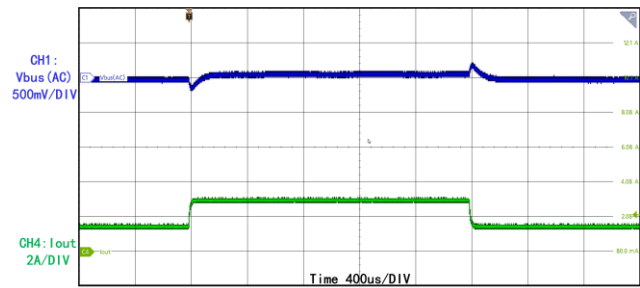


Figure 8-37. Load transient I_{OUT} : 1.5A->3A->1.5A



$V_{IN}=13.5V$, $V_{BUS}=5.15V$, $L=4.7\mu H$, $F_{SW}=400kHz$, mode=PFM with spread spectrum, CC1 connected to ground with a 5.1k Ω resistor, $C_{OUT}=100\mu F/35V$, $T_A=25^{\circ}C$, unless otherwise noted.

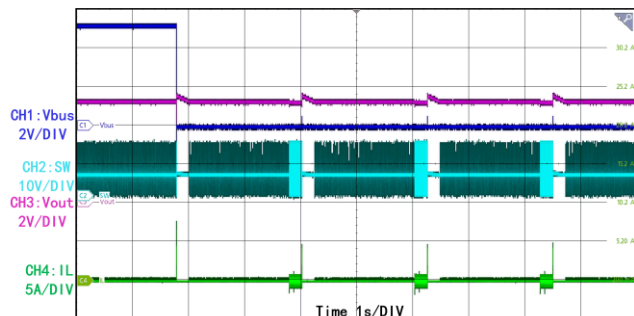


Figure 8-38. USB_OUT Short-to-GND Entry, $I_{out} = 0A \rightarrow$ Short

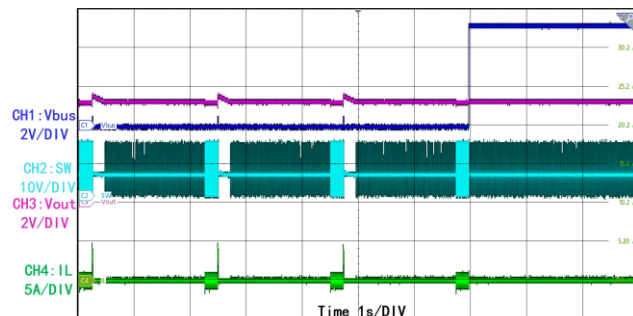


Figure 8-39. USB_OUT Short-to-GND Recovery, $I_{out} = \text{Short} \rightarrow 0A$

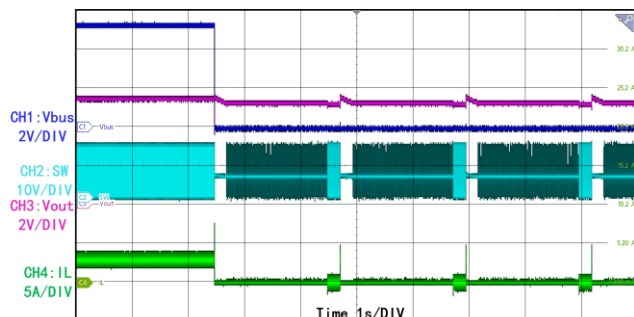


Figure 8-40. USB_OUT Short-to-GND Entry, $I_{out} = 3A \rightarrow$ Short

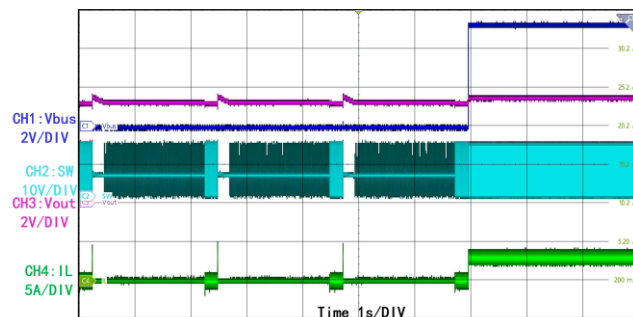


Figure 8-41. USB_OUT Short-to-GND Recovery, $I_{out} = \text{Short} \rightarrow 3A$

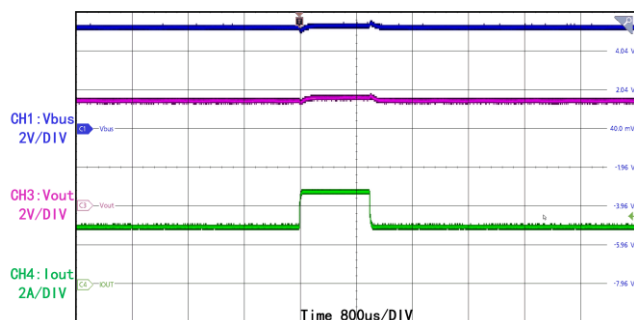


Figure 8-42. MFI Test Type-C mode, $I_{out} = 3A$ to 4.8A, 1ms hold time

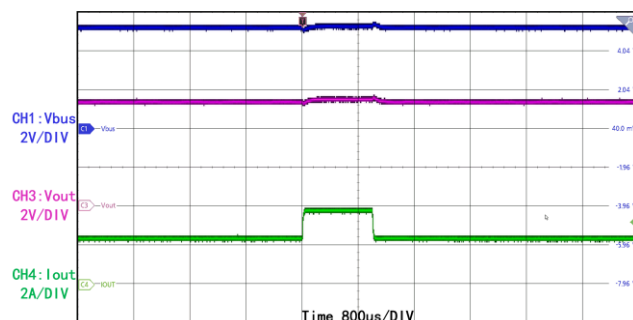


Figure 8-43. MFI Test Type-A mode, $I_{out} = 2.4A$ to 3.84A, 1ms hold time



$V_{IN}=13.5V$, $V_{BUS}=5.15V$, $L=4.7\mu H$, $F_{SW}=400kHz$, mode=PFM with spread spectrum, CC1 connected to ground with a $5.1k\Omega$ resistor, $C_{OUT}=100\mu F/35V$, $T_A=25^\circ C$, unless otherwise noted.

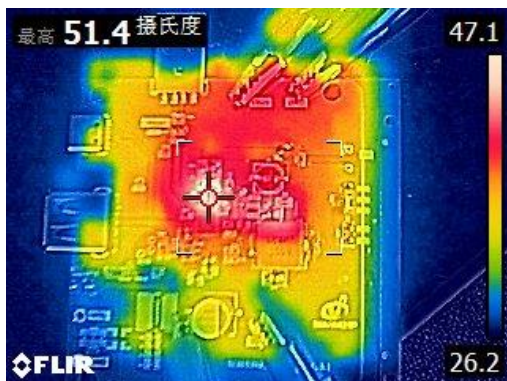


Figure 8-44. Thermal Test
 $I_{OUT}=3A$, measured on 4-layer PCB, Top/Bottom layer:
2oz, middle layers: 1oz

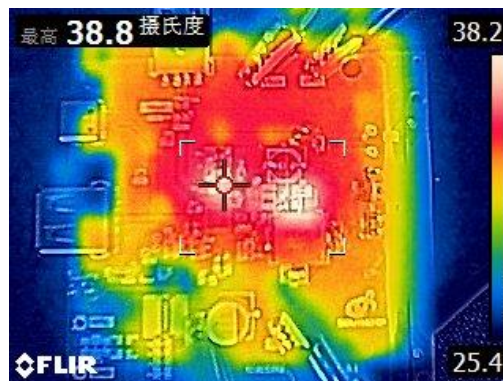


Figure 8-45. Thermal Test
 $I_{OUT}=1.5A$, measured on 4-layer PCB, Top/Bottom layer:
2oz, middle layers: 1oz

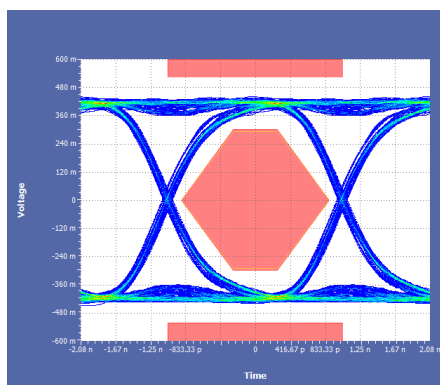


Figure 8-46. SC81530Q Eye diagram (Based on 18nH&1pF
DPDM filter and 10cm Cable)

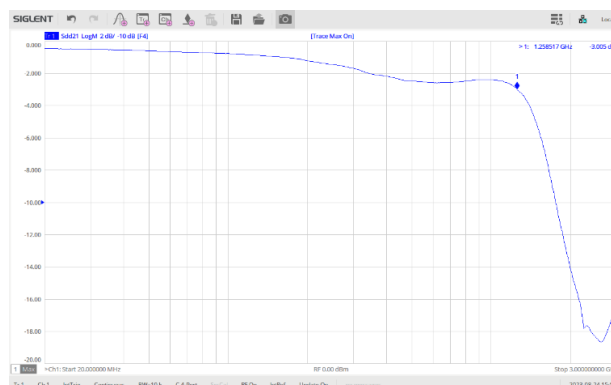


Figure 8-47. Bandwidth of Data Switch



9 Functional Block Diagram

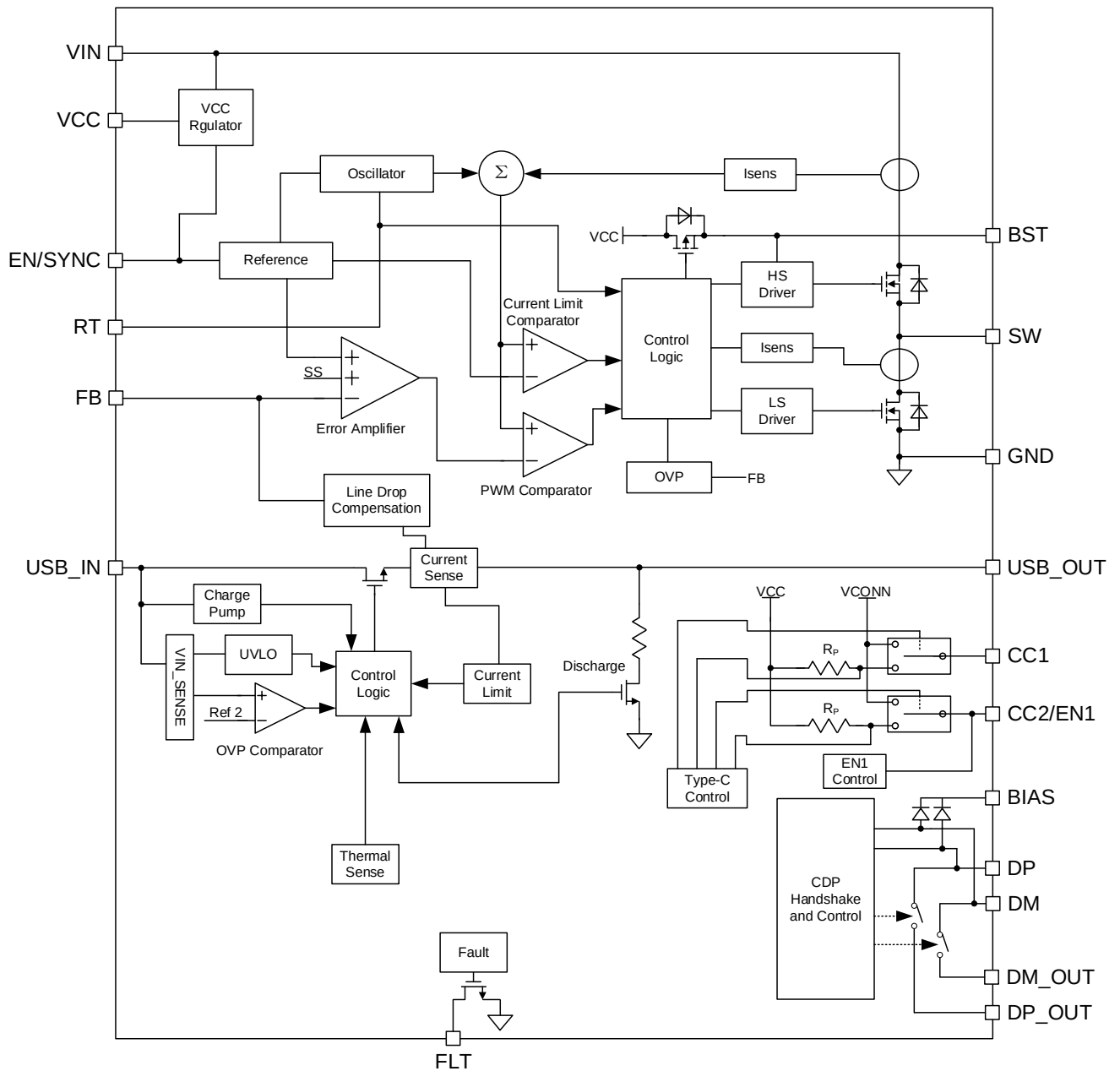


Figure 9-1. Function Block

10 Feature Description

10.1 Overview

SC81530Q is a synchronous buck converter with a USB_SWITCH current-limit switch and BC1.2 charging port controller integrates. It provides a compact solution to achieve 3A of continuous output current across a wide V_{IN} range. Implementing peak-current and valley-current mode, SC81530Q is able to provide excellent line and load transient performance.

SC81530Q could be configured at different frequency from 200kHz to 2.2MHz by RT pin resistor, as well as synchronize to external clock. It operates in Auto PFM in light condition to achieve higher efficiency. SC81530AQ is Forced PWM version, it can operate fixed frequency even in light load to get a small output ripple during all load range.

SC81530Q integrates spread spectrum feature to optimize the EMI performance. SC81530Q includes high bandwidth analog switches, short to battery protection on USB_OUT/DP/DM/CC1/CC2 pins.

10.2 Buck Converter

SC81530Q integrates a synchronous buck converter with high-side and low-side switches inside. It regulates the output voltage by adjusting the duty cycle of HS switch and LS switch. When the high-side switch is ON, the inductor current i_L increase with linear slope $(V_{IN} - V_{OUT}) / L$. The low-side switch is turned on after HS switch is turned off and dead time.

10.3 VCC Power Supply

The SC81530Q integrates an internal LDO to generate VCC for control circuitry and power stage's drivers. The nominal voltage for VCC is 5V. The LDO charges BOOT capacitor when low side MOSFET is ON. A high-quality ceramic capacitor with a value of 4.7 μ F, 10 V or higher rated voltage should be placed as close as possible to VCC and grounded to the AGND pin. When V_{IN} is higher than 6V, the internal LDO is fully regulated and the VCC voltage is 5V. When EN logic is low and VCC is lower than 4.3V, an additional discharge path will be open to discharge the output voltage of V_{BUS} .

10.4 Input Under Voltage Lockout

When the input voltage is above than 3.8V, the SC81530Q can be enabled by pulling EN pin to a high voltage above 1.3V, but the USB_SWITCH won't turn on until the V_{OUT} voltage is higher than 4.3V and a valid USB connection is monitored. After the DCDC starts switching, it won't turn off until the V_{IN} falls to 3.4V.

10.5 EN/SYNC for Enable and Precise Input UVLO

EN/SYNC pin is multiplexed to be either precise enable or external clock synchronization. When it is used as precise enable, start-up and shutdown sequence can be controlled by pulling this pin high or low. Furthermore, precise enable threshold can help build user programmable input UVLO.

The EN/SYNC pin must be properly terminated and cannot be floating. EN/SYNC can be directly connected to V_{IN} for self-start-up for the simplest design. As shown in **Figure 10-1**, in order to build power up sequence and use programmable input UVLO, resistor dividers can be used to set appropriate threshold on EN/SYNC pin. The EN/SYNC has 300mV (typ.) hysteresis to help build robust enable or disable function. The EN/SYNC pin can also connect to an external I/O pin for systematical power sequence management.

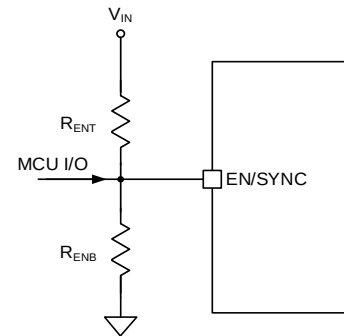


Figure 10-1. EN/SYNC Configuration for Precise Enable

$$R_{ENB} = R_{ENT} \cdot \frac{V_{EN_H}}{V_{IN_R} - V_{EN_H}} \quad (1)$$

$$V_{IN_HYS} = V_{EN_HYS} \cdot \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (2)$$

Equation (1) can be used to calculate resistor values and **Equation (2)** can be used to calculate hysteresis after resistors are selected. V_{IN_R} is the input rising voltage for start-up and V_{IN_HYS} is the hysteresis.

10.6 EN/SYNC for Synchronization

The EN/SYNC pin can be used to synchronize internal oscillator to an external clock. As shown in **Figure 10-2**, internal oscillator is synchronized to the positive clock edge through C_{SYNC} AC coupling. This will prevent external clock when it is in idle state from interfering input UVLO.

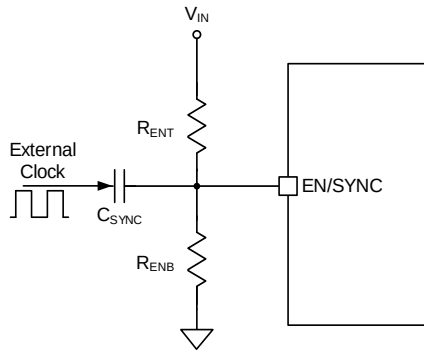


Figure 10-2. EN/SYNC Configuration for Clock Synchronization

The C_{SYNC} , R_{ENT} and R_{ENB} forms a high-pass filter in frequency domain seen from EN/SYNC pin. From demonstration of **Figure 10-3**, the cross-over frequency is determined by time constant τ , which is the product of C_{SYNC} and parallel resistance R_{ENT}/R_{ENB} . The cross-over frequency of the high-pass filter must be much lower than the external clock frequency. The recommended parallel resistance R_{ENT}/R_{ENB} is 100k Ω . The AC coupling capacitor, C_{SYNC} , can be 1nF.

The device's synchronization frequency range is 200kHz to 2.2MHz. When synchronizing external clock, it should be noted that the RT resistor needs to set free-run switching frequency equal or below the lowest synchronization clock frequency, as slope compensation is determined by the RT value.

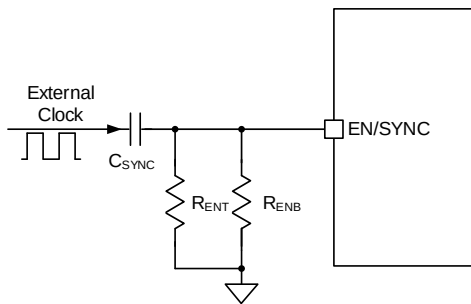


Figure 10-3. EN/SYNC High-pass Filter Demonstration

The amplitude of external clock needs to be higher than V_{EN_SYNC} to trigger internal synchronization pulse detector. An external clock with 5V amplitude can be used on EN/SYNC pin. Moreover, the minimum EN/SYNC rising pulse and falling pulse duration should be longer than t_{SYNC_EDGE} , as what has been shown in **Figure 10-4**. Note that it is recommended to control rise/fall time of clock edge to be less than 30ns. Exerting external clock without meeting the requirements could deteriorate synchronization performance.

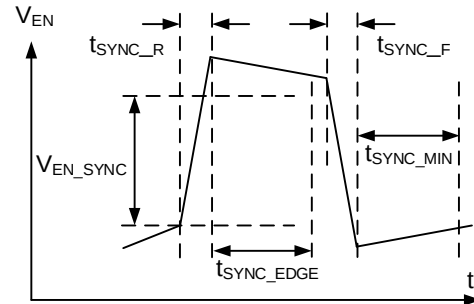


Figure 10-4. Typical EN/SYNC Waveform with External Clock

In order to prevent external clock from interfering the normal start-up, the clock must be off before start-up to allow proper sequencing.

10.7 Internal Soft Start

The integrates soft-start circuit prevents input inrush current and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. If the output of SC81530Q is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage. In order to prevent negative inductor current from pulling output voltage down at start-up, the device is automatically operating in diode emulation mode.

10.8 Over Current Limit and Short Circuit Protection

The SC81530Q has a cycle-by-cycle peak and valley overcurrent limit. If the inductor peak or valley current exceeds the current-limit threshold, and the FB voltage drops below the 40% of the reference, SC81530Q enters hiccup mode to restart the part periodically. It works on current limit for 38ms and then turns off for 480ms to reduce the thermal temperature. This protection mode is especially useful when the output is dead shorted to ground. The SC81530Q exits hiccup mode once the FB voltage is higher than 50% of the reference.

10.9 Over Voltage Protection

SC81530Q has output overvoltage protection. When the output voltage is higher than 120% of V_{REF} , the SC81530Q turns off both high-side switches and low-side switches. The discharge path from USB_OUT pin to ground will turn on. If the FB voltage drops to 110% of V_{REF} , the device will return to normal operation. There is 1ms deglitch for entering or recovering from OVP condition.



10.10 RT and Switching Frequency

A resistor from RT to AGND is needed to set target switching frequency. **Equation (3)** and **Figure 10-5** can be used to determine the resistance. If synchronization to an external clock is needed, do not apply the signal to RT pin. Instead, EN/SYNC can be used for external clock synchronization.

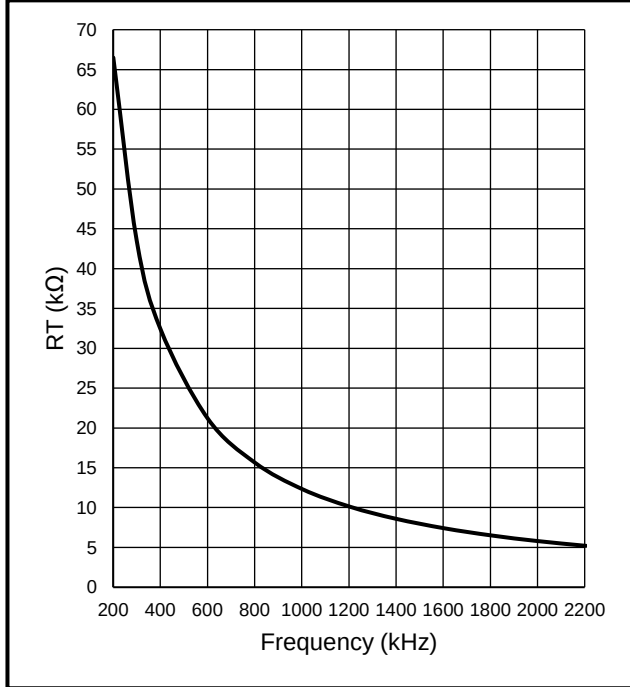


Figure 10-5. RT and Switching Frequency Relationship

$$R_T(k\Omega) = 1.8711 \times 10^4 \times F_{SW}(kHz)^{-1.062} \quad (3)$$

10.11 Spread Spectrum

Spread spectrum is a factory option for applications sensitive to EMI. Through implementing triangular spread spectrum, SC81530Q is able to evenly distribute fundamental frequency and its harmonics. Therefore, peak emissions can be eliminated. The switching frequency is changed per 8 internal oscillator cycles over a $\pm 10\%$ window with total 32 steps. The steps are dependent to nominal setting frequency to optimize the EMI performance.

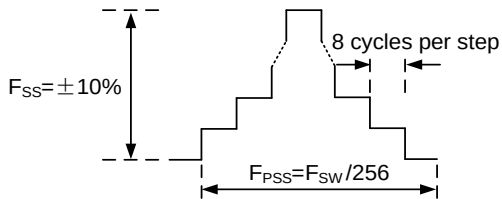


Figure 10-6. Spread-spectrum Mechanism

10.12 Line Drop Compensation

SC81530Q is capable of compensating an output voltage drop, which is helpful when there is high impedance at the output side. The compensated voltage is impacted the output current, upper feedback resistors.

$$V_{BUS} = \left(\frac{R_{up}}{R_{dn}} + 1 \right) \cdot V_{ref} + R_{up} \cdot G_{ADJ} \cdot I_{OUT} \quad (4)$$

Where G_{ADJ} is $2\mu A/A$.

If additional line drop compensation is required, a resistor can be connected in series between the FB pin and the voltage divider network, as shown in Figure 10-7.

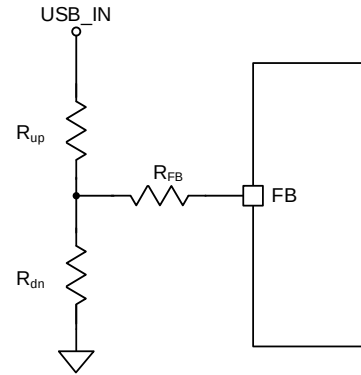


Figure 10-7. Additional Line Drop Compensation

If additional line drop compensation is applied, V_{BUS} is calculated by **Equation (5)**:

$$V_{BUS} = \left(\frac{R_{up}}{R_{dn}} + 1 \right) \cdot V_{ref} + (R_{up} + R_{FB}) \cdot \frac{R_{up} + R_{dn}}{R_{dn}} \cdot G_{ADJ} \cdot I_{OUT} \quad (5)$$

10.13 Over Current Protection

SC81530Q integrates a precise current limit in USB Switch to protect the USB port from extreme overload condition. According to different I_{BUS} and the duration time, the behavior of SC81530Q is different.

- If $I_{LIMIT1} < I_{BUS} < 1.6 \cdot I_{LIMIT1}$ and duration time is shorter than 1.8ms, the device doesn't have OCP behavior which helps it to pass Apple MFI test.
- If $I_{LIMIT1} < I_{BUS} < 1.6 \cdot I_{LIMIT1}$ and the duration time is longer than 1.8ms, the device will limit the I_{BUS} to I_{LIMIT1} after 1.8ms and then enters into the hiccup mode.
- If $I_{BUS} > 1.6 \cdot I_{LIMIT1}$, such as in short circuit condition, device will limit the I_{BUS} to I_{LIMIT} immediately and then enters into the hiccup mode.



10.14 Short to Battery Protection

SC81530Q provides DP/DM/CC1/CC2/USB_OUT short to battery protections to avoid the abnormal fault happen when the cable is short to battery but no device is attached.

When USB_OUT short to battery occurs, the parasitic diode will conduct and USB_IN voltage will charge high to exceed the OVP threshold, then internal DCDC converter will turn off the power stage immediately and the device will turn off the USB switch and data switch. The fault pin will be pulled down after 1ms deglitch time.

When DP/DM short to battery occurs, once the voltage on these pins exceeds 4V, the device turns off the data switch immediate to disable DP/DM output. When CC1/CC2 short to battery occurs, once the voltage on these pins exceeds 5.7V, the device will not only turn off the USB_SWITCH and data switch, but also turn off VCONN switch. Both the deglitch for DP/DM/CC1/CC2 pin is about 16us.

10.15 Charging Downstream Port (CDP) Mode

The SC81530Q supports a charging downstream port (CDP) mode that complies with the USB2.0 definition of a host or a hub.

The CDP handshaking process occurs in two steps:

During step one, the portable equipment outputs a nominal 0.6V output on DP line and reads the voltage on DM line. If the voltage is less than 0.3V, the portable device is detected to an SCP connection. If the voltage is higher than 0.3V and less than 0.8V, the portable device is detected to a CDP connection.

During step two, the portable equipment outputs a nominal 0.6V output on DM line and reads the voltage on DP line. If the voltage is less than 0.3V, the portable device is detected to a CDP connection. If the voltage is higher than 0.3V, the portable device is detected to a DCP connection.

10.16 Client Mode

In Type-A mode, pin22 is configured as EN1. SC81530Q will work in client mode by applying a 0.9V to 1.5V voltage on this pin as show in **Figure 10-8**.

In client mode, the USB_OUT is powered by the external host. The data switch is ON and USB SWITCH is off. It can be used to read and update the head unit software.

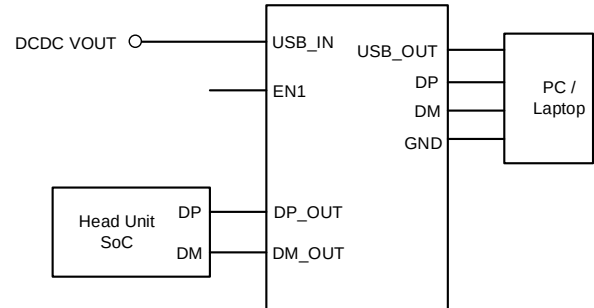


Figure 10-8 Client Mode

10.17 Type-C Mode

SC81530Q use the function of the configuration channel (CC1/CC2 pin) to detect connections and configure the interface across the USB Type-C cables. The detection concept is based on being able to detect terminations in the product. To define the functional behavior of CC, a pull-up resistor (RP) and pull-down resistor termination model is used ad below. A pull-up termination can be replaced by a current source.

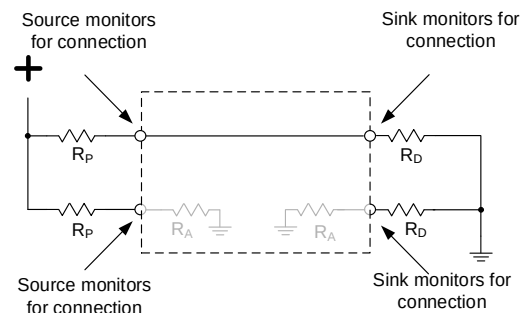


Figure 10-9 USB Type-C Connection

To prevent mistakenly entering TypeA mode, CC1 requires a parallel capacitor of at least 2.2nF.

10.18 Type-A Mode

During start up process, once VCC logic is high, SC81530Q source a 10μA current on CC1 pin for 70μS. When a 100kΩ resistor connected to CC1, an internal 1V voltage will be created and device enter into Type-A mode. In this mode, the CC attached and detach logic is disabled, the current limit changes to the Type-A specifications.

10.19 Load Shedding

When the sensed temperature exceeds 145°C, the USB port's CC1/CC2 pin pull-up resistor will be changed to indicate that the capability has change to 1.5A but the current limit is not changed. If the sensed temperature drops below 105°C and last for 16 seconds, the current capability will be back to 3A.

**10.20 Thermal Shutdown**

The device has an internal overtemperature shutdown threshold T_{SD} to protect the device from damage. If the USB switch silicon temperature exceeds 165°C, the device shuts down and recovery when the temperature falls to 145°C.



11 Application Information

11.1 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage and 25% for systems with a variable input voltage such as the 12V battery in a car. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used. **Equation 5** can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.4 was chosen and an inductance of approximately 5.7μH was found. The next standard value of 4.7μH was selected.

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot K \cdot I_{OUT(MAX)}} \cdot \frac{V_{OUT}}{V_{IN}} \quad (5)$$

The saturation current rating of the inductor must be at least as large as the high-side switch current limit, IL-HS (see Section 8.5). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, IL-LS, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1MHz. To avoid subharmonic oscillation, the inductance value must not be less than that given in **Equation 6**. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L \geq 0.32 \cdot \frac{V_{OUT}}{F_{SW}} \quad (6)$$

Equation 6 assumes that this design must operate with input voltage near or in dropout. If minimum operating

voltage for this design is high enough to limit duty factor to below 50%, **Equation 7** can be used in place of **Equation 6**.

$$L \geq 0.2 \cdot \frac{V_{OUT}}{F_{SW}} \quad (7)$$

Note that choosing an inductor that is larger than the minimum inductance calculated using **Equation 5** through **Equation 7** results in less output capacitance being needed to limit output ripple but more output capacitance being needed to manage large load transients. See Section 11.2.

11.2 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple, control loop stability and load transient performance. **Table 11-1** can be used to find the output capacitor for a few common applications. In this example, improved control loop stability and transient performance is desired giving 4* 22μF ceramic as the output capacitor and 33pF as C_{FF} (Feedforward Capacitor).

Table 11-1. Recommended Output Capacitors

F _{SW}	Recommendation 1	Recommendation 2
400kHz	4X22μF+0.1μF MLCC	100μF (Electrolytic capacitor, ESR<50mΩ) +10μF+0.1μF MLCC
2.2MHz	2X22μF+0.1μF MLCC	NA

Most ceramic capacitors deliver far less capacitance than the rating of the capacitor indicates. Be sure to check any capacitor selected for initial accuracy, temperature derating, and voltage derating. **Table 11-1** have been generated assuming typical derating for 16V, X7R, automotive grade capacitors. If lower voltage, non-automotive grade, or lower temperature rated capacitors are used, more capacitors than listed are likely to be needed.

11.3 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the converter to supply the ripple current and isolate switching noise from other circuits. A minimum of 10μF of ceramic capacitance is required on the input of the device. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100nF ceramic capacitor must be used at input/ground pin pair, immediately adjacent to the converter. This provides a



high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI. The 100nF must also be rated at 50V with an X7R or better dielectric.

Many times, it is desirable and necessary to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the converter. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the input ceramic capacitors. The approximate worst-case RMS value of this current can be calculated from **Equation 8** and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \quad (8)$$

11.4 BOOT Capacitor Selection

The SC81530Q requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high-side power MOSFET. A high-quality (X7R) ceramic capacitor of 100nF and at least 50V is recommended.

11.5 BOOT Resistor Selection

A BOOT resistor and capacitor can be connected in series between the BOOT and SW pins. Unless EMI for the application being designed is critical, R_{BOOT} can be shorted. To maximize efficiency, 0Ω is chosen for this example. Under most circumstances, selecting an R_{BOOT} resistor value above 20Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

11.6 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a 4.7μF, 16V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup (FLT or NTC function) or logic level (CC2 logic high). A pullup resistor with a value of 10kΩ is a good choice in this case.

11.7 External UVLO

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in **Figure 11-1**. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then **Equation 9 and 10** is used to calculate R_{ENT} and V_{OFF} :

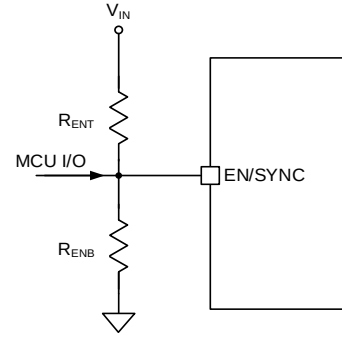


Figure 11-1. EN/SYNC Configuration for Precise Enable

$$R_{ENB} = R_{ENT} \cdot \frac{V_{EN_H}}{V_{IN_R} - V_{EN_H}} \quad (9)$$

$$V_{IN_HYS} = V_{EN_HYS} \cdot \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (10)$$

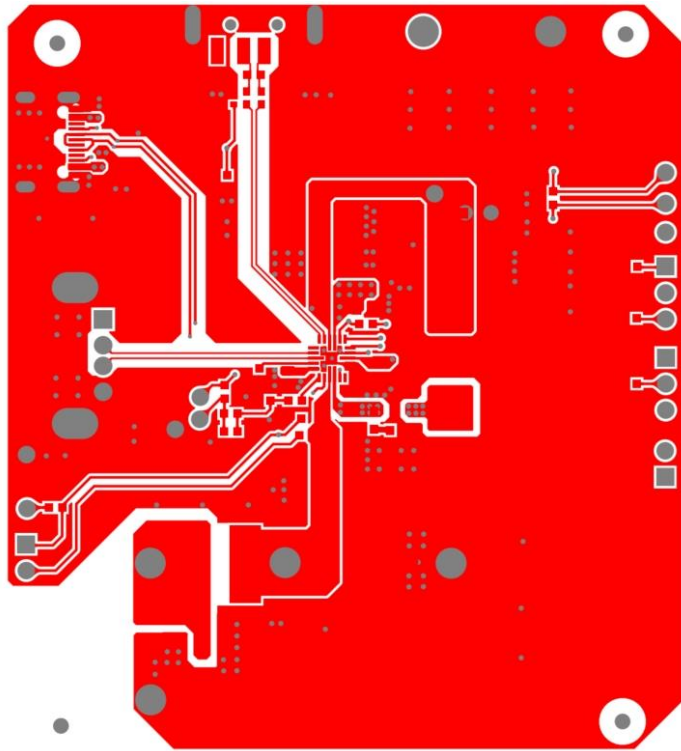
Equation (9) can be used to calculate resistor values and **Equation (10)** can be used to calculate hysteresis after resistors are selected. V_{IN_R} is the input rising voltage for start-up and V_{IN_HYS} is the hysteresis.



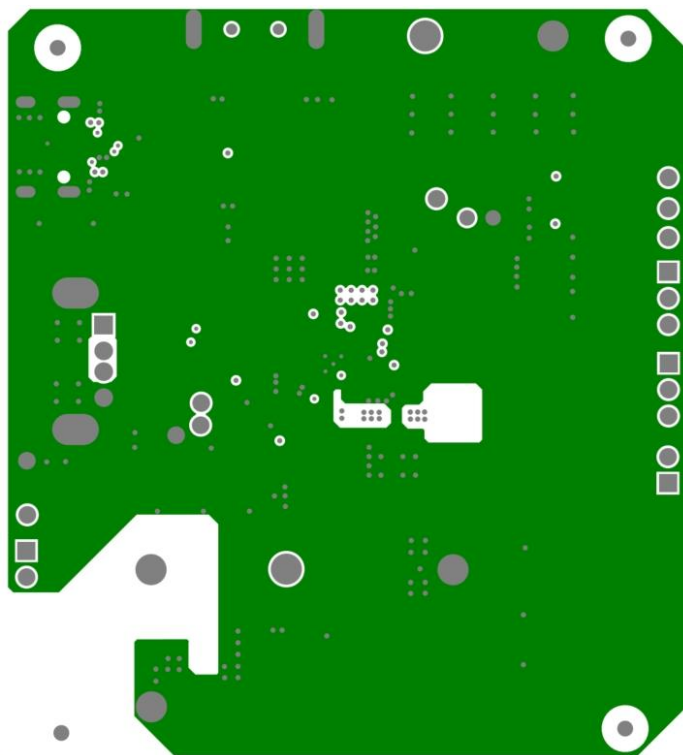
12 Layout Guide

The PCB layout is critical to get the optimal performance and thermal dissipation. For SC81530Q, the loop consisting of VIN-SW-GND and VIN-SW-USB_IN is the most important. Poor layout means larger parasitic parameters and noise. Generally, to reduce the PCB inductance, the area of this loop must be small, and the trace must be wide. **Figure 12-1** shows a recommended layout.

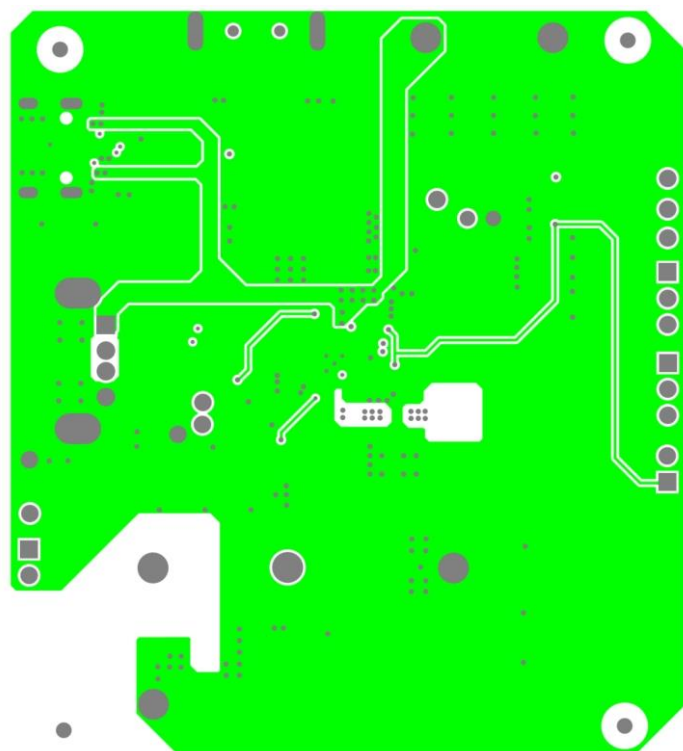
1. Place the ceramic input capacitors as close to VIN pin and GND as possible, especially the small package size (recommend 0603) input bypass capacitor.
2. The VIN, USB_IN and GND paths must be wide and short enough to reduce any voltage drops on the input or output paths of the converter.
3. Place the VCC/BIAS capacitor as close to the VCC/BIAS pin.
4. The VCC/BIAS and GND paths must be as wide and short as possible. More vias should be placed near GND of C_{VCC}/C_{BIAS} .
5. Recommend to connect a large ground plane to GND on all layers. Add vias near GND if there are several ground planes on different layers.
6. Place SW and BOOT away from sensitive analog areas, such as FB.
7. The area of SW and BOOT should be small to reduce EMC noise.
8. If an R_{BOOT} resistor is used, place it as close as possible to BOOT pins. If high efficiency is desired, R_{BOOT} can be shorted.
9. The DP/DM and DP_OUT/DM_OUT traces should be equal in width and length. Differential impedance of DP/DM and DP_OUT/DM_OUT should be controlled within $90\Omega \pm 10\%$.
10. If GND is near DP/DM and DP_OUT/DM_OUT, there should be enough distance (typically 20mil) to avoid new signal integrity issues caused by GND.
11. Use as less vias and corners as possible on DP/DM and DP_OUT/DM_OUT traces. Replace 90° turn with two 45° turns.



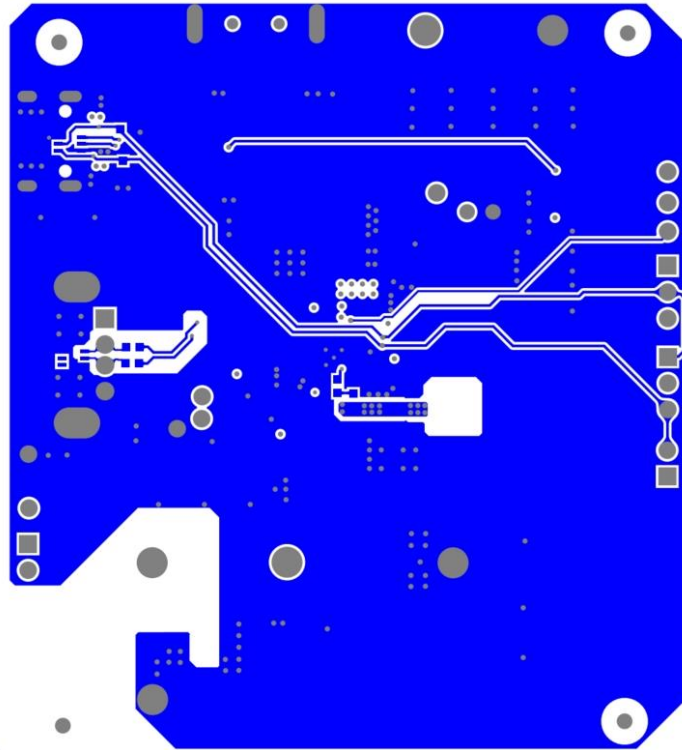
(a) Top Layer



(b) GND1 Layer



(c) GND2 Layer



(d) Bottom Layer

Figure 12-1 Layout Example

13 Typical Application Circuits

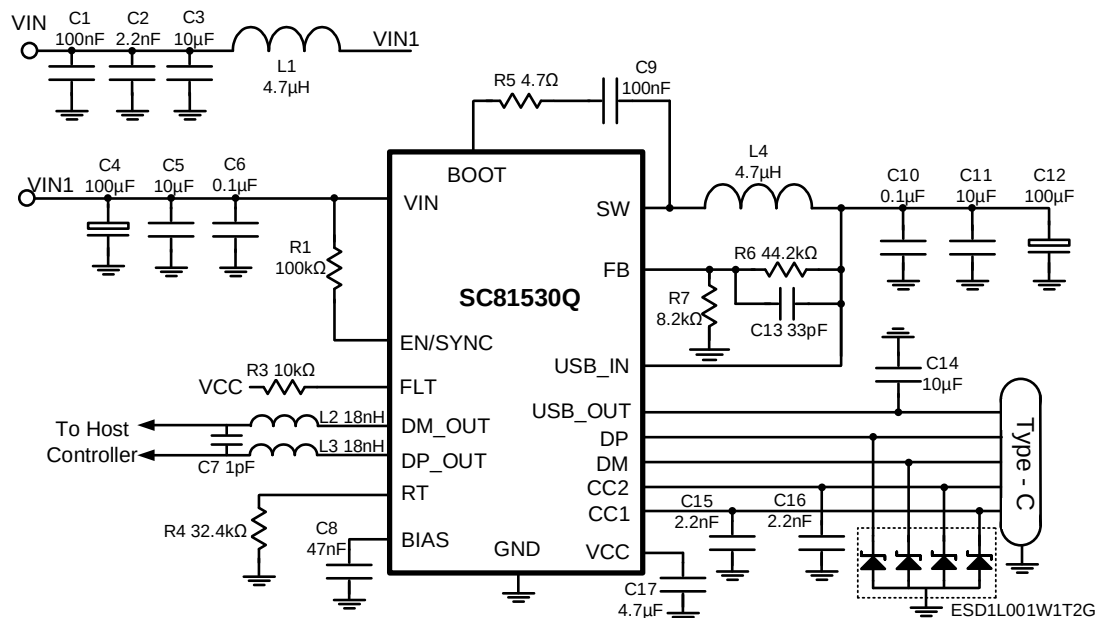


Figure 13-1 $V_{IN}=12V$, $V_{OUT}=5V$, $I_{OUT}=3A$, $F_{SW}=400kHz$, Type-C DFP with BC1.2 CDP Mode

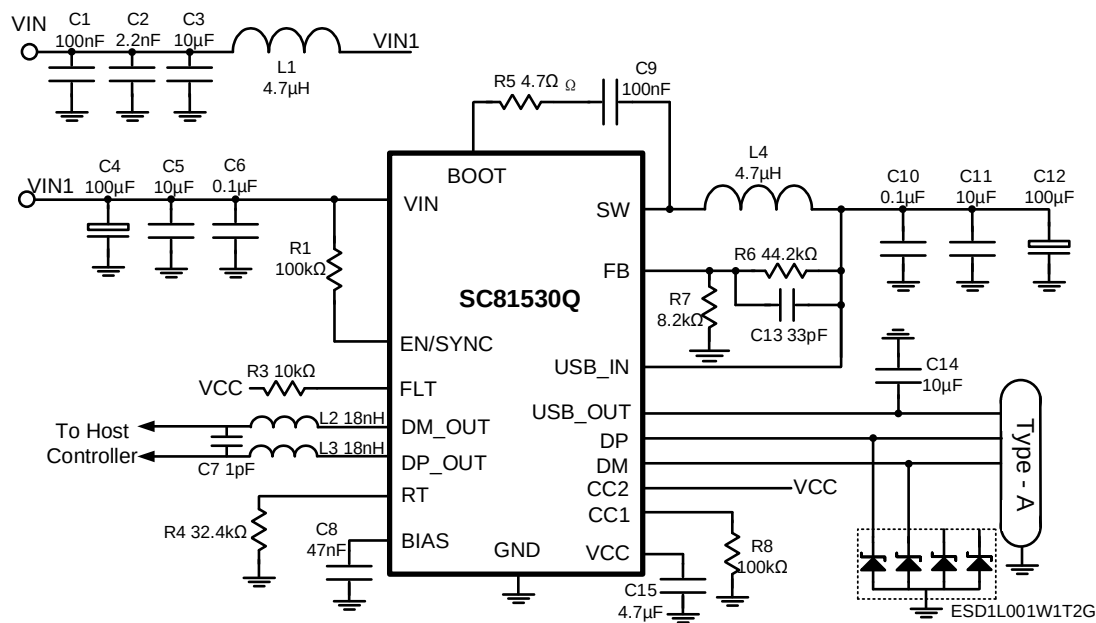
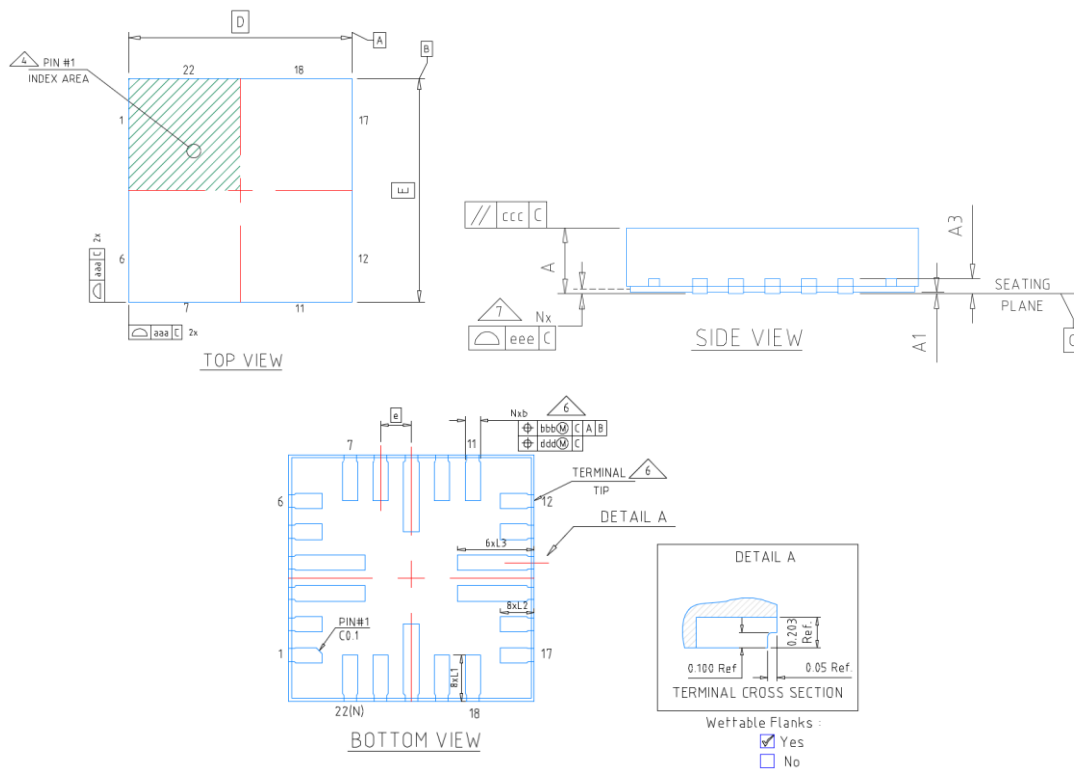


Figure 13-2 $V_{IN}=12V$, $V_{OUT}=5V$, $I_{OUT}=2.4A$, $F_{SW}=400kHz$, Type-A DFP with BC1.2 CDP Mode



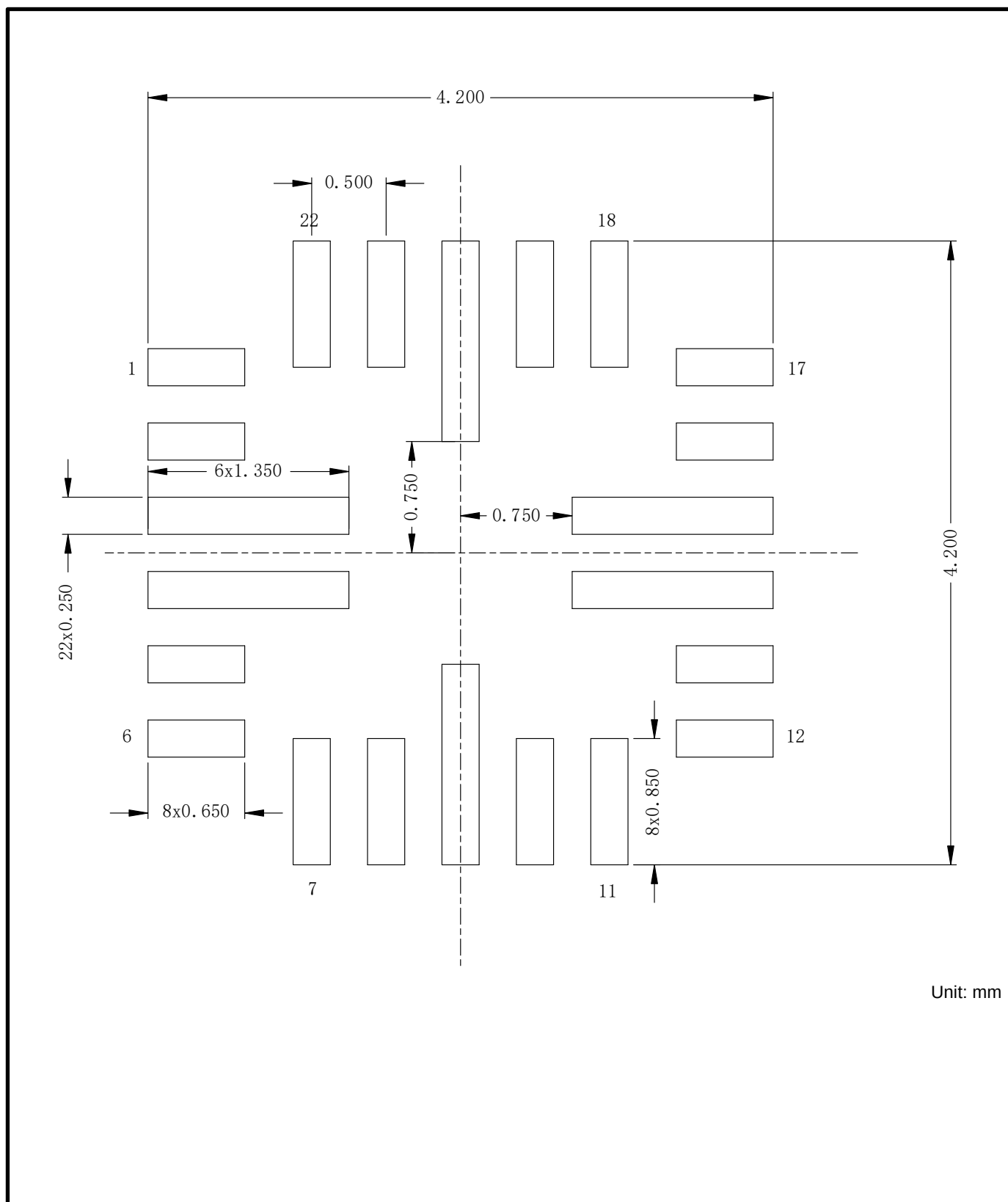
MCHANICAL DATA



Dimension Table			
Thickness Symbol	V		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.203 Ref.	---
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC		
L1	0.65	0.75	0.85
L2	0.45	0.55	0.65
L3	1.15	1.25	1.35
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Unit:mm

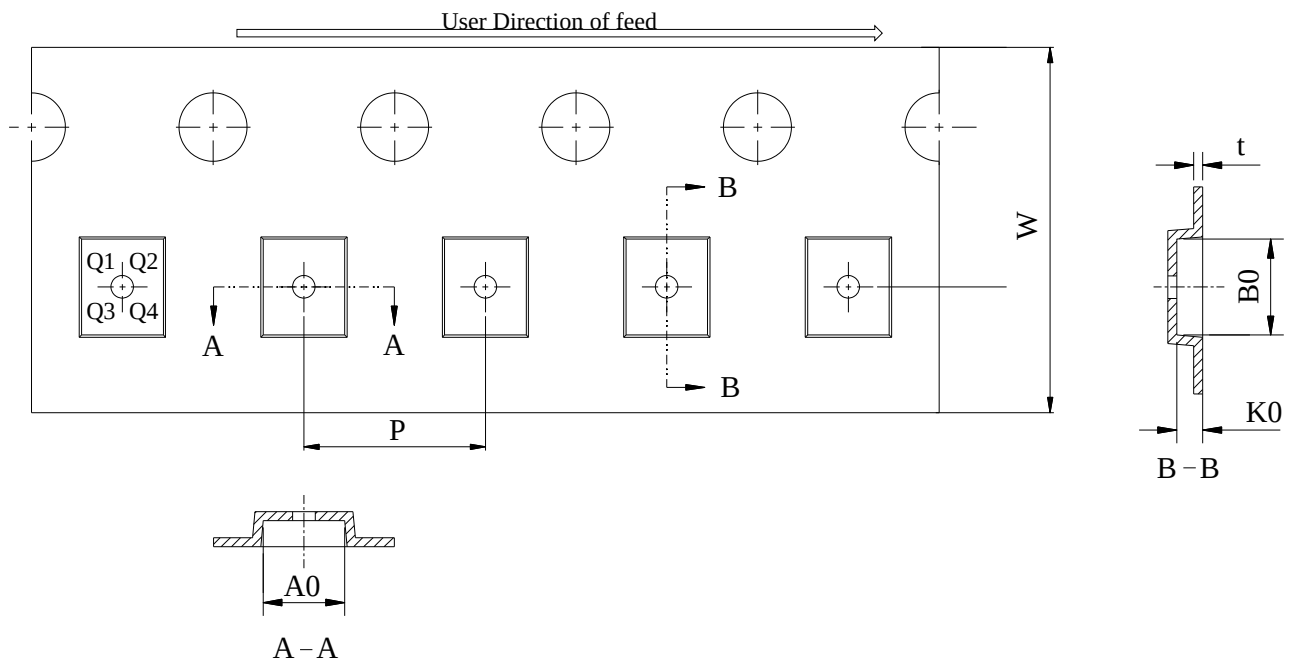
RECOMMENDED FOOTPRINT



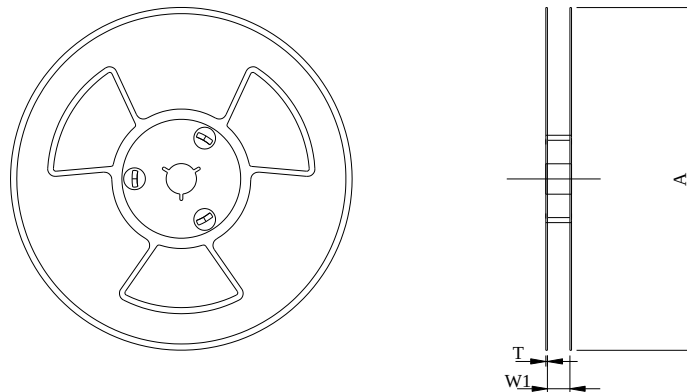
Unit: mm



TAPE AND REEL INFORMATION

Carrier Tape

Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	$12.00 +0.30/-0.10$	8.00 ± 0.10	4.30 ± 0.10	4.30 ± 0.10	1.10 ± 0.10	0.30 ± 0.03	Q1

REEL

Item	A	W1	T
Size (mm)	330 ± 2	$12.4 +2/-0$	2.1 ± 0.15



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