Triple-C Port Fast Charge Protocol Controller supporting PD3.2 EPR Applications

1 Descriptions

SC2006Q is a triple-C Port Type-C/PD fast charge controller. It complies with the most popular high voltage fast charge protocols with CC & DPDM interface. It targets for the powerbank, car charger and electronic tools applications.

SC2006Q minimizes external components by integrating USB PD baseband PHY, Type-C detection, VBUS discharging path, VCONN supply, DPDM fast charge protocol PHY, voltage and current sense, 11-bit high performance ADC, two (10+1) bit VDAC, NMOS gate driver, I2C interface and protection circuits. It embedded 32-bit high performance micro-controller with 128K-Byte flash(another 16kB for ECC), and 8K-Byte SRAM, which provides cost effective solutions to many applications.

SC2006Q supports various protection mechanisms including over voltage protection, under voltage protection, over current protection, short circuit protection, over temperature protection, DPDM over voltage protection, CC over voltage protection, VCONN over voltage, over current and short protection, so to effectively ensure stable and reliable operation of system..

2 Features

- **AEC-Q100 qualified for automotive applications**
- **Fast Charge Protocol Interface**
  - Two pairs of independent CC pins and one pair of reused CC pins for Type-C and PD3.2 usage, supporting Vconn supply
  - Two pairs of independent DPDM pins and one pair of reused DPDM pins for USB fast charge usage, including BC1.2, DCP, HVDCP, FC, AFC, FCP, SCP, VOOC, UFCS and various proprietary protocols
- **Power and Analog Blocks**
  - 30V operating voltage range, supporting PD3.2 EPR application.
  - Support 48V EPR by sampling output voltage through voltage division
  - Integrated two VBUS discharging paths
  - Integrated high-side current sense amplifier and 11-bit ADC
  - Integrated up to three N-MOS driver blocks
  - Integrated up to three IN_DET blocks
  - Built-in protections: OVP, OCP, SCP, UVP, OTP, CC OVP, DPDM OVP
- **MCU Subsystem**
  - 32bit ARM Cortex-M0 Core
  - 12 MHz CPU frequency
  - 128kB flash (another 16kB for ECC)
  - 8 kB SRAM
  - Master/Slave I2C interface and UART TX/RX interface
  - SWD debug supporting
  - 48MHz PWM output supporting
- **Package**
  - QFN-44(5*5), 5.0mm x 5.0mm x 0.75mm

3 Applications

- Car charger.

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC2006QQDTR	QFN-44(5*5)	5.0mm x 5.0mm x 0.75mm

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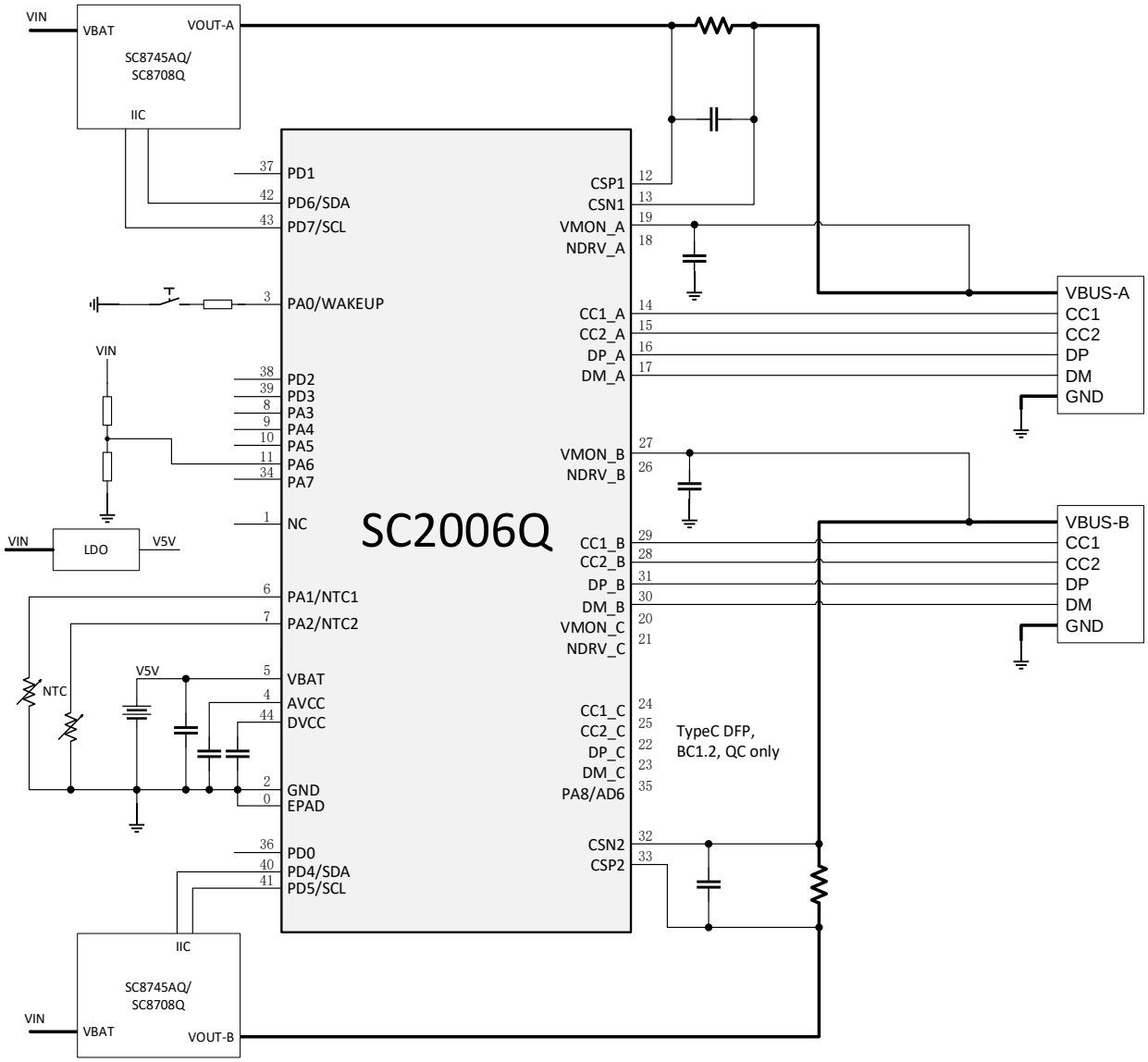
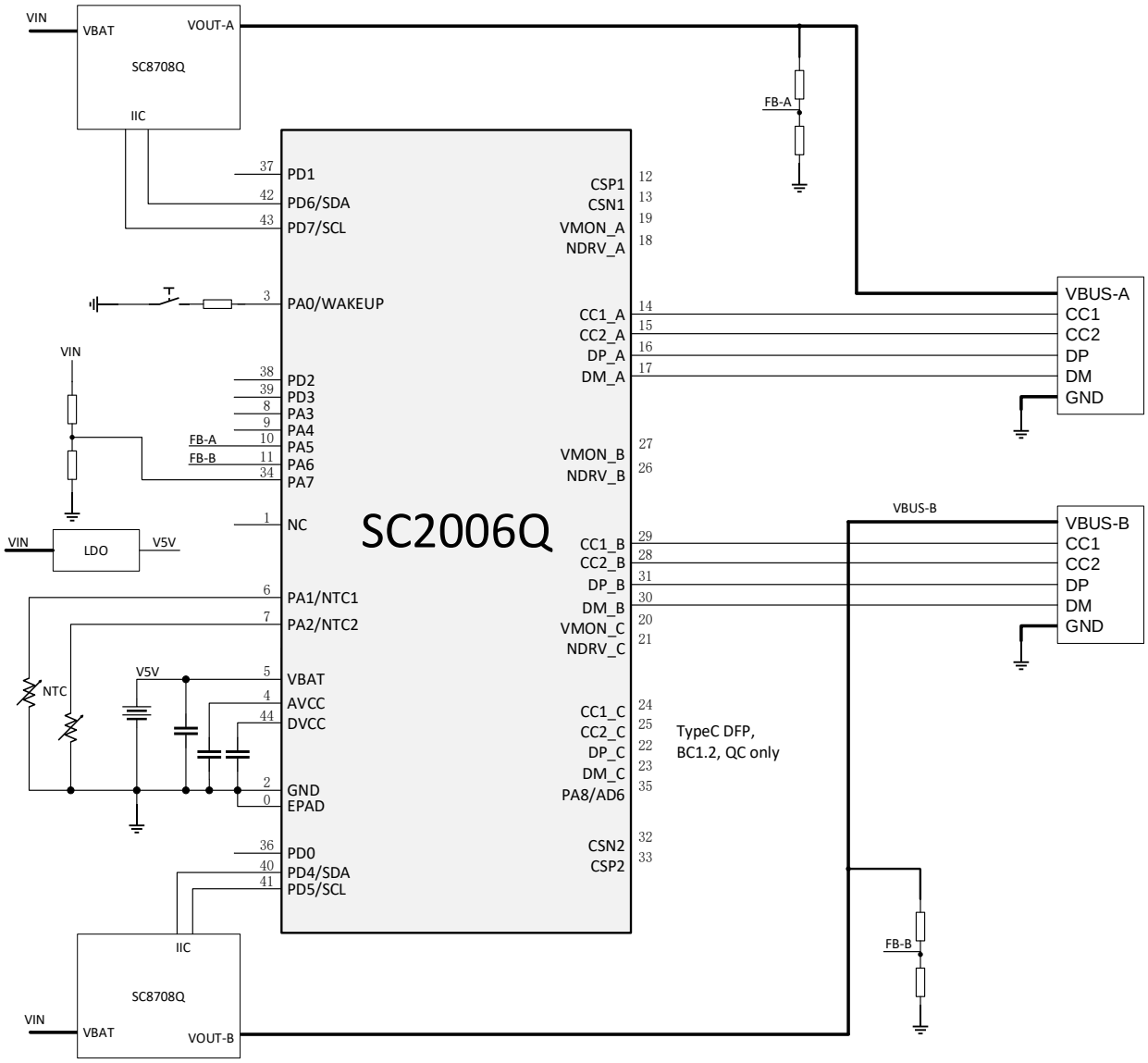
5 Typical Application Circuit

Please refer to Southchip reference design for the schematic diagram.

SPR(with SC8745AQ) and 28V 140W EPR(SC8708Q) solution

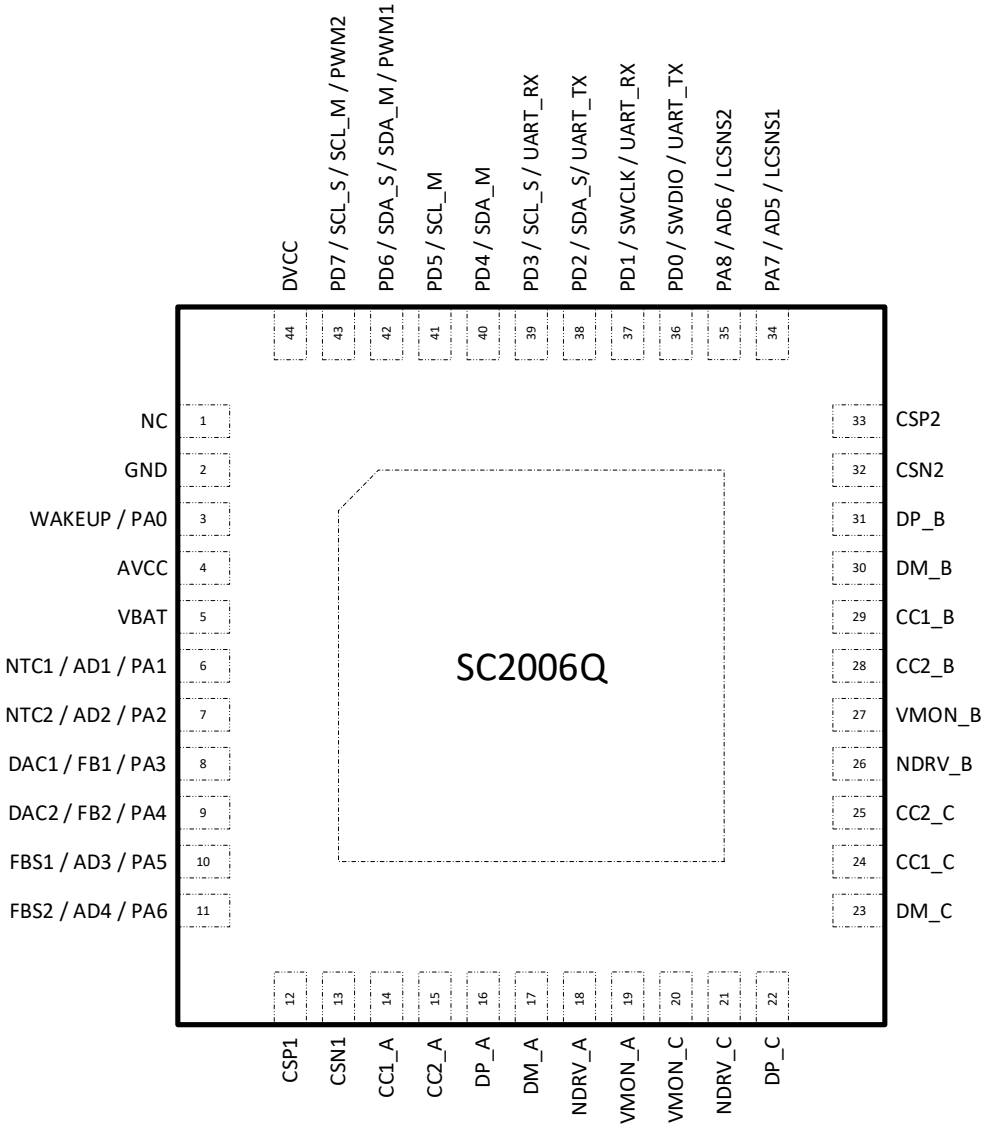


48V 240W EPR(SC8708Q) solution



6 Terminal Configuration and Functions

44-pin
TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	NC	-	
2	GND	-	Ground of the IC.

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3	PA_0	IO	GPIO, push-pull.
	WAKEUP		Wait for a rising edge to wake up the MCU from suspend mode.
4	AVCC	PWR	5V LDO output. Connect to GND with a 1μF capacitor.
5	VBAT	PWR	Battery power supply.
6	PA1	IO	GPIO, push-pull.
	NTC1		Remote thermal sensor connection node for board temperature monitoring.
	AD1		General ADC
7	PA2	IO	GPIO, push-pull.
	NTC2		Remote thermal sensor connection node for board temperature monitoring.
	AD2		General ADC
8	PA3	IO	GPIO, push-pull.
	DAC1		DAC output.
	FB1		Connect this pin to the feedback divider of a buck controller.
9	PA4	IO	GPIO, push-pull.
	DAC2		DAC output.
	FB2		Connect this pin to the feedback divider of a buck controller.
10	PA5	IO	GPIO, push-pull.
	AD3		General ADC
	FBS1		Connect this pin to GND through a resistor to adjust the FB current if FB function is enabled.
11	PA6	IO	GPIO, push-pull.
	AD4		General ADC
	FBS2		Connect this pin to GND through a resistor to adjust the FB current if FB function is enabled.
12	CSP1	I	Positive input of the internal high-side current sense amplifier. Connect to the high side current sense resistor.
13	CSN1	I	Negative input of the internal high-side current sense amplifier. Connect to the low side current sense resistor.
14	CC1_A	IO	Type-C configure channel1. It also supports VCONN output.

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15	CC2_A	IO	Type-C configure channel2. It also supports VCONN output.
16	DP_A	IO	USB DP line of the fast-charging interface.
	SDA_S1		Slave I2C interface, data line.
	UART_TX0		Transmit port when configure as UART interface.
17	DM_A	IO	USB DM line of the fast-charging interface.
	SCL_S1		Slave I2C interface, clock line.
	UART_RX0		Receive port when configure as UART interface.
18	NDRV_A	IO	I2C interface clock. Connect to a pull up resistor.
19	VMON_A	I	Port voltage monitor and device plug-in detector.
20	VMON_C	I	Port voltage monitor and device plug-in detector.
21	NDRV_C	IO	I2C interface clock. Connect to a pull up resistor.
22	DP_C	IO	USB DP line of the fast-charging interface.
23	DM_C	IO	USB DM line of the fast-charging interface.
24	CC1_C	IO	Type-C configure channel1. It also supports VCONN output.
25	CC2_C	IO	Type-C configure channel2. It also supports VCONN output.
26	NDRV_B	IO	I2C interface clock. Connect to a pull up resistor.
27	VMON_B	I	Port voltage monitor and device plug-in detector.
28	CC2_B	IO	Type-C configure channel2. It also supports VCONN output.
29	CC1_B	IO	Type-C configure channel1. It also supports VCONN output.
30	DM_B	IO	USB DM line of the fast-charging interface.
	UART_RX1		Receive port when configure as UART interface.
31	DP_B	IO	USB DP line of the fast-charging interface.
	UART_TX1		Transmit port when configure as UART interface.
32	CSN_2	I	Negative input of the internal high-side current sense amplifier. Connect to the low side current sense resistor.
33	CSP_2	I	Positive input of the internal high-side current sense amplifier. Connect to the high side current sense resistor.
34	PA7	IO	GPIO, push-pull.

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	AD5		General ADC.
	LCSNS1		Low-Side Current Sense input.
35	PA8	IO	GPIO, push-pull.
	AD6		General ADC.
	LCSNS2		Low-Side Current Sense input.
36	PD0	IO	GPIO, push-pull.(Digital Die)
	UART_TX2		Transmit port when configure as UART interface.
	SWDIO		SWD debug interface, data line.
37	PD1	IO	GPIO, push-pull.(Digital Die)
	UART_RX2		Receive port when configure as UART interface.
	SWCLK		SWD debug interface, clock line.
38	PD_2	IO	GPIO, push-pull.(Digital Die)
	SDA_S2		Slave I2C interface, data line.
	UART_TX2		Transmit port when configure as UART interface.
39	PD_3	IO	GPIO, push-pull.(Digital Die)
	SCL_S2		Slave I2C interface, clock line.
	UART_RX2		Receive port when configure as UART interface.
40	PD_4	IO	GPIO, push-pull.(Digital Die)
	SDA_M1		Master I2C interface, data line.
41	PD_5	IO	GPIO, push-pull.(Digital Die)
	SCL_M1		Master I2C interface, clock line.
42	PD_6	IO	GPIO, push-pull.(Digital Die)
	SDA_S3		Slave I2C interface, data line.
	SDA_M2		Master I2C interface, data line.
	PWM_1		PWM output.
43	PD_7	IO	GPIO, push-pull.(Digital Die)

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	SCL_S3		Slave I2C interface, clock line.
	SCL_M2		Master I2C interface, clock line.
	PWM_2		PWM output.
44	DVCC	PWR	1.5V LDO output. Connect to GND with a 1μF capacitor.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	Unit
Voltage range at terminals(2)	VBAT, CSP, CSN, VMON	-0.3	30	V
	NDRV	-0.3	35	V
	CC, DP, DM	-0.3	28	V
	VCC, GPIO	-0.3	5.5	V
T_J	Operating junction temperature range	-40	125	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) (2)	All pins	-2	2	kV
	Charged-device model (CDM) (3)	All pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Symbol	Description	MIN	TYP	MAX	UNIT
V_{IN}	V_{IN}(V_{BAT} or V_{MON})operation voltage	3.0		28.0	V
T_A	Operating ambient temperature	-40		105	°C
T_J	Operating junction temperature	-40		125	°C

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7.4 Electrical Characteristics

T_J = -40°C to 125°C and V_{BUS} = 5V, V_{BAT} = 5V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{BUS_RANGE}	V_{MON} supply range		4.0		30	V
V_{BAT_RANGE}	V_{BAT} supply range		3.0		30	V
V_{BAT_TURNON}	V_{BAT} turn on threshold		2.80	2.90	3.00	V
$V_{BAT_TURNOFF}$	V_{BAT} turn off threshold		V_{BAT_TURNON} - 0.3		V_{BAT_TURNON} - 0.15	V
V_{MON_TURNON}	V_{MON} turn on threshold				4.00	V
$T_{VBAT_TURNOFF_DEGLITCH}$	Time for V_{BAT} turn off deglitch	Trim option	40	50		µs
		Trim option	80	100		µs
I_{Q_ACTIVE}	Quiescent current in active mode				10	mA
$I_{Q_STANDBY}$	Quiescent current in standby mode.				6	mA
I_{Q_GREEN}	Quiescent current in green mode				150	µA
$I_{Q_SUSPEND}$	Quiescent current in suspend mode			24	32	µA
$I_{Q_SHIPPING}$	Quiescent current in shipping mode			6	15	µA
5V LDO						
V_{LDO_5V}	5V LDO regulation voltage	V_{IN} = 5.5V~30V	5.0	5.15	5.3	V
I_{LDO_OUPUT}	LDO current output capability	V_{IN} = 5V	50			mA
1.5V LDO						
$V_{LDO_1.5V}$	1.5V LDO regulation voltage	V_{IN} = 3.3V~30V	1.35	1.5	1.65	V
I_{LDO_OUPUT}	LDO current output capability	V_{IN} = 5V	20			mA
VBUS DISCHARGE						
$I_{DIS_VBUS_PWR}$	Discharging current at CSPx	Register-Programmable	40	50		mA
		Register-Programmable	80	100		mA
$R_{DCHG_VBUSMON}$	Discharging resistor at VBUS_MON		0.5	1	1.5	kΩ
NGATE DRIVER						
V_{NDRV}	N-MOS load switch driving voltage	VSUPPLY = 3.0V ~30V	V_{MON}+5	V_{MON}+6.2	V_{MON}+6.9	V
I_{ndrv_chg}	The capability of NDRV block to charge C_{gs}	Register Programmable		50		µA
		Register Programmable		6		µA
I_{ndrv_dischg}				420		µA

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	The capability of NDRV block to discharge C_{gs}.	In suspend mode			8	μA
DAC						
N_{DAC}				11		Bits
V_{DAC_MIN}	The minimum output of DAC	VSUPPLY = 3.0V ~30V	0	0	10	mV
V_{DAC_MAX}	The maximum output of DAC	VSUPPLY = 3.0V ~30V	2038	2048	2058	mV
$r_{DAC_ramping}$	DAC slew rate (1LSB = 2mV)	Register-Programmable		200		μs/ LSB
		Register-Programmable		40		μs / LSB
I_{OUT_DAC}	Accuracy	I_{OUT}=1-3A	-100		100	mA
Plug-in Detect						
V_{INDET_OPEN}	INDET source open voltage		2.4	2.74		V
I_{INDET}	The capability of the INDET source.	Register-Programmable	2.2	3.4	5.7	μA
		Register-Programmable	6.4	9	11.6	μA
V_{INDET_TH}	The trigger voltage of INDET	Register-Programmable		85%*V_{INDET}		
		Register-Programmable		65%*V_{INDET}		
		Register-Programmable		45%*V_{INDET}		
		Register-Programmable		30%*V_{INDET}		
$V_{INDET_LEAKING}$	The leaking voltage on CSP pin to support the usage of INDET in single-loadswitch applications.		$V_{INDET, MAX}$ - 0.7V			
$V_{DPDM_INDET_OPEN}$	Indetect Source open voltage		2.4	2.7		V
I_{DPDM_INDET}	The capability of the indetect Source.	Register-Programmable	1.2	2.0	3	μA
		Register-Programmable	3.2	4	6	μA
$V_{DPDM_INDET_TH}$	The trigger voltage of DPDM_INDET			85%*V_{DPDM_INDET}		
PROTECT						
V_{VBUS_OVP}	VCSPx OVP threshold.	Register Programmable	6	6.5		V
		Register Programmable	14.5	15		V
		Register Programmable	23	24		V
		Register Programmable	29	30		V
$T_{OVP_Deglitch}$	OVP deglitch time.	Register Programmable		5		μs
		Register Programmable		40		μs

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$V_{SCP_Threshold}$	The voltage threshold between CS+ and CS- when SCP(Short-circuit protect) occurred.	Register Programmable		150		mV
		Register Programmable		200		mV
		Register Programmable		250		mV
		Register Programmable		300		mV
$T_{SCP_Deglitch}$	The deglitch time for SCP			5		μs
$I_{vconn_ocp_threshold}$	Vconn OCP threshold.		35	55	75	mA
$T_{VCONN_OCP\ Deglitch}$	VCONN OCP deglitch time.		0.5	1	1.5	ms
Peak_Load						
$V_{peak_load_Threshold}$	The voltage threshold between CS+ and CS- when Peak_Load interrupt flag rises.(Only available in OTG orientation)	Register Programmable		300		mV
		Register Programmable		500		mV
		Register Programmable		600		mV
		Register Programmable		1000		mV
$T_{peak_load_deglitch}$	Peak load detect deglitch.			5		μs
NTC						
V_{NTC_OPEN}	NTC open voltage		2.253			V
I_{NTC}	NTC pin bias current.	Register Programmable	92	100	108	μA
		Register Programmable	16	20	24	μA
		Register Programmable	3.5	4	4.5	μA
ADC						
V_{ADC_REF}	Reference voltage for ADC.	Register-Programmable	2.23	2.253	2.28	V
		Register-Programmable	1.022	1.024	1.026	V
N_{ADC}	Resolution of ADC.			11		bits
f_{ADC_sample}	Sample rate.			25		kHz
K_{ADC_VBUS}	Ratio from CSPx/VMON voltage sense-PIN.	Register programable		1/10		
		Register programable		1/14.5		
K_{ADC_CSNS}	Ratio from CSNS1 / CSNS2 to ADC input.	Register programable		20x		
		Register programable		40x		
K_{ADC_CC}	Ratio from CC voltage sense.			1/2		
K_{ADC_DPDM}	Ratio from DPDM voltage sense.			1/2		
$K_{ADC_General}$	Ratio from GPIO channel to ADC input.	When configured as general AD		1		
		When configured as low-side CSNS		20x		
K_{ADC_NTC}	Ratio from NTC channel.			1		

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K_{ADC_VDD5V}	Ratio from VDD_5V voltage sense.			1/4		
K_{ADC_TJ}	Ratio from internal temperature sense			1		
E_{ADC}	Steady-state error of all ADC channels except Tj.		-2		+2	LSB
E_{TJ}	Internal temperature sense sample error.		-15		+15	℃
GPIO						
V_{IH_GPIO}	Input voltage high range	VSUPPLY = 3.0V ~30V, measured as VIO	2.7			V
V_{IL_GPIO}	Input voltage low range	VSUPPLY = 3.0V ~30V, measured as VIO			1.0	V
V_{OH_GPIO}	Output voltage high threshold	VSUPPLY = 6V, apply 5 mA sink current from IO pin to GND externally	4.4			V
V_{OL_GPIO}	Output voltage low threshold	VSUPPLY = 6V, apply 5 mA source current from VDD_5V to IO pin externally			0.3	V
R_{pullup}	Pull up resistor value at GPIO pin	VSUPPLY = 3.0V ~30V	2.8	5.6	8.4	kΩ
$R_{pulldown}$	Pull down resistor value at GPIO pin	VSUPPLY = 3.0V ~30V	2.8	5.6	8.4	kΩ
PROTOCOL INTERFACE (DPDM)						
R_{SHORT}	DP DM short resistance	VSUPPLY = 4.8~5.5V， T = 25°	9		20	Ω
		VSUPPLY = 4.8~5.5V， T > 80°	9		40	Ω
$V_{buffer_3.3V}$	Output voltage at DP, DM pin	VSUPPLY = 5V	3.2	3.3	3.4	V
$V_{buffer_2.7V}$	Output voltage at DP, DM pin	VSUPPLY = 3.0-5V	2.6	2.7	2.8	V
$V_{BUFFER_0.6V}$	Output voltage at DP, DM pin	VSUPPLY = 3.0-5V	0.5	0.6	0.7	V
I_{buffer_OUT}	The current capability of DP/DM output buffer measured when the voltage drops to 80% of set value.	Register Programmable	7	10	13	μA
		Register Programmable	250		2000	μA
R_{OUT_30k}	Output resistance of DP or DM buffer	VSUPPLY = 4.8~5.5V， T = 25°	24	30	36	kΩ
V_{TH_3V}	Comparision threshold at DPDM pin	VSPPLY = 5V	2.9	3	3.1	V
$V_{TH_2.2V}$		VSPPLY = 3.0V	2.1	2.2	2.3	V
$V_{TH_1.35V}$		VSPPLY = 3.0V	1.3	1.35	1.4	V
$V_{TH_0.425V}$		VSPPLY = 3.0V	0.4	0.425	0.45	V
$V_{TH_0.325V}$		VSPPLY = 3.0V	0.25	0.325	0.4	V
R_{DP/DM_DWN}	DP/DM pull down resistance	T = 25°	16	20	24	kΩ
R_{DP/DM_LKG}	DP/DM leakage		300	500	700	kΩ

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I_{DP/DM_LKG}	DP/DM leakage current		75	100	125	μA
$V_{DATA_HIGH_3.3}$	DP/DM data ouput high voltage, Data_high_sel = 0b	VSUPPLY = 5V	3	3.3	3.6	V
		VSUPPLY = 3.0V	2.6		3.6	V
I_{DMDATA_OH}	DPDM data output high current capability (source)	VSUPPLY = 3.0V, DM = 2.6V, T = 25°	5			mA
I_{DMDATA_OL}	DPDM data output low current capability (sink)	VSUPPLY = 5V, DM = 0.4V, register programmable, T = 25°	1.2		6	mA
V_{DATA_LOW}	DP/DM data output low voltage	SCP output low logic, external pull up capability 100uA.			0.1	V
V_{IH_TH}	DPDM input data rising threshold	00b	0.7	0.8	0.9	V
		01b	1.1	1.2	1.3	V
		10b	1.3	1.4	1.5	V
		11b	1.7	1.8	1.9	V
V_{IL_TH}	DPDM input data falling threshold	00b	0.5	0.6	0.7	V
		01b	0.9	1.0	1.1	V
		10b	1.0	1.1	1.2	V
		11b	1.4	1.5	1.6	V
T_{DATA_RISING}	Data output from low to high			0.3	1	μs
$T_{DATA_Falling}$	Data output from high to low			0.3	1	μs
T_{UI}	Unit interval time		144	160	176	μs
T_{PING_ST}	Adapter transmit slave ping duration time		2304	2560	2816	μs
T_{PING_SR}	Adapter receive master ping duration		2304	2560	2816	ms
T_{PSR}/T_{PST}	Ping received and transmit ratio		99	100	101	%
T_{MREQ}	Terminal request bus window after slave ping		1		2	UI
T_{SREQ_SLV}	Adapter request bus window after slave ping		3		5	UI
T_{SREQ_MST}	Adapter request bus window after master ping		2		5	UI
t_{AD}	Terminal attach deglitch		450	500	550	μs
t_{DD}	Terminal detach deglitch	00b	0.475	0.5	0.525	ms
		01b	0.95	1	1.05	ms
		10b	1.9	2	2.1	ms
		11b	3.8	4	4.2	ms
CC						
I_{CC_80uA}	CCA1/2 or CCB1/2 pull up current	VSUPPLY=3.0V, CSRC_I = 00b	64	80	96	μA
I_{CC_180uA}	CCA1/2 or CCB1/2 pull up current	VSUPPLY =3.0V,	165.6	180	194.4	μA

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		CSRC_I = 01b				
I_{CC_330uA}	CCA1/2 or CCB1/2 pull up current	VSUPPLY =3.0V, CSRC_I = 10b	303.6	330	356.4	μA
$V_{RP_PULL_UP}$	Rp pull up voltage	VSUPPLY>3.3V		3.3		V
R_d	Rd impedance	Power on	4.59	5.1	5.61	kΩ
$V_{cc_deadbattery}$	The voltage on CC pins when a Rp source is connected during dead battery status.	Rp = 80μA (±20%)	0.25		1.6	V
		Rp = 180μA (±20%)	0.45		1.6	V
		Rp = 330μA (±20%)	0.85		2.6	V
R_{CC_open}	CC1/2 open impedance	CC1/2 in disable status	126			kΩ
$V_{CC_0P2_th_src}$	CC1/2 0.2V comparison threshold	CC1/2 as source	0.15	0.2	0.25	V
$V_{CC_0P4_th_src}$	CC1/2 0.4V comparison threshold	CC1/2 as source	0.35	0.4	0.45	V
$V_{CC_0P66_th_src}$	CC1/2 0.66V comparison threshold	CC1/2 as source	0.61	0.66	0.7	V
$V_{CC_0P8_th_src}$	CC1/2 0.8V comparison threshold	CC1/2 as source	0.75	0.8	0.85	V
$V_{CC_1P23_th_src}$	CC1/2 1.23V comparison threshold	CC1/2 as source	1.18	1.23	1.28	V
$V_{CC_1P6_th_src}$	CC1/2 1.6V comparison threshold	CC1/2 as source	1.55	1.6	1.65	V
$V_{CC_2P6_th_src}$	CC1/2 2.6V comparison threshold	CC1/2 as source	2.45	2.6	2.75	V
$T_{CC_cmp_deglitch}$	The deglitch time of CC comparator			500		μs
V_{vconn_supply}	The voltage range of Vconn.	VSUPPLY = 5V	4.0		5.5	V
R_{vconn_switch}	The resistance of Vconn switch.	T = 25℃	10		55	Ω
I_{vconn_supply}	The current capability of Vconn befor it drops below 3.0V.	VSUPPLY = 5V	25		75	mA
PD						
Z_{Driver}	PD data Tx output impedance	Source output impedance at the Nyquist frequency of [USB 2.0] low speed (750 kHz) while the source is driving the CC line.	33		75	Ω
V_{Swing}	High level voltage Swing for CC PD data		1.05	1.125	1.2	V
V_{PD_LOW}	Low level voltage for CC PD data			0	0.2	V
T_{PD_RISING}	PD data rising time	Capacitance on CC1/CC2 pin <600pF	300			ns
$T_{PD_FALLING}$	PD data falling time	Capacitance on CC1/CC2 pin <600pF	300			ns
$T_{EndDriveBMC}$	Time to cease driving the line after the end of the last bit of the Frame.				23	μs

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$T_{HoldLowBMC}$	Time to cease driving the line after the final high-to-low transition.		1			μs
SYSTEM CLOCK						
$f_{HF_OSC_DIG}$	High frequence OSC on DDIE	VSUPPLY = 3.0V ~30V	46.56	48	49.44	MHz
$f_{LF_OSC_DIG}$	Low frequence OSC on DDIE		340	375	420	kHz
f_{OSC_ANA}	Major OSC frequency on ADIE	VSUPPLY = 3.0V ~30V	3.7	4	4.3	MHz
$f_{OSC_GREEN_ANA}$	Reduced OSC frequency on ADIE in Green Mode			32		kHz
THERMAL SHUTDOWN						
T_{TH}	Thermal shutdown threshold (LDO)	T_{TH} rising	130	145		℃
T_{TH_HYS}	Over temperature hysteresis	T_J falling below T_{TH} - T_{TH_HYS}, Sunny will restart.		15		℃

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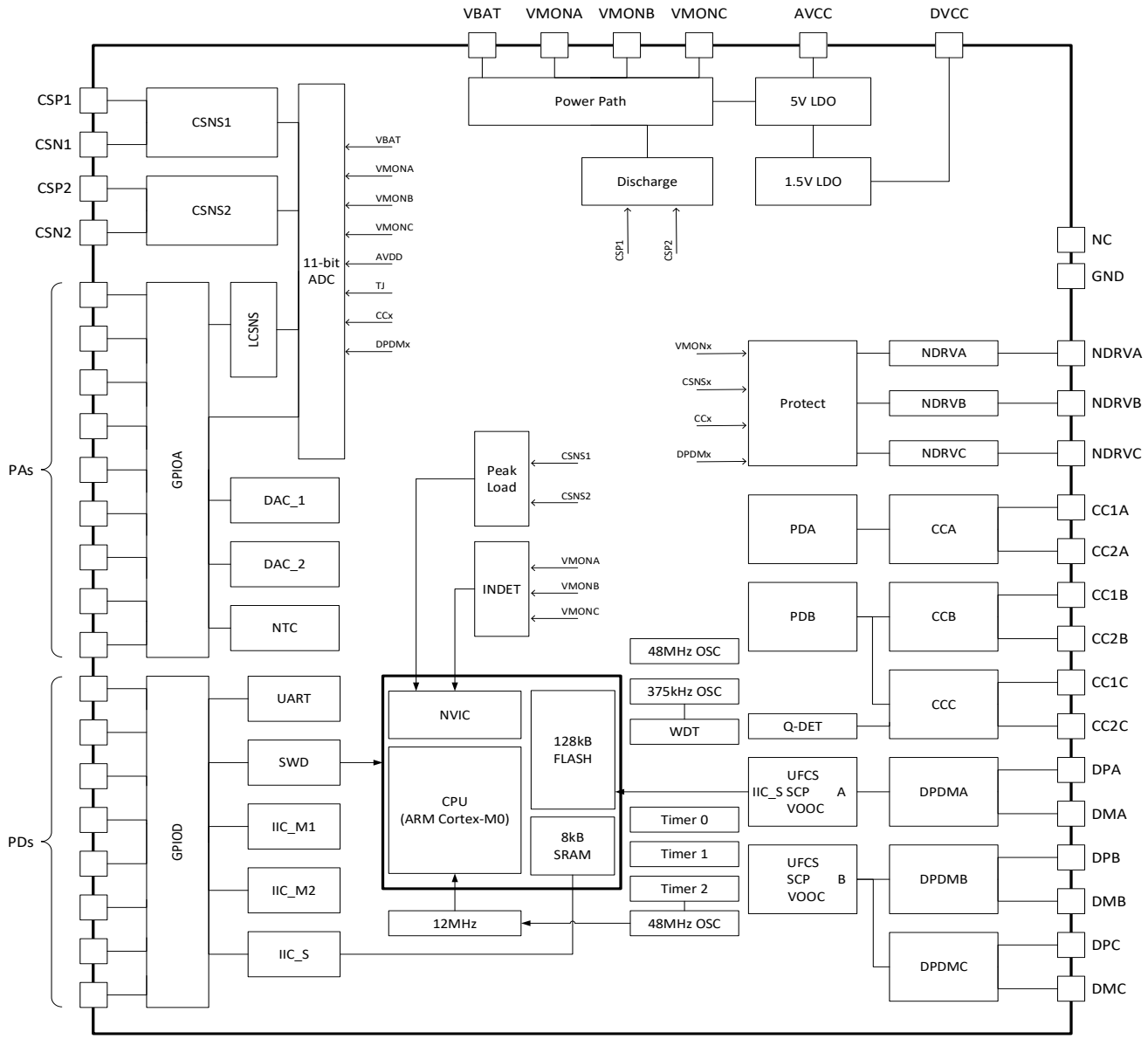
8 Functional Block Diagram



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9 Feature Description

9.1 Power Supply

The power supply pins for SC2006Q are VBAT, VMON_A, VMON_B, VMON_C.

The power supply voltage input range supports normal operation between 3.0V and 28V (falling to 2.7V).

The AVCC output voltage is 5.1V, used to provide bias for the analog circuit. The DVCC output voltage is 1.5V, used to provide bias for the digital circuit. Both the AVCC and DVCC pins require an external 1μF capacitor.

Additionally, for higher voltage or specialized applications, the SC2006Q supports independent 5V AVCC power supply. When AVCC power is enabled, the IC no longer draws power from VBAT & VMONx (register-controlled).

9.1.1 Power Supply Path Selection

When multiple power supplies are connected, the power drawing logic is as follows:

(1) All VMON pins are grouped together and powered from a high voltage via an internal diode circuit;

(2) When both VBAT and VMON_MAX are below 6V, power is sourced from the high voltage; when both are above 6V, power is sourced from the low voltage; when one is high and the other is low, power is sourced from the high voltage;

Additionally, the SC2006Q supports the Force VBUS feature, which, when enabled via software configuration, the power is fixed to be sourced from VBUS.

9.2 Lower Power Mode

9.2.1 Lower Power Mode Overview

To meet power consumption requirements in different scenarios, the SC2006Q supports 6 operating modes (including Active Mode), as detailed in the table below:

NO.	System Mode	Operational State Description	Power Consumption Level
0	Active mode	Description: All modules are functioning correctly. Entry sequence: Activated upon power-up. Exit sequence: Manually initiated via software configuration to transition to alternative modes.	<12mA
1	Standby Mode	Description: Analog modules operate normally; CPU halts. Entry Sequence: Software executes the WFI assembly instruction. Exit Sequence: Triggered by any qualified interrupt.	<8mA
2	Sleep Mode	Description: High-frequency clock disabled. Analog modules and low-speed digital modules operate normally. Entry Sequence: Configure `SLEEPDEEP` register + Software executes WFI instruction. Exit Sequence: Triggered by any low-frequency interrupt.	<3mA

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3	Green Mode	Description: High-frequency clock disabled. Analog and low-speed digital modules operate normally, but system frequency is further reduced to 32 kHz. Entry Sequence: Software configures system downclocking, then configures MCU for Sleep Mode entry. Exit Sequence: Triggered by any low-frequency interrupt.	<100μA
4	Suspend Mode	Description: Most system modules powered down completely. INDET insertion wake-up, VMON wake-up, and IO wake-up modules remain active. Entry Sequence: Software configures specific registers Exit Sequence: System wakes up and reboots upon trigger from any enabled wake-up source.	<50μA
5	Shipping Mode	Description: Most system modules powered down completely. VMON wake-up and IO wake-up modules remain active. Entry Sequence: Software configures specific registers Exit Sequence: System wakes up and reboots upon trigger from any enabled wake-up source.	<10μA

9.2.2 Transitions Between Low-Power Modes

(1) When an external device is inserted and the system requires rapid response to stimulus signals, transitions can occur between Level 0-2 modes .

(2) When no external device is inserted and further power reduction is required, either Level 3 or Level 4 mode (Green or Suspend) can be selected.

(3) Level 5 mode is recommended for battery-powered devices during initial production storage periods to minimize power consumption.

(4) Recommended practice for low-power software design: All low-power states should only transition from/to Active Mode. Avoid direct transitions between different low-power modes.

(5) One simplest implementation: Always remain in Active Mode during normal operation. Always use Sleep Mode during low-power standby states.

9.2.3 Wake-up Sources

The wake-up sources referenced in the various low-power modes are as follows:

a) Any Enabled Interrupt Source:

1.Activation: Always available when enabled for Standby Mode.

2.Function: Wakes the system from Standby Mode. All interrupt sources are described in detail in the MCU chapter.

b) Any Enabled Low-Frequency Interrupt Source:

1.Activation: Always available when enabled for Sleep Mode.

2.Function: Wakes the system from Sleep Mode. This refers to the subset of all interrupt sources that operate within the low-frequency clock domain.

c) VMON Power-On Detection:

1.Activation: Automatically enabled when AVCC is present and software configures entry into Suspend or Shipping Mode.

2.Function: Generates a wake-up signal if the voltage on any VMON input is higher than its UVLO threshold.

d) WAKEUP IO Edge Detection:

1.Activation: Automatically enabled when AVCC is present and software configures entry into Suspend or Shipping Mode.

2.Function: Upon activation, an internal pull-up resistor on the dedicated WAKEUP IO pin (PA0) is enabled. When WAKEUP IO is pulled low (e.g., by an external button press), the IC detects the falling edge and triggers a wake-up event.

e) VBUS/DPDM Insertion Detection:

1.Activation: Automatically enabled when AVCC is present and software configures entry into Suspend Mode (Note: Disabled in Shipping Mode). Requires software pre-enablement of the detection logic.

2.Function: Detects insertion events on the VBUS power source or USB D+/D- lines and generates a wake-up signal.

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9.2.4 Post-Wake Behavior

a) Wake from Standby, Sleep, or Green Mode:

The CPU resumes program execution from the exact instruction that initiated sleep entry. Register contents and SRAM data are preserved unchanged.

b) Wake from Suspend or Shipping Mode:

The entire system undergoes a full reboot. Program execution restarts from the initialization sequence.

9.3 System Clock

The SC2006Q integrates both a 375 kHz low-frequency clock and a 48MHz high-frequency clock.

a) The high-frequency clock operates normally only in Active Mode and Standby Mode.

b) During Green Mode operation, the system clock frequency is further reduced to 32 kHz.

9.4 MCU

The SC2006Q features an ARM Cortex-M0 core with SWD debug interface support. The core operates at a 12 MHz clock frequency.

9.4.1 NVIC

The interrupt vector table is listed below:

NO.	Interrupt	NO.	Interrupt
0	TIMER_0	16	GPIO
1	TIMER_1	17	Reserved
2	TIMER_2	18	Reserved
3	PWM	19	DPDMA
4	WDT	20	DPDMB
5	UART_0	21	DPDMC
6	UART_1	22	Reserved
7	UART_2	23	Reserved
8	IIC_ML	24	Reserved
9	Soft IIC 0	25	Reserved
10	Soft IIC 1	26	Reserved
11	PDA	27	Reserved
12	PDB	28	Reserved
13	AFCPA	29	Reserved
14	AFCPB	30	Reserved
15	IIC_S	31	Reserved

***Note: The ARM Cortex-M0 core does not support interrupt vector table offset.**

9.4.2 NVM & SRAM

FLASH:128kB memory. Address space: 0x0000_0000 - 0x0002_0000

SRAM:8kB memory. Address space: 0x2000_0000 - 0x2000_2000

9.4.3 Debug

a) Supports two-wire SWD debugging, programming

b) Supports instruction breakpoints and conditional breakpoints

9.4.4 Programming Interface

a) Default programming pin: DPDM_A

b) Can be reconfigured to GPIO through specific register settings

9.4.5 Boot Options

a) Boot from specific offset address in FLASH

b) Boot from specific offset address in SRAM

9.4.6 TIMER & ePWM

The SC2006Q integrates three general-purpose timers and one additional ePWM module with phase adjustment capability.

Timer Features:

a) Clock Source Selection:

Configurable between 48 MHz high-frequency clock or 375 kHz low-frequency clock.

b) Counting Operation:

Up-counting mode: Generates interrupt and auto-clears upon reaching configured overflow value.

c) Capture Function Configuration:

Trigger/end conditions selectable from:

1.Rising edge on DP

2.Falling edge on DP

3.Any edge on DP

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4.Rising edge on DM

5.Falling edge on DM

6.Any edge on DM

Capture Termination:

Ends upon end-condition detection or overflow. Generates interrupt and auto-disables capture until software re-enable.

Capture Initialization:

Hardware auto-clears capture counter and starts counting from 0 upon trigger condition detection.

ePWM Module Features:

1.Dual PWM outputs with independent configuration

2.Adjustable duty cycle, resolution (up to 16-bit), and phase shift

9.4.7 Watchdog

The SC2006Q integrates a watchdog timer supporting interrupt, wake-up, and reset functions.

Watchdog Features:

a) Generates interrupt, wake-up, or reset upon overflow. Clock source: Low-frequency clock.

b) Implements lock register preventing accidental writes. After unlocking, only one register write operation is permitted before automatic relocking.

9.4.8 UART

The SC2006Q integrates three UART modules (UART_0, UART_1, UART_2).

a) Pin Multiplexing:

UART_0: DPDM_A

UART_1: DPDM_B

UART_2: PDx pins only

b) Auto-Baud Detection:

Automatically calculates baud rate and updates configuration registers when enabled.

c) Auto-Baud Timeout:

Hardware timeout mechanism for baud rate detection.

d) RX Frame Timeout:

Hardware timeout for intra-frame data reception.

e) Automatic Inter-Byte Idle:

Configurable idle insertion (1.5byte duration) between consecutively transmitted bytes.

9.4.9 I²C Slave(I²C_S)

The SC2006Q integrates a hardware I²C slave controller. Default interface: DPDM_A (reconfigurable to PDx via registers).

I²C_S Features:

Address Configuration: Slave address software-programmable.

Speed Support: 40 kHz to 400 kHz operation.

Register Access: Direct APB bus peripheral register access via I²C writes.

SRAM Mapping: Direct access to dedicated SRAM memory regions.

9.4.10 Soft I²C

SC2006Q integrates two software IIC modules, which can be configured via software to perform master or slave functions and can be reused for GPIOD or DPDM. IICM_0 can be reused for DPDM_A or PDx, while IICM_1 can be reused for DPDM_B and PDx.

9.5 GPIO

The SC2006Q provides multiple general-purpose I/O banks organized into PDx and PAx groups with distinct multiplexing capabilities.

GPIO Features:

a) Output Modes:

Configurable as push-pull or pull-up/down outputs. Input comparators remain active regardless of output mode.

b) Edge-Triggered Interrupts:

Supports rising-edge, falling-edge, or dual-edge triggering. These interrupts can serve as system wake-up sources.

***Note: Available I/O count varies by package option across the SC2006Q product family.**

9.5.1 PDx

The PDx series GPIOs feature direct peripheral bus connection for ultra-fast interrupt response. During Suspend and Shipping modes, all PDx pins automatically switch to high-impedance state.

NO.	Function	SC2006Q

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PD_0	SWDIO	PIN_36
	GPIO	
	UART_TX1	
PD_1	SWCLK	PIN_37
	GPIO	
	UART_RX1	
PD_2	SDA_S1	PIN_38
	GPIO	
	UART_TX2	
PD_3	SCL_S1	PIN_39
	GPIO	
	UART_RX2	
PD_4	SDA_M1	PIN_40
	GPIO	
PD_5	SCL_M1	PIN_41
	GPIO	
PD_6	SDA_S2 / SDA_M2	PIN_42
	PWM_1	
	GPIO	
PD_7	SCL_S2 / SCL_M2	PIN_43
	PWM_2	
	GPIO	

***NOTE: SCL_S and SCL_M signals operate without priority arbitration. Both may function simultaneously when enabled.**

9.5.2 PAx

The PAx series GPIOs utilize indirect bus connectivity, resulting in slightly slower interrupt response compared to PDx pins. In suspend and shipping modes, PAx can maintain the configured high or low level.

NO.	Function	SC2006Q
PA_0	WAKEUP	PIN_3
	GPIO	
PA_1	NTC1	PIN_6
	ADC1	
	GPIO	
PA_2	NTC2	PIN_7
	ADC2	
	GPIO	
PA_3	DAC1	PIN_8
	FB1	
	GPIO	
PA_4	DAC2	PIN_9
	FB2	
	GPIO	
PA_5	FBS1	PIN_10
	ADC3	
	GPIO	
PA_6	FBS2	PIN_11
	ADC4	

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	GPIO	
PA_7	ADC5	PIN_34
	LCSNS1	
	GPIO	
PA_8	ADC6	PIN_35
	LCSNS2	
	GPIO	

9.6 Protection

SC2006Q integrates multiple hardware protection features. Upon triggering a specific protection action, the corresponding protective measure is automatically executed (register configurable), a corresponding protection flag is generated and the interrupt is triggered.

9.6.1 Vconn OCP

Over-current protection for the CC pin when configured as Vconn.

Triggering Condition: Triggered when Vconn current exceeds the protection threshold (rising edge), and resets when current falls below the threshold (falling edge).

Protection Action: Disables the corresponding Vconn;

9.6.2 VBUS OVP

Over-voltage protection for the CSP1/CSP2 pins.

Triggering Condition: Triggered when the CSP1/CSP2 voltage rises above the protection threshold; resets when the voltage falls below the threshold.

Protection Action: Disables the specified Load Switch (register 6bit controls 2×3 ports);

9.6.3 VBUS SCP

Short-circuit protection for CSNS1 & CSNS2 (applies only to discharge scenarios).

Trigger Condition: Voltage difference between CSPx and corresponding CSNx exceeds comparator threshold;

Protection Action: Disables the specified Load Switch (register 6bit controls 2×3 ports);

9.7 Liquid Presence Detection

SC2006Q supports liquid presence detection, SW1 connect a current source and several switches which connected CC1/CC2/DP/DM. SC2006Q can sense voltage between SW1 and CC1/CC2/DP/DM, thus can calculate the resistance of CC1/CC2/DP/DM to GND. ADC can be enabled even when SW1 is disable, then ADC can sense the voltage of CC1/CC2/DP/DM to check if there is a short circuit or liquid between VBUS and CC1/CC2/DP/DM. SW1 can be enabled by register.

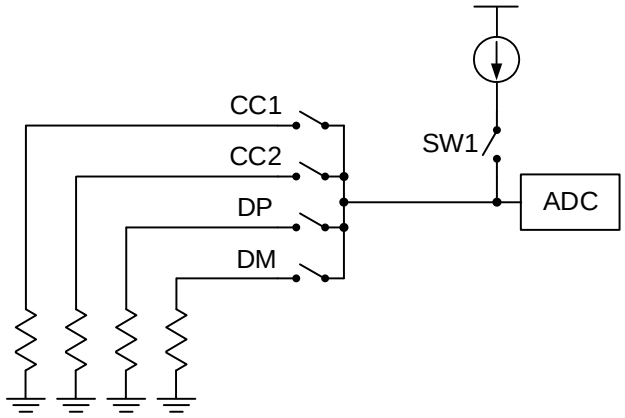

Figure 1 Liquid Detection Circuit

9.8 ADC

SC2006Q integrates an 11-bit ADC with 10kHz conversion rate. The internal reference can be selected between 2.253V and 1.024V, with 1 LSB being 1.1mV and 0.5mV respectively. The 1.024V reference is effective only during CSNSx channel sampling. All other channels use the 2.253V reference.

NO.	Channel	NO.	Channel
0	VBAT	16	DM_A
1	AVSS	17	DP_B
2	VCSP2	18	DM_B
3	AVDD	19	DP_C
4	VMON_B	20	DM_C
5	CC1_A	21	AD1 / NTC1

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6	VMON_A	22	AD2 / NTC2
7	CSNS_1	23	AD5
8	CSNS_2	24	AD6
9	VMON_C	25	AD7
10	CC2_A	26	AD8
11	CC1_B	27	LCSNS1
12	CC2_B	28	LCSNS2
13	CC1_C	29	Tj
14	CC2_C	30	VCSP1
15	DP_A	31	--

The sampling channels may be categorized into five groups based on their function:

High-voltage group: VBAT / VMONx / CSPx channels, featuring integrated voltage-dividing circuits.

Current group: CSNSx / LCSNSx channels, incorporating integrated operational amplifiers and capable of switching to a 1.024V reference range.

Channel group: CCx / DPDMx channels, incorporating 2x voltage-dividing circuits.

IO Group: Channels on NTCx /PAx.

Other: Tj channels acquire IC junction temperature, VDD channels acquire AVCC voltage signals.

9.8.1 Current Sense

The SC2006Q integrates two sets of high-side differential current sampling circuits, CSNS1 and CSNS2, with the sampling current direction configurable via register settings.

The circuit structure for the two high-side sampling channels is illustrated below:

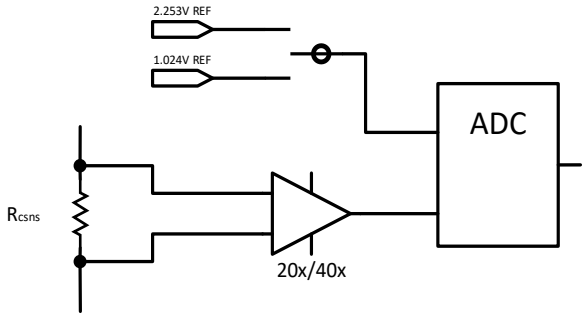

Figure 2 Current Sense Circuit

Following processing through a 20x/40x differential amplifier internally, the signal is input to the ADC.

When using a 2.253V reference(20x), the range is 0–112.65mV, with 1 LSB equating to 55μV; with a 5mΩ sampling resistor, the corresponding currents are 22.53A and 11mA respectively.

When using a 1.024V reference (20x), the measurement range is 0-51.2mV, with 1 LSB equating to 25μV. With a 5mΩ sense resistor, the corresponding currents are 10.24A and 5mA respectively.

9.8.2 CSPx/VMONx/VBAT

This group primarily concerns high-voltage sampling within the system. It comprises the following channels: VBAT, CSP_1, CSP_2, VMON_A, VMON_B, and VMON_C. It supports a voltage sampling range of 2V to 30V, with voltage divider ratios of 10:1 (sampling voltage range: 0-22.53V, 1 LSB = 11mV) and 14.5:1 (sampling voltage range: 0-32.67V, 1 LSB = 15.95mV). These are selectable via register configuration.

9.8.3 CCx/DPDMx

This section primarily concerns sampling within the system's signal pathways. The SC2006Q incorporates three CC groups and three DPDM groups. Both CC and DPDM feature a voltage divider ratio of 2:1 (sampling voltage range: 0–4.506 V, 1 LSB = 2.2 mV).

9.8.4 I/O

This section primarily concerns sampling of the PAx and NTC channels within the system. The SC2006Q incorporates two NTC pins (which may also be repurposed as ADCs) and four independent ADC pins. These ADC channels lack internal voltage dividers (sampling voltage range: 0–2.253V, 1 LSB = 1.1mV).

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9.8.5 Others

The Tj channel acquires IC junction temperature data with an error margin of approximately ±15°C, enabling temperature compensation for certain parameters where high precision is not required. The calculation formula is as follows:

$$T = \frac{code_{Tj} - \text{offset}_{0℃}}{14} * 5$$

Where offset0℃ may be set to a typical value of 500 in applications with less stringent temperature accuracy requirements. For scenarios demanding higher temperature precision, the specific offset value for each IC, pre-stored by the manufacturer, may be retrieved (using the software package provided by SOUTHCHIP). Under such circumstances, the calculated IC junction temperature can achieve an accuracy range of ±10℃.

The AVCC channel monitors the 5V LDO voltage, employing a 1/4 voltage divider. The DVCC channel is not monitored.

9.9 Analog Peripheral Control

9.9.1 NDRV

The SC2006Q integrates three sets of port NMOS load switch drivers, with the drive voltage referenced to the corresponding VMON.

The port load switches support the following two connection methods.

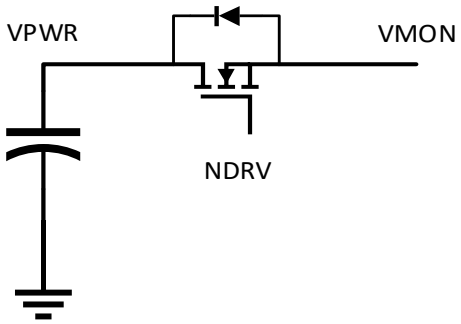

Figure 3 Single NMOS Connection

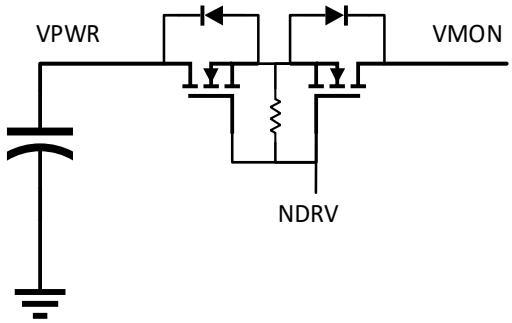

Figure 4 Back-to-Back NMOS Connection

When the load switch is activated, the SC2006Q supports a soft-start function. In practice, it accommodates two distinct NDRV drive capabilities: a low-current mode and a high-current mode. For applications requiring soft-start, the software controls the use of the low-current drive to charge Cgs. Once the MOS switch is fully turned on, it switches to the high-current drive mode. For applications not requiring soft-start, the high-current drive mode is used directly to turn on the MOS switch.

For single MOS applications, the SC2006Q also incorporates a software-controllable NDRV clamping function for VMON. This provides a rapid discharge path when the Vgs voltage differential becomes excessive, preventing load switch damage. (Note: When using back-to-back MOSFETs with a GS resistor, this protection function is not required for GS.)

Upon load switch deactivation, the default implementation employs a robust pull-down capability for swift MOS deactivation. Furthermore, to ensure VMON leakage to ground remains minimal during VGS clamping, this pull-down capability supports software configuration for a weaker pull-down mode.

9.9.2 Power Path Discharge Function

The SC2006Q integrates discharge circuits on both the CSPx and VMONx pins.

CSPx: Features a dual-stage discharge current source supporting 50mA (for EPR applications) and 100mA (for SPR applications).

VMONx: Integrates a 1kΩ discharge resistor to discharge port capacitance.

9.9.3 NTC

The SC2006Q includes an integrated NTC current source with three configurable output levels: 100μA, 20μA, and 4μA. This source can be multiplexed to pins PA1 and PA2,

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enabling time-multiplexed sampling of NTC resistors at two distinct physical locations.

9.9.4 DAC&FB

The SC2006Q integrates two 11-bit DACs with an output voltage range of 0V to 2.048V. It is employed to provide a voltage reference for external circuits.

Furthermore, this DAC can be paired with the FB pin / FBS pin to deliver a set of feedback control functions for buck converters. A typical buck control circuit is illustrated below:

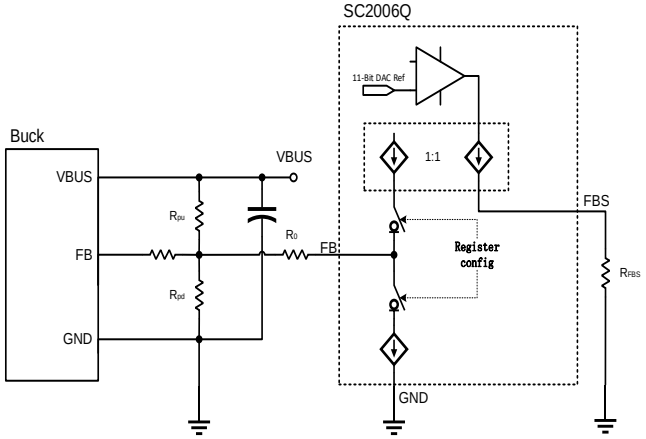

Figure 5 FB/FBS Illustration

The FBS pin incorporates an additional resistor to ground, providing a bias current reference I_{fbs}. An integrated bidirectional current mirror (register configuration) on the FB pin supports either source or sink current.

The relationship between the calculated VBUS voltage regulation value and the DAC setpoint is as follows:

$$VBUS = V_{fb} \cdot (1 + \frac{R_{pu}}{R_{pd}}) \pm V_{DAC} \cdot \frac{R_{pu}}{R_{fbs}}$$

It follows that the maximum voltage value VBUSmax, minimum voltage value VBUSmin, and default voltage value VBUSdef of the VBUS output are respectively:

$$VBUS_{max} = VBUS_{def} + V_{DAC,max} \cdot \frac{R_{pu}}{R_{fbs}}$$

$$VBUS_{min} = VBUS_{def} - V_{DAC,max} \cdot \frac{R_{pu}}{R_{fbs}}$$

$$VBUS_{def} = V_{fb} \cdot (1 + \frac{R_{pu}}{R_{pd}})$$

The voltage adjustment value VLSB for each step is:

$$V_{LSB} = V_{DAC,LSB} \cdot \frac{R_{pu}}{R_{fbs}}$$

where VDAC, LSB is a fixed value of 1mV.

The application of 30V and 20V is detailed in the table below

	20V Application		30V Application	
V_{LSB}	10mV		20mV	
R_{pu} / R_{fbs}	10		20	
V_{def}	5V		5V	
V_{range}	V_{def}±20.48V (0 - 25.48V)		V_{def}±40.96V (0 - 45.96V)	
R_{pu} / R_{pd}	V_{FB} = 0.6V	7.333	V_{FB} = 0.6V	7.333
	V_{FB} = 1.2V	3.167	V_{FB} = 1.2V	3.167

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Additionally, the DAC supports slope control with two configurable settings: 100μs/LSB and 20μs/LSB.

9.10 Fast Charging Protocol Interface

The SC2006Q supports bidirectional Source/Sink functionality on both its CC and DPDM pins. The device integrates three sets of CC PHYs and three sets of DPDM PHYs.

For fast charging protocols, it includes:

a) Two sets of PD PHYs (Power Delivery PHYs)

b) Two sets of DPDM fast charging protocol PHYs (supporting UFCS / SCP, etc.)

9.10.1 CC Module

Rp can be configured to three levels: 330μA, 180μA, and 80μA;

When the Type-C module is off, the passive Rd is automatically enabled. After the Type-C module is turned on, the active Rd can be enabled via software configuration. After being configured into the corresponding role, the digital enable register is activated, and the comparator continuously performs comparisons. When the current CC level changes (500μs glitch), the current CC state is marked based on the changed level, and a CC Change interrupt is reported.

When the CC Toggle function is enabled, the digital state machine automatically cycles between the configured Rp and Rd values. Upon detecting an attached state (Rd detecting Rp or Rp detecting Rd), the toggle sequence automatically stops and a CC Change interrupt is reported.

The CC Toggle timing can be software-configured with the following parameters:

Period: 55ms, 65ms, 75ms, 85ms, 95ms

Duty Cycle: 35%, 50%, 65%

9.10.2 DPDM Module

DPDM module implements all major market-proven proprietary protocols and UFCS (Universal Fast Charging Specification) and supports functional multiplexing for I²C, UART, GPIO, and other digital interfaces.

9.10.3 Thermal Shutdown (TSD)

TSD trigger temperature is 145°C (typical), hysteresis temperature is 20°C. After triggering, the LDO output automatically shuts down and the system stops working until the temperature returns to normal.

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10 Application Information

10.1 Capacitor Selection

VBAT, AVCC, and DVCC require 1μF capacitors placed close to the IC pins; where space permits, an additional 1μF capacitor may also be added near the VMONx pin close to the IC (port capacitors must still be retained).

10.2 CSNS RC Selection

Typically, RC or RCR filter circuits may be incorporated within the current sampling path to enhance the sampling circuit's immunity to interference and suppress switching noise. Due to the operational amplifier design of the SC2006Q, resistors of equal value must be connected in series across both CSP and CSN. Furthermore, as the CSPx pin integrates both voltage sampling and discharge functions, to prevent increased software processing complexity due to voltage drops introduced during discharge, it is recommended to filter only with a 1nF to 100nF capacitor in parallel between CSP and CSN, without adding additional series resistors.

10.3 NTC Resistor Selection

Typically, NTC resistors exhibit a slower rate of change at elevated temperatures. To ensure sufficient temperature detection accuracy under high-temperature conditions, NTC resistors with the highest possible resistance values should be selected. Furthermore, the SC2006Q incorporates three internally integrated current sources of differing magnitudes. Software-controlled switching between these current sources enables high detection accuracy across the entire temperature range.

10.4 Keypad Resistor Selection

PA0 incorporates an internal pull-up source, pull-up resistor, and falling-edge interrupt trigger, eliminating the need for an external pull-up source. External keypads may be connected via a single resistor to ground. To ensure correct key detection across all states, the total resistance between PA0 and ground must not exceed 1.1kΩ.

10.5 CC & DPDM RC Selection

To enhance the ESD capability of CC & DPDM and reduce coupling glitches between these signal pins, resistors may be series-connected on the lines and capacitance to ground added. The capacitor should be placed near the port, while the resistor should be positioned near the IC pin. The recommended resistor-capacitor combination is 33Ω+330pF, which may be adjusted according to project requirements.

Furthermore, the SC2006Q incorporates internal slope control for the PD BMC signal. The rise and fall rates required in eye diagram testing are unaffected by the external RC network values.

10.6 Considerations for HV Applications

VMONx incorporates internally integrated ESD devices with early turn-on capability to protect internal circuitry from electrostatic surges. These ESD components possess robust current handling capability, enabling rapid dissipation of static energy during momentary exposure to high voltages. Should the VMONx pin potentially remain exposed to DC voltages exceeding 32V for extended periods, a current-limiting resistor not exceeding 50Ω must be connected in series with the VMONx pin. This provides protection against overheating damage caused by excessive leakage current.

Furthermore, the IC's power supply originates from the LDO AVCC. When the input voltage is high, the LDO efficiency is relatively low. Continuing to use the SC2006Q to drive certain peripherals under these conditions will result in a significant increase in IC power consumption. In this scenario, an additional buck converter may be employed to supply the system's 5V domain devices. This power supply may be directly connected to the SC2006Q's AVCC pin, with software configuration directing the SC2006Q to draw power solely from AVCC. Consequently, the VBAT pin ceases to function as a power source and may instead be connected via a voltage divider resistor to the input voltage, serving as a high-voltage sampling point.

10.7 Processing of I²C

The SC2006Q integrates two software-controlled I²C masters (or slaves) alongside one hardware I²C slave. Both master configurations incorporate internal pull-up sources (the GPIO's inherent pull-up can be enabled in this mode), eliminating the need for external pull-ups. Should external pull-ups be employed, the internal pull-up can be disabled via software configuration.

Furthermore, the I²C slave supports direct access to data within a specific address space in SRAM (the range is defined by software configuration), significantly reducing communication overhead when operating as a slave.

The I²C high/low thresholds and pull-up/pull-down capabilities are consistent with the GPIO pins used.

10.8 DPDM Used as GPIO

In certain applications, the number of GPIO pins may be insufficient, necessitating the reuse of DPDM's GPIO

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functionality. Note that while DPDM also offers pull-up/pull-down output modes and level triggering like standard I/O, its pull-up capability aligns with the DPDM protocol itself, operating at 3.3V—distinct from the GPIO's 5V.

10.9 Driving LEDs and 188-Digit Displays

The PDx series GPIO offers faster processing speeds compared to the PAx series. When driving LEDs or 188-segment displays via scanning, prioritising PDx series GPIOs is recommended to reduce software processing load.

Furthermore, these GPIOs possess current capabilities exceeding 5mA (total not exceeding AVCC's inherent capacity), enabling direct driving of LEDs or 188-segment displays.

10.10 NDRV Circuit Selection

The NDRV pin supports either a single N-MOSFET or back-to-back N-MOSFETs. For Type-C ports, certification considerations necessitate employing back-to-back N-MOSFETs as port load switches. To mitigate the risk of MOSFET drain-source over-voltage during abnormal operating conditions, it is advisable to configure the source terminals inward and incorporate a gate-source (GS) resistor (as illustrated in Figure 3). The GS resistor should be rated at 500kΩ or higher.

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11 Layout Guide

1. Use Kelvin connections to sense resistors for the current sense signals CSP and CSN and run lines in parallel from the Rsense terminals to the IC pins.Place the filter capacitor for the current sense signal as close to the IC pins as possible.

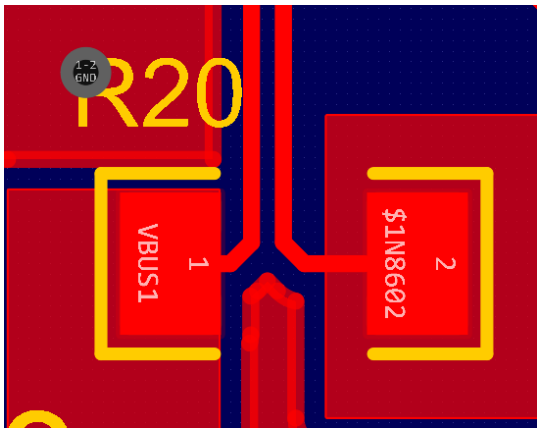

Figure 6 High-Side Current Sense

2. The 1uF capacitors connected at VBAT/AVCC/DVCC pins should be placed near the IC. Where space permits, a 1μF capacitor may also be placed near the pins on the VMONx.

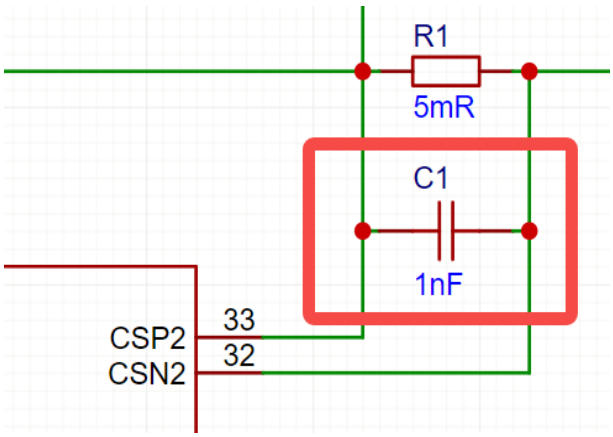

Figure 7 Filter Capacitor

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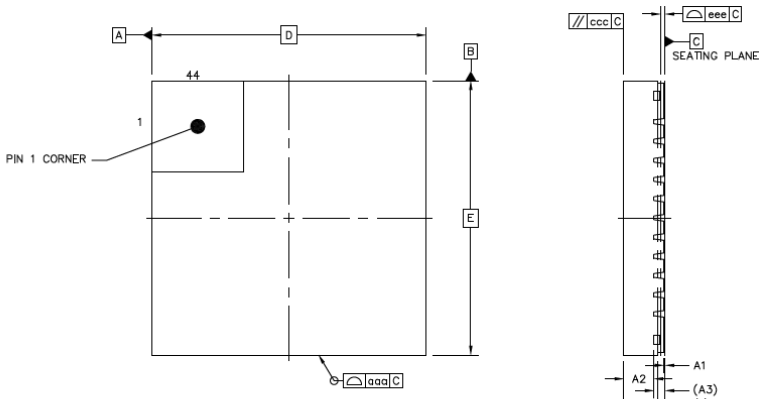
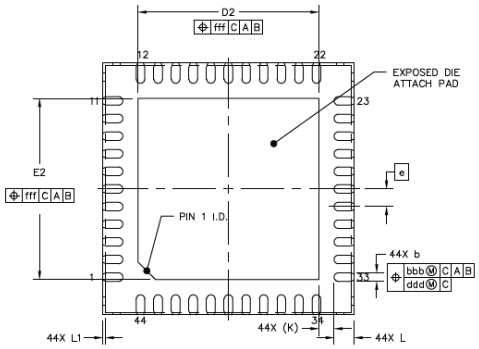
MECHANICAL DATA

QFN-44(5×5)





BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.1	---	0.18
LEAD WIDTH		b	0.12	0.17	0.22
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	3.5	3.6	3.7
	Y	E2	3.5	3.6	3.7
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	

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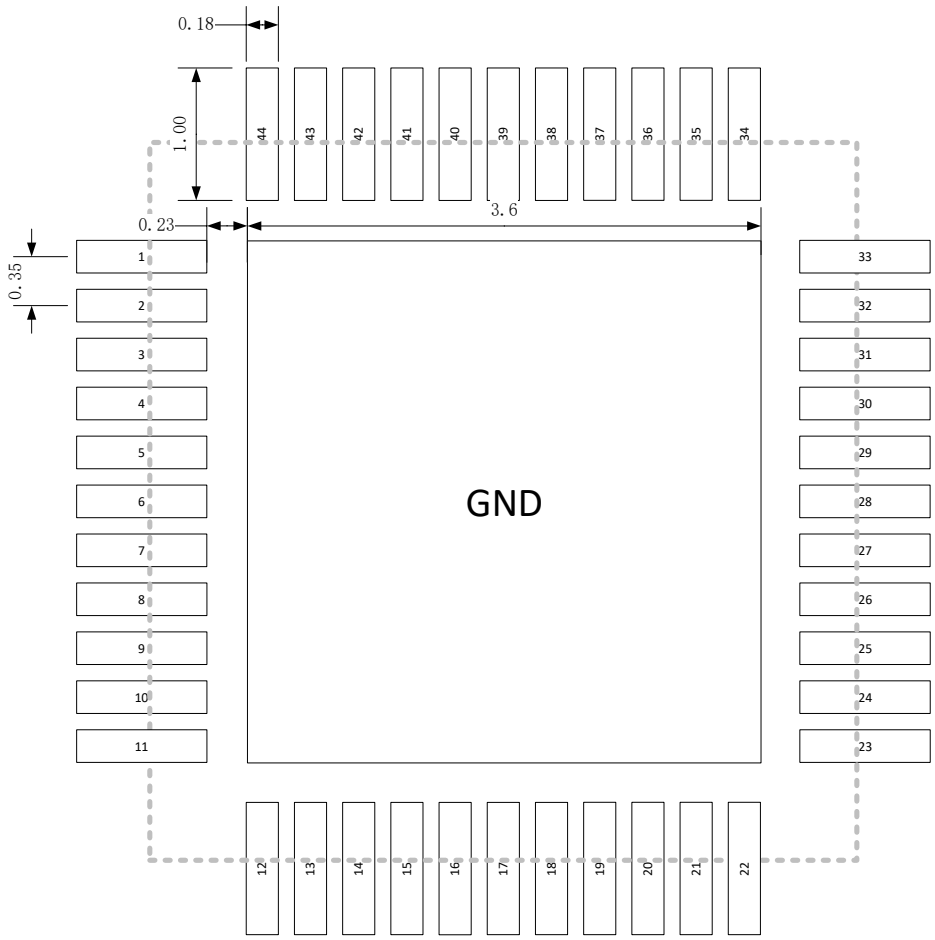
RECOMMENDED FOOTPRINT



UNIT:mm

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