

2-Cell High Efficiency 10-A Switched Capacitor Direct Charger

1 Descriptions

SC8571 is a 98.5% efficiency, 10-A battery charging solution using a switched cap architecture. The switched cap architecture and the integrated FETs are optimized to enable a 50% cycle, allowing the cable current to be half the current delivered to the battery, reducing the losses over the charging cable as well as limiting the temperature rise in the application.

SC8571 adopts 80pin CSP 3.425mm X 4.151mm package

2 Applications

- Smartphones
- Tablet PCs

3 Device Information

Part Number	Package	Dimension
SC8571CFFR	CSP (80)	3.425mm x 4.151mm

4 Features

- Dual-phase charger pump
 - ✓ 10-A output current capability
 - ✓ Up to 98.5% efficiency
 - ✓ Up to 12-A charging current for parallel charging with dual synchronized SC8571
- 5-way switched cap switch protection
 - ✓ VBUS2OUT_ERRORHI protection before switching
 - ✓ VBUS2OUT_ERRORLO protection before switching
 - ✓ CFLY short protection before switching
 - ✓ VPMD2OUT_OVP during switching
 - ✓ VPMD2OUT_UVP during switching
- 11-way system protection
 - ✓ VAC1_OVP
 - ✓ VAC2_OVP
 - ✓ VBUS_OVP
 - ✓ IBUS_OCP
 - ✓ IBUS_UCP
 - ✓ VOUT_OVP
 - ✓ VBAT_OVP
 - ✓ IBAT_OCP
 - ✓ TSBUS_FLT
 - ✓ TSBAT_FLT
 - ✓ TSHUT
- 5-way system alarm
 - ✓ VBUS_OVP_ALM
 - ✓ VBAT_OVP_ALM
 - ✓ IBAT_OCP_ALM
 - ✓ TSBUS_TSBAT_ALM
 - ✓ TDIE_ALM
- 10-channel 12-bit ADC
 - ✓ VAC1, VAC2, VBUS, IBUS, VOUT, VBAT, IBAT, TSBUS, TSBAT, TDIE



5 Typical Application Circuit

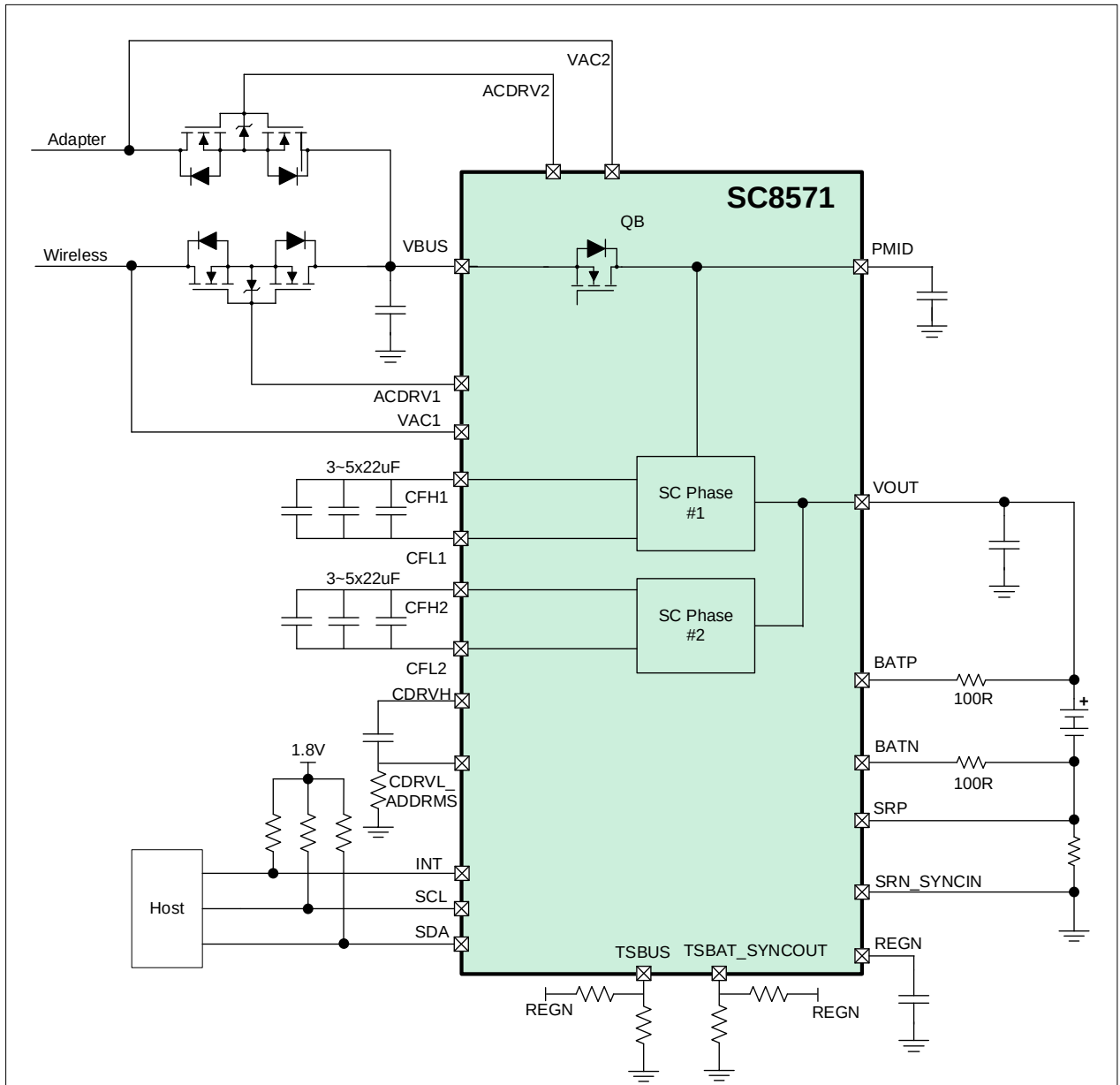
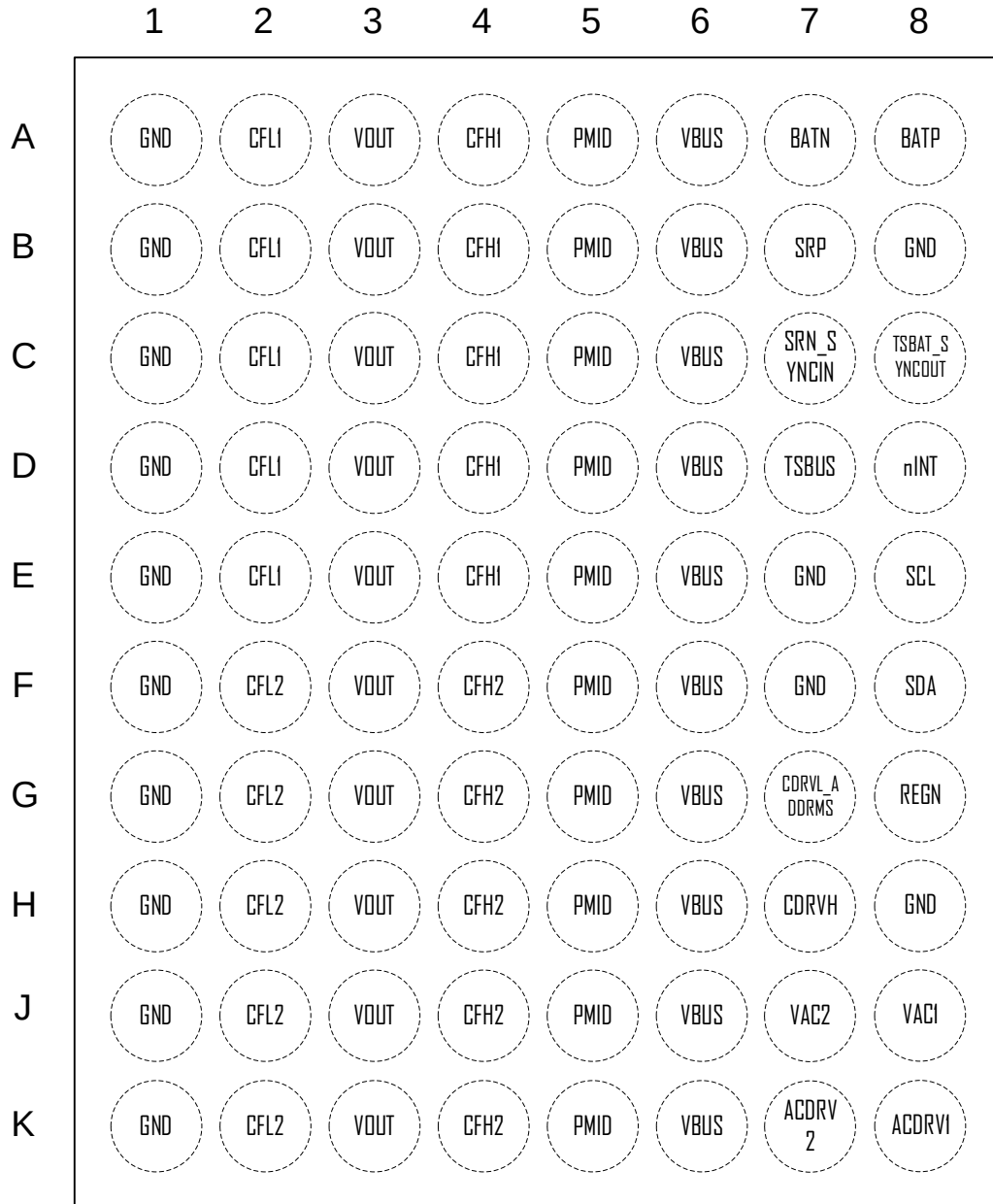


Fig 1. SC8571 typical application



6 Terminal Configuration and Functions

SC8571



(Top View)

Fig 2. SC8571 Pin Out



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
A1, B1, C1, D1, E1, F1, G1, H1, J1, K1, B8, E7, F7, H8	PGND	Power	Power ground
A2, B2, C2, D2, E2	CFL1	Power	Bottom plate of flying cap C1. Connect 3~5 pieces 22uF caps in parallel between this pin and CFH1
F2, G2, H2, J2, K2	CFL2	Power	Bottom plate of flying cap C2. Connect 3~5 pieces 22uF caps in parallel between this pin and CFH2
A3, B3, C3, D3, E3, F3, G3, H3, J3, K3	VOUT	Power	Device power output. Connect a 10μF capacitor between this pin and PGND
A4, B4, C4, D4, E4	CFH1	Power	Top plate of flying cap C1. Connect 3~5 pieces 22uF caps in parallel between this pin and CFL1
F4, G4, H4, J4, K4	CFH2	Power	Top plate of flying cap C2. Connect 3~5 pieces 22uF caps in parallel between this pin and CFL2
A5, B5, C5, D5, E5, F5, G5, H5, J5, K5	PMID	Power	The input to the switched cap power stage. Connect a 10μF cap between this pin to PGND as close to device as possible
A6, B6, C6, D6, E6, F6, G6, H6, J6, K6	VBUS	Power	Device power input. Place a 10μF cap to PGND as close to device as possible
A7	BATN	I	Negative input for battery voltage sensing. Connect to negative terminal of battery pack. Place 100Ω series resistance between BATN and battery pack negative terminal
A8	BATP	I	Positive input for battery voltage sensing. Connect to positive terminal of battery pack. Place 100Ω series resistance between BATP and battery pack positive terminal
B7	SRP	I	Positive input for low side battery current sensing. Place sense resistor between SRN_SYNCIN and SRP. Short SRN_SYNCIN and SRP together to GND if not used or in Slave mode.
C7	SRN_SYNCIN	I	Negative input for low side battery current sensing. Place sense resistor between SRN_SYNCIN and SRP. Short SRN_SYNCIN and SRP together to GND if not used. If configured as Slave for parallel operation, this pin functions as SYNCIN, and connect to TSBAT_SYNCOUT of Master.
D7	TSBUS	I	BUS temperature sense pin. Needs external resistor divider, NTC and voltage reference



G7	CDRVL_ADDRMS	Power	Bootstrap capacitor for gate driver. Connect 0.22uF cap between CDRVH and CRLV_ADDRMS. During Power On Reset (POR), this pin is used to assign the address of the device and the mode of the device as Standalone, Master or Slave.
H7	CDRVH	Power	Bootstrap capacitor for gate driver. Connect 0.22uF cap between CDRVH and CRLV_ADDRMS.
J7	VAC2	I	VAC2 Input voltage sense pin. Connect to VBUS if ACFET2 and RBFET2 are not used
K7	ACDRV2	Power	Input FETs driver pin 2. The switched cap output to drive the port #2 input N-channel MOSFET (ACFET2) and reverse blocking N-channel MOSFET (RBFET2). ACDRV2 voltage becomes 5 V above the common source connection of the ACFET2 and RBFET2, when the turn-on condition is met. If ACFET2 and RBFET2 are not used, connect ACDRV2 to ground.
C8	TSBAT_SYNCOUT	I/O	Battery temperature voltage input and Master mode SYNCOUT. Needs external resistor divider, NTC and voltage reference. If the device is in Master mode, connect this pin to SRN_SYNCIN of the Slave device.
D8	nINT	O	Active low interrupt output. Open drain connection, needs to pull up to voltage reference with 10-kΩ series resistor.
E8	SCL	I/O	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ). The IC works as a slave.
F8	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ)
G8	REGN	O	Internal LDO output. Connect a 4.7-μF cap between this pin and GND.
J8	VAC1	I	VAC1 Input voltage sense pin. Connect to VBUS if ACFET1 and RBFET1 are not used
K8	ACDRV1	Power	Input FETs driver pin 1. The switched cap output to drive the port #1 input N-channel MOSFET (ACFET1) and reverse blocking N-channel MOSFET (RBFET1). ACDRV1 voltage becomes 5 V above the common source connection of the ACFET1 and RBFET1, when the turn-on condition is met. If ACFET1 and RBFET1 are not used, connect ACDRV1 to ground.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VAC1, VAC2 (converter not switching)	-0.3	36	V
	ACDRV1, ACDRV2	-0.3	30	V
	VBUS (converter not switching)	-0.3	28	V
	PMID (converter not switching)	-0.3	28	V
	PMID-VBUS (QB)	-0.3	11	V
	PMID to CFH1/CFH2	-0.3	26	V
	CFH1/CFH2 to VOUT	-0.3	11	V
	VOUT to CFL1, VOUT to CFL2	-0.3	11	V
	CFL1/CFL2 to GND	-0.3	11	V
	VOUT to PGND	-0.3	11	V
	CDRVH	-0.3	28	V
	BATP	-0.3	11	V
	SRP	-0.3	6	V
	SCL, SDA, nINT, CDRVL_ADDRMS, REGN, BATN, SRN_SYNCIN, TSBAT_SYNCOUT, TSBUS	-0.3	6	V
	BATP-BATN	-0.3	11	V
	SRP-SRN_SYNCIN	-0.3	0.3	V
Current Range	DC output current (VOUT)	8		A
Temperature Range	Operating Junction, T _j	-40	125	°C
	Storage temperature range, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2000	2000	V
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

**7.3 Recommended Operating Conditions**

		MIN	TYP	MAX	UNIT
Voltage	VAC1/VAC2			22	V
	VBUS			22	V
	PMID			22	
	VOUT			10	V
	CFH1-VOUT, CFH2-VOUT, CFL1, CFL2			10	V
C _{fly}	Flying capacitor	20			μF
C _{iin}	Input capacitor	5			μF
C _{out}	Output capacitor	5			μF
T _A	Operating ambient temperature	-40		85	°C
T _J	Operating junction temperature	-40		125	°C



7.4 Electrical Characteristic

$V_{BUS} = 20V$, $V_{OUT}=4.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$ for minimum and maximum specifications, and $T_A = 25^{\circ}C$ for typical specifications, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current						
I _{Q_VAC}	VAC quiescent current	ADC disabled, charger disabled, VOUT not present. Measure quiescent current on VAC1 or VAC2, VACDRV1 and VACDRV2 disabled, VAC=20V		710		μA
		ADC disabled, charger disabled, VOUT not present. Measure quiescent current on VAC1 or VAC2, VACDRV1 and VACDRV2 enabled, VAC=20V		1100		μA
I _{Q_VOUT}	VOUT quiescent current	ADC disabled, charger disabled, VAC1 and VAC2 not present. Measure quiescent current on VOUT, VOUT=10V		20		μA
		ADC enabled, charger disabled, VAC1 and VAC2 not present. Measure quiescent current on VOUT, VOUT=10V		890		μA
Resistances						
R _{QB_ON}	QB on resistance			3		mΩ
R _{Q1A/Q1B_ON}	On resistance of Q1A/Q1B			10		mΩ
R _{Q2A/Q2B_ON}	On resistance of Q2A/Q2B			8		mΩ
R _{Q3A/Q3B_ON}	On resistance of Q3A/Q3B			6		mΩ
R _{Q4A/Q4B_ON}	On resistance of Q4A/Q4B			6		mΩ
R _{VBUS_PD}	VBUS pull-down resistance			4		kΩ
R _{PMID_PD}	PMID pull-down resistance			2		kΩ
R _{VAC_PD}	VAC pull-down resistance			100		Ω
Internal threshold						
V _{VAC1_UVLO}	VAC1 rising threshold for active I2C, no battery. Also, for enable VACDRV1	Rising threshold		3.9	4.3	V
		Falling hysteresis		220		mV
V _{VAC2_UVLO}	VAC2 rising threshold for active I2C, no battery. Also, for enable VACDRV2	Rising threshold		3.9	4.3	V
		Falling hysteresis		220		mV
V _{BUS_PRESENT}	VBUS present status will be set to ‘1’ and I2C starts working once VBUS voltage is above this threshold	Rising threshold		3	3.3	V
		Falling hysteresis		100		mV
V _{BUS_TH_CHG_EN}	VBUS-VOUT threshold to allow user to set CHG_EN=1	Rising threshold		-0.05*V _{OUT}		V
		Falling threshold		-0.07*V _{OUT}		V



V _{OUT_UVLO}	VOUT for active I2C, no adapter	Rising threshold	3.5	3.7	V
		Falling hysteresis	200		mV
V _{OUT_OK_CHG}	Minimum VOUT threshold to allow user set CHG_EN=1	Rising threshold	5.8	6	6.2
		Falling hysteresis	200		mV
V _{OUT_TH_SW_REG} N	The internal VCC will draw current from VOUT instead of VAC1 or VAC2 when VOUT rises above this threshold in charger mode.	Rising threshold	3.2	3.3	3.4
		Falling hysteresis	150		mV
Input over-voltage protection and alarm					
V _{AC1_OVP}	Rising threshold		6.5	24	V
	Step size		2.5		V
	Falling hysteresis		490		mV
	Comparator accuracy	Accuracy for 6.5V	-2%	2%	
	Comparator accuracy	Accuracy for 11.5V through 24V	-2%	2%	
V _{AC2_OVP}	Rising threshold		6.5	24	V
	Step size		2.5		V
	Falling hysteresis		490		mV
	Comparator accuracy	Accuracy for 6.5V	-2%	2%	
	Comparator accuracy	Accuracy for 11.5V through 25V	-2%	2%	
V _{BUS_OVP}	Forward 2:1 mode	Rising threshold	14	26.7	V
		Step size	100		mV
		Accuracy, VBUS=22V	-2%	2%	
	Forward 1:1 mode	Rising threshold	7	13.35	V
		Step size	50		mV
		Accuracy, VBUS=11V	-1%	1%	
V _{BUS_OVP_ALM}	Forward 2:1 Mode	Rising threshold	14	26.7	V
		Step Size	100		mV
		Hysteresis	150		mV
		Accuracy	-2%	2%	mV
	Forward 1:1 Mode	Rising threshold	7	13.35	V
		Step Size	50		mV
		Hysteresis	75		mV
		Accuracy	-1%	1%	
Output over-voltage protection and alarm					
V _{OUT_OVP}	Rising threshold		9.4	10	V
	Step size		200		mV
	Comparator accuracy	VOUT=10V	-1%	1%	
V _{BAT_OVP}	Rising threshold		7	9.54	V



	Step size		20	mV
	Comparator accuracy	VBAT=8.8V	-0.5% 0.5%	
V _{BAT_OVP_ALM}	Rising threshold		7 9.54	V
	Step size		20	mV
	Hysteresis	Falling	81	mV
	Comparator accuracy	From VBAT=7V to 8.8V	-0.5% 0.5%	
Vbus in-range protection				
V _{BUS2OUT_ERROR_HI}	Rising threshold for switched cap stops switching	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.166*V _{OUT}	V
	Falling threshold for switched cap starts switching	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.133*V _{OUT}	V
V _{BUS2OUT_ERROR_LO}	Rising threshold for switched cap starts switching	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0*V _{OUT}	V
	Falling threshold for switched cap stops switching	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	-0.03*V _{OUT}	V
Input short protection				
V _{PMID2OUT_UVP}	Over V _{PMID} /2-V _{OUT} in 2:1 charger mode or Over V _{PMID} -V _{OUT} in 1:1 charger mode	Falling threshold Adjustable in register 0x42h	-275 -100	mV
	Step size		-25	mV
	Hysteresis	Rising	50	mV
	Comparator accuracy		-50 50	mV
Output short protection				
V _{PMID2OUT_OVP}	Over V _{PMID} /2-V _{OUT} in 2:1 charger mode or Over V _{PMID} -V _{OUT} in 1:1 charger mode	Rising threshold Adjustable in register 0x42h	50 200 400	mV
	Step size		50	mV
	Hysteresis	Falling	50	mV
	Comparator accuracy		-50 50	mV
Input current protection				



I _{BUS_OCP}	Rising threshold	2:1 Mode	1	8	A
		1:1 Mode	1	8	A
	Step size		250		mA
	Comparator accuracy	IBUS=3A, T _A = -20°C to +85°C	-5%	5%	
I _{BUS_UCP_RISING}	Rising threshold	Adjustable in register 0x05h, bit[6]=0	300	500	mA
		Adjustable in register 0x05h, bit[6]=1	500	750	mA
I _{BUS_UCP_FALLING}	Falling threshold	Adjustable in register 0x05h, bit[6]=0	10	150	mA
		Adjustable in register 0x05h, bit[6]=1	128	250	mA
Output over-current protection and alarm					
I _{BAT_OCP}	Rising threshold		0	12.7	A
	Step size		100		mA
	Comparator accuracy	IBAT=6A	-5%	5%	
I _{BAT_OCP_ALM}	Rising threshold		0	12.7	A
	Step size		100		mA
	Hysteresis		100		mA
	Comparator accuracy		-5%	5%	
Over temperature protection					
T _{BUS_FLT}	Rising Threshold of REGN		0%	50%	
	Step size		0.1953%		
	Comparator accuracy	TSBUS_FLT=4.1%	-2%	2%	
T _{BAT_FLT}	Rising Threshold of REGN		0%	50%	
	Step size		0.1953%		
	Comparator accuracy	TSBAT_FLT=4.1%	-2%	2%	
T _{SHUT}	Rising threshold		150		°C
T _{DIE_ALM}	Rising Threshold		30	125	150
	Step size		0.5		°C
Timers					
f _{SW}	Switching frequency	Programmable range	300	500	750
t _{VAC_ON_DG}	Deglitch time between VAC over VAC_UVLO and turn on external MOS when VOUT is already present		20		ms
	Deglitch time between VAC over VAC_UVLO and turn on		320		ms



	external MOS when VOUT is not present			
t _{VAC_OVP}	VAC OVP reaction time	VAC rising slew rate>10V/us	0.2	μs
t _{VAC_PD}	VAC Pull-down time		400	ms
t _{VBUS_IN_RANGE}	Minimum VBUS in-range duration before switched cap start switching	VBUS slow UVP/OVP	20	ms
t _{VBUS_OVP}	VBUS OVP reaction time		1	μs
t _{IBUS_OCP}	IBUS OCP reaction time		75	μs
t _{IBUS_UCP_FALLING}	IBUS UCP falling reaction time	Adjustable in register 0x11h	0.01 150	ms
t _{VBUS_PD}	VBUS pull-down time before turn on ACDRV		20	ms
t _{VPID2OUT_OVP}	VPID/2-VOUT OVP reaction time or VPID-VOUT OVP reaction time		0.1	μs
t _{VPID2OUT_UVP}	VPID/2-VOUT UVP reaction time or VPID-VOUT UVP reaction time		0.1	μs
t _{VOUT_OVP}	VOUT OVP reaction time		1	μs
t _{VBAT_OVP}	VBAT OVP reaction time		0.1	μs
t _{IBAT_OCP}	IBAT OCP reaction time		500	μs
t _{SS_TIMEOUT}	Soft start timeout	Adjustable in register 0x11h	6.5m 13	s
t _{WD_TIMEOUT}	Watchdog timeout	Adjustable in register 0x10h	0.65 39	s
t _{INT_LOW}	During that INT is pulled low when an event occurs		256	μs
t _{INT_HIGH}	Minimum high level time after an INT low event		256	μs
REGN LDO				
V _{REGN}	REGN LDO output voltage	VBUS=16V	5	V
I _{REGN}	REGN LDO current limit	VBUS=16V	50	mA
Logic Input (SRN_SYNCIN)				
V _{IH_SRN_SYNCIN}	Input high threshold level		1.35	V
V _{IL_SRN_SYNCIN}	Input low threshold level		0.4	V
I _{LEAKAGE}	High level leakage current	Pull up to 1.8V	1	μA



Logic Output (nINT, TSBAT_SYNCOUT)				
V _{OL}	Output low voltage	I _{OL} =1mA, V _{PULL_UP} =1.8V	0.4	V
I _{OL}	Output low leakage current	Pull up rail 1.8V	1	μA
I2C Interface (SCL & SDA)				
F _{SCL}	Serial-clock frequency		1000	kHz
V _{IH}	Input logic high		0.9	V
V _{IL}	Input logic low		0.37	V
I _{LEAKAGE}	Input leakage current		1	μA
ADC MEASUREMENT				
IBUS_ADC	Range		0 10.24	A
	LSB		2.5	mA
	Accuracy	IBUS=3A	-5% 5%	
VBUS_ADC	Range		0 25.6	V
	LSB		6.25	mV
	Accuracy	VBUS=20V	-1% 1%	
VAC1_ADC	Range		0 25.6	V
	LSB		6.25	mV
	Accuracy	VUSB=20V	-1% 1%	
VAC2_ADC	Range		0 25.6	V
	LSB		6.25	mV
	Accuracy	VUSB=20V	-1% 1%	
VOUT_ADC	Range		0 10.24	V
	LSB		2.5	mV
	Accuracy	VOUT=10V	-1% 1%	
VBAT_ADC	Range		0 10.24	V
	LSB		2.5	mV
	Accuracy	VBAT=9V	-0.5% 0.5%	
IBAT_ADC	Range		0 12.8	A
	LSB		3.125	mA
	Accuracy	IBAT=6A with 2mΩ R _{SENSE}	-1.5% 1.5%	
TSBUS_ADC	ADC TSBUS pin voltage	Range	0.2 2.7	V
	ADC TSBUS percentage of REGN readable in registers 0x34h and 0x35h	Range	0 50	%
		LSB	0.09766	%
	Accuracy	TSBUS pin voltage 2V	-1 1	%
TSBAT_ADC	ADC TSBAT pin voltage	Range	0.2 2.7	V
		Range	0 50	%



	ADC TSBAT percentage of REGN readable in registers 0x36h and 0x37h	LSB	0.09766	%
	Accuracy	TSBAT pin voltage 2V	-1 1	%
TDIE_ADC	ADC Die temperature readable in registers 0x38h	Range	0 150	°C
		LSB	0.5	°C
	Accuracy		± 4	°C

8 Function Block Diagram

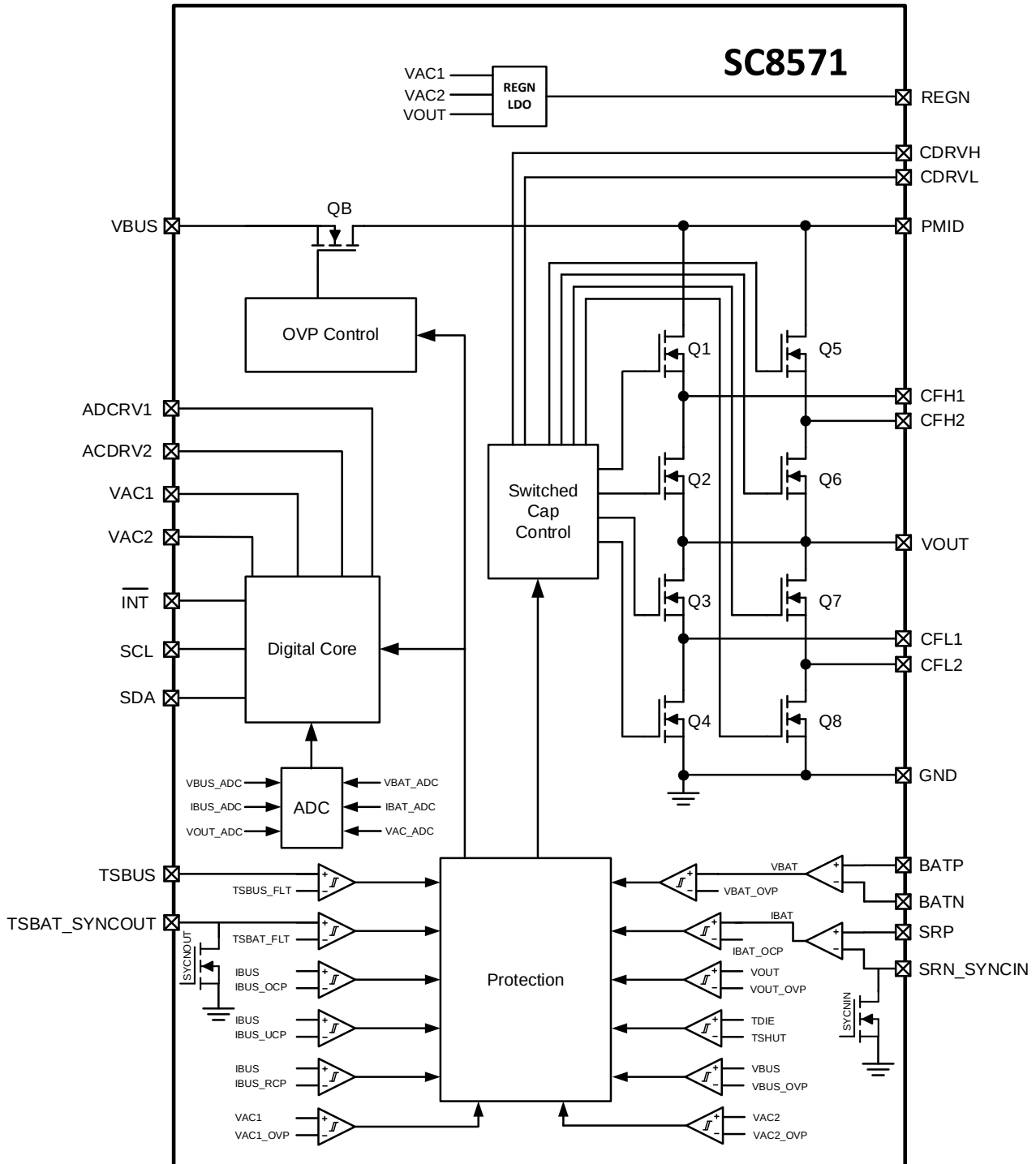


Fig 3. SC8571 simplified function block diagram

9 Detailed Description

9.1 Overview

SC8571 is a high efficiency 4:2 fast charger for 2-cell Li-ion or Li-polymer battery. The device integrates a dual phase switched-cap converter with a reverse blocking MOSFET (QB). By configuring the mode register, the power stage can work in different modes, like 4:2 or 2:2 charging. QB is controlled by CP_EN bit in forward charger mode.

9.2 Device Power Up

The device is powered from the highest among VAC1, VAC2 or VOUT. The voltage must be greater than the V_{VAC1_UVLO} , V_{VAC2_UVLO} or V_{OUT_UVLO} threshold to be a valid supply. When only VOUT is above V_{OUT_UVLO} , the device enters bat-only modes, in which device consumes the least power. When VAC1 rises above V_{AC1_UVLO} or VAC2 rises above V_{AC2_UVLO} , I2C interface is activated and ready for communication and all registers are reset to their default values. To enable charging, the host needs to wait VBUS_TH_CHG_EN_STAT and VOUT_OK_CHG_STAT go high before setting CP_EN=1.

9.3 Operation Modes

9.3.1 Charging Mode

Prior to enable the switched cap (CHG_EN=1), set all the protections to the desired threshold and the VBUS voltage must be between VBUS2OUT_ERRORLO and VBUS2OUT_ERRORHI. After reading VOUT_OK_CHG_STAT and VBUS_TH_CHG_EN_STAT=1, host can set CHG_EN=1. This VBUS in-range protection is only effective during the power-up. Once the switched cap has already been enabled, the VBUS in-range protection will be disabled. VBUS over-voltage will be protected by VBUS_OVP, IBUS_OCP, while VBUS under-voltage will be protection by IBUS_UCP.

During the start-up, IBUS must reach the rising threshold before the SS timeout. IBUS_UCP and IBUS_UCP_ALM are disabled until IBUS reaches the rising threshold

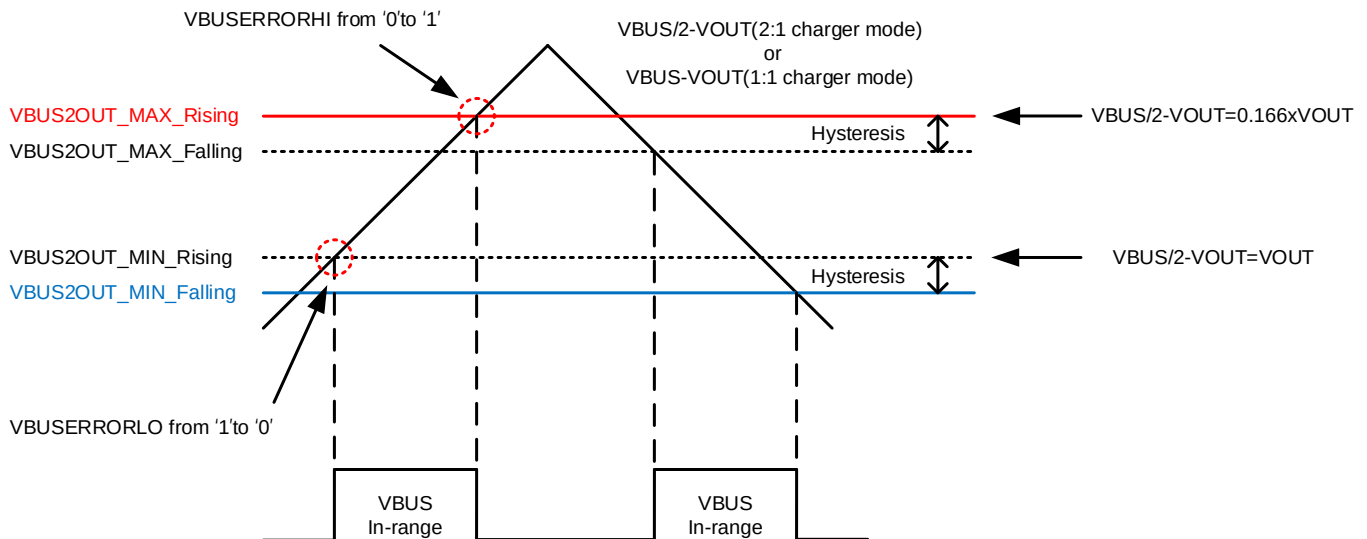


Fig 4. VBUS in-range detection for enabling charging

**9.3.2 OTG Mode**

To enter OTG mode, the host should follow the steps below:

1. Host writes ACDRV_MANUAL_EN=1, ACDRV1_EN=0 and ACDRV2_EN=0
2. Host enables main charger working in OTG mode
3. Host set OTG_EN=1
4. Host writes ACDRV1_EN=1 or ACDRV2_EN=1 depending on the which port is desired
5. Device checks if $V_{BUS} > V_{VBUS_present}$, ACDRV1 or ACDRV2 will pull high if this condition satisfied
6. If VAC1_OVP or VAC2_OVP occurs, the corresponding ACDRV will be pulled low, but bit OTG_EN will stay unchanged.
Host should write proper voltage setting to VAC1_OVP and VAC2_OVP. After fault cleared, the ACDRV will pull high immediately if corresponding ACDRV_EN is 1.
7. OTG_EN will be cleared by WD_TIMEOUT

To exit OTG mode, the host should follow the steps below:

1. Host turns off the OTG source
2. Host writes BUS_PD_EN=1 or corresponding VAC1/2_PD_EN=1 to discharge the port which was used.
3. Wait for VBUS and VAC to be discharged
4. Host writes ACDRV1/2_EN=0
5. Host writes OTG_EN=0

It should be noted that the OTG_EN only changes the pre-condition of turning on ACDRV1/2, the ACDRV_MANUAL_EN does not change with OTG_EN.

9.3.3 BAT-ONLY Mode

In BAT-ONLY Mode,

1. REGN disable
2. I2C alive

If each of the following conditions is not satisfied, the device enters into BAT-ONLY Mode. Any of the conditions below occurs, the device exits BAT-ONLY Mod

1. $VAC > VAC_PRESENT$
2. Host enables ADC
3. OTG_EN=1

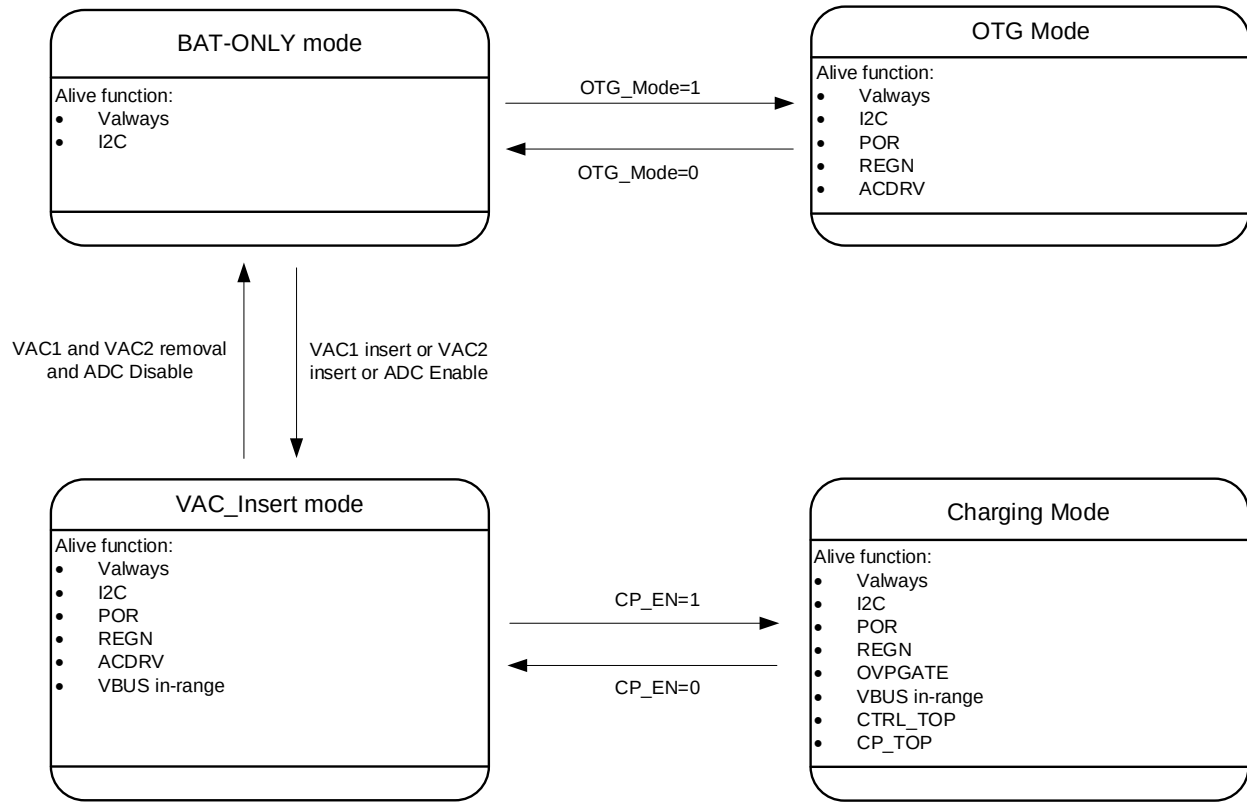


Fig 5. State diagram of SC8571

9.4 I2C Address Setting

The device features I2C address configuration based on CDRVL pin as showed in below table. Please be noted that I2C address detection function only works during the device POR period.

RESISTOR VALUE to GND on CDRVL_ADDRMS	I2C ADDRESS	MASTER, SLAVE OR STANDALONE OPERATION
>75k	0x65	Standalone
6.19k	0x67	Standalone
8.06k	0x66	Slave
10.5k	0x66	Master
14k	0x66	Standalone
18.2k	0x67	Slave
27.4k	0x65	Master



9.5 Parallel Operation

For higher power systems, it is possible to use two SC8571 devices in parallel. This has the effect of reducing the losses in the device and outputting high power to battery. User can configure the device's role based on resistance attached from CDRVL pin to ground as stated in the former section.

Once a device is configured as master, the TSBAT-SYNCOOUT pin works as transmitting synchronized signal to slave device automatically. The SRN-SYNCCIN pin of slave device is used to receive the synchronized signal.

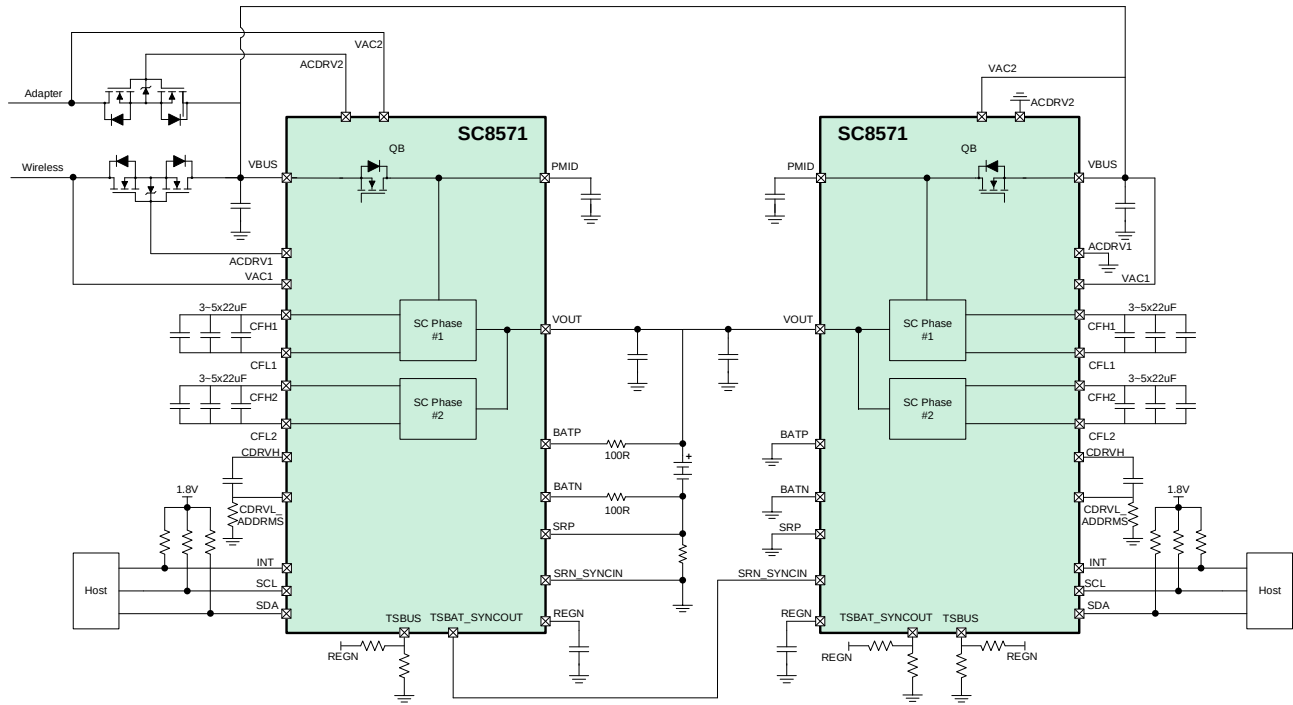


Fig 6. Parallel operation of SC8571

9.6 AC DRV1 and AC DRV2

AC DRV1 and AC DRV2 gate driver supports both GaN FET and traditional back-to-back N-MOSFET.

Here take AC DRV1 as an example to explain the behavior

1. To turn-on the load switch, AC DRV1 is rising from ground to 5V above max [VAC1, VBUS] to perform soft turn on
2. To turn-off the load switch, AC DRV is pull down to ground. For common source back-to-back N-MOSFET and GaN FET, a diode should be connected from source to gate to prevent negative overvoltage between gate and source.

9.7 Dual-Input Power Mux Logic

The device has two sets of input ports which support using GaN FET and back-to-back N-channel MOSFET as input switch. The device also supports two modes of controlling AC DRVs (gate drivers), Auto-mode and Manual mode. In Auto-mode, the first powered input port is selected to turn on the corresponding AC DRV. If two ports are powered simultaneously, the VAC1 has higher priority to turn on AC DRV1. In Manual mode, the turning on and off of AC DRVs is depending on the register AC DRV_EN. Before writing AC DRV1/2_EN to 1, make sure both AC DRV1_EN and AC DRV2_EN are 0, since these two registers can not be 1 simultaneously.

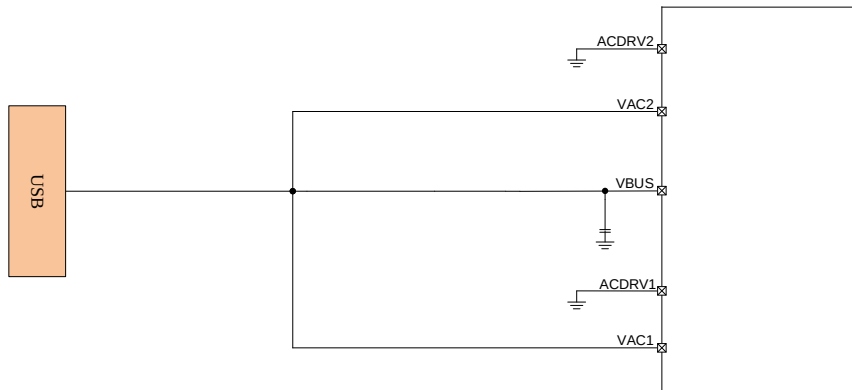
The following conditions should be satisfied to turn on AC DRV:



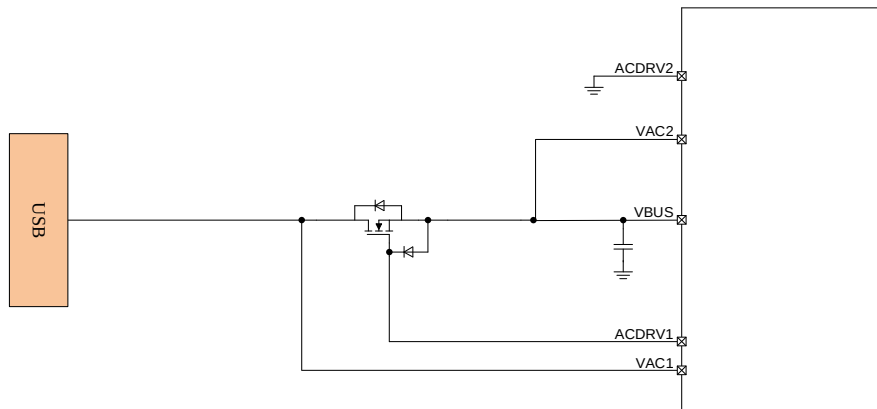
1. The corresponding FET is populated, VAC is not short to VBUS and ACDRV is not short to ground;
2. VAC voltage is higher than V_{VAC_UVLO} and lower than V_{ACOV} ;

The device supports following input configurations

9.7.1 Single input without ACFET-RBFET



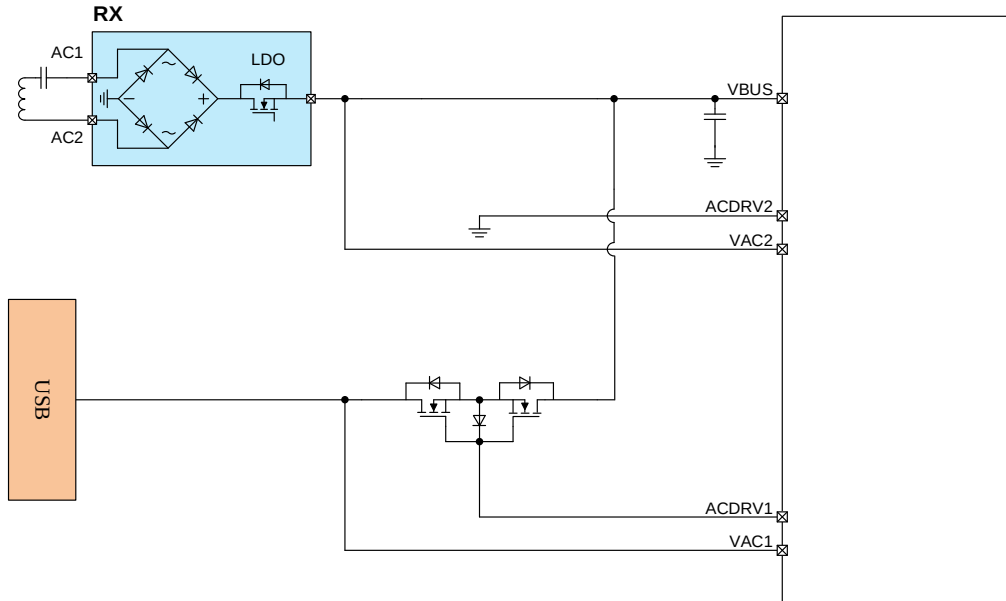
Register	Description
ACRB1_CONFIG_STAT=0	ACDRV1 shorts to ground
ACRB2_CONFIG_STAT=0	ACDRV2 shorts to ground
ACDRV1_STAT=0	ACDRV1 is off
ACDRV2_STAT=0	ACDRV2 is off
ACDRV1_EN	
ACDRV2_EN	
ACDRV_MANUAL_EN	
OTG_EN=0	

**9.7.2 Single input with ACFET1**

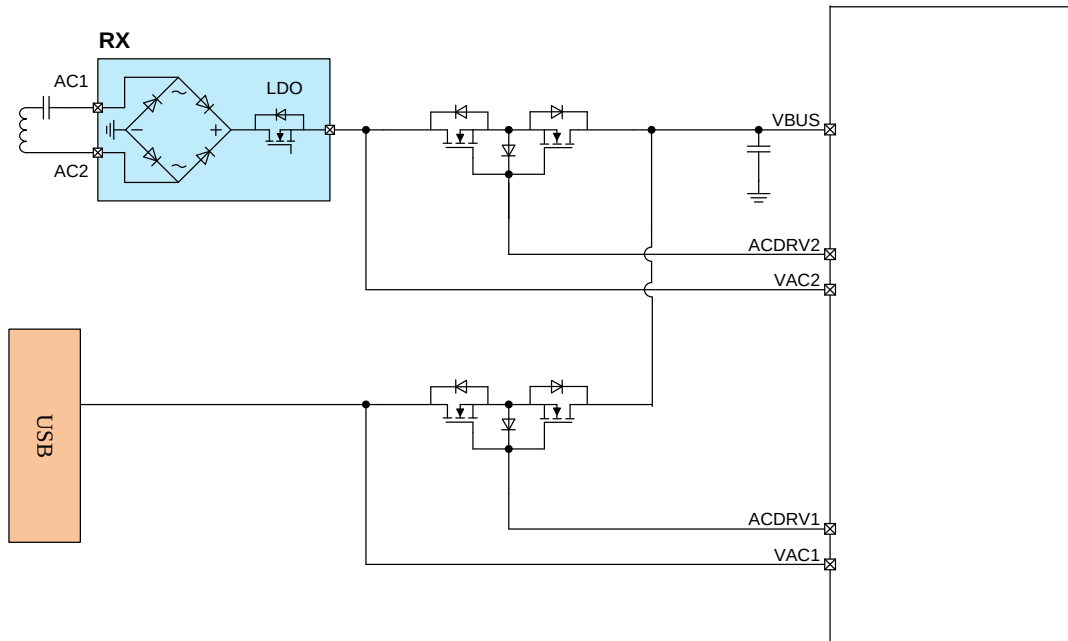
Register	Description
ACRB1_CONFIG_STAT=1	ACDRV1 is active
ACRB2_CONFIG_STAT=0	ACDRV2 shorts to ground
ACDRV1_STAT=1	ACDRV1 is on
ACDRV2_STAT=0	ACDRV2 is off
ACDRV1_EN	Write 1 to turn on ACDRV1 and 0 to turn off ACDRV1 in Manual Mode
ACDRV2_EN	
ACDRV_MANUAL_EN	Write 1 to work in Manual mode and 0 to work in Auto-mode
OTG_EN=0	



9.7.3 Single input ACFET1-RBFET1



Register	Description
ACRB1_CONFIG_STAT=1	ACDRV1 is active
ACRB2_CONFIG_STAT=0	ACDRV2 shorts to ground
ACDRV1_STAT=1	ACDRV1 is on
ACDRV2_STAT=0	ACDRV2 is off
ACDRV1_EN	Write 1 to turn on ACDRV1 and 0 to turn off ACDRV1 in Manual Mode
ACDRV2_EN	
ACDRV_MANUAL_EN	Write 1 to work in Manual mode and 0 to work in Auto-mode
OTG_EN=0	

**9.7.4 Two input with ACFET1-RBFET1 and ACFET2-RBFET2**

Register	Description
ACRB1_CONFIG_STAT=1	ACDRV1 is active
ACRB2_CONFIG_STAT=1	ACDRV2 is active
ACDRV1_STAT	
ACDRV2_STAT	
ACDRV1_EN	Write 1 to turn on ACDRV1 and 0 to turn off ACDRV1 in Manual Mode
ACDRV2_EN	Write 1 to turn on ACDRV2 and 0 to turn off ACDRV2 in Manual Mode
ACDRV_MANUAL_EN	Write 1 to work in Manual mode and 0 to work in Auto-mode
OTG_EN=0	



9.9 Device Modes and Protection Status

FUNCTIONS	BAT-ONLY (VAC<VAC_PRESENT)	VAC>VAC_PRESENT CHG_EN=0 or OTG_EN=1	VBUS>VBUS_PRESENT CHG_EN=1 (Switched cap enabled)	
			During charge soft start	Charging
I2C allowed	√	√	√	√
Allow user ADC request	√	√	√	√
REGN Alive	X	√	√	√
VAC FET gate drive		√	√	√
VAC_OVP		√	√	√
VBUS_OVP		X	√	√
VBUS_OVP_ALM			√	√
IBUS_OCP			√	√
IBUS_UCP			X	√
VBAT_OVP			√	√
VBAT_OVP_ALM			√	√
VOUT_OVP			√	√
IBAT_OCP			√	√
IBAT_OCP_ALM			√	√
VBUS In-range		√	√	X
PMID2OUT_OVP			X	√
PMID2OUT_UVP			X	√
WD_TIMEOUT	√	√	√	√
SS_TIMEOUT			√	X
PIN_DIAG_FAIL			√	X
TSHUT			√	√
TSBUS_FLT			√	√
TSBAT_FLT			√	√
TSBUS_TSBAT_ALM			√	√
TDIE_ALM			√	√

**9.10 Register map and default value**

ADDRESS (Hex)	ACRONYM	Default value (Hex)	WDT RST	REG RST
0x00	VBAT_OVP	0x5A	N	Y
0x01	VBAT_OVP_ALM	0x46	N	Y
0x02	IBAT_OCP	0x51	N	Y
0x03	IBAT_OCP_ALM	0x50	N	Y
0x04	CONFIG1	0x28	N	Y
0x05	CTRL1	0x00	N	Y
0x06	VBUS_OVP	0x26	N	Y
0x07	VBUS_OVP_ALM	0x22	N	Y
0x08	IBUS_OCP	0x0D	N	Y
0x09	CONFIG3	0x0C	N	Y
0x0A	TEMP_CTRL	0x60	N	Y
0x0B	TDIE_ALM	0xC8	N	Y
0x0C	TSBUS_FLT	0x15	N	Y
0x0D	TSBAT_FLT	0x15	N	Y
0x0E	VAC_CTRL	0x00	N	Y
0x0F	CTRL2	0x00	[4:5]	Y
0x10	CTRL3	0x80	N	Y
0x11	CTRL4	0x71	N	Y
0x12	CTRL5	0x60	N	Y
0x13	STAT1	0x00	N	Y
0x14	STAT2	0x00	N	Y
0x15	STAT3	0x00	N	Y
0x16	STAT4	0x00	N	Y
0x17	STAT5	0x00	N	Y
0x18	FLAG1	0x00	N	Y
0x19	FLAG2	0x00	N	Y
0x1A	FLAG3	0x00	N	Y
0x1B	FLAG4	0x00	N	Y
0x1C	FLAG5	0x00	N	Y
0x1D	MASK1	0x00	N	Y
0x1E	MASK2	0x00	N	Y
0x1F	MASK3	0x00	N	Y
0x20	MASK4	0x00	N	Y
0x21	MASK5	0x00	N	Y
0x22	PART_INFO	0x41	N	Y
0x23	ADC_CTRL	0x00	[7]	Y
0x24	ADC_FN_DIS	0x00	N	Y
0x25	IBUS_ADC1	0x00	N	Y
0x26	IBUS_ADC0	0x00	N	Y



0x27	VBUS_ADC1	0x00	N	Y
0x28	VBUS_ADC0	0x00	N	Y
0x29	VAC1_ADC1	0x00	N	Y
0x2A	VAC1_ADC0	0x00	N	Y
0x2B	VAC2_ADC1	0x00	N	Y
0x2C	VAC2_ADC0	0x00	N	Y
0x2D	VOUT_ADC1	0x00	N	Y
0x2E	VOUT_ADC0	0x00	N	Y
0x2F	VBAT_ADC1	0x00	N	Y
0x30	VBAT_ADC0	0x00	N	Y
0x31	IBAT_ADC1	0x00	N	Y
0x32	IBAT_ADC0	0x00	N	Y
0x33	TSBUS_ADC1	0x00	N	Y
0x34	TSBUS_ADC0	0x00	N	Y
0x35	TSBAT_ADC1	0x00	N	Y
0x36	TSBAT_ADC0	0x00	N	Y
0x37	TDIE_ADC1	0x00	N	Y
0x38	TDIE_ADC0	0x00	N	Y
0x40	INTERNAL1	0x05	Reset "ACDRV_MANUAL_EN" bit, "ACDRV1_EN" bit, "ACDRV2_EN" bit	Y
0x41	INTERNAL2	0x00	N	Y
0x42	PMID2OUT_OVP_UVP	0x4C	N	Y
0x43	DEGLITCH	0x00	N	Y



Table1. VBAT_OVP Register (Address=00h) [reset=5Ah]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_DIS	R/W	0h	N/A	0: Enable the VBAT_OVP protection (default) 1: Disable the VBAT_OVP protection
6	VBAT_OVP[6]	R/W	1h	1280mV	Battery Over-Voltage Protection Setting. When the battery voltage goes above the programmed threshold, an INT is sent and CP_EN bit is set to '0' Offset: 7V Range: 7V (b00000000) – 9.54V (b11111111) Default: 8.8V (b1011010)
5	VBAT_OVP[5]	R/W	0h	640mV	
4	VBAT_OVP[4]	R/W	1h	320mV	
3	VBAT_OVP[3]	R/W	1h	160mV	
2	VBAT_OVP[2]	R/W	0h	80mV	
1	VBAT_OVP[1]	R/W	1h	40mV	
0	VBAT_OVP[0]	R/W	0h	20mV	

Table2. VBAT_OVP_ALM Register (Address=01h) [reset=46h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_ALM_DIS	R/W	0h	N/A	0: Enable the VBAT_OVP_ALM alarm (default) 1: Disable the VBAT_OVP_ALM alarm
6	VBAT_OVP_ALM[6]	R/W	1h	1280mV	Battery Over-Voltage Alarm Setting. When the battery voltage goes above the programmed threshold, an INT is sent. The VBAT_OVP_ALM should be lower than VBAT_OVP. Offset: 7V Range: 7V (b00000000) – 9.54V (b11111111) Default: 8.4V (b1000110)
5	VBAT_OVP_ALM[5]	R/W	0h	640mV	
4	VBAT_OVP_ALM[4]	R/W	0h	320mV	
3	VBAT_OVP_ALM[3]	R/W	0h	160mV	
2	VBAT_OVP_ALM[2]	R/W	1h	80mV	
1	VBAT_OVP_ALM[1]	R/W	1h	40mV	
0	VBAT_OVP_ALM[0]	R/W	0h	20mV	



Table3. IBAT_OCP Register (Address=02h) [reset=51h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_OCP_DIS	R/W	0h	N/A	0: Enable the IBAT_OCP protection (default) 1: Disable the IBAT_OCP protection
6	IBAT_OCP[6]	R/W	1h	6400mA	BAT Over-Current Protection Setting. When the bat current reaches the programmed threshold, an INT is sent and CP_EN bit is set to '0' Offset: 0A Range: 0A (b00000000) – 12.7A (b11111111) Default: 8.1A (b1010001)
5	IBAT_OCP[5]	R/W	0h	3200mA	
4	IBAT_OCP[4]	R/W	1h	1600mA	
3	IBAT_OCP[3]	R/W	0h	800mA	
2	IBAT_OCP[2]	R/W	0h	400mA	
1	IBAT_OCP[1]	R/W	0h	200mA	
0	IBAT_OCP[0]	R/W	1h	100mA	

Table4. IBAT_OCP_ALM Register (Address=03h) [reset=50h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_OCP_ALM_DIS	R/W	0h	N/A	0: Enable the IBAT_OCP_ALM alarm (default) 1: Disable the IBAT_OCP_ALM alarm
6	IBAT_OCP_ALM[6]	R/W	1h	6400mA	BAT Over-Current Alarm Setting. When the bat current reaches the programmed threshold, an INT is sent. IBAT_OCP_ALM should be lower than IBAT_OCP Offset: 0A Range: 0A (b00000000) – 12.7A (b11111111) Default: 8A (b1010000)
5	IBAT_OCP_ALM[5]	R/W	0h	3200mA	
4	IBAT_OCP_ALM[4]	R/W	1h	1600mA	
3	IBAT_OCP_ALM[3]	R/W	0h	800mA	
2	IBAT_OCP_ALM[2]	R/W	0h	400mA	
1	IBAT_OCP_ALM[1]	R/W	0h	200mA	
0	IBAT_OCP_ALM[0]	R/W	0h	100mA	

**Table5. CONFIG1 Register (Address=04h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
0-7	RESERVED	R/W	0h	N/A	Reserved

Table6. CTRL1 Register (Address=05h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_UCP_DIS	R/W	0h	N/A	0: Enable the IBUS_UCP protection (default) 1: Disable the IBUS_UCP protection
6	IBUS_UCP_TH	R/W	0h	N/A	BUS under current protection setting. IBUS must reach the rising threshold before the ss_timeout. IBUS_UCP and IBUS_UCP_ALM are disabled until IBUS reaches the rising threshold. When the IBUS reaches the falling threshold, an INT is sent and CP_EN bit is set to '0'. 0: 150mA falling, 300mA rising(default) 1: 250mA falling, 500mA rising
5	REVSERVED	R/W	0h	N/A	Reserved
4	REVSERVED	R/W	0h	N/A	Reserved
3	REVSERVED	R/W	0h	N/A	Reserved
2	VBUS_IN_RANGE_DIS	R/W	0h	N/A	0: Enable the VBUS_IN_RANGE protection (default) 1: Disable the VBUS_IN_RANGE protection
1	RESERVED	R/W	0h	N/A	Reserved
0	RESERVED	R/W	0h	N/A	Reserved



Table7. VBUS_OVP Register (Address=06h) [reset=26h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	BUS_PD_EN	R/W	0h	N/A	VBUS pull down resistor control 0: Disable (default) 1: Enable
6	VBUS_OVP[6]	R/W	0h	3200mV	Bus Over-Voltage Protection Setting. When the bus voltage reaches the programmed threshold, an INT is sent and CP_EN bit is set to '0' Forward 2:1 mode: Offset: 14V Range: 14V(b0000000) – 26.7V (b1111111) Default: 17.8V (b0100110)
5	VBUS_OVP[5]	R/W	1h	1600mV	
4	VBUS_OVP[4]	R/W	0h	800mV	
3	VBUS_OVP[3]	R/W	0h	400mV	
2	VBUS_OVP[2]	R/W	1h	200mV	
1	VBUS_OVP[1]	R/W	1h	100mV	
0	VBUS_OVP[0]	R/W	0h	50mV (bit value x2 for 2:1 mode)	Forward 1:1 mode Offset: 7V Range: 7V(b0000000) – 13.35V (b1111111) Default: 8.9V (b0100110)

Table8.VBUS_OVP_ALM Register (Address=07h) [reset=22h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_OVP_ALM_DIS	R/W	0h	N/A	0: Enable the VBUS_OVP alarm (default) 1: Disable the VBUS_OVP alarm
6	VBUS_OVP_ALM[6]	R/W	0h	3200mV	BUS Over-Voltage Alarm Setting. When the bus voltage reaches the programmed threshold, an INT is sent. The VBUS_OVP_ALM should be lower than VBUS_OVP_ALM. Forward 2:1 mode: Offset: 14V Range: 14V(b0000000) – 26.7V (b1111111) Default: 17.4V (b0100010)
5	VBUS_OVP_ALM[5]	R/W	1h	1600mV	
4	VBUS_OVP_ALM[4]	R/W	0h	800mV	
3	VBUS_OVP_ALM[3]	R/W	0h	400mV	
2	VBUS_OVP_ALM[2]	R	0h	200mV	
1	VBUS_OVP_ALM[1]	R/W	1h	100mV	
0	VBUS_OVP_ALM[0]	R/W	0h	50mV (bit value x2 for 2:1 mode)	Forward 1:1 mode Offset: 7V Range: 7V(b0000000) – 13.35V (b1111111) Default: 8.7V (b0100010)



Table9. IBUS_OCP Register (Address=08h) [reset=0Dh]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_DIS	R/W	0h	N/A	0: Enable the IBUS_OCP(default) 1: Disable the IBUS_OCP
5-6	REVSERVED	R/W	0h	N/A	Reserved
4	IBUS_OCP[4]	R/W	0h	4000mA	Bus Over-Current Protection Setting. When the bus current reaches the programmed threshold, an INT is sent and CP_EN bit is set to '0' Offset: 1A Range: 1A (b00000) – 8A (b11100) Default: 4.25A (b01101)
3	IBUS_OCP[3]	R/W	1h	2000mA	
2	IBUS_OCP[2]	R/W	1h	1000mA	
1	IBUS_OCP[1]	R/W	0h	500mA	
0	IBUS_OCP[0]	R/W	1h	250mA	

Table10. CONFIG3 Register (Address=09h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
0-7	RESERVED	R	0h	N/A	Reserved

Table11. TEPMP_CTRL Register (Address=0Ah) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSHUT_DIS	R/W	0h	N/A	0: Enable the TSHUT protection (default) 1: Disable the TSHUT protection
5-6	RESERVED	R	0h	N/A	Reserved
4	TDIE_ALM_DIS	R	0h	N/A	0: Enable the TDIE alarm (default) 1: Disable the TDIE alarm
3	TSBUS_FLT_DIS	R/W	0h	N/A	0: Enable the TSBUS protection (default) 1: Disable the TSBUS protection
2	TSBAT_FLT_DIS	R/W	0h	N/A	0: Enable the TSBAT protection (default) 1: Disable the TSBAT protection
0-1	RESERVED	R/W	0h	N/A	Reserved



Table12. TDIE_ALM Register (Address=0Bh) [reset=C8h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TDIE_ALM[7]	R/W	1h	64°C	Die Over-Temperature Alarm setting. When the junction temperature reaches the programmed threshold, an INT is sent. Offset: 25°C Range: 25°C(b00000000)-150°C(b11111111) Default: 125°C
6	TDIE_ALM[6]	R/W	1h	32°C	
5	TDIE_ALM[5]	R/W	0h	16°C	
4	TDIE_ALM[4]	R/W	0h	8°C	
3	TDIE_ALM[3]	R/W	1h	4°C	
2	TDIE_ALM[2]	R/W	0h	2°C	
1	TDIE_ALM[1]	R/W	0h	1°C	
0	TDIE_ALM[0]	R/W	0h	0.5°C	

Table13. TSBUS_FLT Register (Address=0Ch) [reset=15h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBUS_FLT[7]	R/W	0h	25%	TSBUS percentage of REGN fault threshold. When the TSBUS/REGN ratio is under the programmed threshold, an INT is sent and CP_EN bit is set to '0' Offset: 0% Range: 0%(b00000000)-50%(b11111111) Default: 4.1%(b00010101) A TSBUS_TSBAT_ALM interrupt will be sent when TSBUS is lower than 5%+TSBUS_FLT
6	TSBUS_FLT[6]	R/W	0h	12.5%	
5	TSBUS_FLT[5]	R/W	0h	6.25%	
4	TSBUS_FLT[4]	R/W	1h	3.125%	
3	TSBUS_FLT[3]	R/W	0h	1.5625%	
2	TSBUS_FLT[2]	R/W	1h	0.78125%	
1	TSBUS_FLT[1]	R/W	0h	0.39063%	
0	TSBUS_FLT[0]	R/W	1h	0.19531%	



Table14. TSBAT_FLT Register (Address=0Dh) [reset=15h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBAT_FLT[7]	R/W	0h	25%	TSBAT percentage of REGN fault threshold. When the TSBAT/REGN ratio is under the programmed threshold, an INT is sent and CP_EN bit is set to '0' Offset: 0% Range: 0%(b00000000)-50%(b11111111) Default: 4.1% A TSBUS_TSBAT_ALM interrupt will be sent when TSBAT is lower than 5%+TSBAT_FLT
6	TSBAT_FLT[6]	R/W	0h	12.5%	
5	TSBAT_FLT[5]	R/W	0h	6.25%	
4	TSBAT_FLT[4]	R/W	1h	3.125%	
3	TSBAT_FLT[3]	R/W	0h	1.5625%	
2	TSBAT_FLT[2]	R/W	1h	0.78125%	
1	TSBAT_FLT[1]	R/W	0h	0.39063%	
0	TSBAT_FLT[0]	R/W	1h	0.19531%	

Table15. VAC_CTRL Register (Address=0Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP[2]	R/W	0h	10V	VAC1 Over-Voltage Protections Setting. When VAC1 reaches the programmed threshold, ACDRIV1 is turned off. Offset: 6.5V Range: 6.5V(b000) – 24V(b111) Default: 6.5V(b000)
6	VAC1_OVP[1]	R/W	0h	5V	
5	VAC1_OVP[0]	R/W	0h	2.5V	
4	VAC2_OVP[2]	R/W	0h	10V	VAC2 Over-Voltage Protections Setting. When VAC1 reaches the programmed threshold, ACDRIV1 is turned off. Offset: 6.5V Range: 6.5V(b000) – 24V(b111) Default: 6.5V(b000)
3	VAC2_OVP[1]	R/W	0h	5V	
2	VAC2_OVP[0]	R/W	0h	2.5V	
1	VAC1_PD_EN	R/W	0h	N/A	0: Disable the VAC1 pull down resistor (default) 1: Enable the VAC1 pull down resistor
0	VAC2_PD_EN	R/W	0h	N/A	0: Disable the VAC2 pull down resistor (default) 1: Enable the VAC2 pull down resistor



Table16. CTRL2 Register (Address=0Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	REG_RST	R/W	0h	N/A	Register reset. Reset registers to default value and reset time. This bit automatically goes back to '0' after reset 0: Not reset register (default) 1: reset register
6	RESERVED	R/W	0h	N/A	RESERVED
5	OTG_EN	R/W	0h	N/A	Power path control during the OTG mode 0: Precondition of ACDRV is VAC_OK (default) 1: Precondition of ACDRV is VBUS_PRESENT
4	CHG_EN	R/W	0h	N/A	Charge Enable. 0: Disable charge (default) 1: Enable charge
3	MODE	R/W	0h	N/A	Enable bypass mode 0: 2:1 charger mode (default) 1: 1:1 bypass mode
2	RESERVED	R/W	0h	N/A	RESERVED
1	ACDRV1_STAT	R	0h	N/A	Status of external ACFET1-RBFET1 gate driver. It is not reset by the REG_RST or the WATCHDOG 0: ACDRV1 is off (default) 1: ACDRV1 is on
0	ACDRV2_STAT	R	0h	N/A	Status of external ACFET2-RBFET2 gate driver. It is not reset by the REG_RST or the WATCHDOG 0: ACDRV2 is off (default) 1: ACDRV2 is on



Table17. CTRL3 Register (Address=10h) [reset=80h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	FSW_Set[2]	R/W	1h	N/A	Set switched cap switching frequency in forward 2:1 charger mode. 000: 300kHz 001: 350kHz 010: 400kHz 011: 450kHz 100: 500kHz (default) 101: 550kHz 110: 600kHz 111: 750kHz For parallel operation, the maximum switching frequency is 500KHz
6	FSW_Set[1]	R/W	0h	N/A	
5	FSW_Set[0]	R/W	0h	N/A	
4	WD_TIMEOUT[1]	R/W	0h	N/A	Watchdog Timeout protection 00: 0.65s (default) 01: 1.3s 10: 6.5s 11: 39s
3	WD_TIMEOUT[0]	R/W	0h	N/A	
2	WD_TIMEOUT_DIS	R/W	0h	N/A	0 = Enable watchdog (default) 1 = Disable watchdog
1	RESERVED	R	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved



Table18. CTRL4 Register (Address=11h) [reset=70h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	SET_IBAT_SNS_RES	R/W	0h	N/A	Battery current sense resistor value 0: 2mΩ 1: 5mΩ
6	SS_TIMEOUT[2]	R/W	1h	N/A	Adjustable timeout for IBUS to rise to the IBUS_UCP_RISE_THRESHOLD 000: 6.5ms 001: 13ms 010: 26ms 011: 52ms 100: 104ms 101: 416ms 110: 1.6s 111: 13s (default)
5	SS_TIMEOUT[1]	R/W	1h	N/A	
4	SS_TIMEOUT[0]	R/W	1h	N/A	
3	IBUS_UCP_FALL_DEGLITCH_SET[1]	R/W	0h	N/A	This bit sets the deglitch time for IBUS_UCP_FALL 00: 10us (default) 01: 5ms 10: 50ms 11: 150ms
2	IBUS_UCP_FALL_DEGLITCH_SET[0]	R/W	0h	N/A	
1	RESERVED	R/W	0h	N/A	Reserved
0	RESERVED	R/W	0h	N/A	Reserved



Table19. CTRL5 Register (Address=12h) [reset=60h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VOUT_OVP_DIS	R/W	0h	N/A	Disable VOUT_OVP protection 0: Enable VOUT_OVP protection (default) 1: Disable VOUT_OVP protection
6	VOUT_OVP[1]	R/W	1h	N/A	VOUT Over-Voltage protection. When output voltage reaches the programmed threshold, an INT is sent and CP_EN bit is set to '0' 00: 9.4V 01: 9.6V 10: 9.8V 11: 10V
5	VOUT_OVP[0]	R/W	1h	N/A	
4	FREQ_SHIFT[1]	R/W	0h	N/A	Adjust switching frequency for EMI 00: Nominal frequency 01: +60KHz 10: -60KHz 11: Spread spectrum varies frequency $\pm 60\text{KHz}$
3	FREQ_SHIFT[0]	R/W	0h	N/A	
2	RESERVED	R/W	0h	N/A	Reserved
1	MS[1]	R	0h	N/A	Mode selection. 00: Standalone 01: Slave 10: Master 11: Reserved
0	MS[0]	R	0h	N/A	



Table20. STAT1 Register (Address=13h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_STAT	R	0h	N/A	VBAT_OVP status 0: Not in BAT_OVP 1: In BAT_OVP
6	VBAT_OVP_ALM_STAT	R	0h	N/A	VBAT_OVP_ALM status 0: Not in VBAT_OVP_ALM 1: In VBA_OVP_ALM
5	VOUT_OVP_STAT	R	0h	N/A	VOUT_OVP status 0: Not in VOUT_OVP 1: In VOUT_OVP
4	IBAT_OCP_STAT	R	0h	N/A	IBAT_OCP status 0: Not in IBAT_OCP 1: In IBAT_OCP
3	IBAT_OCP_ALM_STAT	R	0h	N/A	IBAT_OCP_ALM status 0: Not IBAT_OCP_ALM 1: In IBAT_OCP_ALM
2	RESERVED	R	0h	N/A	Reserved
1	VBUS_OVP_STAT	R	0h	N/A	VBUS_OVP status 0: Not in VBUS_OVP 1: In VBUS_OVP
0	VBUS_OVP_ALM_STAT	R	0h	N/A	VBUS_OVP_ALM status 0: Not in VBUS_OVP_ALM 1: In VBUS_OVP_ALM

**Table21. STAT2 Register (Address=14h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_STAT	R	0h	N/A	IBUS_OCP status 0: Not in IBUS_OCP 1: In IBUS_OCP
6	RESERVED	R	0h	N/A	Reserved
5	IBUS_UCP_FALL_STAT	R	0h	N/A	IBUS_UCP status 0: Not in IBUS_UCP 1: In IBUS_UCP
4	RESERVED	R	0h	N/A	Reserved
3	RESERVED	R	0h	N/A	Reserved
2	PIN_DIAG_FAIL_STAT	R	0h	N/A	Pin diagnostic fail flag. CFLY short/open and CBOOT short/open will be checked before switch. 0: Not in PIN_DIAG_FAIL 1: In PIN_DIAG_FAIL
1	RESERVED	R	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved

Table22. STAT3 Register (Address=15h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP_STAT	R	0h	N/A	VAC1_OVP status 0: Not in VAC1_OVP 1: In VAC1_OVP
6	VAC2_OVP_STAT	R	0h	N/A	VAC2_OVP status 0: Not in VAC2_OVP 1: In VAC2_OVP
5	VBAT_INSERT_STAT	R	0h	N/A	VBAT_INSERT status 0: VOUT not present 1: VOUT present
4	VAC1_INSERT_STAT	R	0h	N/A	VAC1_INSERT status 0: VAC1 not present 1: VAC1 present
3	VAC2_INSERT_STAT	R	0h	N/A	VAC2_INSERT status 0: VAC2 not present 1: VAC2 present
2	VBUS_PRESENT_STAT	R	0h	N/A	VBUS_PRESENT status 0: VBUS not present 1: VBUS present
1	ACRB1_CONFIG_STAT	R	0h	N/A	ACFET1-RBFET1 status 0: ACFET1-RBFET1 is not placed 1: ACFET1-RBFET1 is placed
0	ACRB2_CONFIG_STAT	R	0h	N/A	ACFET2-RBFET2 status 0: ACFET2-RBFET2 is not placed 1: ACFET2-RBFET2 is placed



Table23. STAT4 Register (Address=16h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	Reserved
6	SS_TIMEOUT_STAT	R	0h	N/A	Soft start timeout status 0: Device not in soft start timeout 1: Device in soft start time out
5	TSBUS_TSBAT_ALM_STAT	R	0h	N/A	TSBUS and TSBAT ALM status. 0: TSBUS or TSBAT is NOT within 5% of the TSBUS_FLT or TSBAT_FLT set threshold 1: TSBUS or TSBAT is within 5% of the TSBUS_FLT or TSBAT_FLT set threshold
4	TSBUS_FLT_STAT	R	0h	N/A	TSBUS_FLT status 0: Not in TSBUS_FLT 1: In TSBUS_FLT
3	TSBAT_FLT_STAT	R	0h	N/A	TSBAT_FLT status 0: Not in TSBAT_FLT 1: In TSBAT_FLT
2	TSHUT_FLT_STAT	R	0h	N/A	TSHUT status 0: Not in TSHUT 1: In TSHUT
1	TDIE_ALM_STAT	R	0h	N/A	TDIE_ALM status 0: Not in TDIE_ALM 1: In TDIE_ALM
0	WD_TIMEOUT_STAT	R	0h	N/A	I2C watch dog timeout status 0: Normal 1: WD timer expired

**Table24. STAT5 Register (Address=17h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	Reserved
6	CP_SWITCHING_STAT	R	0h	N/A	Converter active status 0: Switched cap is not switching 1: Switched cap is switching
5	RESERVED	R	0h	N/A	Reserved
4	VBUS2OUT_ERRORHI_STAT	R	0h	N/A	VBUS2OUT_ERRORHI status 0: Not in VBUS2OUT_ERRORHI 1: In VBUS2OUT_ERRORHI
3	VBUS2OUT_ERRORLO_STAT	R	0h	N/A	VBUS2OUT_ERRORLO status 0: Not in VBUS2OUT_ERRORLO 1: In VBUS2OUT_ERRORLO
2	RESERVED	R	0h	N/A	Reserved
1	RESERVED	R	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved



Table25. FLAG1 Register (Address=18h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBATOVP_FLG	R	0h	N/A	VBAT_OVP flag 0: Normal 1: VBAT_OVP status changed
6	VBATOVP_ALM_FLG	R	0h	N/A	VBAT_OVP_ALM flag 0: Normal 1: VBAT_OVP_ALM status changed
5	VOUT_OVP_FLG	R	0h	N/A	VOUT_OVP flag 0: Normal 1: VOUT_OVP status changed
4	IBAT_OCP_FLG	R	0h	N/A	IBAT_OCP flag 0: Normal 1: VBAT_OCP status changed
3	IBAT_OCP_ALM_FLG	R	0h	N/A	IBAT_OCP_ALM flag 0: Normal 1: VBAT_OCP_ALM status changed
2	RESERVED	R	0h	N/A	Reserved
1	VBUS_OVP_FLG	R	0h	N/A	VBUS_OVP flag 0: Normal 1: VBUS_OVP status changed
0	VBUS_OVP_ALM_FLG	R	0h	N/A	VBUS_OVP_ALM flag 0: Normal 1: VBUS_OVP_ALM status changed



Table26. FLAG2 Register (Address=19h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_FLG	R	0h	N/A	IBUS_OCP flag 0: Normal 1: IBUS_OCP status changed
6	RESERVED	R	0h	N/A	Reserved
5	IBUS_UCP_FALL_FLG	R	0h	N/A	IBUS_UCP flag 0: Normal 1: IBUS_UCP status changed
4	RESERVED	R	0h	N/A	Reserved
3	RESERVED	R	0h	N/A	Reserved
2	PIN_DIAG_FAIL_FLG	R	0h	N/A	PIN_DIAG_FAIL flag 0: Normal 1: PIN_DIAG_FAIL status changed
1	RESERVED	R	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved



Table27. FLAG3 Register (Address=1Ah) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP_FLG	R	0h	N/A	VAC1_OVP flag 0: Normal 1: VAC1_OVP status changed
6	VAC2_OVP_FLG	R	0h	N/A	VAC2_OVP flag 0: Normal 1: VAC2_OVP status changed
5	VBAT_INSERT_FLG	R	0h	N/A	VOUT_PRESENT flag 0: Normal 1: VOUT_PRESENT status changed
4	VAC1_INSERT_FLG	R	0h	N/A	VAC1_PRESENT flag 0: Normal 1: VAC1_PRESENT status changed
3	VAC2_INSERT_FLG	R	0h	N/A	VAC2_PRESENT flag 0: Normal 1: VAC2_PRESENT status changed
2	VBUS_PRESENT_FLG	R	0h	N/A	VBUS_PRESENT flag 0: Normal 1: VBUS_PRESENT status changed
1	ACRB1_CONFIG_FLG	R	0h	N/A	ACFET1-RBFET1_CONFIG flag 0: Normal 1: ACFET1-RBFET1_CONFIG status changed
0	ACRB2_CONFIG_FLG	R	0h	N/A	ACFET2-RBFET2_CONFIG flag 0: Normal 1: ACFET2-RBFET2_CONFIG status changed



Table28. FLAG4 Register (Address=1Bh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	Reserved
6	SS_TIMEOUT_FLG	R	0h	N/A	SS_TIMEOUT flag 0: Normal 1: SS_TIMEOUT status changed
5	TSBUS_TSBAT_ALM_FLG	R	0h	N/A	TSBUS_TSBAT_ALM flag 0: Normal 1: TSBAT_TSBAT_ALM status changed
4	TSBUS_FLT_FLG	R	0h	N/A	TSBUS_FLT flag 0: Normal 1: TSBUS_FLT status changed
3	TSBAT_FLT_FLG	R	0h	N/A	TSBAT_FLT flag 0: Normal 1: TSBAT_FLT status changed
2	TSHUT_FLG	R	0h	N/A	TSHUT flag 0: Normal 1: TSHUT status changed
1	TDIE_ALM_FLG	R	0h	N/A	TDIE_ALM flag 0: Normal 1: TDIE_ALM status changed
0	WD_TIMEOUT_FLG	R	0h	N/A	I2C watch dog timeout flag 0: Normal 1: WD timeout status changed

**Table29. FLAG5 Register (Address=1Ch) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	Reserved
6	RESERVED	R	0h	N/A	Reserved
5	RESERVED	R	0h	N/A	Reserved
4	VBUS2OUT_ERRO RHI_FLG	R	0h	N/A	VBUS2OUT_ERRORHI flag 0: Normal 1: VBUS2OUT_ERRORHI status changed
3	VBUS2OUT_ERRO RLO_FLG	R	0h	N/A	VBUS2OUT_ERRORLO flag 0: Normal 1: VBUS2OUT_ERRORLO status changed
2	RESERVED	R	0h	N/A	Reserved
1	RESERVED	R	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved



Table30. MASK1 Register (Address=1Dh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_MASK	R/W	0h	N/A	VBAT_OVP mask 0: VBAT_OVP flag produce INT 1: VBAT_OVP flag does not produce INT
6	VBAT_OVP_ALM_MASK	R/W	0h	N/A	VBAT_OVP_ALM mask 0: VBAT_OVP_ALM flag produce INT 1: VBAT_OVP_ALM flag does not produce INT
5	VOUT_OVP_MASK	R/W	0h	N/A	VOUT_OVP mask 0: VOUT_OVP flag produce INT 1: VOUT_OVP flag does not produce INT
4	IBAT_OCP_MASK	R/W	0h	N/A	IBAT_OCP mask 0: IBAT_OCP flag produce INT 1: IBAT_OCP flag does not produce INT
3	IBAT_OCP_ALM_MASK	R/W	0h	N/A	IBAT_OCP_ALM mask 0: IBAT_OCP_ALM flag produce INT 1: IBAT_OCP_ALM flag does not produce INT
2	RESERVED	R	0h	N/A	Reserved
1	VBUS_OVP_MASK	R/W	0h	N/A	VBUS_OVP mask 0: VBUS_OVP flag produce INT 1: VBUS_OVP flag does not produce INT
0	VBUS_OVP_ALM_MASK	R/W	0h	N/A	VBUS_OVP_ALM mask 0: VBUS_OVP_ALM flag produce INT 1: VBUS_OVP_ALM flag does not produce INT

**Table31. MASK2 Register (Address=1Eh) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_MASK	R/W	0h	N/A	IBUS_OCP mask 0: IBUS_OCP flag produce INT 1: IBUS_OCP flag does not produce INT
6	RESERVED	R/W	0h	N/A	Reserved
5	IBUS_UCP_FALL_MASK	R/W	0h	N/A	IBUS_UCP mask 0: IBUS_UCP flag produce INT 1: IBUS_UCP flag does not produce INT
4	RESERVED	R/W	0h	N/A	Reserved
3	RESERVED	R/W	0h	N/A	Reserved
2	PIN_DIAG_FAIL_MAKS	R/W	0h	N/A	PIN_DIAG_FAIL mask 0: PIN_DIAG_FAIL flag produce INT 1: PIN_DIAG_FAIL flag does not produce INT
1	RESERVED	R/W	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved



Table32. MASK3 Register (Address=1Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP_MASK	R/W	0h	N/A	VAC1_OVP mask 0: VAC1_OVP flag produce INT 1: VAC1_OVP flag does not produce INT
6	VAC2_OVP_MASK	R/W	0h	N/A	VAC2_OVP mask 0: VAC2_OVP flag produce INT 1: VAC2_OVP flag does not produce INT
5	VBAT_INSERT_MASK	R/W	0h	N/A	VBAT_INSERT mask 0: VBAT_INSERT flag produce INT 1: VBAT_INSERT flag does not produce INT
4	VAC1_INSERT_MASK	R/W	0h	N/A	VAC1_INSERT mask 0: VAC1_INSERT flag produce INT 1: VAC1_INSERT flag does not produce INT
3	VAC2_INSERT_MASK	R/W	0h	N/A	VAC2_INSERT mask 0: VAC2_INSERT flag produce INT 1: VAC2_INSERT flag does not produce INT
2	VBUS_PRESENT_MASK	R/W	0h	N/A	VBUS_PRESENT mask 0: VBUS_PRESENT flag produce INT 1: VBUS_PRESENT flag does not produce INT
1	ACRB1_CONFIG_MASK	R/W	0h	N/A	ACRB1_CONFIG mask 0: ACRB1_CONFIG flag produce INT 1: ACRB1_CONFIG flag does not produce INT
0	ACRB2_CONFIG_MASK	R/W	0h	N/A	ACRB2_CONFIG mask 0: ACRB2_CONFIG flag produce INT 1: ACRB2_CONFIG flag does not produce INT



Table33. MASK4 Register (Address=20h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R/W	0h	N/A	Reserved
6	SS_TIMEOUT_MASK	R/W	0h	N/A	SS_TIMEOUT mask 0: SS_TIMEOUT flag produce INT 1: SS_TIMEOUT flag does not produce INT
5	TSBUS_TSBAT_ALM_MASK	R/W	0h	N/A	TSBUS_TSBAT_ALM mask 0: TSBUS_TSBAT_ALM flag produce INT 1: TSBUS_TSBAT_ALM flag does not produce INT
4	TSBUS_FLT_MASK	R/W	0h	N/A	TSBUS_FLT mask 0: TSBUS_FLT flag produce INT 1: TSBUS_FLT flag does not produce INT
3	TSBAT_FLT_MASK	R/W	0h	N/A	TSBAT_FLT mask 0: TSBAT_FLT flag produce INT 1: TSBAT_FLT flag does not produce INT
2	TSHUT_MASK	R/W	0h	N/A	TSHUT mask 0: TSHUT flag produce INT 1: TSHUT flag does not produce INT
1	TDIE_ALM_MASK	R/W	0h	N/A	TDIE_ALM mask 0: TDIE_ALM flag produce INT 1: TDIE_ALM flag does not produce INT
0	WD_TIMEOUT_MASK	R/W	0h	N/A	WD_TIMEOUT mask 0: WD_TIMEOUT flag produce INT 1: WD_TIMEOUT flag does not produce INT



Table34. MASK5 Register (Address=21h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R/W	0h	N/A	Reserved
6	RESERVED	R	0h	N/A	Reserved
5	RESERVED	R/W	0h	N/A	Reserved
4	VBUS2OUT_ERRORHI_MASK	R/W	0h	N/A	VBUS2OUT_ERRORHI mask 0: VBUS2OUT_ERRORHI flag produce INT 1: VBUS2OUT_ERRORHI flag does not produce INT
3	VBUS2OUT_ERRORLO_MASK	R/W	0h	N/A	VBUS2OUT_ERRORLO mask 0: VBUS2OUT_ERRORLO flag produce INT 1: VBUS2OUT_ERRORLO flag does not produce INT
2	RESERVED	R	0h	N/A	Reserved
1	RESERVED	R	0h	N/A	Reserved
0	RESERVED	R	0h	N/A	Reserved

Table35. Device_info Register (Address=22h) [reset=41h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	DEVIC_ID[7]	R	0h	N/A	0x41
6	DEVIC_ID[6]	R	1h	N/A	
5	DEVIC_ID[5]	R	0h	N/A	
4	DEVIC_ID[4]	R	0h	N/A	
3	DEVIC_ID[3]	R	0h	N/A	
2	DEVIC_ID[2]	R	0h	N/A	
1	DEVIC_ID[1]	R	0h	N/A	
0	DEVIC_ID[0]	R	1h	N/A	

**Table36. ADC_CTRL Register (Address=23h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	ADC_EN	R/W	0h	N/A	ADC enable. 0: Disable 1: Enable
6	RESERVED	R/W	0h	N/A	Reserved
5	RESERVED	R/W	0h	N/A	Reserved
4	RESERVED	R/W	0h	N/A	Reserved
3	RESERVED	R/W	0h	N/A	Reserved
2	RESERVED	R/W	0h	N/A	Reserved
1	IBUS_ADC_DIS	R/W	0h	N/A	IBUS ADC Control 0: Enable 1: Disable
0	VBUS_ADC_DIS	R/W	0h	N/A	VBUS ADC Control 0: Enable 1: Disable

**Table37. ADC_FN_DISABLE Register (Address=24h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_ADC_DIS	R	0h	N/A	VAC1 ADC Control 0: Enable 1: Disable
6	VAC2_ADC_DIS	R	0h	N/A	VAC2 ADC Control 0: Enable 1: Disable
5	VOUT_ADC_DIS	R	0h	N/A	VOUT ADC Control 0: Enable 1: Disable
4	VBAT_ADC_DIS	R	0h	N/A	VBAT ADC Control 0: Enable 1: Disable
3	IBAT_ADC_DIS	R	0h	N/A	IBAT ADC Control 0: Enable 1: Disable
2	TSBUS_ADC_DIS	R	0h	N/A	TSBUS ADC Control 0: Enable 1: Disable
1	TSBAT_ADC_DIS	R	0h	N/A	TSBAT ADC Control 0: Enable 1: Disable
0	TDIE_ADC_DIS	R	0h	N/A	TDIE ADC Control 0: Enable 1: Disable

**Table38. IBUS_ADC1 Register (Address=25h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	IBUS ADC LSB: 2.5mA
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBUS_ADC[11]	R	0h	N/A	
2	IBUS_ADC[10]	R	0h	N/A	
1	IBUS_ADC[9]	R	0h	N/A	
0	IBUS_ADC[8]	R	0h	N/A	

Table39. IBUS_ADC0 Register (Address=26h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_ADC[7]	R	0h	N/A	IBUS ADC LSB: 2.5mA
6	IBUS_ADC[6]	R	0h	N/A	
5	IBUS_ADC[5]	R	0h	N/A	
4	IBUS_ADC[4]	R	0h	N/A	
3	IBUS_ADC[3]	R	0h	N/A	
2	IBUS_ADC[2]	R	0h	N/A	
1	IBUS_ADC[1]	R	0h	N/A	
0	IBUS_ADC[0]	R	0h	N/A	

**Table40. VBUS_ADC1 Register (Address=27h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VBUS ADC LSB: 6.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VBUS_ADC[11]	R	0h	N/A	
2	VBUS_ADC[10]	R	0h	N/A	
1	VBUS_ADC[9]	R	0h	N/A	
0	VBUS_ADC[8]	R	0h	N/A	

Table41. VBUS_ADC0 Register (Address=28h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_ADC[7]	R	0h	N/A	VBUS ADC LSB: 6.25mV
6	VBUS_ADC[6]	R	0h	N/A	
5	VBUS_ADC[5]	R	0h	N/A	
4	VBUS_ADC[4]	R	0h	N/A	
3	VBUS_ADC[3]	R	0h	N/A	
2	VBUS_ADC[2]	R	0h	N/A	
1	VBUS_ADC[1]	R	0h	N/A	
0	VBUS_ADC[0]	R	0h	N/A	



Table42. VAC1_ADC1 Register (Address=29h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VAC1 ADC LSB: 6.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VAC1_ADC[11]	R	0h	N/A	
2	VAC1_ADC[10]	R	0h	N/A	
1	VAC1_ADC[9]	R	0h	N/A	
0	VAC1_ADC[8]	R	0h	N/A	

Table43. VAC1_ADC0 Register (Address=2Ah) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_ADC[7]	R	0h	N/A	VAC1 ADC LSB: 6.25mV
6	VAC1_ADC[6]	R	0h	N/A	
5	VAC1_ADC[5]	R	0h	N/A	
4	VAC1_ADC[4]	R	0h	N/A	
3	VAC1_ADC[3]	R	0h	N/A	
2	VAC1_ADC[2]	R	0h	N/A	
1	VAC1_ADC[1]	R	0h	N/A	
0	VAC1_ADC[0]	R	0h	N/A	



Table44. VAC2_ADC1 Register (Address=2Bh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VAC2 ADC LSB: 6.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VAC2_ADC[11]	R	0h	N/A	
2	VAC2_ADC[10]	R	0h	N/A	
1	VAC2_ADC[9]	R	0h	N/A	
0	VAC2_ADC[8]	R	0h	N/A	

Table45. VAC2_ADC0 Register (Address=2Ch) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC2_ADC[7]	R	0h	N/A	VAC2 ADC LSB: 6.25mV
6	VAC2_ADC[6]	R	0h	N/A	
5	VAC2_ADC[5]	R	0h	N/A	
4	VAC2_ADC[4]	R	0h	N/A	
3	VAC2_ADC[3]	R	0h	N/A	
2	VAC2_ADC[2]	R	0h	N/A	
1	VAC2_ADC[1]	R	0h	N/A	
0	VAC2_ADC[0]	R	0h	N/A	



Table46. VOUT_ADC1 Register (Address=2Dh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VOUT ADC LSB: 2.5mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VOUT_ADC[11]	R	0h	N/A	
2	VOUT_ADC[10]	R	0h	N/A	
1	VOUT_ADC[9]	R	0h	N/A	
0	VOUT_ADC[8]	R	0h	N/A	

Table47. VOUT_ADC0 Register (Address=2Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VOUT_ADC[7]	R	0h	N/A	VOUT ADC LSB: 2.5mV
6	VOUT_ADC[6]	R	0h	N/A	
5	VOUT_ADC[5]	R	0h	N/A	
4	VOUT_ADC[4]	R	0h	N/A	
3	VOUT_ADC[3]	R	0h	N/A	
2	VOUT_ADC[2]	R	0h	N/A	
1	VOUT_ADC[1]	R	0h	N/A	
0	VOUT_ADC[0]	R	0h	N/A	



Table48. VBAT_ADC1 Register (Address=2Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VBAT ADC LSB: 2.5mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VBAT_ADC[11]	R	0h	N/A	
2	VBAT_ADC[10]	R	0h	N/A	
1	VBAT_ADC[9]	R	0h	N/A	
0	VBAT_ADC[8]	R	0h	N/A	

Table49. VBAT_ADC0 Register (Address=30h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_ADC[7]	R	0h	N/A	VBAT ADC LSB: 2.5mV
6	VBAT_ADC[6]	R	0h	N/A	
5	VBAT_ADC[5]	R	0h	N/A	
4	VBAT_ADC[4]	R	0h	N/A	
3	VBAT_ADC[3]	R	0h	N/A	
2	VBAT_ADC[2]	R	0h	N/A	
1	VBAT_ADC[1]	R	0h	N/A	
0	VBAT_ADC[0]	R	0h	N/A	

**Table50. IBAT_ADC1 Register (Address=31h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	IBAT ADC LSB: 3.125mA
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBAT_ADC[11]	R	0h	N/A	
2	IBAT_ADC[10]	R	0h	N/A	
1	IBAT_ADC[9]	R	0h	N/A	
0	IBAT_ADC[8]	R	0h	N/A	

Table51. IBAT_ADC0 Register (Address=32h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_ADC[7]	R	0h	N/A	IBAT ADC LSB: 3.125mA
6	IBAT_ADC[6]	R	0h	N/A	
5	IBAT_ADC[5]	R	0h	N/A	
4	IBAT_ADC[4]	R	0h	N/A	
3	IBAT_ADC[3]	R	0h	N/A	
2	IBAT_ADC[2]	R	0h	N/A	
1	IBAT_ADC[1]	R	0h	N/A	
0	IBAT_ADC[0]	R	0h	N/A	



Table52. TSBUS_ADC1 Register (Address=33h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	TSBUS_ADC[9]	R	0h	50%	
0	TSBUS_ADC[8]	R	0h	25%	

Table53. TSBUS_ADC0 Register (Address=34h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBUS_ADC[7]	R	0h	12.5%	TSBUS pin voltage as a percentage of VOUT TSBUS percentage = TSBUS_ADC [9:0] * 0.09766%
6	TSBUS_ADC[6]	R	0h	6.25%	
5	TSBUS_ADC[5]	R	0h	3.125%	
4	TSBUS_ADC[4]	R	0h	1.5625%	
3	TSBUS_ADC[3]	R	0h	0.78125 %	
2	TSBUS_ADC[2]	R	0h	0.39063 %	
1	TSBUS_ADC[1]	R	0h	0.19531 %	
0	TSBUS_ADC[0]	R	0h	0.09766 %	



Table54. TSBAT_ADC1 Register (Address=35h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	TSBAT_ADC[9]	R	0h	50%	
0	TSBAT_ADC[8]	R	0h	25%	

Table55. TSBAT_ADC0 Register (Address=36h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBAT_ADC[7]	R	0h	12.5%	TSBAT pin voltage as a percentage of VOUT TSBAT percentage = TSBAT_ADC [9:0] * 0.09766%
6	TSBAT_ADC[6]	R	0h	6.25%	
5	TSBAT_ADC[5]	R	0h	3.125%	
4	TSBAT_ADC[4]	R	0h	1.5625%	
3	TSBAT_ADC[3]	R	0h	0.78125 %	
2	TSBAT_ADC[2]	R	0h	0.39063 %	
1	TSBAT_ADC[1]	R	0h	0.19531 %	
0	TSBAT_ADC[0]	R	0h	0.09766 %	

**Table56. TDIE_ADC1 Register (Address=37h) [reset=00h]**

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	TDIE_ADC[8]	R	0h	128°C	

Table57. TDIE_ADC0 Register (Address=38h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TDIE_ADC[7]	R	0h	64°C	DIE temperature = TDIE_ADC [8:0] * 0.5°C
6	TDIE_ADC[6]	R	0h	32°C	
5	TDIE_ADC[5]	R	0h	16°C	
4	TDIE_ADC[4]	R	0h	8°C	
3	TDIE_ADC[3]	R	0h	4°C	
2	TDIE_ADC[2]	R	0h	2°C	
1	TDIE_ADC[1]	R	0h	1°C	
0	TDIE_ADC[0]	R	0h	0.5°C	



Table48. Internal1 Register (Address=40h) [reset=05h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	POR_FLAG	R	0h	N/A	Indicate a POR event has ever happened
6	ACDRV_MANUAL_EN	R/W	0h	N/A	0 = Auto-mode (default) 1 = Manual-mode WD_TIMEOUT will reset this bit
5	ACDRV1_EN	R/W	0h	N/A	0 = Disable ACDRV1 (default) 1 = Enable ACDRV1 WD_TIMEOUT will reset this bit
4	ACDRV2_EN	R/W	0h	N/A	0 = Disable ACDRV2 (default) 1 = Enable ACDRV2 WD_TIMEOUT will reset this bit
3	IBUS_UCP_RISE_FLAG	R	0h	N/A	IBUS under-current threshold rising flag. An INT is sent when this occurs, and is cleared upon read.
2	IBUS_UCP_RISE_MASK	R/W	1h	N/A	IBUS under-current threshold rising /INT mask 0: Not masked 1: Masked
1	VOUT_OK_CHG_FLAG	R	0h	N/A	Indicates the VOUT_OK_CHG threshold has been exceeded. An INT is sent when this occurs and is cleared upon read
0	VOUT_OK_CHG_MASK	R/W	1h	N/A	0 = Not Masked; 1 = Masked



Table49. INTERNAL2 Register (Address=41h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	SS_TIMEOUT_DIS	R/W	0h	N/A	0: Enable the SS_TIMEOUT protection (default) 1: Disable the SS_TIMEOUT protection
6	VBUS_OVP_DIS	R/W	0h	N/A	0: Enable the VBUS_OVP protection (default) 1: Disable the VBUS_OVP protection
5	PMID2OUT_OVP_DIS	R/W	0h	N/A	0 = PMID2OUT OVP protection enabled (default) 1 = PMID2OUT OVP protection disabled
4	PMID2OUT_UVP_DIS	R/W	0h	N/A	0 = PMID2OUT UVP protection enabled (default) 1 = PMID2OUT UVP protection disabled
3	ACRB1_DET_DIS	R/W	0h	N/A	0 = Enable ACDRV1 grounded detection (default) 1 = Disable ACDRV1 grounded detection
2	ACRB2_DET_DIS	R/W	0h	N/A	0 = Enable ACDRV2 grounded detection (default) 1 = Disable ACDRV2 grounded detection
1	IBAT_SNS_DIS	R/W	0h	N/A	0 = Enable IBAT_SNS block when VAC_OK or ADC_EN=1 (default) 1 = Disable IBAT_SNS block even VAC_OK or ADC_EN=1
0	VBAT_SNS_DIS	R/W	0h	N/A	0 = Enable VBAT_SNS block when VAC_OK or ADC_EN=1 (default) 1 = Disable VBAT_SNS block when VAC_OK or ADC_EN=1



Table50. PMID2OUT_OVP_UVP Register (Address=42h) [reset=4Ch]

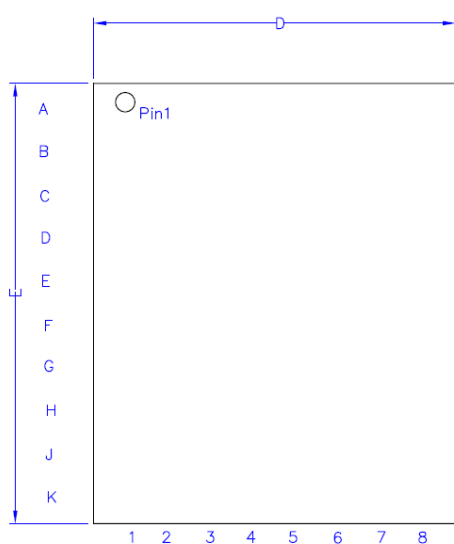
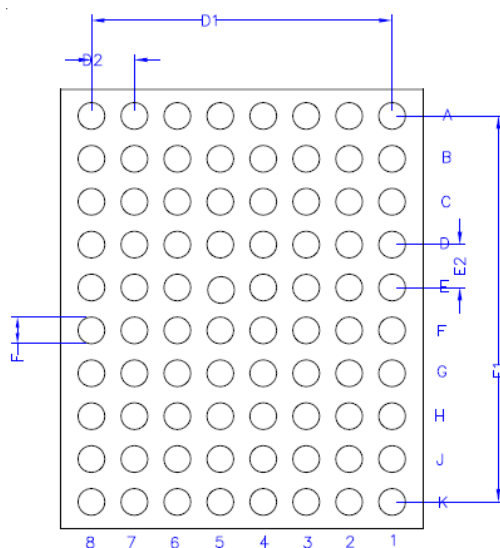
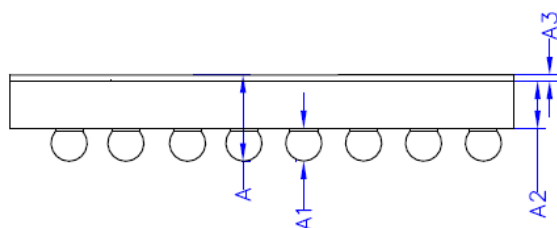
Bit	Field	Type	Default value @POR	Bit Value	Notes
7	PMID2OUT_UVP[2]	R/W	0h	-100mV	PMID/2-VOUT UVP is used to protect input short. Offset: -100mV(b000) Range: -100mV(b000) ~ -275mV(b111) Default: -150mV(b010)
6	PMID2OUT_UVP[1]	R/W	1h	-50mV	
5	PMID2OUT_UVP[0]	R/W	0h	-25mV	
4	PMID2OUT_OVP[2]	R/W	0h	200mV	PMID/2-VOUT OVP is used to protect output short. Offset: 50mV(b000) Range: 50mV(b000) ~ 400mV(b111) Default: 200mV(b011)
3	PMID2OUT_OVP[1]	R/W	1h	100mV	
2	PMID2OUT_OVP[0]	R/W	1h	50mV	
1	PMID2OUT_UVP_F LAG	R	0h	N/A	PMID/2-VOUT under-voltage flag. An INT is sent and CHG_EN bit is set to '0' when this event happens. This bit is cleared when read.
0	PMID2OUT_OVP_F LAG	R	0h	N/A	PMID/2-VOUT over-voltage flag. An INT is sent when this event happens, and is cleared when read.

Table51. DEGLITCH Register (Address=43h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
4-7	RESERVED	R	0h	N/A	Reserved
3	PMID2OUT_UVP_ MASK	R/W	0h	N/A	PMID2OUT_UVP mask 0: PMID2OUT_UVP flag produce INT 1: PMID2OUT_UVP flag does not produce INT
2	PMID2OUT_OVP_ MASK	R/W	0h	N/A	PMID2OUT_OVP mask 0: PMID2OUT_OVP flag produce INT 1: PMID2OUT_OVP flag does not produce INT
1	VBUS_TH_CHG_E N_STAT	R	0h	N/A	Indicates the VBUS_TH_CHG_EN threshold is exceeding
0	VOUT_TH_SW_RE GN_STAT	R	0h	N/A	Indicates the VOUT_TH_SW_REGN threshold is exceeding



10 MECHANICAL DATA

TOP VIEW
Ball DownBOTTOM VIEW
Ball Up

SIDE VIEW

Unit: mm

		No.	Mean	Tolerance
Total Thickness		A	0.575	±0.0405
Ball Height+UBM Thicknesss		A1	0.216	±0.023
Wafer/Grinding Thickness		A2	0.319	±0.0125
Backside Coating Thickness		A3	0.040	±0.005
PKG Die size	X	D	3.425	±0.025
	Y	E	4.151	±0.025
Ball diameter		F	0.265	±0.020
Ball Pitch		D1	2.800	NA
		D2	0.400	NA
		E1	3.600	NA
		E2	0.400	NA