



SC81535Q Automotive Fully Integrated USB PD and UFCS Solution with Integrated Step-Down Converter

1 Descriptions

The SC81535Q is a fully integrated USB PD and UFCS solution. It integrates a Buck converter with 2 integrated power switches and a USB PD and UFCS controller. The SC81535Q operates over 4.9V to 26V wide input voltage and can output 3.3V to 12V voltage. It also supports up to 3A continuous output current.

The SC81535Q supports USB PD3.1 with PPS and backward supports UFCS, DCP/CDP schemes for Battery Charging specification (BC1.2), 3A Divider Mode, 1.2V/1.2V Mode. It also supports QC2.0/QC3.0, Huawei FCP/SCP as well.

The SC81535Q's buck converter employs current mode control scheme. The switching frequency could be set at 250kHz/420kHz/2.1MHz through Efuse. The SC81535Q also provides optional spread spectrum to optimize EMI performance.

The SC81535Q supports a flexible power management state machine when the battery voltage is low, or the temperature is high. When two SC81535Q are used in dual PD or UFCS ports, the internal power sharing logic can smartly distribute the total power.

The SC81535Q offers input over-voltage protection, output over-voltage protection, cycle-by-cycle current limit, DP/DM/CCx short to battery protection, output short circuit protection, average output current limit and thermal shutdown protection

The SC81535Q is available in 21-pin 3mm X 4mm Wettable Flank QFN.

3 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature Grade 1: T_A range: -40°C to 125 °C
- Integrates synchronous Buck converter:
 - 4.9V to 26V continuous operating input range, 40V ABS voltage
 - 3.3V-12V output voltage range, up to 33W output power
 - 250k/420k/2.1MHz frequency selectable
 - Spread Spectrum
 - Integrates 45mΩ/30mΩ switching power FETs
 - Accurate internal output CC current limit
 - Selectable Forced PWM operation and Automatic PFM/FPWM operation
- Integrates multiple protocols:
 - Support BC1.2 modes(DCP and CDP), 3A Divider Mode, and 1.2V/1.2V Mode
 - Supports USB Type-C DFP mode
 - Support USB PD3.1 and PPS
 - Support UFCS
 - Support FC2.0/3.0 Specification, Huawei FCP/SCP
 - Support USB3.0 Hub Application
- 11-bit ADC to monitor the output voltage / current
- Low IQ during Type-C unattached
- CCx/DP/DM short to VOUT/VBAT protection
- Line drop compensation
- Programmable Power Management during low battery or high temperature
- Support two ports Power sharing

2 Applications

- Automotive USB Charging
- Automotive USB Hub



4 Device Information

ORDER NUMBER	GPIO1	GPIO2	Protocol	PACKAGE
SC81535QQFNR	NTC_POWER_SHARE_1	FAULT	PD3.1, APPLE 3A, DCP, FC, FCP, SCP, UFCS	FCQFN 3X4

*Notes: Refer to **Table1** on Section14 for more information about different part number. If more different configurations are required, contact the FAE of Southchip to get a new part number

5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.0.1	2025/6	24	1.Update EC Table 2.Update PDP State Machine
V1.0.0	2025/3	/	1.Initial version.

6 Typical Application Circuit

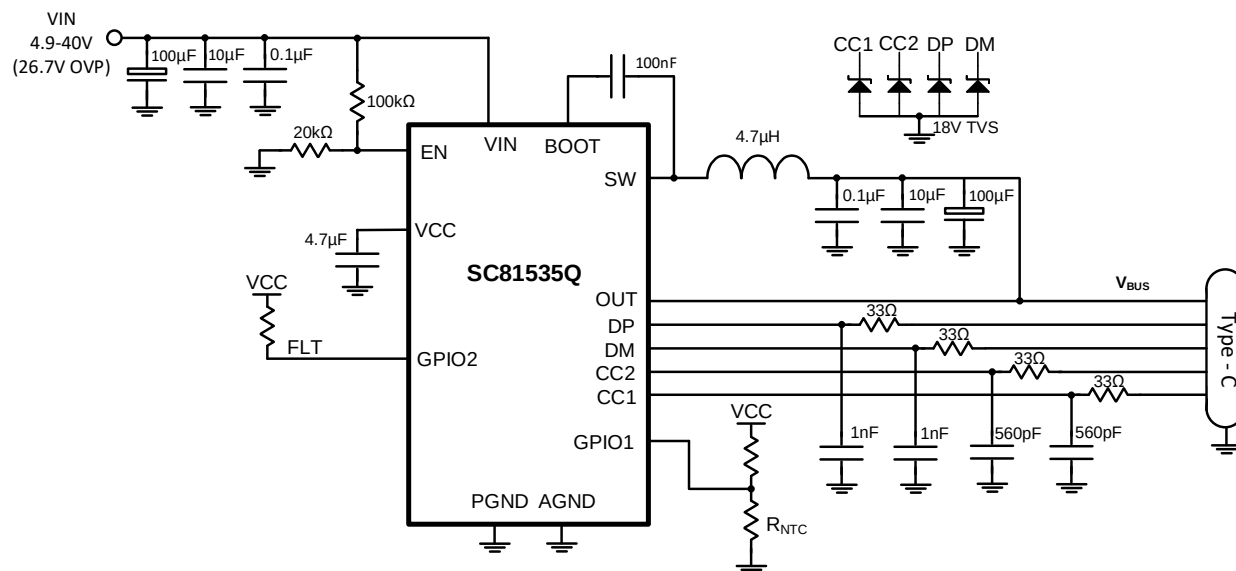
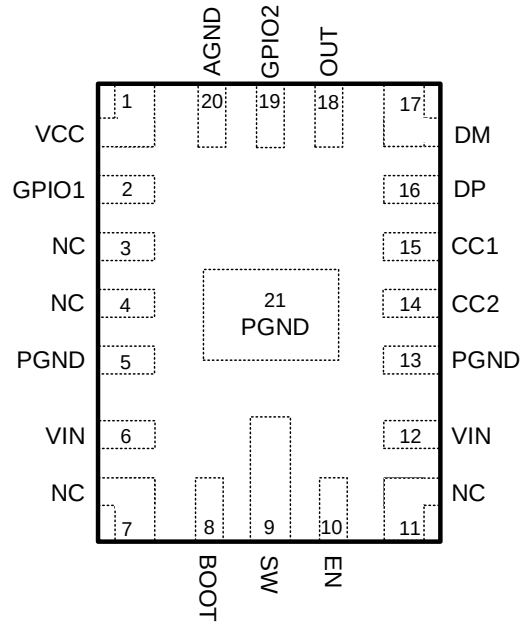


Figure 6-1. Typical Application Circuit



7 Terminal Configuration and Functions



Terminal		I/O	DESCRIPTION	
NUMBER	NAME			
1	VCC	O	Internal LDO regulator output. Decouple with a 4.7μF/0603 capacitor between this pin and the AGND pin.	
2	GPIO1	O	POL	Type-C polarity indication, open drain. When CC1 is selected as CC line, the POL is pull-low; When CC2 is selected as CC line, the POL is open drain.
		I	NTC_Power_Share_1	NTC or Power sharing input. When input is low, PDP will reduce to NTC_POWER_SHARE_1 set value.
		O	ALT	Attach and fault indicator, open drain output. It pull-low for 15μs when sink plug in if no fault event occurs. When fault happens, it pull-low.
3	NC	-		
4	NC	-		
5	PGND	-	Power Ground.	
6	VIN	I	Input power supply for the IC.	
7	NC	-		
8	BOOT	O	Connect a 100nF capacitor between BOOT and SW to provide bias voltage for MOSFET drive on Buck controller.	
9	SW	O	Switching node pin of the buck side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.	
10	EN	I	EN input. Apply logic high to enable the chip. EN pin has internal 6μA pull-up.	
11	NC	-		
12	VIN	I	Input power supply for the IC.	



13	PGND	-	Power Ground.	
14	CC2	I/O	Type-C configure channel2. It also supports VCONN output	
15	CC1	I/O	Type-C configure channel1. It also supports VCONN output	
16	DP	I/O	DP is the input/output used to handshake with portable devices.	
17	DM	I/O	DM is the input/output used to handshake with portable devices.	
18	OUT	I	Buck output feedback.	
19	GPIO2	O	FLT	Fault indication, open drain output. It indicates OCP, OTP, OVP, GND/DP/DM/CCx short to battery.
		O	Attach	Output to indicate device is attached or not. Active low.
		I	Power_Share_2	Power sharing 2 input, active high. When this pin voltage >1.87V, the PD power will be reduced to PS_PDP_THD setting.
20	AGND	-	Analog Ground.	
21	PGND	-	Power Ground.	



8 Specifications

8.1 Absolute Maximum Ratings

Within operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VIN, EN	-0.3	40	V
	SW	-0.3	29	V
	BOOT	SW-0.3	SW+6	V
	OUT	-0.3	18	V
	CC1, CC2, DP, DM	-0.3	18	V
	Others	-0.3	5.5	V
T _J	IC operating junction temperature range	-40	150	°C
Tstg	IC storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human Body Model (HBM) ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾ , corner pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range	4.9		26	V
V _{OUT}	Output voltage range	3.3		12	V
I _{OUT}	Output DC current range	0		3	A
L	Inductance	2.2	4.7	10	μH
F _{SW}	Buck switching frequency range	250	420	2100	kHz
T _J	Operating junction temperature	-40		150	°C



T_A	Operating ambient temperature range	-40		125	°C
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8.4 Thermal Information

THERMAL RESISTANCE		FCQFN21 (3mm x 4mm)	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (SC81535Q EVM) ⁽¹⁾	36	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance (JESD 51-7) ⁽²⁾	48	°C/W

- (1) Measured on SC81535Q EVM. 4-layer, 2oz Cu per top and bottom layer and 1oz Cu per inner layer.
- (2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

8.5 Electrical Characteristic

$T_J = -40^{\circ}\text{C}$ to 150°C , $V_{IN} = 12\text{V}$ and $V_{EN} = 5\text{V}$. Typical value is tested at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{IN_UVLO}	Under voltage lockout threshold	V _{IN} rising		4.9	5.1	V
		V _{IN} falling	4.5	4.7		V
I _Q	Quiescent current when no device attached			690	750	μA
	Quiescent current when device attached	CC attached, No switching, no load.		2		mA
I _{SD}	Shutdown current into the VIN pin	IC disabled, V _{EN} =0V		20	40	μA
V _{CC}	Internal regulator output		4.8	5.0	5.2	V
EN						
V _{EN_VCC_H}	EN input level to turn on internal LDO	Rising threshold			1.06	V
V _{EN_VCC_L}	EN input level to turn off internal LDO	Falling threshold	0.4			V
V _{EN_H}	EN input level to start switching	Rising threshold	1.2	1.26	1.32	V
V _{EN_L}	EN input level to stop switching	Falling threshold	0.94	1.00	1.06	V
MOSFETS						
R _{DS(ON)_HS}	High-side MOSFET on resistance			45	90	mΩ
R _{DS(ON)_LS}	Low-side MOSFET on resistance			30	60	mΩ
BOOT UVLO						
V _{BOOT_OK}	Falling voltage on BOOT pin compared to SW which will turn off high-side switch			2.3		V
REFERENCE						
V _{OUT1}	Output Voltage	T _J = +25°C	-2.5%	3.3	+2.5%	V
V _{OUT2}			-2.5%	5.0	+2.5%	V
V _{OUT3}			-2.5%	9.0	+2.5%	V
V _{OUT4}			-2.5%	11.0	+2.5%	V
OVER VOLTAGE PROTECTION						
V _{OUT_OVP_R}	Output OVP rising		115%	120%	125%	V _{FB}
V _{OUT_OVP_F}	Output OVP falling		105%	110%	115%	V _{FB}



V _{OVLO_R1}	Voltage on VIN pin to stop buck switching		26.15	26.7	27.2	V	
V _{OVLO_R2}	Voltage on VIN pin to stop buck switching		17.3	17.8	18.3	V	
V _{OVLO_HYS}	Input voltage protection hysteresis		1.0			V	
R _{DIS}	Output discharge resistor		230			Ω	
INTERNAL CLOCK							
F _{SW1}	Oscillator frequency		250			kHz	
F _{SW2}			420				
F _{SW3}			2100				
T _{ON_Max}	Maximum HS switch on time		8			μs	
T _{ON_MIN}	Minimum HS switch on time		99	150		ns	
T _{OFF_MIN}	Minimum HS switch off time		140	175	210	ns	
SPREAD SPECTRUM							
F _{SRANGE}	Frequency dithering span		6			%	
f _M *	Modulation frequency		1/256			F _{SW}	
SOFT START							
T _{SS}	Soft Start Time	For 5V _{OUT} condition from 10% to 90%	2.9			ms	
CURRENT LIMIT							
I _{SENS1}	Current loop accuracy	OC threshold=1A, T _J = +25°C	0.9	1	1.1	A	
I _{SENS2}		OC threshold=3A, T _J = +25°C	2.9	3	3.1	A	
I _{PEAK}	High-side peak current limit		6.2	7.7	9.2	A	
I _{VALLEY}	Low-side valley current limit		4.2	5.6	7	A	
I _{LSNEG}	Low-side negative current limit		-3			A	
ZCD	Zero cross		10			mA	
LINE DROP COMPENSATION							
V _{DROP}	Line drop compensation	LDC_GAIN=01b, I _{OUT} =3A	100			mV	
		LDC_GAIN=10b, I _{OUT} =3A	300			mV	
		LDC_GAIN=11b, I _{OUT} =3A	600			mV	
VBUS_UV							
V _{BUS_UV1}	V _{BUS_UV} falling voltage, when minimum PPS voltage is 5V		4.4			4.6	V
V _{BUS_UV2}	V _{BUS_UV} falling voltage, when minimum PPS voltage is 3.3V		2.7			2.9	V
ADC							
N _{ADC}	Resolution		11			Bits	
V _{BUS_ADC}	Range		0			12	V
	LSB		7.5				mV



	Accuracy	$V_{BUS} = 5\sim 12V$	-100	+100	mV	
I_{BUS_ADC}	Range		0	3.6	A	
	LSB		3.125		mA	
	Accuracy	$0A<I_{BUS}<0.5A$	-300	+300	mA	
		$0.5A\leq I_{BUS}<3A$	-200	+100	mA	
NTC						
V_{NTC_ETY}	External thermal sense trigger voltage		10%		VCC	
V_{NTC_RCY}	External thermal sense recover voltage		20%		VCC	
GPIO1 – Power Share						
V_{IH_PS}	Power share input high		2		V	
V_{IL_PS}	Power share input low		0.4		V	
GPIO2 – POL						
R_{PD_POL}	POL pull-down resistor		40		Ω	
I_{LKG_POL}	POL Leakage		3		μA	
BC1.2 DCP MODE						
R_{DP/DM_SHORT}	DP and DM short resistance	$V_{DP} = 0.8V, I_{DM} = 1mA,$ $T_J = -40^{\circ}C$ to $+150^{\circ}C$	50		Ω	
V_{DP/DM_OVPT}	DP and DM over-voltage threshold		3.8	4	4.2	V
3A DIVIDER MODE						
$V_{DP_DIVIDER}$	DP output voltage		2.7		V	
$R_{DP_DIVIDER}$	DP output impedance		30		k Ω	
$V_{DM_DIVIDER}$	DM output voltage		3.3		V	
$R_{DM_DIVIDER}$	DM output impedance		30		k Ω	
1.2V/1.2V MODE						
$V_{DP/DM_1p2mode}$	DP/DM output voltage		1.12	1.2	1.28	V
$R_{DP/DM_1p2mode}$	DP/DM output impedance		70	100	130	k Ω
QUICK CHARGE 3.0 MODE						
V_{QC_LOW}	DP/DM low voltage	`	0.3	0.35	0.4	V
V_{QC_HIGH}	DP/DM high voltage		2.1	2.2	2.3	V
R_{DP_QC}	Resistance pull down on DP		20		k Ω	
R_{DM_QC}	Resistance pull down on DM		20		k Ω	
$R_{DP_500K_PD}$	Resistance pull down on DP		500		k Ω	
$R_{DM_500K_PD}$	Resistance pull down on DM		500		k Ω	
$t_{GLITCH_DM}^{*}$	DM low glitch time		1		ms	
$t_{GLITCH_DP}^{*}$	DP high glitch time		1200		ms	
$t_{GLITCH_V_CHANGE_QC2}^{*}$	Output voltage change glitch time		40		ms	
$t_{GLITCH_V_CHANGE_QC3}^{*}$	Output voltage change glitch time		60		ms	
$V_{BUS_CONT_}$	Bus voltage (VBUS) step		200		mV	



STEP						
VBUS SLEW RATE						
$t_{SLEW RATE}^*$	Rising slew rate for VBUS		0.1			mV/ μ s
	Falling slew rate for VBUS		0.1			mV/ μ s
CDP MODE						
V_{DM_SRC}	DM CDP output voltage	DM data output high, VBUS $\geq 3.3V$	0.6	0.65	0.7	V
		DM data output low			62	mV
V_{DA_REF}	DP rising lower window threshold for V_{DM_SRC}	Force DM $>0.4V$, DM output low, measure sink current	0.35			V
V_{LGC_SRC}	DP rising upper window threshold for V_{DM_SRC}		0.9	1	1.1	V
$t_{IN_CDP_START_DEGH}^*$	CDP_DET mode、DP_PU DET mode to CDP_start mode deglich		4			ms
$t_{IN_CDP_DET_DEGH}^*$	CDP_START mode、DP_PU DET mode to CDP_start mode deglich		10			ms
$t_{IN_DPPU_DET_DEGH}^*$	CDP_START mode、CDP_start mode to DP_PU DET mode deglich		2			ms
UFCS/FCP/SCP MODE						
V_{DATA_HIGH}	DP/DM data output high voltage	DP/DM data output high, VBUS $\geq 3.3V$	3	3.3	3.6	V
I_{DPDM_HIGH}	DP/DM output high capability	Force DP/DM $< 2.9V$, DP/DM output high, measure source current	5		16	mA
I_{DPDM_LOW}	DP/DM output low sink capability	Force DP/DM $>0.4V$, DP/DM output low, measure sink current	2		6	mA
V_{IH_TH}	DP/DM input data rising threshold		1.1	1.2	1.3	V
V_{IL_TH}	DP/DM input data falling threshold		1	1.1	1.2	V
$t_{RX_PING}^*$	PING length			2.56		ms
$t_{RX_UI/4}^*$	UI/4 length		33	40	47	μ s
t_{TUI}/t_{RUI}^*				100		%
USB Type-C						
$R_{p_180\mu A}$	CC Rp pull up 180 μA capability		165.6	180	194.4	μA
$R_{p_330\mu A}$	CC Rp pull up 330 μA capability		303.6	330	356.4	μA
$t_{CC_DEBOUNCE_F}^*$	CC voltage falling debounce timer			150		mS
$t_{CC_DEBOUNCE_R}^*$	CC voltage rising debounce timer			10		mS
I_{VCONN_OCP}	Internal V_{CONN} over current threshold		30	35	56	mA
$t_{VCONN_OC_DEG}^*$	Internal V_{CONN} over-current deglitch time			24		μ s
V_{CCOVP_TH}	CC OVP rising threshold		5.7	6	6.3	V
V_{CCOVP_HYST}	CC OVP hysteresis			0.26		V
$f_{BITRATE}^*$	Bit rate		270		330	kbps
$\rho_{BitRate}^*$	Maximum difference between the bitrate during the part of the packet				0.25	%



	following the Preamble and the reference bitrate.			
$t_{\text{EndDriveBMC}}^*$	Time to cease driving the line after the end of the last bit of the Frame.		23	μs
$t_{\text{InterFrameGap}}^*$	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble		25	μs
t_{RISE}^*	Rise time	$C = 330\text{pF}$	300	ns
t_{FALL}^*	Fall time	$C = 330\text{pF}$	300	ns
Z_{Driver}^*	PD data Tx output impedance		33 66 75	Ω
V_{Swing}	High level voltage for CC PD data		1.05 1.125 1.2	V
THERMAL SHUTDOWN				
T_{SD}^*	Thermal shutdown temperature	T_{J} rising	165	$^{\circ}\text{C}$
	Thermal shutdown hysteresis	T_{J} falling below T_{SD}	20	$^{\circ}\text{C}$

* Guarantee by Design

8.6 Typical Characteristics

$V_{\text{IN}}=12\text{V}$, $V_{\text{OUT}}=5\text{V}$, $L=4.7\mu\text{H}$, $F_{\text{SW}}=420\text{kHz}$, mode=FPWM with spread spectrum, $T_{\text{A}}=25^{\circ}\text{C}$, unless otherwise noted.

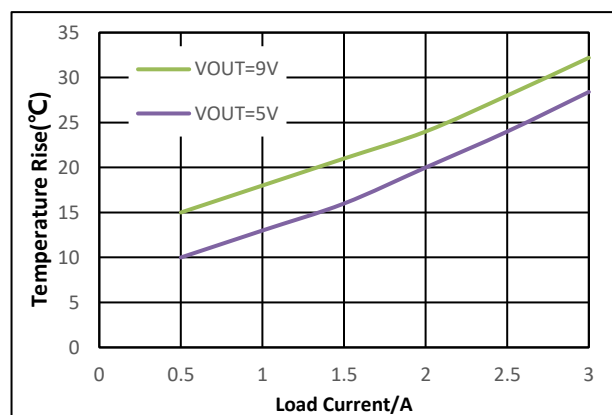


Figure 8-1. Case Temperature Rise, DCR=9mR

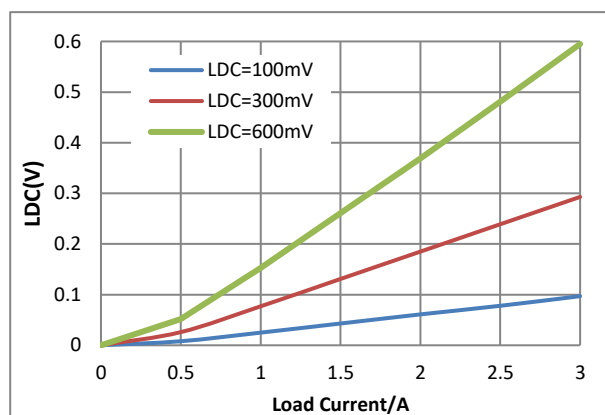


Figure 8-2. Line Drop Compensation

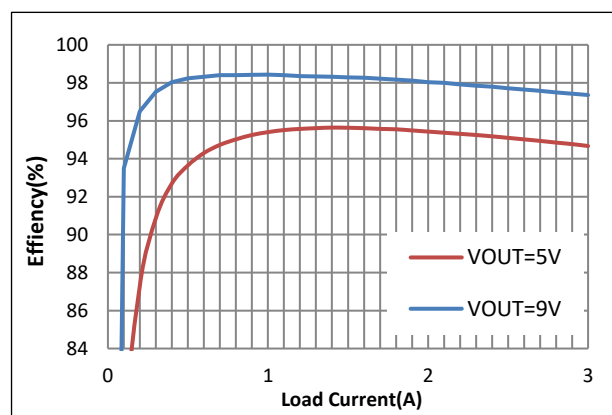


Figure 8-3. Efficiency, $V_{\text{IN}}=9\text{V}$, DCR=9mR

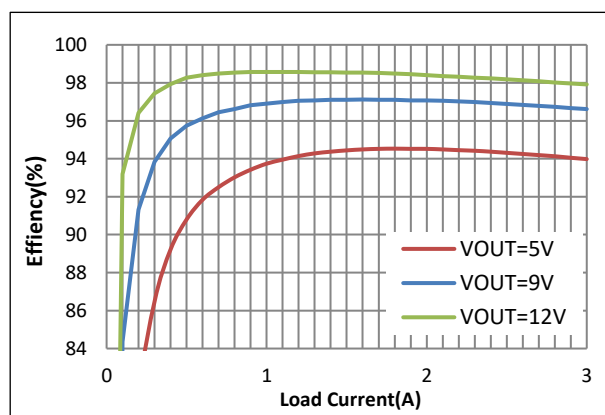


Figure 8-4. Efficiency, $V_{\text{IN}}=12\text{V}$, DCR=9mR

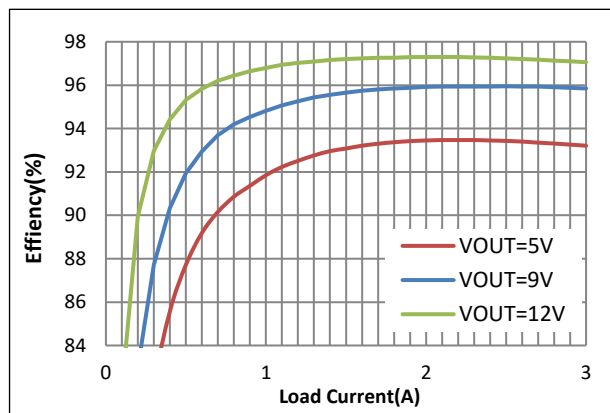
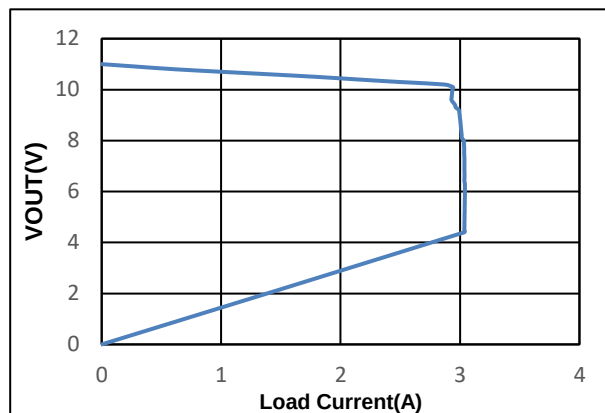
Figure 8-5. Efficiency, $V_{IN}=16V$, $DCR=9mR$ 

Figure 8-6. CC/CV Curve

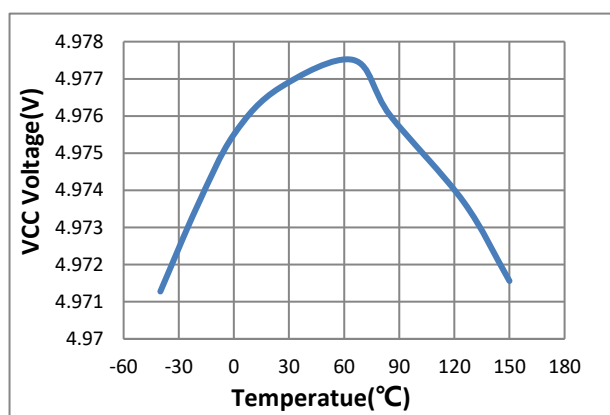


Figure 8-7. VCC Voltage

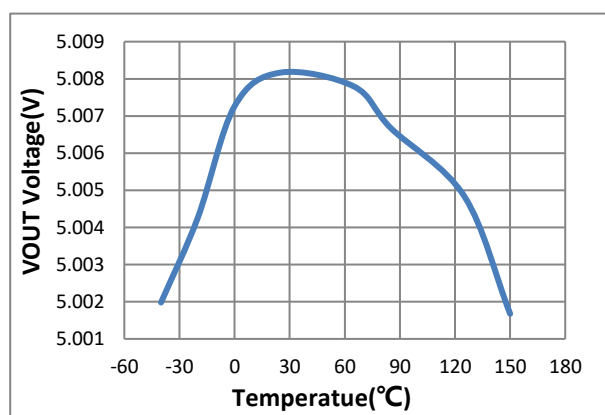
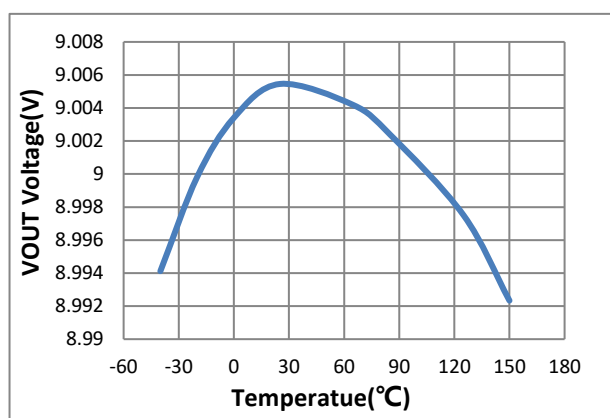
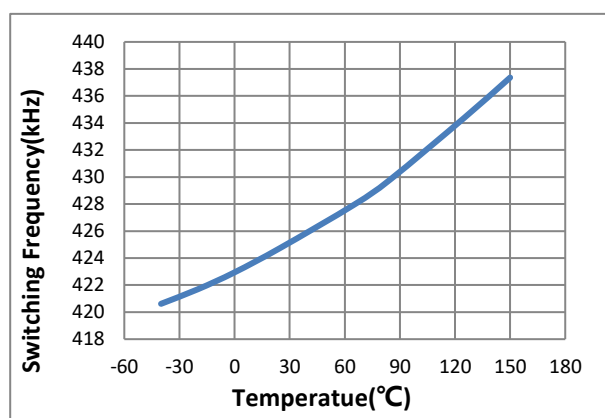
Figure 8-8. V_{OUT} Voltage-5VFigure 8-9. V_{OUT} Voltage-9V

Figure 8-10. Switching Frequency

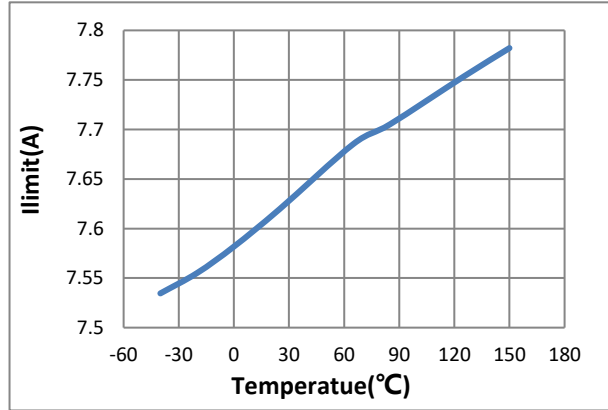


Figure 8-11. Buck High-side peak current limit

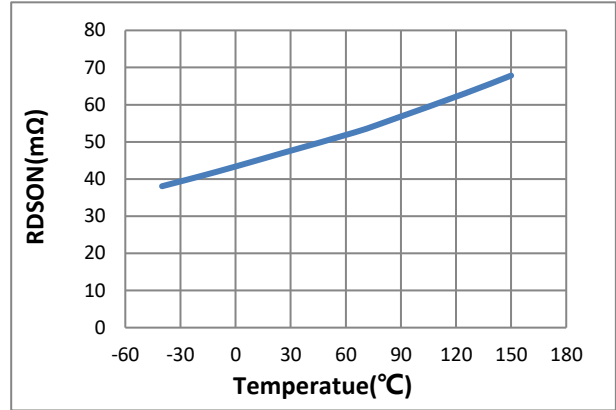


Figure 8-12. Buck high-side fet on-resistance

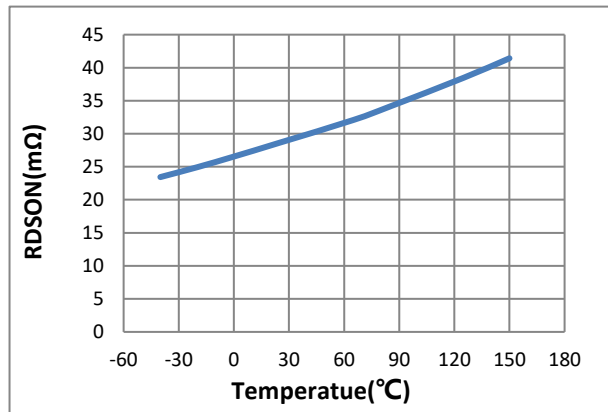


Figure 8-13. Buck low-side fet on-resistance

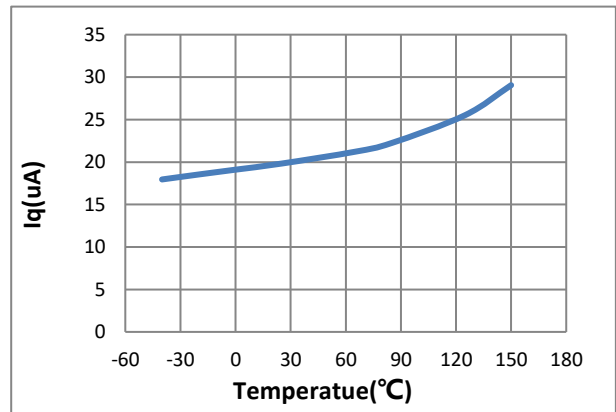


Figure 8-14. IQ Shutdown

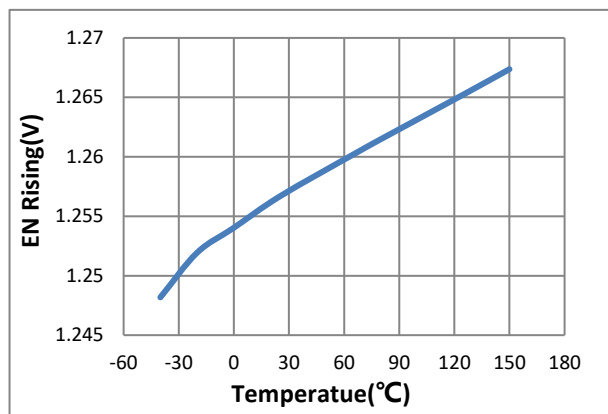


Figure 8-15. Enable Rising Thresholds

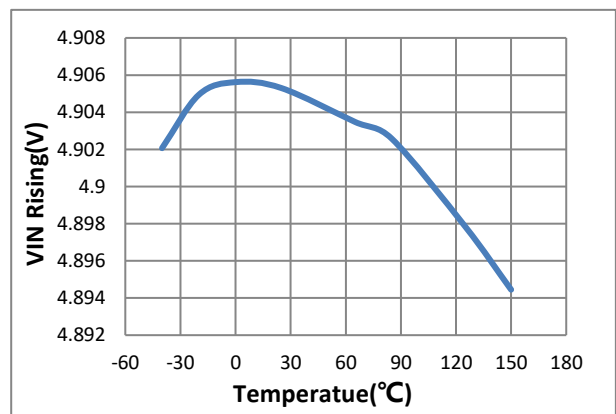


Figure 8-16. VIN UVLO Rising

8.7 Typical Performance Characteristics

V_{IN}=12V, V_{OUT}=5V, L=4.7μH, F_{SW}=420kHz, mode=FPWM with spread spectrum, T_A=25°C, unless otherwise noted.

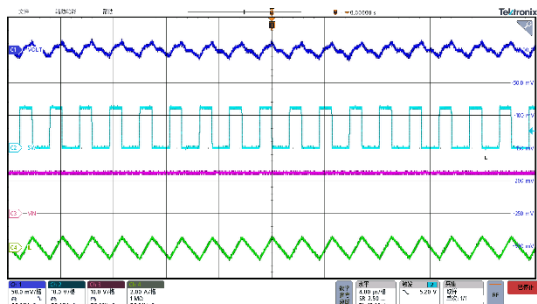


Figure 8-17. Steady State, $V_{OUT}=5V$, $I_{OUT}=0A$

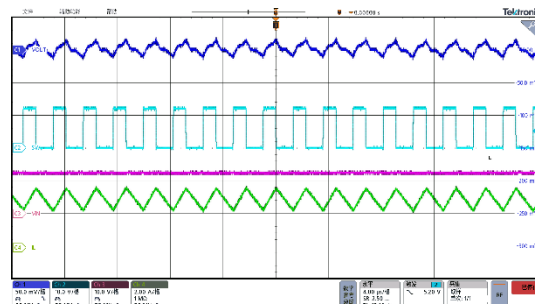


Figure 8-18. Steady State, $V_{OUT}=5V$, $I_{OUT} = 3A$

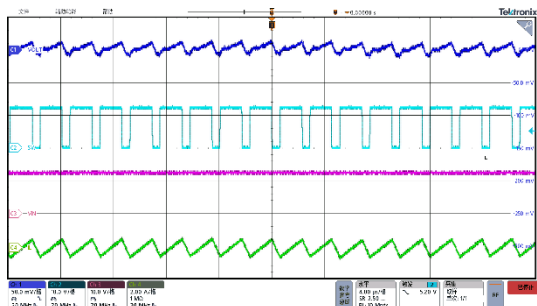


Figure 8-19. Steady State, $V_{OUT}=9V$, $I_{OUT} = 0A$

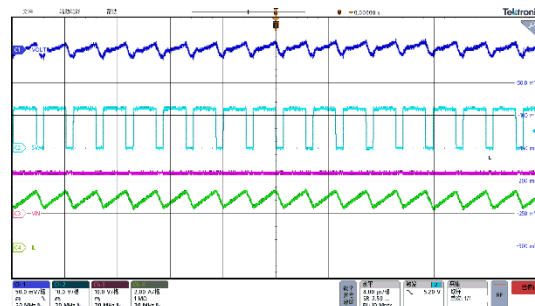


Figure 8-20. Steady State, $V_{OUT}=9V$, $I_{OUT} = 3A$

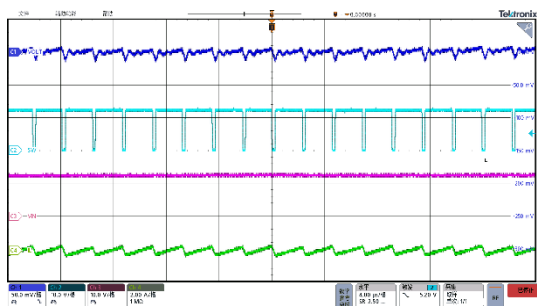


Figure 8-21. Steady State, $V_{OUT}=11V$, $I_{OUT} = 0A$

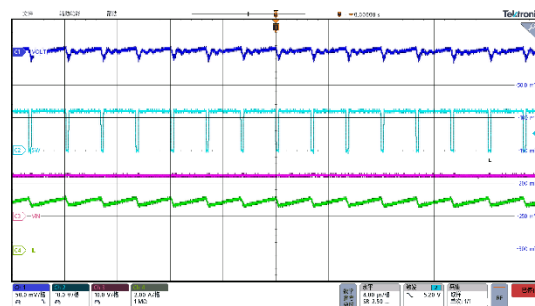
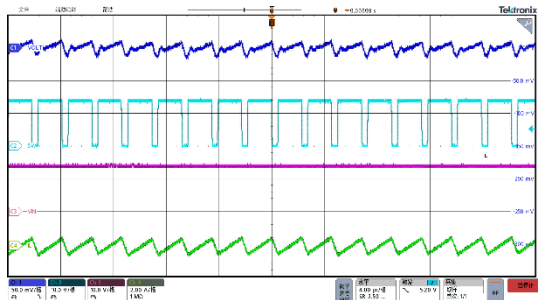
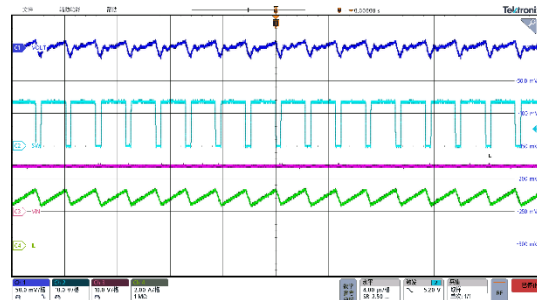
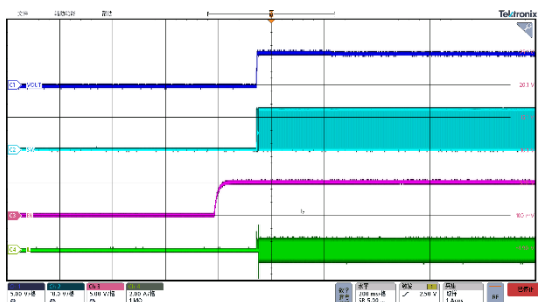
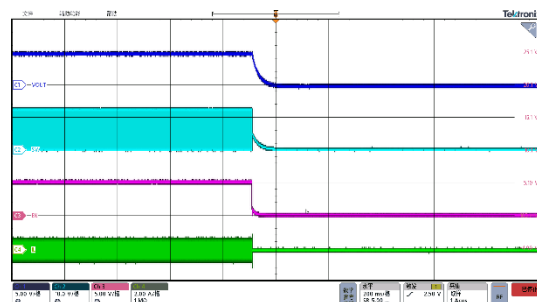
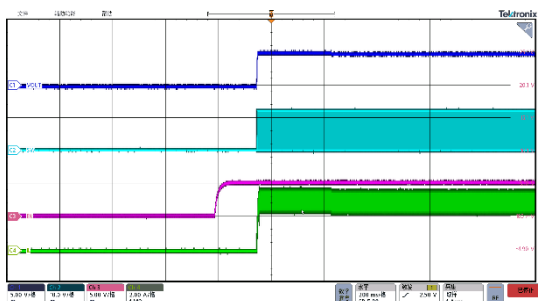
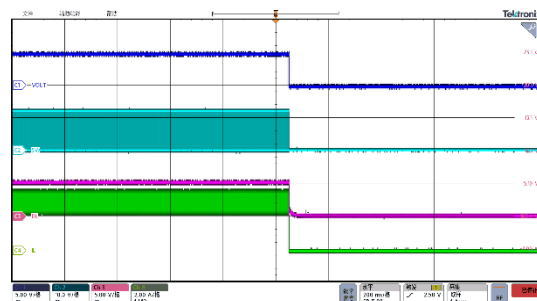


Figure 8-22. Steady State, $V_{OUT}=11V$, $I_{OUT} = 3A$

Figure 8-23. Steady State, $V_{IN}=13.5V$, $V_{OUT}=11V$, $I_{OUT}=0A$ Figure 8-24. Steady State, $V_{IN}=13.5V$, $V_{OUT}=11V$, $I_{OUT}=3A$ Figure 8-25. Start up through EN; $I_{OUT}=0A$ Figure 8-26. Shut down through EN; $I_{OUT}=0A$ Figure 8-27. Start up through EN; $I_{OUT}=3A$ Figure 8-28. Shut down through EN; $I_{OUT}=3A$

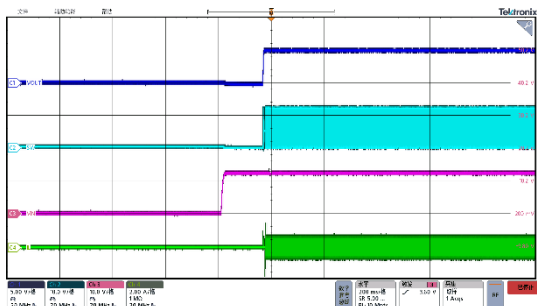


Figure 8-29. Start up through V_{IN} ; $I_{OUT} = 0A$

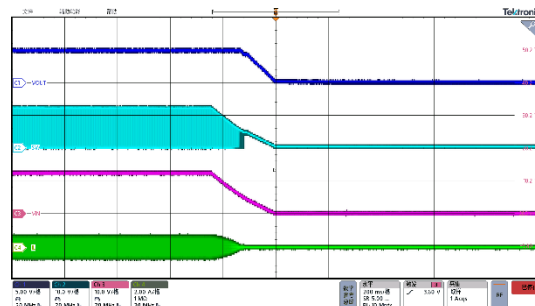


Figure 8-30. Shut down through V_{IN} ; $I_{OUT} = 0A$

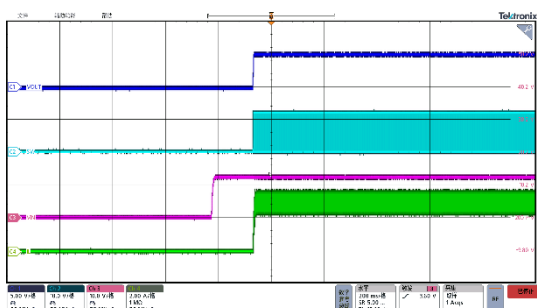


Figure 8-31. Start up through V_{IN} ; $I_{OUT} = 3A$

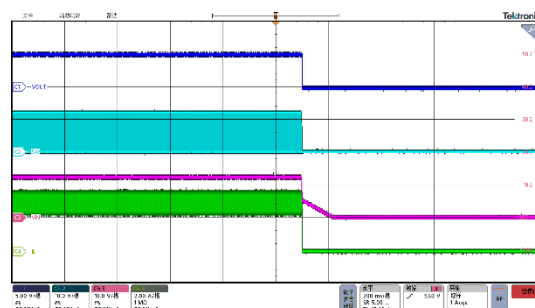


Figure 8-32. Shut down through V_{IN} ; $I_{OUT} = 3A$

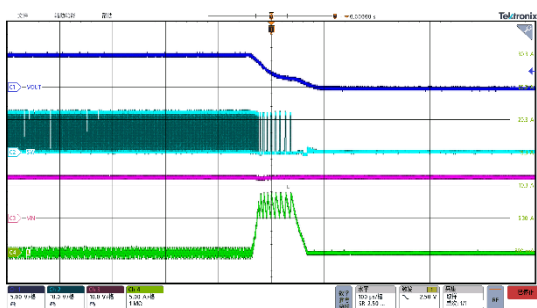


Figure 8-33. SCP Entry

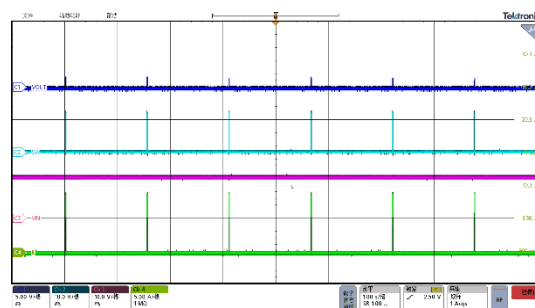


Figure 8-34. SCP Steady State

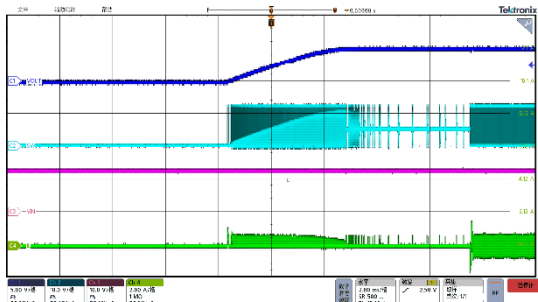


Figure 8-35. SCP Recovery

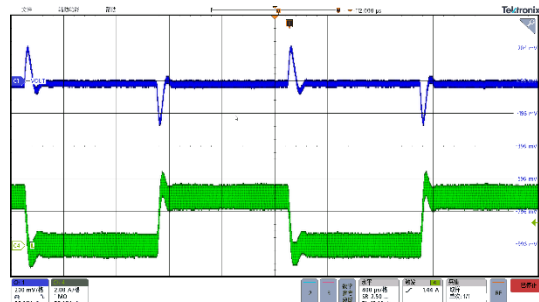
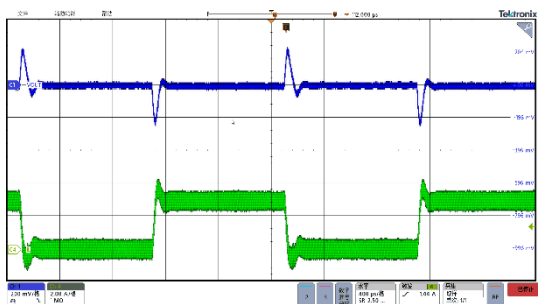
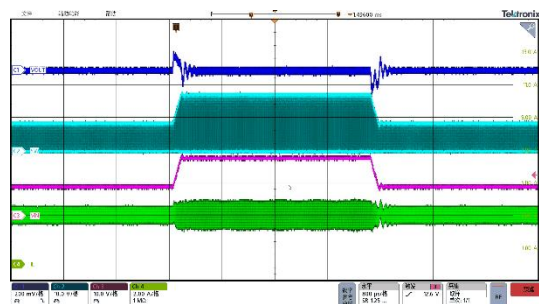
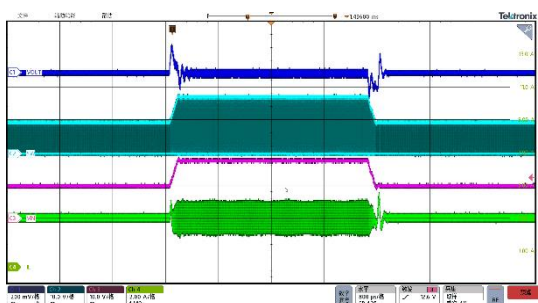
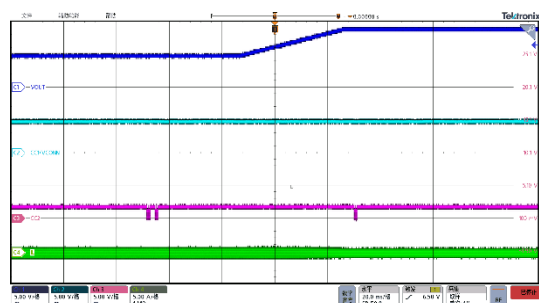
Figure 8-36. Load Transient, $V_{OUT}=5V$, $I_{OUT}=0-3A$ Figure 8-37. Load Transient, $V_{OUT}=9V$, $I_{OUT}=0-3A$ Figure 8-38. Line Transient, $V_{IN}=9-18V$, $V_{OUT}=5V$, $I_{OUT}=3A$ Figure 8-39. Line Transient, $V_{IN}=10-18V$, $V_{OUT}=9V$, $I_{OUT}=3A$ 

Figure 8-40. PDO Transition 5V-9V

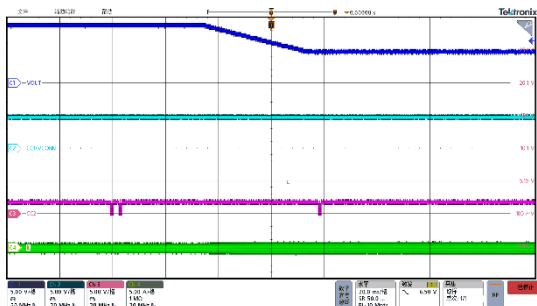


Figure 8-41. PDO Transition 9V-5V

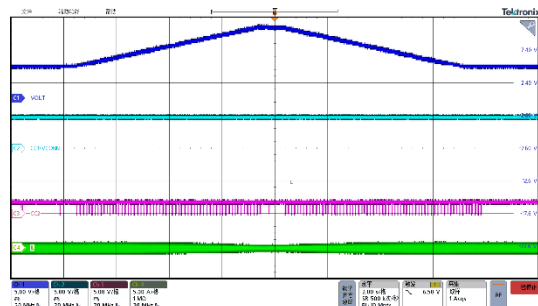


Figure 8-42. PDO Transition PPS 5V-11V-5V

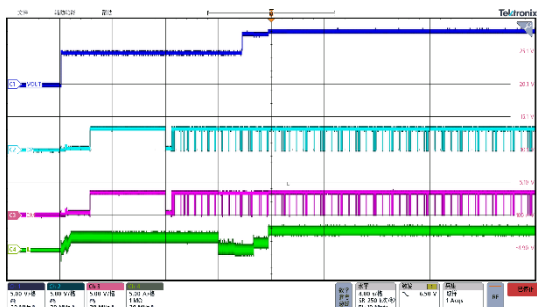


Figure 8-43. UFCS Charging Test

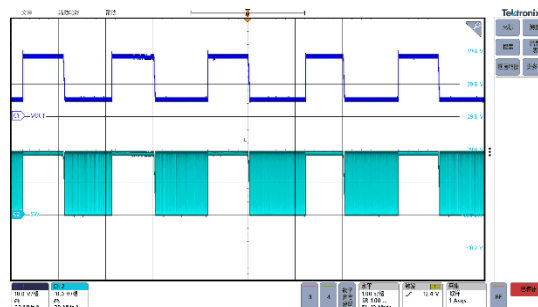


Figure 8-44. VOUT Short to 18V Battery

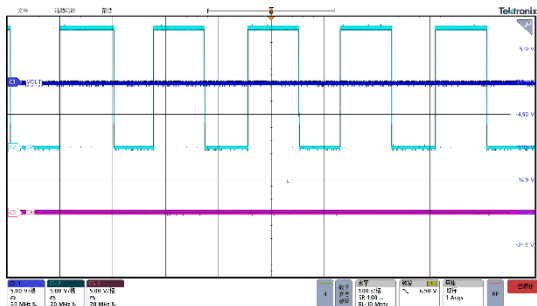


Figure 8-45. DP Short to 18V Battery

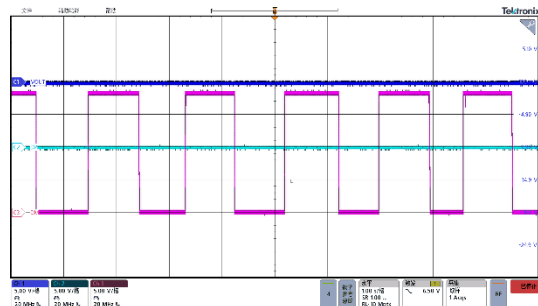


Figure 8-46. DM Short to 18V Battery

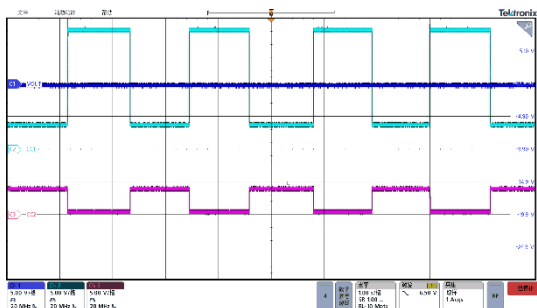


Figure 8-47. CC1 Short to 18V Battery (Detach)

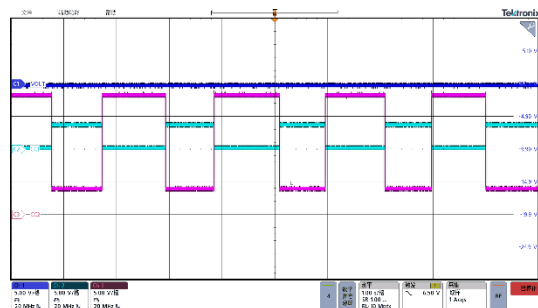


Figure 8-48. CC2 Short to 18V Battery (Detach)

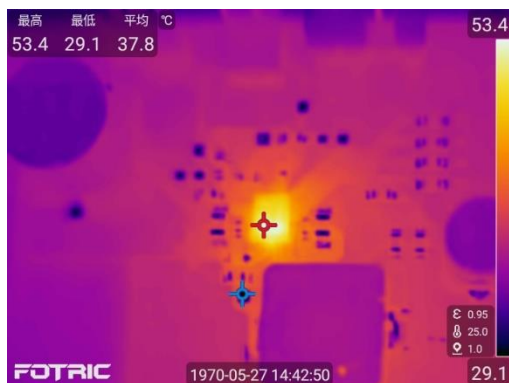


Figure 8-49. Thermal Image;
 $V_{IN}=12V$, $V_{OUT}=5V$, $I_{OUT}=3A$, $f_{SW}=420kHz$, top/bottom
layer: 2oz, mid-layer: 1oz

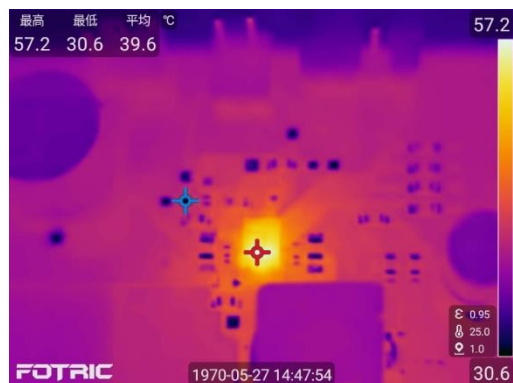


Figure 8-50. Thermal Image;
 $V_{IN}=12V$, $V_{OUT}=9V$, $I_{OUT}=3A$, $f_{SW}=420kHz$, top/bottom
layer: 2oz, mid-layer: 1oz



9 Functional Block Diagram

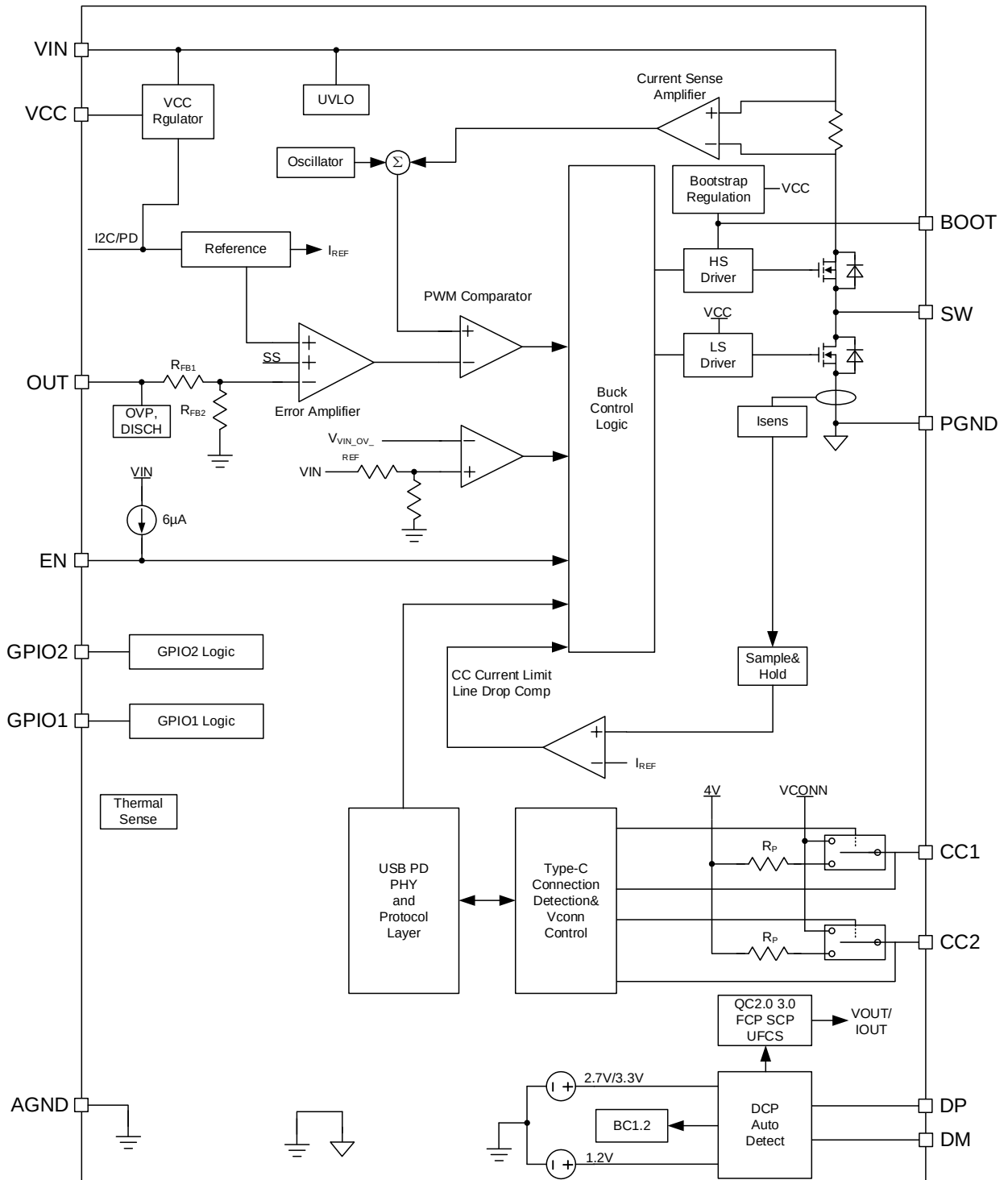


Figure 9-1. Function Block



10 Feature Description

10.1 Overview

SC81535Q is a wide range of 4.9V to 26V input voltage and an output voltage of 3.3V to 12V buck DCDC converter with 2-MOSFETs and USB Charging protocols integrated. Implementing peak current mode, SC81535Q is able to provide excellent line and load transient performance. SC81535Q could be configured during three frequency options 250kHz / 420kHz / 2100kHz to achieve small filter size or higher efficiency.

10.2 Buck Converter

SC81535Q integrates a synchronous buck converter with high-side and low-side switches inside. It regulates the output voltage by adjusting the duty cycle of HS switch and LS switch. When the high-side switch is ON, the inductor current i_L increase with linear slope $(V_{IN} - V_{OUT}) / L$. The low-side switch is turned on after HS switch is turned off and dead time.

10.3 VCC Power Supply

An internal LDO to supply SC81535Q outputs regulated 5V at the VCC pin. The VCC will get the source from VIN.

Both VCC and BT should have enough voltage to enable SC81535Q. A high-quality ceramic cap of 4.7μF or higher is required between this pin and AGND.

10.4 Input Undervoltage Lockout

When the input voltage is above than 4.9V, the SC81535Q can be enabled by pulling EN pin to a high voltage above 1.32V. When it starts running, SC81535Q couldn't be disabled until the input voltage is below 4.7V.

10.5 EN Control

The SC81535Q has an enable control pin(EN). The voltage on the EN pin controls the ON/OFF operation. A voltage of less than 0.94V shuts down the device, while a voltage of greater than 1.32V is required to start the device. EN pin has internal 6μA pull-up.

SC81535Q EN is a high voltage pin, it can be connected to VIN directly or through resistor. It could establish a precision system UVLO level by inserting a resistor. An external logic signal can also be used to drive EN input for system sequencing and protection.

10.6 Soft Start

The integrated soft-start circuit prevents input inrush current and the input power supply. Soft start is achieved by slowly

ramping up the internal reference voltage when the device is first enabled or powered up.

10.7 Output Current Limit and Hiccup

If IOUT current exceeds the set constant current limit threshold in PPS,SCP or UFCS mode, SC81535Q will enter constant current limit mode. In this mode the current amplitude is limited. As the reducing of load resistance, output voltage drops. Once the output voltage is lower than 4.4V, SC81535Q will enters hiccup mode to periodically restart the part.

10.8 Switching Current Limit

SC81535Q limits both inductor's peak current and valley current through cycle-by-cycle current limiting. Peak current limit is implemented by sensing the current in high-side switch after a short blanking time.

In terms of valley current limit, the low-side switch's current is sensed and limited. Before low-side switch is turned off, its current is compared with IL-LS. If the current is higher than IL-LS, the low-side switch's ON time is extended until LSFET's current is lower than IL-LS. Then high-side switch is allowed to turn on per duty controlled by compensation loop.

10.9 Output Over-Voltage Protection

SC81535Q has output overvoltage protection, When the output voltage is higher than 120% of VREF, the SC81535Q turns off both high-side switch and low-side switch. The discharge path from OUT to ground will turn on. If the OUT pin voltage drops to 115% of VREF, the device will return to normal operation.

10.10 Input Over-Voltage Protection

SC81535Q has Input over-voltage protection. If the input voltage is higher than VIN OVP rising threshold (typical 26.7V), the SC81535Q turns off both high-side switch and low-side switch. When the input voltage drops to VIN OVP falling threshold, the chip returns to normal operation. VIN OVP is controlled by OTP trim.

10.11 Switching Frequency and Spread Spectrum Function

SC81535Q frequency could be selectable at 250kHz, 420kHz and 2100kHz by OTP trim. Normally a 420kHz frequency is recommended. SC81535Q has a frequency spread spectrum function, which could help minimize the peak emissions. SC81535Q uses a triangle wave to modulate the internal oscillator, whose frequency is 1/256



of the switching frequency. The frequency span of the spread spectrum operation is 6%.

10.12 Shutdown and Load Discharge

When EN pin voltage is pulled down below 0.94V, the SC81535Q is in shutdown mode and all functions are disabled. SC81535Q integrates output discharge function when the output voltage needs to be discharged to the goal voltage.

10.13 Output Line Drop Compensation

SC81535Q is capable of compensating an output voltage drop, which is helpful when there is high impedance at the output side. The compensated voltage is impacted by the output current and the line drop compensation gain. Refer to the OTP trim map for detail line drop compensation amplitude.

10.14 Thermal Shutdown

SC81535Q is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165C(Typical). The internal soft-start circuit is reset but all internal registers values remain unchanged. The DCDC portion will automatically restarts when the junction temperature drops below the thermal shutdown hysteresis.

10.15 CC Interface

SC81535Q use the function of the configuration channel (CC1/CC2 pin) to detect connections and configure the interface across the USB Type-C cables. The detection concept is based on being able to detect terminations in the product. To define the functional behavior of CC, a pull-up resistor (RP) and pull-down resistor termination model is used ad below. A pull-up termination can be replaced by a current source.

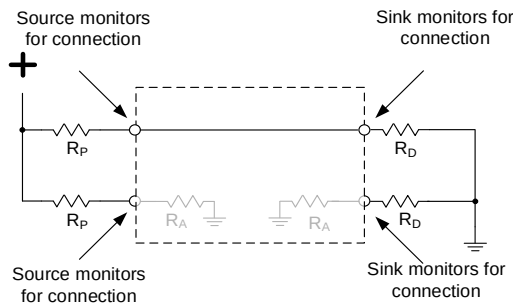


Figure 10-1 USB Type-C Connection

10.16 DPDM Interface

The SC81535Q contains DPDM interface. The DPDM interfaces are available for USB-A port applications or

Type-C port applications. It supports Apple-3A, 1.2V/1.2V Mode, BC1.2 DCP/CDP, HVDCP, QC2.0, QC3.0, FCP, SCP and UFCS.

SC81535Q supports Apple-3A mode, which broadcasts 2.7V voltage on DP and 3.3V voltage on DM pin with 30kΩ output impedance.

If a BC1.2 device is attached, SC81535Q operates in 1.2V/1.2V and DCP mode, which complies with the BC1.2 specification. SC81535Q shorts DP and DM pin through a 20Ω resistor.

SC81535Q supports HVDCP mode for some high voltage protocols. Under HVDCP mode, DP and DM can check the voltage by internal comparators or detect some proprietary fast charging protocols such as FCP, SCP, UFCS, QC2.0 or QC3.0.

SC81535Q also supports BC1.2 CDP (Charging Downstream Port) handshaking as well. It can be enabled by OTP.

10.17 VCONN Switch

SC81535Q features a 20mA VCONN power with a fixed Overcurrent Protection (OCP) of 35mA.

The IC supports electronically marked cables assembly for more than 3A power delivery. By default, passive cables support up to 3A. The IC can check the cable types through internal CC comparators. If an e-marker cable is detected, the IC supplies the cable with VCONN and communicates with it to check the cable current ratings. Therefore, source power supply advertises any PDO if cable is identified as able to sustain such current.

When VCONN switch is turned on, SC81535Q will continuously monitor current on CC pin. If VCONN output current is above 35mA, VCONN switch is turned off.

10.18 USB PD Protocol

The IC provides USB PD physical layer for PD protocols communication. The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.1 standard. Once the insertion direction of Type-C port is detected by CC comparator, the IC can select either CC1 or CC2 channels to send and receive PD packets. All processes of PD communication are controlled by state machine.

10.19 NTC Function

When the GPIO1 pin is set to the NTC_POWER_SHARE_1 function, the device compares the voltage of GPIO1 to



VREF (0.5V Typical). If the voltage is below the threshold, the device will reduce the PD power.

PD power of NTC_POWER_SHARE_1 status can be configured via OTP by NTC_PS_PDO_SELECT in Table 1.

If the voltage of GPIO1 rises above the recovery threshold (1V Typical), the device recovers to a normal state.

10.20 Low-Battery Operation

If the SC81535Q detects that the battery voltage (its VIN voltage) is lower than the VBATT_LOW_THLD1 falling threshold(11.8V Typical), it reduces the PD power rating according to the set value. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP.

If the SC81535Q detects that the battery voltage (its VIN voltage) is below 10.2V, it reduces the PD power rating to 15W. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP.

PD power of Low-Battery1 status can be configured via OTP by VBATT_LOW1_PDO_SELECT in Table 1.

When the battery voltage recovers and exceeds the VBATT_LOW_THLD rising threshold with a 1s digital deglitch time, the PDO recovers to normal PDP.

The VBATT_LOW detection circuitry starts to work when a USB Type-C receptacle is attached; it is reset by UVLO or an EN shutdown. It can be disabled by OTP.

10.21 GPIO1 Power Share1 Function

The GPIO1_POWER_SHARE falling threshold is typically 0.5V. If the second SC81535Q (SC81535Q-B) detects that a valid sink is attached in, the first SC81535Q's (SC81535Q-A) GPIO1_POWER_SHARE pin is pulled down by the SC81535Q-B's GPIO2_ATTACH pin (see Figure 10-2).

When the power share function is triggered, the PDO list and current are determined by NTC_PS_PDO_SELECT.

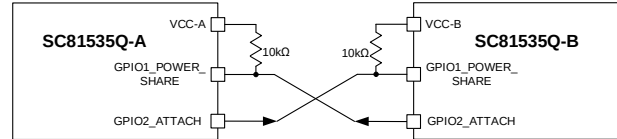


Figure 10-2 GPIO1 Power Share Connection Between Two SC81535Qs

10.22 GPIO2 Power Share2 Function

The GPIO2_POWER_SHARE rising threshold is typically 1.87V(VTH_PS_R). When the GPIO2 pin is set for the power share function, and the SC81535Q-A detects that its GPIO2 voltage exceeds VTH_PS_R, the power share function is triggered.

The SC81535Q exits the power sharing status after the GPIO2 voltage drops below VTH_PS_F (typically 1.67V). Figure 10-3 shows the GPIO2_POWER_SHARE connection block. When VBUS exceeds 7.1V, the power share function is triggered.

PD power of Power Share1 and Power Share2 status can be configured via OTP by NTC_PS_PDO_SELECT in Table 1.

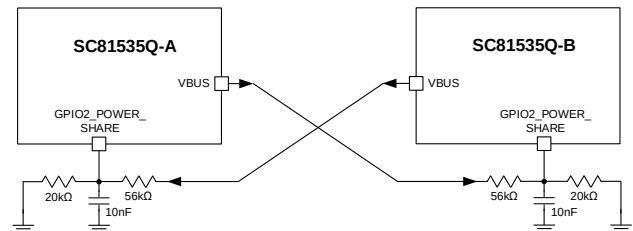


Figure 10-3 GPIO2 Power Share Connection Between Two SC81535Qs



Figure 10-4 shows the PDP state machine.

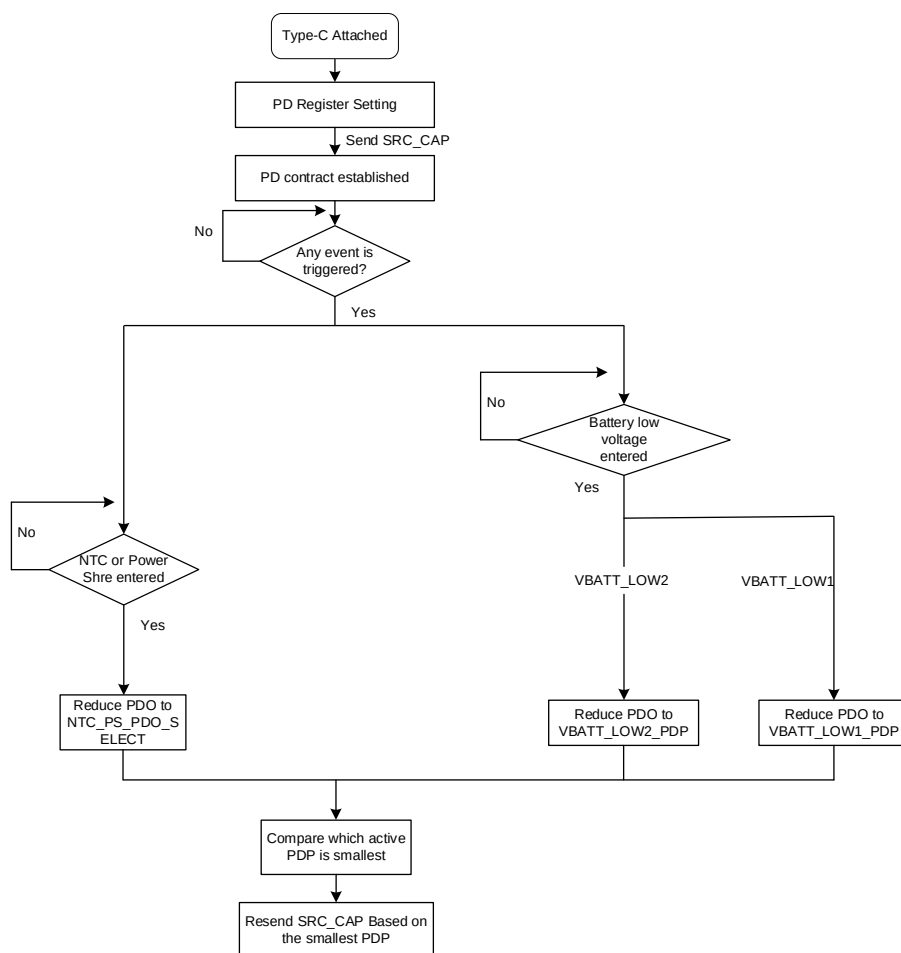


Figure 10-4 PDP State Machine



11 Application Information

11.1 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage and 25% for systems with a variable input voltage such as the 12V battery in a car. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used. **Equation 1** can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example, K = 0.4 was chosen and an inductance of approximately 5.7μH was found. The next standard value of 4.7μH was selected.

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot K \cdot I_{OUT(MAX)}} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The saturation current rating of the inductor must be at least as large as the high-side switch current limit, IL-HS (see Section 10.8). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, IL-LS, is designed to reduce the risk of current run-away, a saturated inductor can cause the current to rise to high values very rapidly. This can lead to component damage; do not allow the inductor to saturate. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies typically above 1MHz. To avoid subharmonic oscillation, the inductance value must not be less than that given in **Equation 2**. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L \geq 0.32 \cdot \frac{V_{OUT}}{F_{SW}} \quad (2)$$

Equation 2 assumes that this design must operate with input voltage near or in dropout. If minimum operating

voltage for this design is high enough to limit duty factor to below 50%, **Equation 3** can be used in place of **Equation 2**.

$$L \geq 0.2 \cdot \frac{V_{OUT}}{F_{SW}} \quad (3)$$

Note that choosing an inductor that is larger than the minimum inductance calculated using **Equation 1** through **Equation 3** results in less output capacitance being needed to limit output ripple but more output capacitance being needed to manage large load transients. See Section 11.2.

11.2 Output Capacitor Selection

The value of the output capacitor and its ESR determine the output voltage ripple, control loop stability and load transient performance. **Table 11-1** can be used to find the output capacitor for a few common applications.

Table 11-1. Recommended Output Capacitors

F _{SW}	Recommendation 1	Recommendation 2
250kHz	220μF (Electrolytic capacitor, ESR<50mΩ) +10μF+0.1μF MLCC	100μF (Electrolytic capacitor, ESR<50mΩ) +10μF+0.1μF MLCC
420kHz	4X22μF+0.1μF MLCC	100μF (Electrolytic capacitor, ESR<50mΩ) +10μF+0.1μF MLCC
2.1MHz	2X22μF+0.1μF MLCC	NA

Most ceramic capacitors deliver far less capacitance than the rating of the capacitor indicates. Be sure to check any capacitor selected for initial accuracy, temperature derating, and voltage derating. **Table 11-1** have been generated assuming typical derating for 16V, X7R, automotive grade capacitors. If lower voltage, non-automotive grade, or lower temperature rated capacitors are used, more capacitors than listed are likely to be needed.

11.3 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the converter to supply the ripple current and isolate switching noise from other circuits. A minimum of 10μF of ceramic capacitance is required on the input of the device. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased



to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size 100nF ceramic capacitor must be used at input/ground pin pair, immediately adjacent to the converter. This provides a high-frequency bypass for the control circuits internal to the device. These capacitors also suppress SW node ringing, which reduces the maximum voltage present on the SW node and EMI. The 100nF must also be rated at 50V with an X7R or better dielectric.

Many times, it is desirable and necessary to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads or traces are used to connect the input supply to the converter. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the input ceramic capacitors. The approximate worst-case RMS value of this current can be calculated from **Equation 4** and must be checked against the manufacturers' maximum ratings.

$$I_{RMS} \approx \frac{I_{OUT}}{2} \quad (4)$$

11.4 BOOT Capacitor Selection

The SC81535Q requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high-side power MOSFET. A high-quality (X7R) ceramic capacitor of 100nF and at least 50V is recommended.

11.5 BOOT Resistor Selection

A BOOT resistor and capacitor can be connected in series between the BOOT and SW pins. Unless EMI for the application being designed is critical, R_{BOOT} can be shorted. To maximize efficiency, 0Ω is chosen for this example. Under most circumstances, selecting an R_{BOOT} resistor value above 20Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

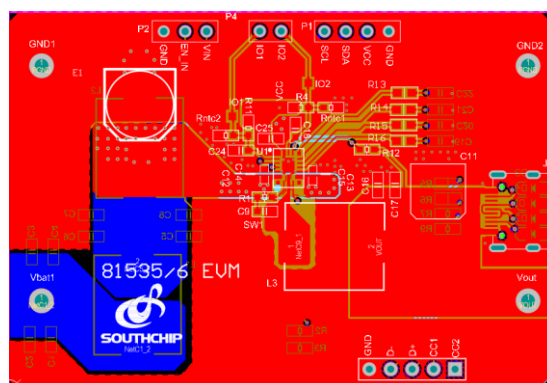
11.6 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a $4.7\mu F$, 16V ceramic capacitor connected from VCC to GND for proper operation. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup (FLT or POL function) or logic level. A pullup resistor with a value of $10k\Omega$ is a good choice in this case.

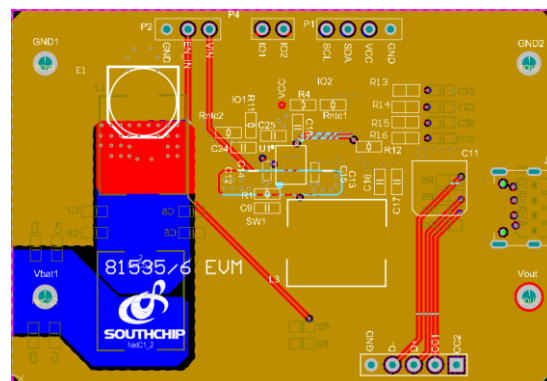
12 Layout Guide

The PCB layout is critical to get the optimal performance and thermal dissipation. For SC81535Q, the loop consisting of VIN-SW-GND and VIN-SW-OUT is the most important. Poor layout means larger parasitic parameters and noise. Generally, to reduce the PCB inductance, the area of this loop must be small, and the trace must be wide. Figure 12-1 shows a recommended layout.

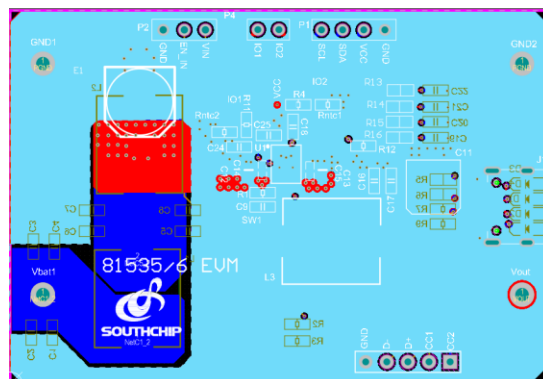
1. Place the ceramic input capacitors as close to VIN pin and GND as possible, especially the small package size (recommend 0402) input bypass capacitor. With the QFN package, there are two VIN/PGND pairs on either side of the package, VIN1 to PGND1 and VIN2 to PGND2, which provides for a symmetrical layout and helps minimize switching noise and EMI generation
2. The VIN, OUT and GND paths must be wide and short enough to reduce any voltage drops on the input or output paths of the converter.
3. Minimize the parasitic inductance of the input and output by using wide and short traces. Minimize the parasitic inductance of the input by placing the input capacitors as close to the input pins as possible. Minimize the parasitic inductance of the output by placing the output capacitors as close to the output pins as possible.
4. Minimize the parasitic inductance of the input and output by using wide and short traces. Minimize the parasitic inductance of the input by placing the input capacitors as close to the input pins as possible. Minimize the parasitic inductance of the output by placing the output capacitors as close to the output pins as possible.
5. Minimize the parasitic inductance of the input and output by using wide and short traces. Minimize the parasitic inductance of the input by placing the input capacitors as close to the input pins as possible. Minimize the parasitic inductance of the output by placing the output capacitors as close to the output pins as possible.
6. Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.
7. If an R_{BOOT} resistor is used, place it as close as possible to BOOT pins. If high efficiency is desired, R_{BOOT} can be shorted.



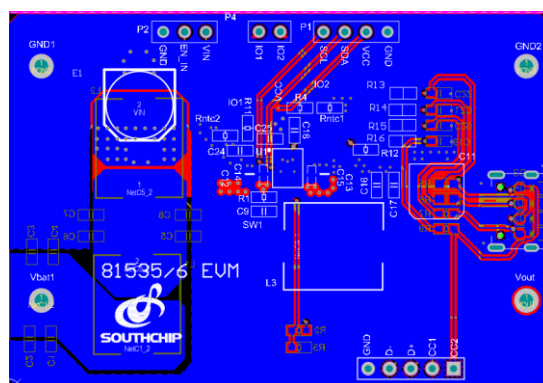
(a) Top Layer



(b) GND1 Layer



(c) GND2 Layer



(d) Bottom Layer

Figure 12-1 Layout Example

13 Typical Application Circuits

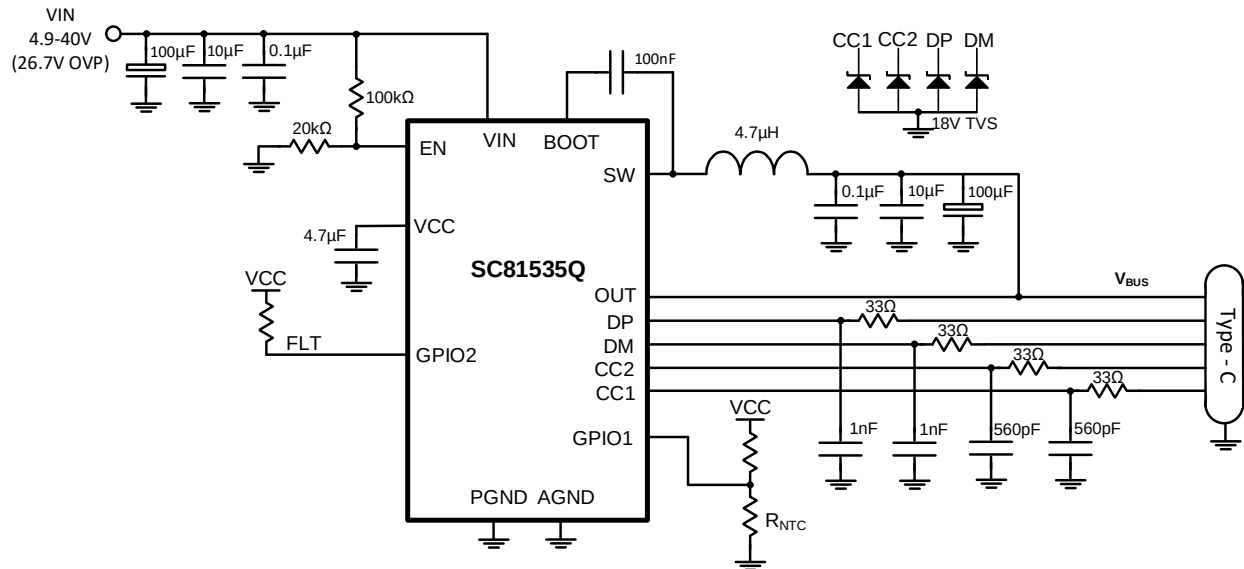


Figure 13-1 SC81535Q 27W PD and 33W UFCS Application

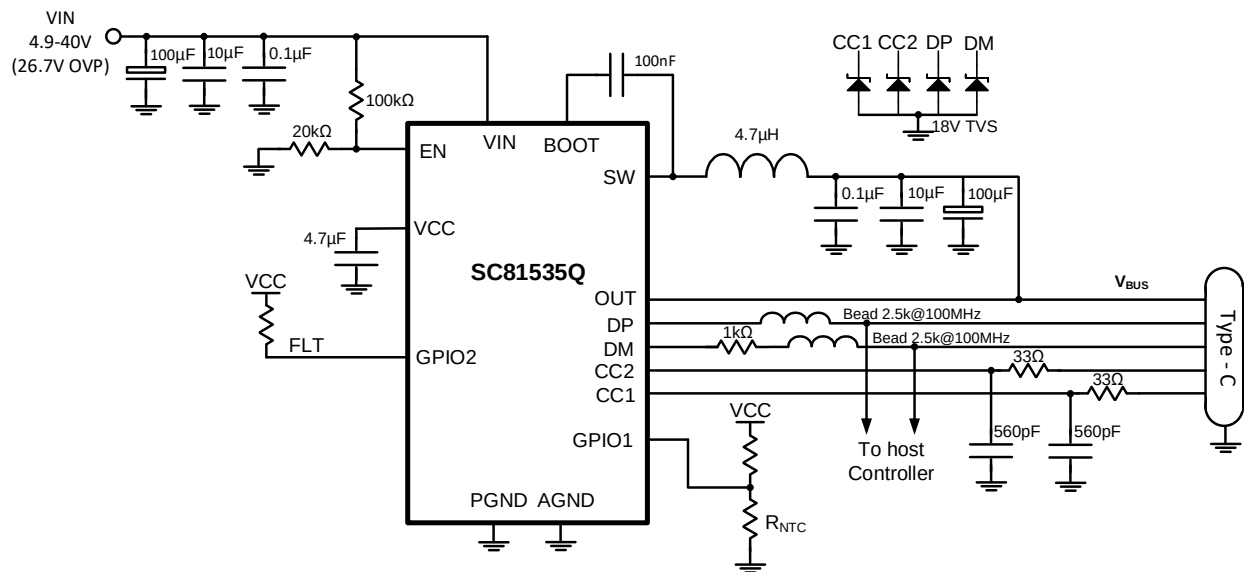


Figure 13-2 SC81535Q 27W PD+USB2.0 Application



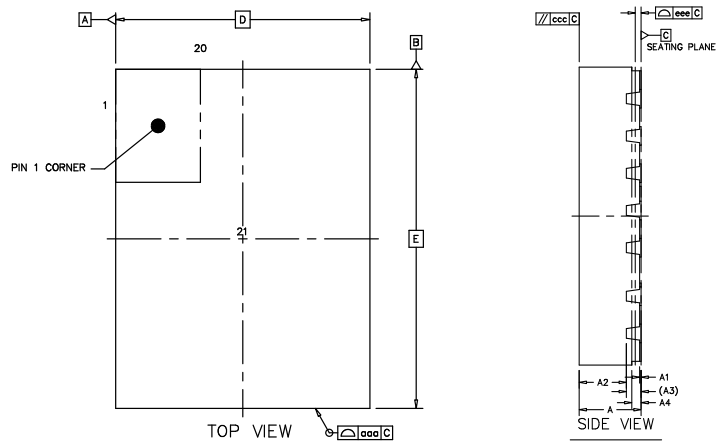
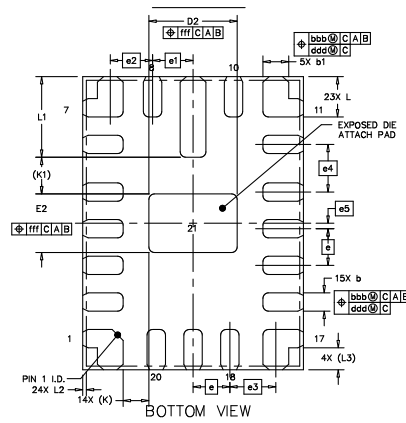
14 Configuration Table

Table1 OTP Description

OTP Items	Description	Value
GPIO1	Configures the GPIO1 pin's function.	0: POL 1: NTC_POWER_SHARE_1 2 :NA 3: Attach_FLT_ALT
GPIO2	Configures the GPIO2 pin's function.	0: NA 1: ATTACH 2: POWER_SHARE_2 3: FAULT
PDP_SEL	Set the default power.	0:27W 1:15W
VBATT_LOW	Set the VIN detection function	0:Enable 1:Disable
VBATT_LOW1_PDO_SELECT	Sets the maximum power rating when VBATT falls below its first threshold.	0: 15W 1: 18W 2: 20W 3: 27W
NTC_PS_PDO_SELECT	Set the thresholds to which the PDO power rating is reduced.	0: 15W 1: 18W 2: 20W 3: 27W
VBUS_VOLTAGE	Sets the default VBUS voltage.	0: 5.16V 1: 5.06V
FREQ	Sets the switching frequency.	0: 420kHz 1: 250kHz 2: 2100kHz 3: NA
LINE_DROP_COMP	Sets the output voltage compensation vs load feature.	0: No LDC 1: 100mV@3A 2: 300mV@3A 3: 600mV@3A
VIN_OVP	. VIN_OVP function	0: 26.7V 1: 17.8V
CDP_EN	Select CDP mode	0:Disable 1:Enable
USB_COM	Select USB_COMMUNICATE bit in PD source cap	0:Disable 1:Enable



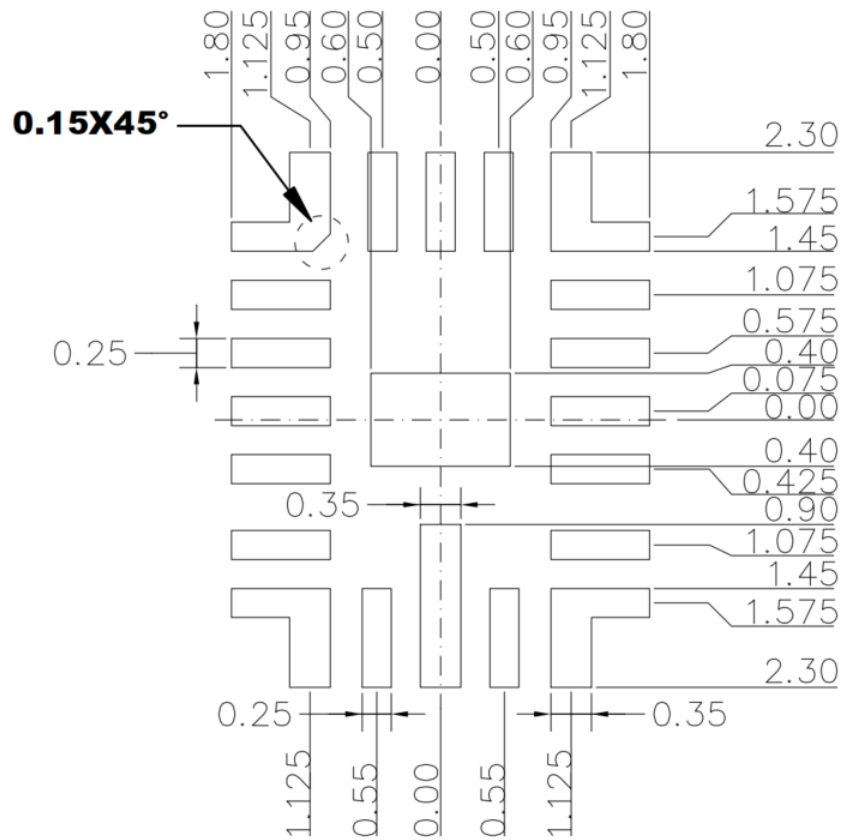
MCHANICAL DATA



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.65	---
L/F THICKNESS	A3	---	0.203 REF	---
SIDE WETTABLE DEPTH	A4	0.075	---	0.18
LEAD WIDTH	b	0.2	0.25	0.3
	b1	0.3	0.35	0.4
BODY SIZE	X	D	3 BSC	
	Y	E	4 BSC	
LEAD PITCH	e	0.5 BSC		
	e1	0.55 BSC		
	e2	0.575 BSC		
	e3	0.625 BSC		
	e4	0.65 BSC		
LEAD CENTER TO PACKAGE CENTER	e5	0.075 BSC		
EP SIZE	X	D2	1.1	1.2
	Y	E2	0.7	0.8
LEAD LENGTH	L	0.45	0.55	0.65
	L1	1	1.1	1.2
SIDE WETTABLE WIDTH	L2	0.01	---	0.09
LEAD EDGE TO PACKAGE EDGE	L3	---	0.3 REF	
LEAD TOP TO EXPOSED PAD EDGE	K	---	0.35 REF	
	K1	---	0.5 REF	
PACKAGE EDGE TOLERANCE	aaa	---	0.1	
MOLD FLATNESS	ccc	---	0.1	
COPLANARITY	eee	---	0.08	
LEAD OFFSET	bbb	---	0.1	
	ddd	---	0.05	
EXPOSED PAD OFFSET	fff	---	0.1	



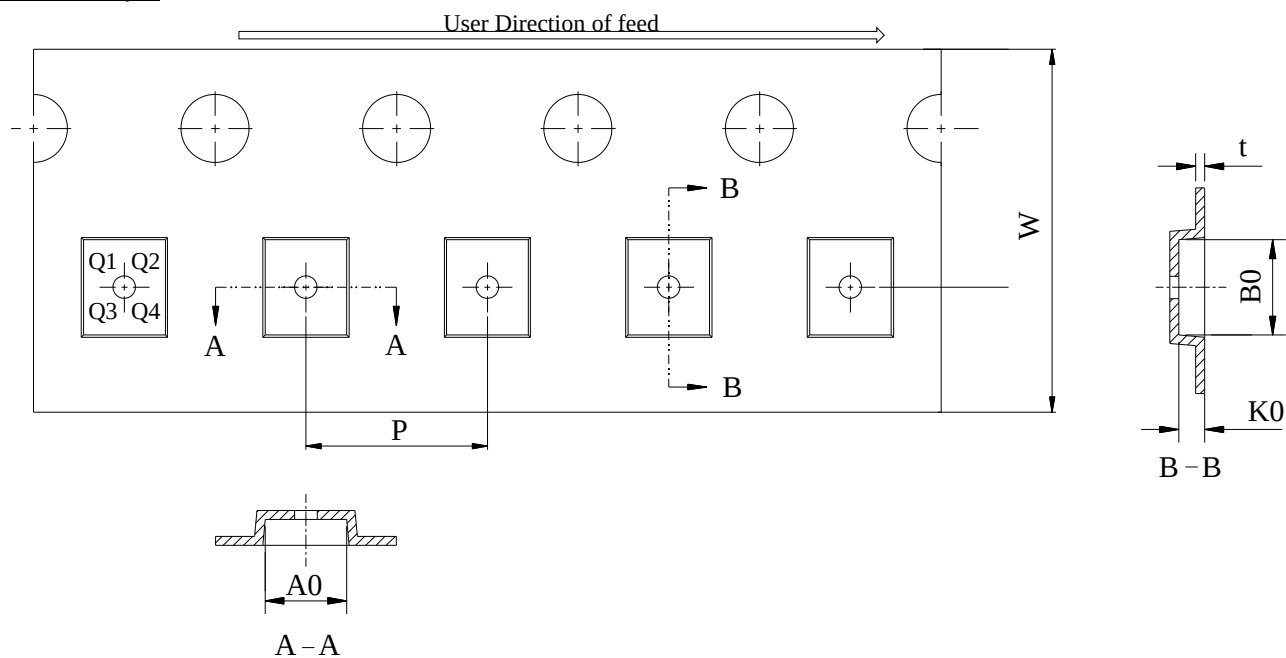
RECOMMENDED FOOTPRINT



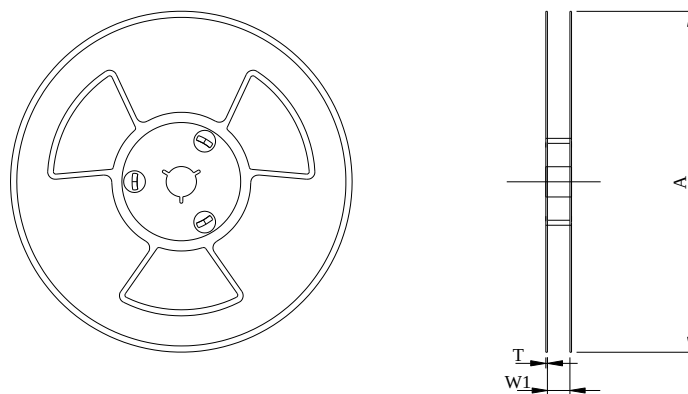
Unit: mm



TAPE AND REEL INFORMATION

Carrier Tape

Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 +0.30/-0.10	8.00 ±0.10	4.30 ±0.08	3.30 ±0.08	1.10 ±0.10	0.25 ±0.05	Q1

REEL

Item	A	W1	T
Size (mm)	330 ±1	12.4 +1/-0	2.6 +1/-0



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