

Single Cell High Efficiency 8-A Switched Capacitor Direct Charger

1 Descriptions

SC8541 is a 97% efficiency, 8-A battery charging solution using a switched cap architecture. The switched cap architecture and the integrated FETs are optimized to enable a 50% cycle, allowing the cable current to be half the current delivered to the battery, reducing the losses over the charging cable as well as limiting the temperature rise in the application.

SC8541 adopts 36pin CSP 2.68mm X 2.68mm package.

2 Applications

- Smartphones
- Tablet PCs

3 Device Information

Part Number	Package	Body Size
SC8541CFFR	CSP36	2.68mm x 2.68mm x 0.575mm

4 Features

- 11-way system protection
 - ✓ VAC1_OVP
 - ✓ VAC2_OVP
 - ✓ VBUS_OVP
 - ✓ IBUS_OCP
 - ✓ IBUS_UCP
 - ✓ VOUT_OVP
 - ✓ VBAT_OVP
 - ✓ IBAT_OCP
 - ✓ TSBUS_FLT
 - ✓ TSBAT_FLT
 - ✓ TSHUT
- 5-way charge-pump protection
 - ✓ VBUS_ERROR_HI protection before switch
 - ✓ VBUS_ERROR_LO protection before switch
 - ✓ CFLY short detection before switch
 - ✓ PMID2OUT_OVP during switch
 - ✓ PMID2OUT_UVP during switch
- 5-way system alarm
 - ✓ VBUS_OVP_ALM
 - ✓ VBAT_OVP_ALM
 - ✓ IBAT_OCP_ALM
 - ✓ TSBUS_TSBAT_ALM
 - ✓ TDIE_ALM
- 10-channel 12-bit ADC
 - ✓ VAC1,VAC2,VBUS,IBUS,VOUT,VBAT,IBAT,TSBUS,TSBAT,TDIE

5 Typical Application Circuit

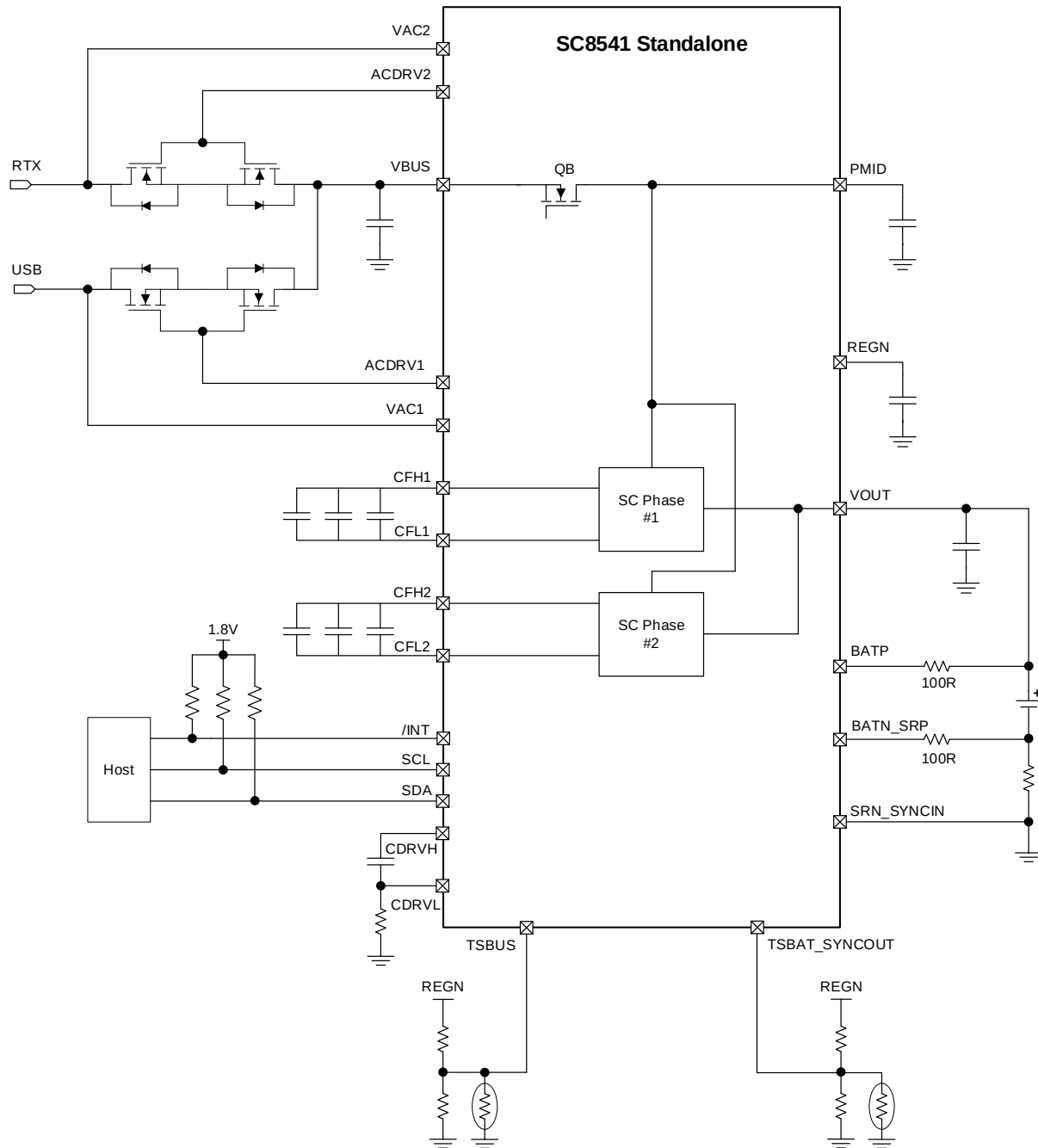
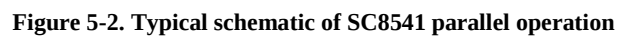
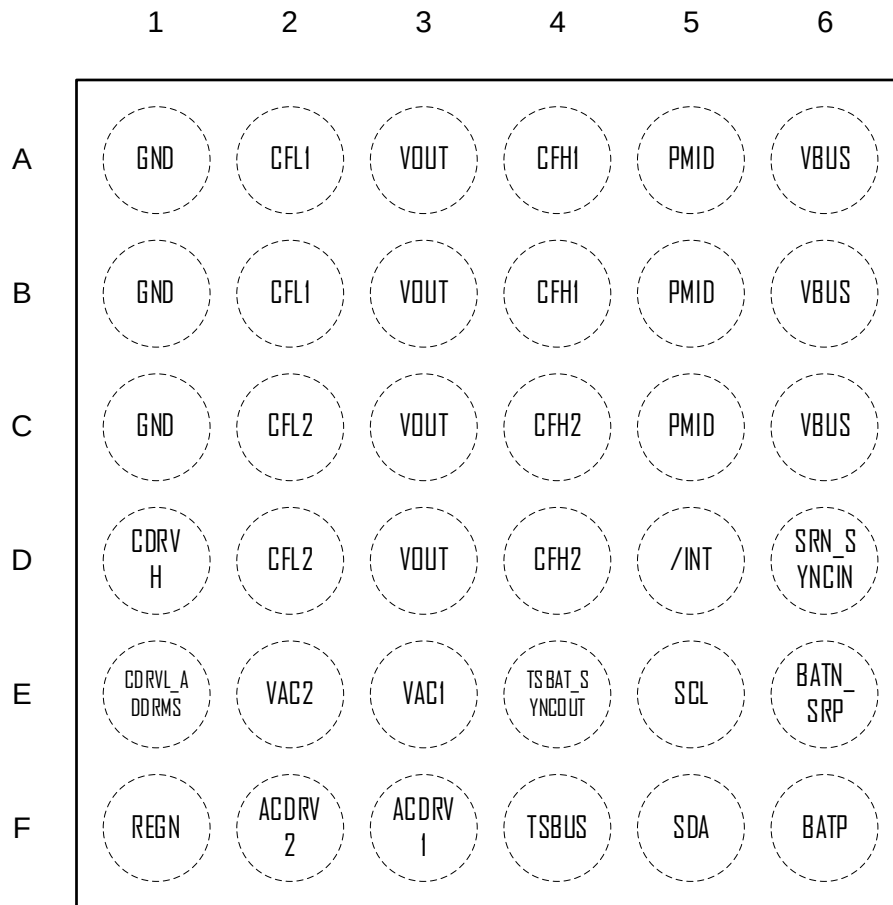


Figure 5-1. Typical schematic of SC8541 standalone operation



6 Terminal Configuration and Functions



(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
A1,B1,C1	GND	Power	Power ground
A2,B2	CFL1	Power	Flying capacitance 1 negative terminal
C2,D2	CFL2	Power	Flying capacitance 2 negative terminal
A3,B3,C3,D3	VOUT	Power	Device power output
A4,B4	CFH1	Power	Flying capacitance 1 positive terminal
C4,D4	CFH2	Power	Flying capacitance 2 positive terminal
A5,B5,C5	PMID	Power	PMID is the input to the switched cap power stage. Connect 10-μF cap to PMID

A6,B6,C6	VBUS	Power	Device power input. Place a 1- μ F bypass cap to GND as close as possible to these pins.
D1	CDRVH	I/O	Charge pump for gate drive. Connect a 0.22- μ F cap between CDRVH and CDRVL
D5	/INT	O	Open drain, active low interrupt output. Pull up to voltage with 10-k Ω resistor
D6	SRN_SYNCIN	I	Negative input for low side battery current sensing. In parallel operation, this pin can be used to monitor the clock input from master
E1	CDRVL/ADDRMS	I/O	Charge pump for gate drive. Connect a 0.22- μ F cap between CDRVH and CDRVL. In parallel operation, this pin can be used to set the I2C address
E2	VAC2	I	Input voltage sense pin2
E3	VAC1	I	Input voltage sense pin1
E4	TSBAT/SYNCOU T	I	Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. In parallel operation, this pin can be used to synchronous the clock to slave
E5	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 k Ω). The IC works as a slave
E6	BATN_SRP	I	Negative input for battery voltage sensing. Series 100 Ω to negative terminal of battery pack. This pin is also the positive input for low side battery current sensing
F1	REGN	O	LDO output. Connect a 4.7- μ F cap between this pin and GND.
F2	ACDRV2	O	External OVPFET gate driver
F3	ACDRV1	O	External OVPFET gate driver
F4	TSBUS	I	BUS temperature sense pin
F5	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 k Ω)
F6	BATP	I	Positive input for battery voltage sensing. Series 100 Ω to positive terminal of battery pack

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	VAC	-0.3	36	V
	VBUS	-0.3	20	V
	PMID	-0.3	20	V
	CFL1, CFL2, VOUT	-0.3	6	V
	BATP	-0.3	6	V
	BATN_SRP	-0.3	1.8	V
	SRN_SYNCIN	-0.3	6	V
	ACDRV1-VBUS, ACDRV2-VBUS	-0.3	6	V
	/INT, SDA, SCL, REGN	-0.3	6	V
	CDRVL_ADDRMS, CDRVH	-0.3	20	V
	TSBUS, TSBAT_SYNCOUT	-0.3	6	V
	CFH1, CFH2, while maintaining CFH-VOUT=7V MAX	-0.3	14	V
	SRP-SRN	-0.3	0.3	V
	VOUT-VBUS	-16	6	V
Temperature Range	Operating Junction, T _j	-40	125	°C
	Storage temperature range, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2000	2000	V
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-500	500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
Voltage	VAC			11	V

	VBUS			11	V
	VOUT			5	V
	CFH1-VOUT,CFH2-VOUT,CFL1,CFL2			5	V
C _{FLY}	Flying capacitor (Effective capacitance at 5V)	20			μF
C _{VBUS}	VBUS capacitor	1			μF
C _{PMID}	PMID capacitor	5			μF
C _{OUT}	Output capacitor	5			μF
T _A	Operating ambient temperature	-40		85	°C
T _J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL RESISTANCE		WLCSP 36	UNIT
Θ _{JA}	Junction to ambient thermal resistance	51.16	°C/W
Θ _{JC}	Junction-to-case thermal resistance	11.01	°C/W
Θ _{JB}	Junction to board thermal resistance	5.94	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.38	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	5.74	°C/W

7.5 Electrical Characteristic

$V_{BUS} = 8V$, $V_{OUT}=4V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$ for minimum and maximum specifications, and $T_A = 25^{\circ}C$ for typical specifications, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current						
I _{Q_VAC}	VAC quiescent current	ADC disabled, charger disabled, VOUT not present. Measure quiescent current on VAC	730			uA
		ADC enabled, charger disabled, VOUT not present. Measure quiescent current on VAC	1100			uA
I _{Q_VOUT}	VOUT quiescent current	ADC disabled, charger disabled, VAC not present. Measure quiescent current on VOUT	12	18		uA
		ADC enabled, charger disabled, VAC not present. Measure quiescent current on VOUT	1030			uA
Resistances						
R _{QB_ON}	QB on resistance	VBUS=9V, VOUT=4.5V	6			mΩ
R _{Q1_ON} / R _{Q5_ON}	On resistance of Q1/Q5	VBUS=9V, VOUT=4.5V	14			mΩ
R _{Q2_ON} / R _{Q6_ON}	On resistance of Q2/Q6	VBUS=9V, VOUT=4.5V	10			mΩ
R _{Q3_ON} / R _{Q7_ON}	On resistance of Q3/Q7	VBUS=9V, VOUT=4.5V	7			mΩ
R _{Q4_ON} / R _{Q8_ON}	On resistance of Q4/Q8	VBUS=9V, VOUT=4.5V	8			mΩ
R _{VBUS_PD}	VBUS pull-down resistance	VBUS_PD_EN='1'	1			kΩ
R _{VAC_PD}	VAC1/VAC2 pull-down resistance	VAC_PD_EN='1'	100			Ω
Internal threshold						
V _{AC_UVLO}	VAC1/2 for active I2C, no battery. Also, for enable ACDRV	Rising threshold	2.9		3.3	V
		Falling hysteresis	200			mV
V _{BUS_PRESENT}	Adapter inserting stat will be set to '1' once VBUS present	Rising threshold	3		3.3	V
		Falling hysteresis	300			mV
V _{OUT_UVLO}	VOUT for active I2C, no adapter	Rising threshold	2.7		2.8	V
		Falling hysteresis	200			mV
V _{OUT_TH_CHG_EN}	Minimum VOUT voltage for charging enable	Rising threshold			3	V
		Falling hysteresis	200			mV
V _{BUS_TH_CHG_EN}	Minimum VBUS-VOUT voltage for I2C write CHG_EN=1 successfully	Rising threshold	-0.05*V _{OUT}			V
		Falling threshold	-0.07*V _{OUT}			V
Input over-voltage protection and alarm						
V _{AC1/2_OVP}	Rising threshold	Adjustable in register 0x0Eh	6.5		18	V

	Step size	Step size valid for 11V through 17V only	2			V
	Falling hysteresis		400			mV
	Comparator accuracy	Accuracy for 6.5V	-2%	2%		
	Comparator accuracy	Accuracy for 10.5V through 18V	-2%	2%		
V _{BUS_OVP}	Rising threshold	Adjustable in register 0x06h	7	13.35		V
	Step size		50			mV
	Comparator accuracy	VBUS=8V	-1%	1%		
V _{BUS_OVP_ALM}	Rising threshold	Adjustable in register 0x07h	7	13.35		V
	Step size		50			mV
	Falling hysteresis	2:1 charger mode	200		mV	
		1:1 charger mode	100		mV	
	Comparator accuracy	VBUS=8V	-1%	1%		
	Vbus in-range protection					
V _{BUS2OUT_MAX}	Rising threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.2*V _{OUT}			V
	Falling threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.17*V _{OUT}			V
V _{BUS2OUT_MIN}	Rising threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0.02*V _{OUT}			V
	Falling threshold	Over V _{BUS} /2-V _{OUT} in 2:1 charger mode; Over V _{BUS} -V _{OUT} in 1:1 charger mode	0			V
Output short protection						
V _{PMID2OUT_OVP}	Rising threshold Over V _{PMID} /2-V _{OUT} (2:1 charger mode) or Over V _{PMID} -V _{OUT} (1:1 charger mode)	Adjustable in register 0x42h	150	300	500	mV
Input short protection						
V _{PMID2OUT_UVP}	Falling threshold Over V _{PMID} /2-V _{OUT} (2:1 charger mode) or Over V _{PMID} -V _{OUT} (1:1 charger mode)	Adjustable in register 0x42h	-50	-125	-225	mV

Output over-voltage protection and alarm						
V _{OUT_OVP}	Rising threshold	Adjustable in register 0x12h	4.7	5	V	
	Step size		100		mV	
	Comparator accuracy	VOUT_OVP=5V	-0.5%	0.5%		
V _{BAT_OVP}	Rising threshold	Adjustable in register 0x00h	3.84	5.11	V	
	Step size		10		mV	
	Comparator accuracy	VBAT_OVP=4.5V	-0.5%	0.5%		
V _{BAT_OVP_ALM}	Rising threshold	Adjustable in register 0x01h	3.84	5.11	V	
	Step size		10		mV	
	Hysteresis	Falling	100		mV	
	Comparator accuracy	VBAT_OVP=4.5V	-0.5%	0.5%		
Input over-current protection and alarm						
I _{BUS_OCP}	Rising threshold	2:1 mode	1	8	A	
	Rising threshold	1:1 mode	1	8	A	
	Step size		250		mA	
	Comparator accuracy	IBUS=3A	-5%	5%		
I _{BUS_UCP_RISING}	Rising threshold		200	300	mA	
I _{BUS_UCP_FALLING}	Falling threshold		10	100	mA	
Output over-current protection and alarm						
I _{BAT_OCP}	Rising threshold	Adjustable in register 0x02h	0	12.7	A	
	Step size		100		mA	
	Comparator accuracy	IBAT_OCP=6A	-5%	5%		
I _{BAT_OCP_ALM}	Rising threshold	Adjustable in register 0x03h	0	12.7	A	
	Step size		100		mA	
	Hysteresis	Falling	100		mA	
	Comparator accuracy	IBAT_OCP_ALM=6A	-5%	5%		
Timers						
f _{SW}	Switching frequency	Programmable range	200	500	750	kHz
t _{VAC_ON_DG}	Deglitch time between VAC over VAC_UVLO and turn on external MOS when VOUT is already present		70		ms	
	Deglitch time between VAC over VAC_UVLO and turn on external MOS when VOUT is not present		300		ms	
t _{VBUS_PD}	VBUS pull-down time before turn on ACDRV		70		ms	
t _{VAC_OVP}	VAC OVP reaction time		200		ns	
t _{VAC_PD}	VAC Pull-down time		400		ms	

t _{VBUS_IN_RANGE}	Minimum VBUS in-range duration before charge pump start switching	VBUS slow UVP/OVP	20	ms
t _{VBUS_OVP}	VBUS OVP reaction time		1	us
t _{IBUS_OCP}	IBUS OCP reaction time		75	us
t _{IBUS_UCP_FALLING}	IBUS UCP falling reaction time	Adjustable in register 0x11h, bit [3:2]=00	10	us
		Adjustable in register 0x11h, bit [3:2]=01	5	ms
		Adjustable in register 0x11h, bit [3:2]=10	50	ms
		Adjustable in register 0x11h, bit [3:2]=11	150	ms
t _{VPID2OUT_OVP}	VPID2/2-VOUT OVP reaction time or VPID2-VOUT OVP reaction time		0.1	us
t _{VPID2OUT_UVP}	VPID2/2-VOUT UVP reaction time or VPID2-VOUT UVP reaction time		0.1	us
t _{VOUT_OVP}	VOUT OVP reaction time		1	us
t _{VBAT_OVP}	VBAT OVP reaction time		0.1	us
t _{IBAT_OCP}	IBAT OCP reaction time		500	us
t _{SS_TIMEOUT}	Soft start timeout	Adjustable in register 0x11h	6.25m 10	s
t _{WD_TIMEOUT}	Watchdog timeout	Adjustable in register 0x10h	0.5 30	s
t _{INT_LOW}	During that INT is pulled low when an event occurs		256	us
t _{INT_HIGH}	Minimum high level time after an INT low event		256	us
REGN LDO				
V _{REGN}	REGN LDO output voltage	VBUS=8V	5	V
I _{REGN}	REGN LDO current limit	VBUS=8V	20	mA
I2C Interface & Interrupt				
F _{SCL}	Serial-clock frequency		1000	kHz
V _{IH}	Input logic high		0.9	V
V _{IL}	Input logic low		0.37	V
I _{LEAKAGE}	Input leakage current		1	uA
ADC MEASUREMENT				
IBUS_ADC	Range		0 10.24	A

	LSB		2.5	mA
	Accuracy	IBUS=3A	-5% 5%	
VBUS_ADC	Range		0 14	V
	LSB		3.75	mV
	Accuracy	VBUS=8V	-1% 1%	
VAC1_ADC	Range		0 14	V
	LSB		5	mV
	Accuracy	VAC1=8V	-1% 1%	
VAC2_ADC	Range		0 14	V
	LSB		5	mV
	Accuracy	VAC2=8V	-1% 1%	
VOUT_ADC	Range		0 5.12	V
	LSB		1.25	mV
	Accuracy	VOUT=4V	-0.5% 0.5%	
VBAT_ADC	Range		0 5.12	V
	LSB		1.25	mV
	Accuracy	VBAT=4V	-0.5% 0.5%	
IBAT_ADC	Range		0 12.8	A
	LSB		3.125	mA
	Accuracy	IBAT=6A with 2mΩ R _{SENSE}	-1.5% 1.5%	
TSBUS_ADC	ADC TSBUS pin voltage	Range	0.2 2.7	V
	ADC TSBUS percentage of VOUT readable in registers 0x33h and 0x34h	Range	0 50	%
		LSB	0.09766	%
	Accuracy	TSBUS pin voltage 2V	-1 1	%
TSBAT_ADC	ADC TSBAT pin voltage	Range	0.2 2.7	V
	ADC TSBAT percentage of VOUT readable in registers 0x35h and 0x36h	Range	0 50	%
		LSB	0.09766	%
	Accuracy	TSBAT pin voltage 2V	-1 1	%
TDIE_ADC	ADC Die temperature readable in registers 0x24h and 0x25h	Range	0 150	°C
		LSB	0.5	°C
	Accuracy		±4	°C
TSHUT				
T _{SHUT}	Thermal shutdown temperature		150	°C

7.6 Typical Efficiency

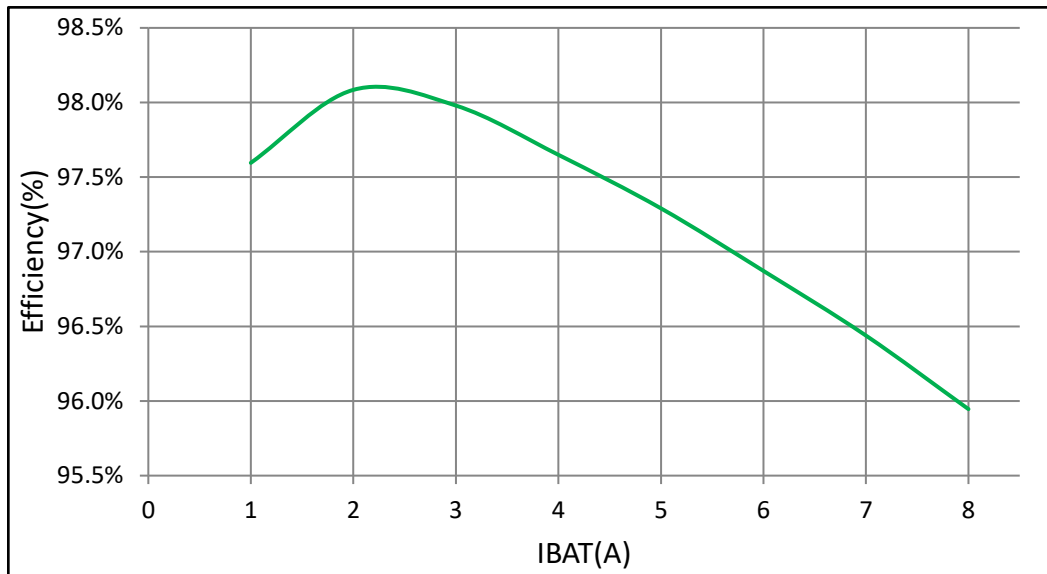


Figure 7-1. Efficiency @ $V_{OUT}=4.4V$, $C_{FLY}=3*22\mu F$, $F_{sw}=500kHz$

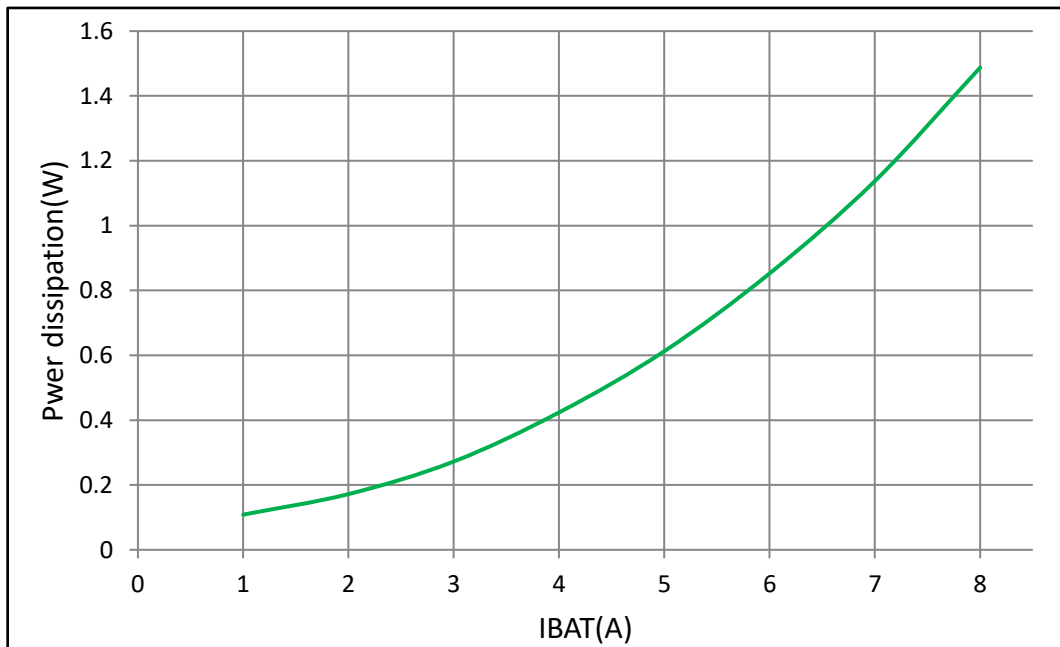
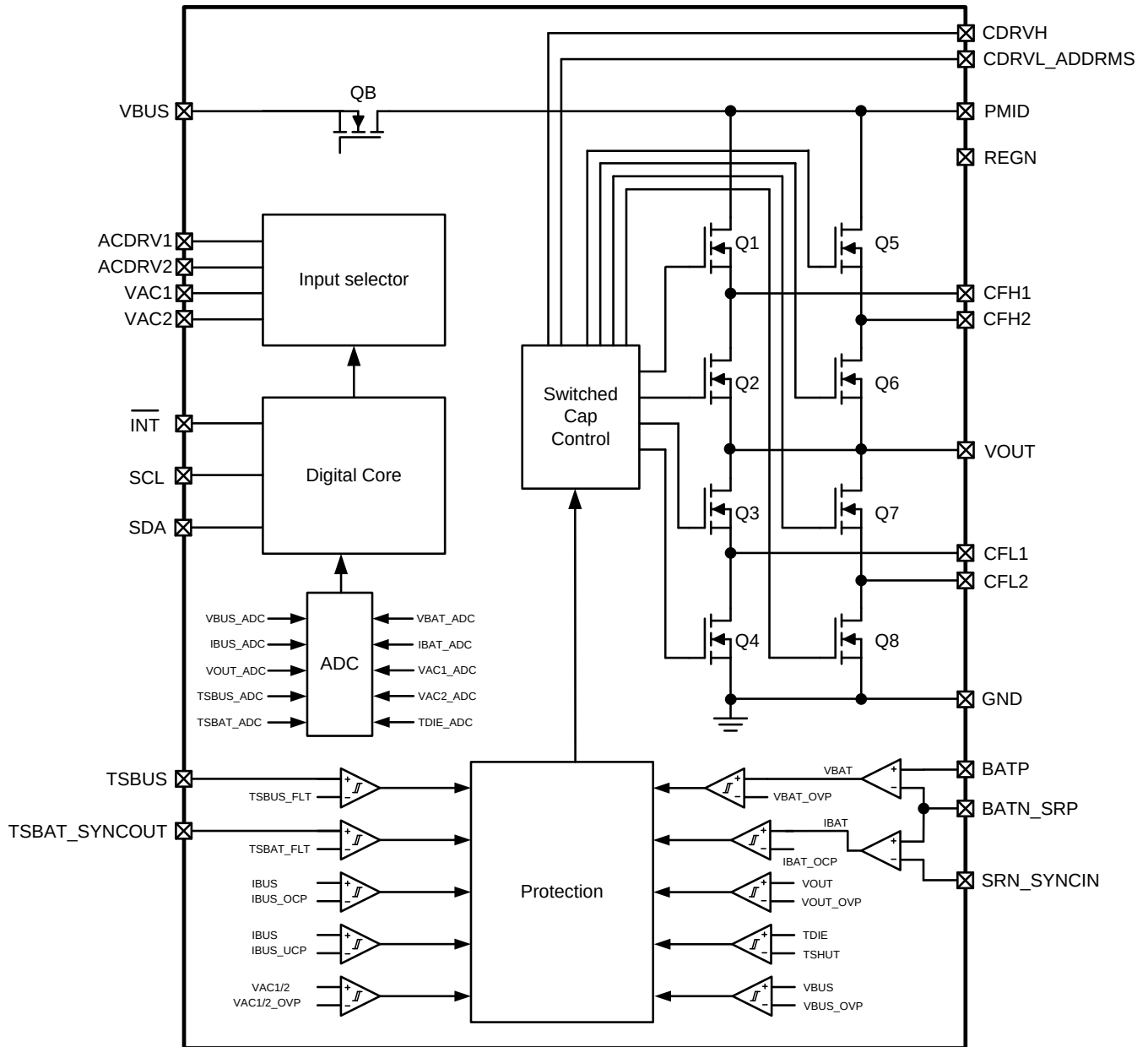


Figure 7-2. Power loss @ $V_{OUT}=4.4V$, $C_{FLY}=3*22\mu F$, $F_{sw}=500kHz$

8 Functional Block Diagram



9 Detailed Description

9.1 Overview

SC8541 is a 97% efficiency, 8-A battery charging solution using a switched cap architecture. The switched cap architecture and the integrated FETs are optimized to enable a 50% cycle, allowing the cable current to be half the current delivered to the battery, reducing the losses over the charging cable as well as limiting the temperature rise in the application. The dual-phase architecture increases charging efficiency and reduces the input and output cap requirements.

The device also operates in bypass mode charging the battery directly from VBUS through QB, Q1 and Q2 in parallel with Q5 and Q6.

The device supports dual input power path management which manages the power flowing from two different input sources. The inputs selection is controlled by host through I2C with default source #1 as the primary input and the source #2 as the secondary source.

The device integrates all the necessary protection features to ensure safe charging, including input overvoltage and overcurrent protection, output overvoltage and overcurrent protection, temperature sensing for the battery and cable, and monitoring the die temperature. The device also integrates special protection functions for switched cap architecture, including input voltage in-range protection, flying cap short protection and short protection for input and output.

The device includes a 12-bit ADC to provide bus voltage, bus current, output voltage, battery voltage, battery current, input connector temperature, battery temperature, junction temperature, and other calculated measurements needed to manage the charging of the battery from the smart wall adapter or wireless input or power bank.

SC8541 adopts 36pin CSP 2.68mm X 2.68mm package.

9.2 Featured Description

9.2.1 Charging System

SC8541 is a high efficiency switched cap charger for 1-cell Li-ion battery, used in parallel with a master charger. A host must set up the protections and alarms on SC8541 before enabling the SC8541. The host must monitor the alarms generated by SC8541 and communicate with the smart adapter to control the current delivered to the charger.

Figure 9-1 illustrates the typical system architecture for application of SC8541.

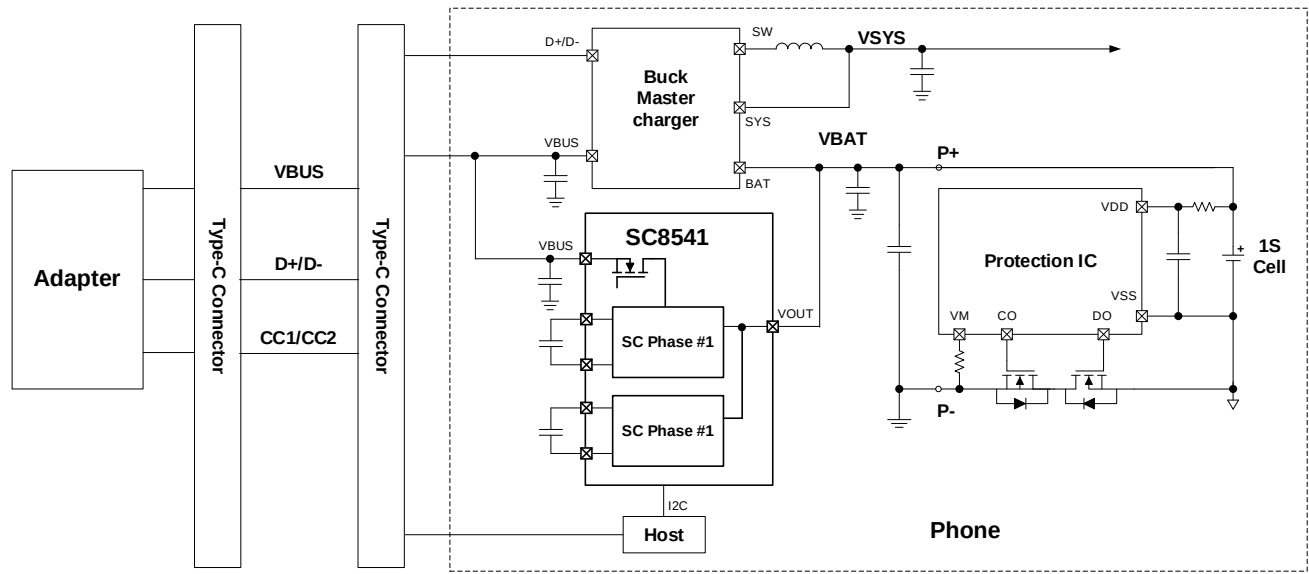


Figure 9-1. SC8541 System Block Diagram

9.2.2 Battery Charging Profile

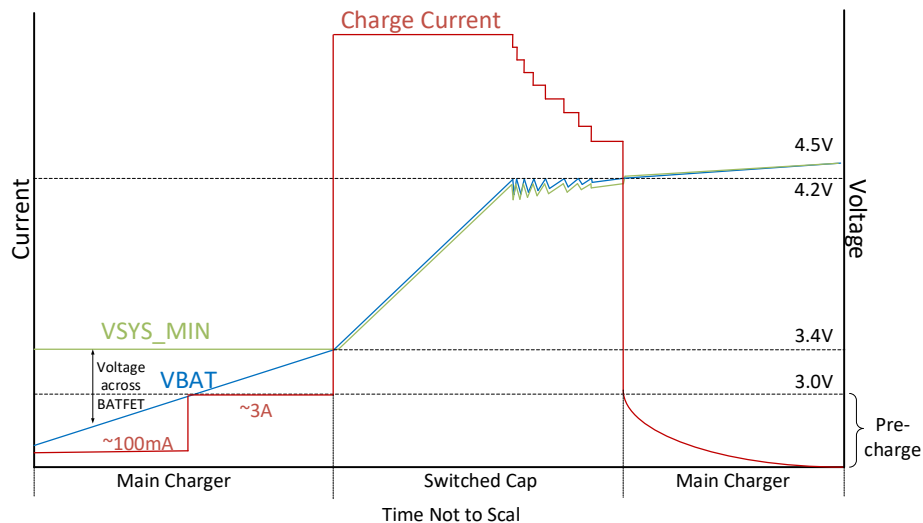


Figure 9-2. Battery Charging Profile

The system has a specific battery charging profile based on the switched cap architecture. The charging will be controlled by the main charger such as a buck charger until system voltage reaches minimum system regulation voltage VSYSMIN. Then the adapter can supply a higher bus voltage, enable SC8541, and regulate the current on VBUS to charge the battery. In the CC

phase, the SC8541 will provide feedback to the system to increase and decrease current as needed, as well as disable the blocking and switching FETs if the voltage is exceeded. Once the CV point is reached, the SC8541 will provide feedback to the adapter to reduce the current. Once the charging current is lower than the falling threshold, the main charger will take over again.

9.2.3 Device Power up

The device is powered from the highest of VAC1 or VAC2 (with VAC1 being primary input), VBUS or VOUT (battery). The voltage must be greater than the V_{AC_UVLO} , V_{BUS_UVLO} or V_{OUT_UVLO} threshold to be a valid supply to power up the device, and the corresponding bit VAC1_INSERT_STAT, VAC2_INSERT_STAT, VBAT_INSERT_STAT will be set to 1. Once the device is powered up, the I2C interface function is enabled and all the registers are reset to default value. Then if the VBUS and VOUT voltage is higher than $V_{BUS_TH_CHG_EN}$ and $V_{OUT_TH_CHG_EN}$ threshold, the host can set CHG_EN=1 and start charging.

9.2.4 Dual Input Bi-Directional Power Path Management

The device has two ACDRV pins to drive two sets of N-channel ACFET-RBFET, which can select and manage the input power from two different sources.

In the POR sequence, the device detects if ACDRV pin is shorted to ground or not to determine if the ACFET-RBFET is applied in the system, and then updates the status register ACRB1_CONFIG_STAT or ACRB2_CONFIG_STAT. If the external ACFET-RBFET is not used in the schematic, then tie VAC to VBUS and connect ACDRV to GND.

9.2.4.1 ACDRV Turn-on Condition

The ACDRV controls input source for both SC8541 and main charger. In order to turn on the ACDRV, all of the following conditions must be valid:

1. The corresponding ACRB1_CONFIG_STAT or ACRB2_CONFIG_STAT is set to 1
2. VAC is above V_{AC_UVLO} and VAC1_INSERT_STAT or VAC2_INSERT_STAT is set to 1
3. VAC is below V_{AC_OVP} threshold
4. VBUS_PRESENT_STAT is not set to 1

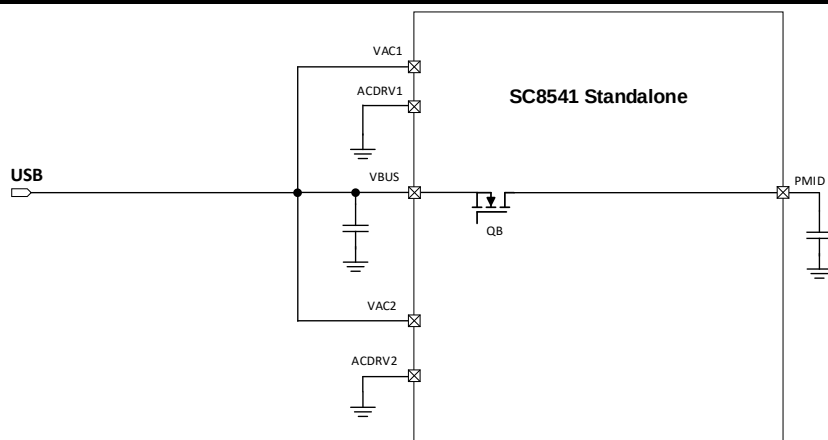
If any of the input source from AC1 and AC2 satisfies the above conditions, the corresponding ACDRV pin will be high and turn on the external MOSFETs. If both the two input sources satisfy the conditions, the ACDRV1 will turn on.

9.2.4.2 Single Input without ACFET-RBFET

The SC8541 can work with single input source and no external FET. Both VAC1 and VAC2 are connected with VBUS and the input power. And the ACDRV1 and ACDRV2 are tied to ground.

Table 9-1. Configuration for Single Input without ACFET-RBFET

Input Configuration	Single Input
External FET Connection	No ACFET1-RBFET1; No ACFET2-RBFET2
Input Pin Connection	VAC1 to input source; VAC2 to input source
ACDRV Pin Connection	ACDRV1 to GND; ACDRV2 to GND
ACDRV1_STAT	0
ACDRV2_STAT	0
ACDRV_MANUAL_EN	No effect
ACDRV1_EN	No Effect
ACDRV2_EN	No Effect

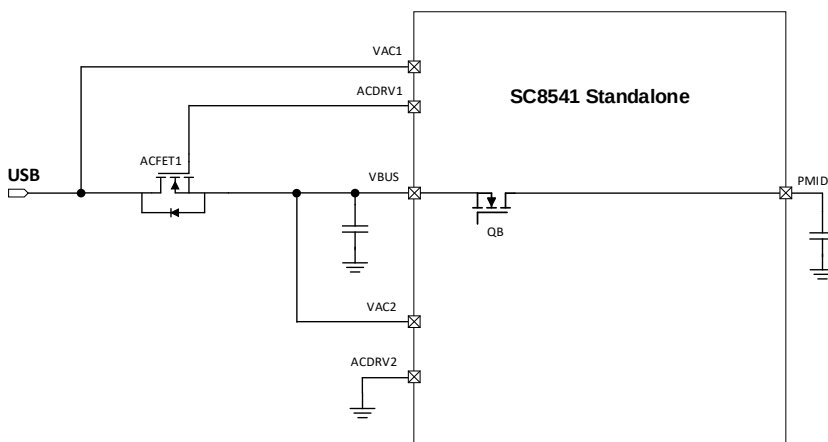

Figure 9-3. Single Input without ACFET-RBFET

9.2.4.3 Single Input with ACFET1

The SC8541 can work with single input source and one external FET. The ACFET1 can block the high input voltage. The VAC1 is connected to the input source and the VAC2 is connected to VBUS. The ACDRV1 is connected to the gate of ACFET1 and the ACDRV2 is short to ground.

Table 9-2. Configuration for Single Input with ACFET1

Input Configuration	Single Input
External FET Connection	ACFET1; No ACFET2-RBFET2
Input Pin Connection	VAC1 to input source; VAC2 to VBUS
ACDRV Pin Connection	ACDRV1 to ACFET1; ACDRV2 to GND
ACDRV1_STAT	1: ACDRV1 is on; 0: ACDRV1 is off
ACDRV2_STAT	0
ACDRV_MANUAL_EN	1: ACDRV state is controlled by ACDRV_EN bit; 0: ACDRV state is determined automatically
ACDRV1_EN	1: Turn on ACDRV1; 0: Turn off ACDRV1
ACDRV2_EN	No Effect


Figure 9-4. Single Input with ACFET1

9.2.4.4 Single Input with ACFET1-RBFET1

The SC8541 can work with single input source. Connect one of the VACs to the input source and the another to the VBUS. One set of external ACFET1-RBFET1 is applied and the gate is connected to the corresponding ACDRV, the another ACDRV is connected to ground. Figure 9-5 shows the schematic of the single input system with ACFET1-RBFET1.

Table 9-3. Configuration for Single Input with ACFET1-RBFET1

Input Configuration	Single Input
External FET Connection	ACFET1-RBFET1; No ACFET2-RBFET2
Input Pin Connection	VAC1 to input source; VAC2 to VBUS
ACDRV Pin Connection	ACDRV1 to ACFET1-RBFET1; ACDRV2 to GND
ACDRV1_STAT	1: ACDRV1 is on; 0: ACDRV1 is off
ACDRV2_STAT	0
ACDRV_MANUAL_EN	1: ACDRV state is controlled by ACDRV_EN bit; 0: ACDRV state is determined automatically
ACDRV1_EN	1: Turn on ACDRV1; 0: Turn off ACDRV1
ACDRV2_EN	No Effect

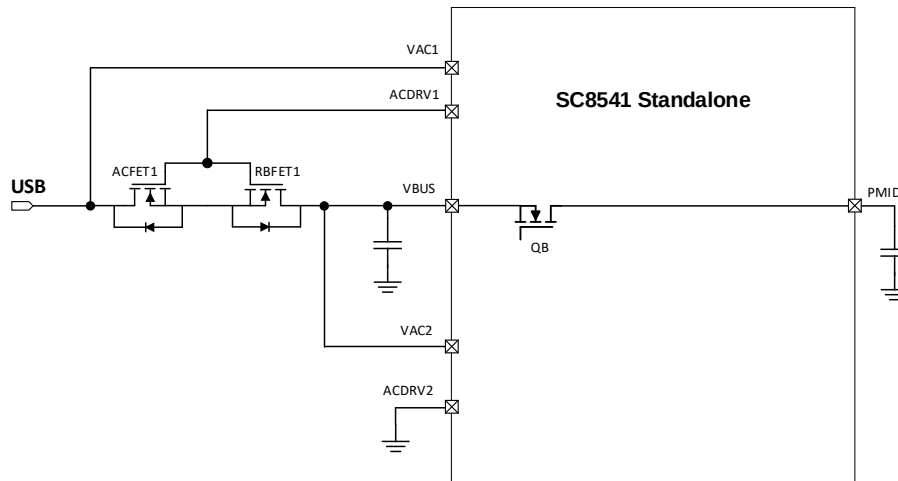


Figure 9-5. Single Input with ACFET1-RBFET1

9.2.4.5 Dual Input with only ACFET1-RBFET1

The SC8541 can work with dual input sources and only ACFET1-RBFET1. The VAC1 is connected to input source1 and the VAC2 is connected to input source 2. The ACDRV1 is connected to the gate of ACFET1-RBFET1 and ACDRV2 is short to ground. The input source 2 connected to VBUS through the LDO of the RTX to block the VBUS voltage when input source 2 is not present.

Table 9-4. Configuration for Dual Input with only ACFET1-RBFET1

Input Configuration	Dual Input
External FET Connection	ACFET1-RBFET1; No ACFET2-RBFET2
Input Pin Connection	VAC1 to input source 1; VAC2 to VBUS
ACDRV Pin Connection	ACDRV1 to ACFET1-RBFET1; ACDRV2 to GND
ACDRV1_STAT	1: ACDRV1 is on; 0: ACDRV1 is off

ACDRV2_STAT	0
ACDRV_MANUAL_EN	1: ACDRV state is controlled by ACDRV_EN bit; 0: ACDRV state is determined automatically
ACDRV1_EN	1: Turn on ACDRV1; 0: Turn off ACDRV1
ACDRV2_EN	No Effect

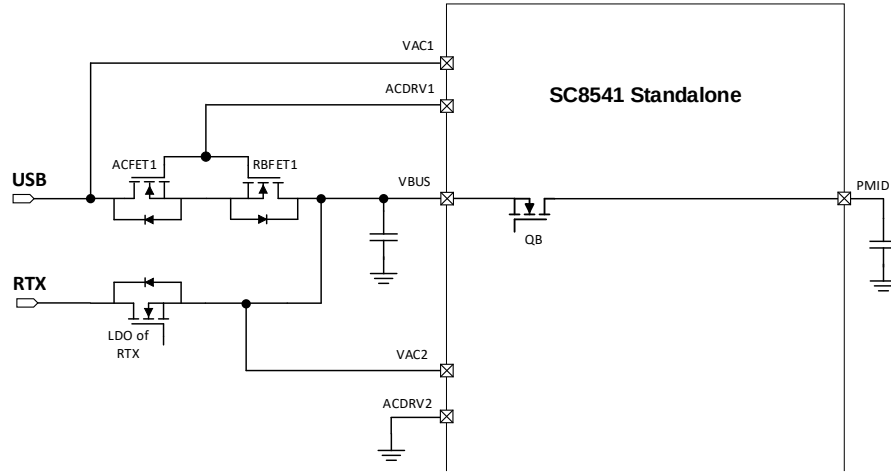


Figure 9-6. Dual Input with only ACFET1-RBFET1

9.2.4.6 Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2

With external MOSFETs ACFET1-RBFET2 and ACFET2-RBFET2, the SC8541 can select the input power from two sources, such as the USB connector and RTX of wireless charging coil. Figure 9-7 shows the schematic of the dual input system.

Table 9-5. Configuration for Dual Input with ACFET1-RBFET1 and ACFET2-RBFET2

Input Configuration	Dual Input
External FET Connection	ACFET1-RBFET1; ACFET2-RBFET2
Input Pin Connection	VAC1 to input source 1; VAC2 to input source 2
ACDRV Pin Connection	ACDRV1 to ACFET1-RBFET1; ACDRV2 to ACFET2-RBFET2
ACDRV1_STAT	1: ACDRV1 is on; 0: ACDRV1 is off
ACDRV2_STAT	1: ACDRV2 is on; 0: ACDRV2 is off
ACDRV_MANUAL_EN	1: ACDRV state is controlled by ACDRV_EN bit; 0: ACDRV state is determined automatically
ACDRV1_EN	1: Turn on ACDRV1; 0: Turn off ACDRV1
ACDRV2_EN	1: Turn on ACDRV2; 0: Turn off ACDRV2

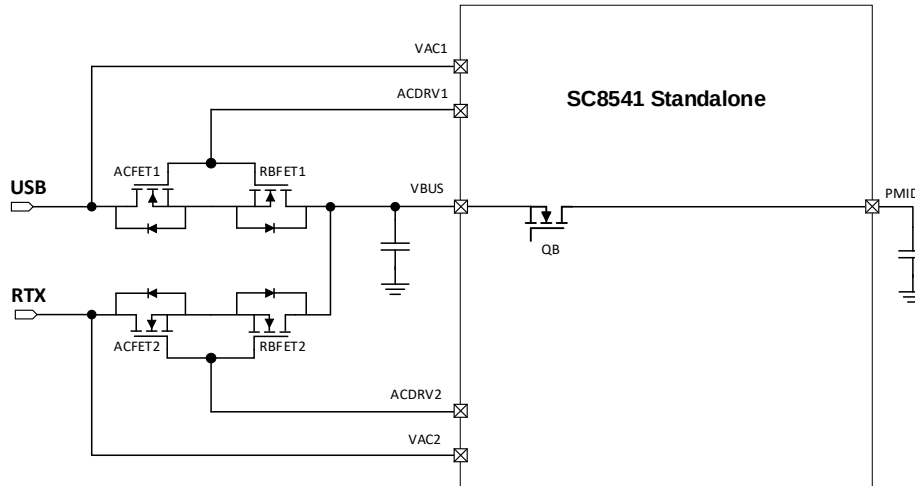


Figure 9-7. Dual Input with ACFET-RBFET1 and ACFET-RBFET2

9.2.4.7 OTG and Reverse TX Mode Operation

When the system works in OTG mode, the ACDRV1 and ACDRV2 can also selected which port to be the OTG output by turning on the corresponding switches.

To enter OTG or reverse TX Mode, the host should follow the steps below:

1. Host writes OTG_EN =1
2. Host writes ACDRV_MANUAL_EN=0, and then writes ACDRV1_EN=1 or ACDRV2_EN=1 depending on which port is desired for OTG or reverse TX output
3. Host enables OTG Mode on main charger
4. If VBUSOV or VACOV fault occurs, ACDRV will be disabled but OTG_EN is still '1'. Host needs to write ACDRV1_EN high or ACDRV2_EN high when the fault is cleared. Set VAC1OV and VAC2OV to the same threshold in the OTG Mode
5. OTG_EN is cleared when watchdog timer expires

To exit OTG or Reverse TX Mode, the host should follow the steps below:

1. Turn off main OTG or reverse TX source
2. Turn on VBUS pulldown resistor by setting VBUS_PD_EN=1 or VAC pulldown resistor by setting VAC1_PD_EN=1 or VAC2_PD_EN=1, depending on which port is to be discharged
3. Wait for VBUS and VAC to be discharged
4. Turn off ACDRV by setting ACDRV1_EN=0 or ACDRV2_EN=0
5. Exit OTG Mode by setting OTG_EN=0

9.2.5 Bypass Mode Operation

When host determines the adapter support bypass mode charging, the device can enable Bypass mode by setting MODE=1. Blocking FET (QB) and four high side switching FET (Q1 and Q2/ Q5 and Q6) are kept turned on to charge from adapter to battery directly. The four low side switching FET (Q3 and Q4/ Q7 and Q8) are kept turn off. During Bypass Mode, when fault occurs, CHG_EN is cleared but MODE stays '1'.

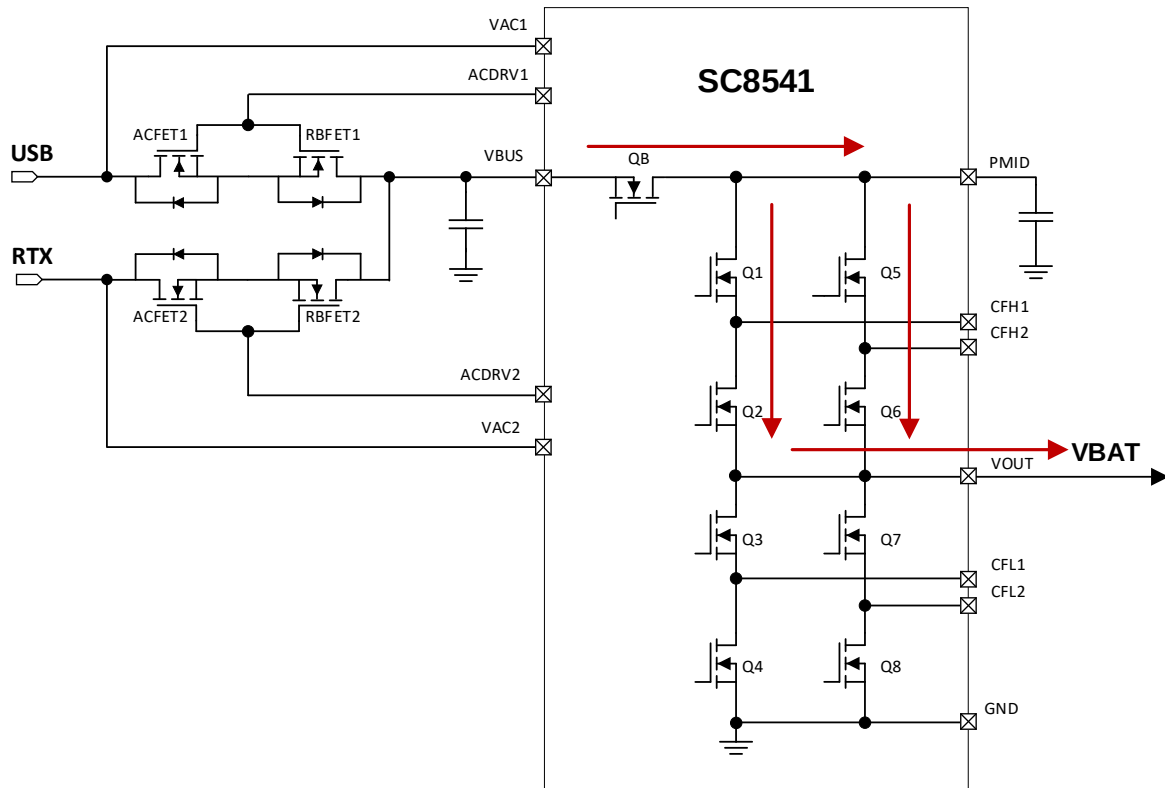


Figure 9-8. SC8541 Bypass Mode

To change from Bypass Mode to Switched Cap Mode or from Switched Cap to Bypass Mode, the host would first set CHG_EN=0 to stop the converter and then set MODE to desired value. The host would also set desired protection threshold based on the selected operation modes and then enable charge by setting CHG_EN=1.

9.2.6 Charging Start-up

The host can start Switched Cap or Bypass Mode charging follow the steps below:

1. Both VBUS and VOUT need to be present. Host can check the status through VBUS_PRESENT_STAT (STAT3[2]) and VBAT_PRESENT_STAT (STAT3[5]). Both of them need to be '1'.
2. Host sets all the protections to the desired thresholds. Refer to the Device Modes and Protection Status section for proper setting.
3. Host sets either Switched Cap Mode or Bypass Mode through MODE bit (CTRL2[3]) based on adapter type.
4. Host sets the desired switching frequency in Switched Cap Mode through FSW_SET [2:0] bits (CTRL3[7:5]).
5. Host can enable charge by setting CHG_EN=1.
6. Once charge has been enabled, the CP_SWITCHING_STAT bit is set to '1' to indicate either switched cap or bypass is active, and current starts to flow to the battery.
7. When watchdog timer expires, CHG_EN is reset to '0' and charging stops. Host needs to read or write any register bit before watchdog expires, or disable watchdog timer (set CTRL3[2]=1) to prevent watchdog timer from expiring.

9.2.7 Adapter Removal

If adapter is removed during soft start timer, CHG_EN will be cleared after soft-start timer expires. The user can program the soft-start timer in SS_TIMEOUT register. If adapter is removed after soft-start timer expires, converter stops switching and CHG_EN is cleared after the deglitch time programmed in IBUS_UCP_FALL_DEGLITCH_SET register. The device prevents boost back when the adapter is removed during and after the soft-start timer. To accelerate VBUS or VAC discharge after adapter removal, the user would turn on the VBUS pulldown resistor and VAC pulldown current resistor by setting BUS_PD_EN or VAC1_PD_EN or VAC2_PD_EN to '1'.

9.2.8 Integrated 16-Bit ADC for Monitoring and Smart Adapter Feedback

The integrated 12-bit ADC of the device allows the user to get system information for optimizing and control the charging system. The control of the ADC is done through the ADC control registers. The ADC_EN bit provides the ability to enable and disable the ADC. The ADC_RATE bit determines the ADC behavior from continuous conversion or one-shot.

To enable the ADC, the ADC_EN bit must be set to '1'. The ADC is allowed to operate if the device is powered up ($V_{AC} > V_{AC_UVLO}$, $V_{BUS} > V_{BUS_UVLO}$ or $V_{OUT} > V_{OUT_UVLO}$). If ADC_EN is set to '1' before VAC, VBUS or VOUT reach their respective PRESENT threshold, then the ADC conversion will be postponed until one of the power supplies reaches the threshold.

The ADC function of IBUS, VBUS, VAC1, VAC2, VOUT, VBAT, IBAT, TSBUS, TSBAT and TDIE can be enabled or disabled by setting the corresponding bit in ADC_CTRL and ADC_FN_DISABLE register. If an ADC parameter is disabled, the value in that register will be from the last valid ADC conversion or the default POR value. If an ADC parameter is disabled in the middle of an ADC measurement cycle, the device will finish the conversion of that parameter, but will not convert the parameter when starting the next conversion cycle. Even though no conversion takes place when all ADC measurement parameters are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in ADC_CTRL and ADC_FN_DISABLE register is set to '0'.

ADC conversion operates independently of the faults present in the device. ADC conversion will continue even after a fault has occurred (such as one that causes the power stage to be disabled), and the host must set ADC_EN = '0' to disable the ADC. ADC readings are only valid for DC states and not for transients. When host writes ADC_EN=0, the ADC stops immediately. If the host wants to exit ADC more gracefully, it is possible to do either of the following:

1. Write ADC_RATE to one-shot, and the ADC will stop at the end of a complete cycle of conversions, or
2. Write all the DIS bits low, and the ADC will stop at the end of the current measurement.

9.2.9 Device Modes and Protection Status

Table 9-1 shows the features and modes of the device depending on the conditions of the device.

Table 9-6. Device Modes and Protection Status

FUNCTIONS	BAT-ONLY (VBUS<VBUS_PRESENT)	VBUS>VBUS_PRESENT CHG_EN=0 (Charge pump disabled)	VBUS>VBUS_PRESENT CHG_EN=1 (Charge pump enabled)	
			During charge soft start	Charging
I2C allowed	√	√	√	√
Allow user ADC	√	√	√	√
ACDRV1/2		√	√	√
VAC1/2_OVP			√	√
VBUS_OVP			√	√
VBUS_OVP_ALM			√	√
IBUS_OCP			√	√
IBUS_UCP			X	√
VBAT_OVP			√	√
VBAT_OVP_ALM			√	√
VOUT_OVP			√	√
IBAT_OCP			√	√
IBAT_OCP_ALM			√	√
VBUS In-range		√	√	√
WD_TIMEOUT			√	√
SS_TIMEOUT			√	√
PIN_DIAG_FAIL			√	√
TDIE_FLT			√	√
TSBUS_FLT			√	√
TSBAT_FLT			√	√
TDIE_ALM			√	√
TSBUS_TSBAT_ALM			√	√

Tripping any of these protections will turn off QB and stop converter switching. Masking the fault or alarm does NOT disable the protection, but only keeps an INT from being triggered by the event. Disabling the fault or alarm protection other than IBUSUCP holds that STAT and FLAG bits in reset, and also prevents an interrupt from occurring. Disable IBUSUCP protection still sets STAT and FLAG bits and sends interrupt to alert host but keeps converter running when triggered. When any fault event is triggered, the CHG_EN bit is set to '0' to disable charging, and the charging start-up sequence must be followed to begin charging again.

9.2.9.1 Input Overvoltage, Overcurrent, Undercurrent and Short-Circuit Protection

Input overvoltage protection (VACOVP) with external N-channel FET(s): The device integrates the functionality of an input overvoltage protector. With external single or back-to-back N-channel FET(s), the device blocks input voltage exceeding VACOVP threshold (VAC1OVP or VAC2OVP). This eliminates the need for a separate OVP device to protect the overall system. When the VACOVP fault occurs, the protector has a response time of t_{VACOVP} before turn of the external FET(s). The VAC1OVP and VAC2OVP threshold is adjustable in the VAC control register with different VAC1OVP and VAC2OVP setting values.

When VAC1OVP or VAC2OVP is tripped, corresponding ACDRV is turned off and VAC1OVP_STAT or VAC2OVP_STAT and VAC1OVP_FLAG or VAC2OVP_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by VAC1OVP_MASK or VAC2OVP_MASK). When VAC2OVP is triggered, the device sends multiple interrupts when the fault persists. Use VAC1 as input unless both VAC1 and VAC2 are needed.

Input overvoltage protection (VBUSOVP): The VBUSOVP threshold is adjustable in the VBUSOVP register. When VBUSOVP is tripped, CHG_EN is set to '0' and the device stops charging. VBUSOVP_STAT and VBUSOVP_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by VBUSOVP_MASK). The start-up sequence must be followed to resume charging.

Input overcurrent protection (IBUSOCP): Input overcurrent protection monitors the current flow into VBUS and through QB. The overcurrent protection threshold is adjustable in the IBUSOCP register. When IBUSOCP is tripped, CHG_EN is set to '0' and the device stops charging. IBUSOCP_STAT and IBUSOCP_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by IBUSOCP_MASK). The start-up sequence must be followed to resume charging.

Input undercurrent protection (IBUSUCP): BUS undercurrent protection (UCP) is implemented to detect adapter unplug. When the device is in start-up process, and IBUSUCP is enabled (IBUSUCP_DIS=0), if the current has not exceeded IBUSUCP rising threshold during soft start time (programmable in SS_TIMEOUT [2:0]), Switched Cap or Bypass Mode is disabled and CHG_EN is set to '0'. BUSUCP_STAT, BUSUCP_FLAG, SS_TIMEOUT_STAT and SS_TIMEOUT_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by BUSUCP_MASK and SS_TIMEOUT_MASK). At any time the BUS current drops below IBUSUCP falling threshold, Switched Cap or Bypass Mode is disabled and CHG_EN is set to '0'. BUSUCP_STAT and BUSUCP_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by BUSUCP_MASK). The start-up sequence must be followed to resume charging.

The deglitch time for IBUSUCP is programmable in IBUS_UCP_FALL_DEGLITCH_SET [1:0] register. Please note that IBUSUCP deglitch time needs to be set shorter than soft start timer in order for IBUSUCP to be effective. When IBUSUCP is disabled (BUSUCP_DIS=1), if the current is below BUSUCP after soft-start timer expires, CHG_EN is not set to '0', BUSUCP_STAT and BUSUCP_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by BUSUCP_MASK). The host can determine if charge needs to be stopped in this case.

Input overvoltage protection alarm (VBUSOVP_ALM): In addition to input overvoltage and overcurrent, the device also integrates alarm function for VBUSOVP_ALM. When alarm is triggered, the corresponding STAT and FLAG bit is set to '1' and INT is asserted low to alert the host (unless it is masked by the MASK bit). However, CHG_EN is not cleared and host can reduce input voltage or input current to prevent VBUS reaching VBUSOVP threshold.

9.2.9.2 Battery Overvoltage and Overcurrent Protection

Battery overvoltage protection (VBATOVP) and alarm (VBATOVP_ALM): The device integrates both overcurrent and overvoltage protection for the battery. The device monitors the battery voltage on BATP and BATN_SRP. In order to reduce the possibility of battery terminal shorts during manufacturing, 100-Ω series resistors on BATP is required. If external sense resistor is not used, place 100-Ω series resistors on BATN as well. When the VBATOVP_ALM is reached, an interrupt is sent to the host to reduce the charge current and thereby not reaching the VBATOVP threshold. If VBATOVP is reached, the switched cap or bypass is disabled and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. At the same time, VBATOVP_STAT and VBATOVP_FLAG are set to '1', and INT is asserted low to alert the host (unless masked by VBATOVP_MASK). VBATOVP and VBATOVP_ALM is disabled when VBATOVP_DIS and VBATOVP_ALM_DIS is set to '1'.

Battery overcurrent protection (IBATOCP) and alarm (IBATOCP_ALM): The device monitors current through the battery by monitoring the voltage across the external series battery sense resistor. The differential voltage of this sense resistor is measured on BATN_SRP and SRN_SYNCIN. When the IBATOCP_ALM is reached, an interrupt is sent to the host to reduce the charge current from reaching the IBATOCP threshold. If IBATOCP is reached, the Switched Cap or Bypass Mode is disabled after a deglitch time of t_{BAT_OCP} and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. At the same time, IBATOCP_STAT and IBATOCP_FLAG are set to '1', and INT is asserted

Output overvoltage protection (VOUTOVP): The device also monitors output voltage between VOUT and ground to protect the system. If VOUTOVP is reached and VOUTOVP_DIS=0, the Switched Cap or Bypass Mode is disabled and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. At the same time, VOUTOVP_STAT and

VOUTOVP_FLAG is set to '1', and INT is asserted low to alert the host (unless masked by VOUTOVP_MASK). If VOUTOVP_DIS=1, the protection is disabled.

9.2.9.3 Input Voltage in Range Protection

VBUS_ERRORHI and VBUS_ERRORLO: To avoid a large current crash or current reverse when device start charging, the VBUS voltage and output voltage will be detected and compared when the Host sets CHG_EN=1. In Switched Cap Mode, if VBUS/2-VOUT is higher than $V_{BUS2OUT_MAX}$, the switched cap mode is disabled and the CHG_EN is set to '0'. At the same time, VBUS_ERRORHI_STAT and VBUS_ERRORHI_FLAG are set to '1', and INT is asserted low to alert the host (unless masked by VBUS_ERRORHI_MASK). If VBUS/2-VOUT is lower than $V_{BUS2OUT_MIN}$, the switched cap mode is disabled and the CHG_EN is set to '0'. At the same time, VBUS_ERRORLO_STAT and VBUS_ERRORLO_FLAG are set to '1', and INT is asserted low to alert the host (unless masked by VBUS_ERRORLO_MASK).

If MODE=1 and device is in Bypass mode, the value of VBUS-VOUT is used to compared with $V_{BUS2OUT_MAX}$ and $V_{BUS2OUT_MIN}$ to determine the VBUS in range protection is triggered or not. Either the VBUS_ERRORHI or VBUS_ERRORLO protection has occurred, the start up process of charging will stop and the new start-up sequence must be followed to resume charging.

9.2.9.4 IC Internal Thermal Shutdown, TSBUS, and TSBAT Temperature Monitoring

The device has three temperature sensing mechanisms to protect the device and system during charging:

1. TSBUS for monitoring the cable connector temperature
2. TSBAT for monitoring the battery temperature
3. TDIE for monitoring the internal junction temperature of the device

The TSBUS and TSBAT both rely on a resistor divider that has an external pullup voltage to REGN. A negative coefficient thermistor (NTC) is in parallel to the low-side resistor. When the temperature rises above threshold, the voltage of TSBUS and TSBAT pin would drop under the voltage threshold and triggered the temperature protection or alarm event. The threshold is adjusted using the TSBUS_FLT and TSBAT_FLT registers.

The typical TS resistor network on TSBAT_SYNCOUT and TSBUS is illustrated in Figure 9-9.

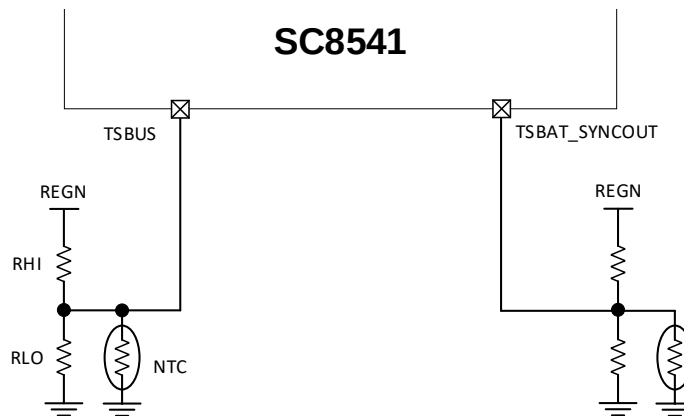


Figure 9-9. TSBAT_SYNCOUT and TSBUS Resistor Network

The RLO and RHI resistors should be chosen depending on the NTC used. If a 10-kΩ NTC is used, use 10-kΩ resistors for RLO and RHI. If a 100-kΩ NTC is used, use 100-kΩ resistors for RLO and RHI. The ratio of VTS/ REGN can be from 0% to 50%.

Additionally, the device measures internal junction temperature, with adjustable threshold TDIE_FLT in TDIE_FLT register.

If the TSBUS_FLT, TSBAT_FLT, and TDIE_FLT thresholds are reached, the Switched Cap or Bypass Mode is disabled and CHG_EN is set to '0', and the start-up sequence must be followed to resume charging. The corresponding STAT and FLAG bit

is set to '1' unless it is masked by the MASK bit. If TSBUS, TSBAT, or TDIE protections are not used, the functions can be disabled in the register by setting the TSBUS_FLT_DIS, TSBAT_FLT_DIS, or TDIE_FLT_DIS bit to '1'.

TSBUS_TSBAT_ALM_STAT and FLAG is set to '1' unless it is masked by corresponding mask bit when one of the following conditions is met: 1) TSBUS is within 5% of TSBUS_FLT threshold or 2) TSBAT is within of TSBAT_FLT. If the TSBUS_FLT or TSBAT_FLT is disabled, it will not trigger a TSBUS_TSBAT_ALM interrupt. Using the TDIE_ALM register, an alarm can be set to notify the host when the device die temperature exceeds a threshold. The TDIE_ALM_STAT and TDIE_ALM_FLAG bit is set to '1' unless it is masked by TDIE_ALM_MASK bit. The device will not automatically stop switching when reaching the alarm threshold and the host may decide on the steps to take to lower the temperature, such as reducing the charge current.

9.2.10 INT Pin, STAT, FLAG, and MASK Registers

The INT pin is an open drain pin that needs to be pulled up to a voltage with a pullup resistor. INT is normally high and will assert low for t_{INT_LOW} when the device needs to alert the host of a fault or status change. The fields in the STAT registers show the current status of the device, and are updated as the status changes. The fields in the FLAG registers indicate that the event has occurred, and the field is cleared once the corresponding register is read. If the event persists after the FLAG register has been read and cleared, another INT signal is not sent to prevent host keep receiving interrupts. The fields in the MASK registers allow the user to disable the interrupt on the INT pin, but the STAT and FLAG registers are still updated even though INT is not pulled low.

9.2.11 Dual Charger Operation Using Primary and Secondary Modes

For higher power systems, it is possible to use two devices for dual charger configuration. This allows each device to operate at lower charging current compared with single device operating at the same total charging current, and the higher efficiency can be achieved. The CDRVL_ADDRMS pin is used to configure the functionality of the device as Standalone, Primary or Secondary during POR. Refer to Section 9.2.12 for detailed setting. When configured as a primary, the TSBAT_SYNCOUT pin functions as SYNCOUT, and the SRN_SYNCIN pin functions as SRN. When configured as a Secondary, the TSBAT_SYNCOUT pin functions as TSBAT, and the SRN_SYNCIN pin functions as SYNCIN. ACDRV1 and ACDRV2 are controlled by the primary, and ACDRV1 and ACDRV2 on the secondary should be grounded. Pullup the SYNCIN/SYNCOUT pins to REGN on the primary SC8541 through a 1-k Ω pull-up resistor. The maximum switching frequency in primary and secondary mode is 500 kHz. The dual charger can operate in Primary and Secondary Mode in Bypass Mode as well. In both Bypass and Switched Cap Mode, the current distribution between the two devices depends on loop impedance and the chargers do not balance it. In order to balance the current, the board layout needs to be as symmetrical as possible.

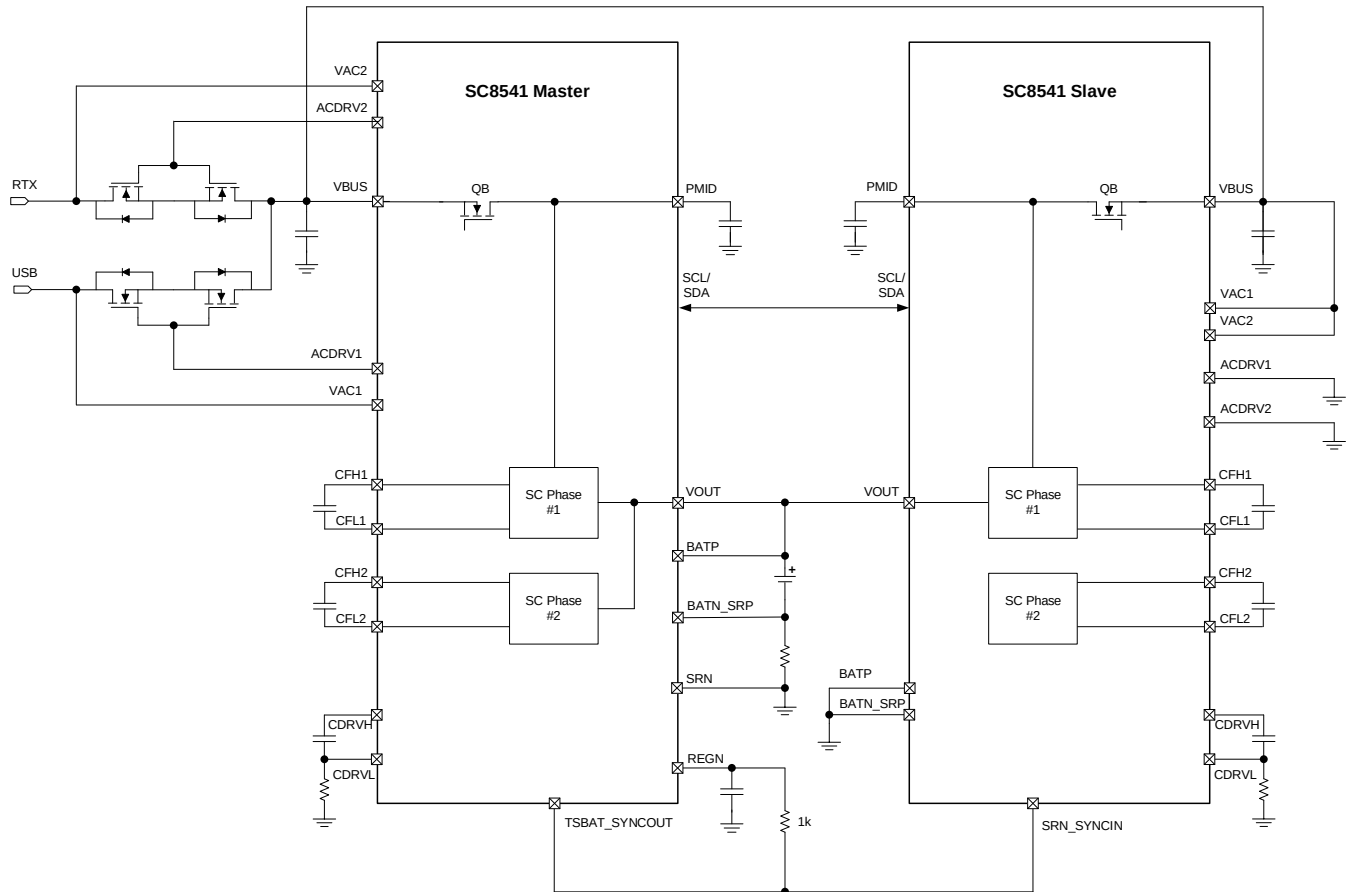


Figure 9-10. Typical schematic of SC8541 parallel operation

9.2.12 I2C Address and Mode Selection

The CDRVL_ADDRMS pin also allows setting the I2C address and device operation mode during device POR. Pull to GND with a resistor for the desired value shown in Table 9-6. The surface mount resistor with $\pm 1\%$ tolerance is recommended. After POR, the host can read back the device's configuration from MS register (CTRL5[1:0]).

Table 9-7. I2C Address and Mode Selection

RESISTOR VALUE to GND on CDRVL_ADDRMS	I2C ADDRESS	MASTER, SLAVE, or STANDALONE OPERATION
>75k	0x6A	Standalone
6.19k	0x6C	Standalone
8.06k	0x6B	Slave
10.5k	0x6B	Master
14k	0x6B	Standalone
18.2k	0x6C	Slave
27.4k	0x6A	Master

9.3 Register map and default value

ADDRESS (Hex)	ACRONYM	Default Value (Hex)	WDT RST	REG RST
0x00	VBAT_OVP	0x5A	N	Y
0x01	VBAT_OVP_ALM	0x46	N	Y
0x02	IBAT_OCP	0x51	N	Y
0x03	IBAT_OCP_ALM	0x50	N	Y
0x04	CONFIG1	0x00	N	Y
0x05	CTRL1	0x00	N	Y
0x06	VBUS_OVP	0x26	N	Y
0x07	VBUS_OVP_ALM	0x22	N	Y
0x08	IBUS_OCP	0x0D	N	Y
0x09	CONFIG3	0x00	N	Y
0x0A	TEMP_CTRL	0x00	N	Y
0x0B	TDIE_ALM	0xC8	N	Y
0x0C	TSBUS_FLT	0x15	N	Y
0x0D	TSBAT_FLT	0x15	N	Y
0x0E	VAC_CTRL	0x0C	N	Y
0x0F	CTRL2	0x00	Reset "CHG_EN" bit and "OTG_EN" bit	Y
0x10	CTRL3	0x80	N	Y
0x11	CTRL4	0x70	N	Y
0x12	CTRL5	0x60	N	Y
0x13	STAT1	0x00	N	Y
0x14	STAT2	0x00	N	Y
0x15	STAT3	0x00	N	Y
0x16	STAT4	0x00	N	Y
0x17	STAT5	0x00	N	Y
0x18	FLAG1	0x00	N	Y
0x19	FLAG2	0x00	N	Y
0x1A	FLAG3	0x00	N	Y
0x1B	FLAG4	0x00	N	Y
0x1C	FLAG5	0x00	N	Y
0x1D	MASK1	0x00	N	Y
0x1E	MASK2	0x00	N	Y
0x1F	MASK3	0x00	N	Y
0x20	MASK4	0x00	N	Y
0x21	MASK5	0x00	N	Y
0x22	PART_INFO	0x41	N	Y
0x23	ADC_CTRL	0x00	Only reset "ADC_EN" bit	Y

0x24	ADC_FN_DIS	0x00	N	Y
0x25	IBUS_ADC1	0x00	N	Y
0x26	IBUS_ADC0	0x00	N	Y
0x27	VBUS_ADC1	0x00	N	Y
0x28	VBUS_ADC0	0x00	N	Y
0x29	VAC1_ADC1	0x00	N	Y
0x2A	VAC1_ADC0	0x00	N	Y
0x2B	VAC2_ADC1	0x00	N	Y
0x2C	VAC2_ADC0	0x00	N	Y
0x2D	VOUT_ADC1	0x00	N	Y
0x2E	VOUT_ADC0	0x00	N	Y
0x2F	VBAT_ADC1	0x00	N	Y
0x30	VBAT_ADC0	0x00	N	Y
0x31	IBAT_ADC1	0x00	N	Y
0x32	IBAT_ADC0	0x00	N	Y
0x33	TSBUS_ADC1	0x00	N	Y
0x34	TSBUS_ADC0	0x00	N	Y
0x35	TSBAT_ADC1	0x00	N	Y
0x36	TSBAT_ADC0	0x00	N	Y
0x37	TDIE_ADC1	0x00	N	Y
0x38	TDIE_ADC0	0x00	N	Y
0x40	CTRL6	0x05	Reset "ACDRV_MANUAL_EN" bit, "ACDRV1_EN" bit, "ACDRV2_EN" bit	Y
0x42	PMID2OUT_OVP_UVP	0x6C	N	Y

Table1. VBAT_OVP Register (Address=00h) [reset=5Ah]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_DIS	R/W	0h	N/A	0: Enable the VBAT_OVP protection (default) 1: Disable the VBAT_OVP protection
6	VBAT_OVP[6]	R/W	1h	640mV	Battery Over-Voltage Protection Setting. When the battery voltage goes above the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Offset: 3.84V Range: 3.84V (b0000000) – 5.11V (b1111111) Default: 4.74V (b1011010)
5	VBAT_OVP[5]	R/W	0h	320mV	
4	VBAT_OVP[4]	R/W	1h	160mV	
3	VBAT_OVP[3]	R/W	1h	80mV	
2	VBAT_OVP[2]	R/W	0h	40mV	
1	VBAT_OVP[1]	R/W	1h	20mV	
0	VBAT_OVP[0]	R/W	0h	10mV	

Table2. VBAT_OVP_ALM Register (Address=01h) [reset=46h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_ALM_DIS	R/W	0h	N/A	0 = Enable the VBAT_OVP_ALM (default) 1 = Disable the VBAT_OVP_ALM
6	VBAT_OVP_ALM[6]	R/W	1h	640mV	Battery Over-Voltage Alarm Setting. When the battery voltage goes above the programmed threshold an INT is sent. Offset: 3.84V Range: 3.84V (b0000000) – 5.11V (b1111111) Default: 4.54V (b1000110)
5	VBAT_OVP_ALM[5]	R/W	0h	320mV	
4	VBAT_OVP_ALM[4]	R/W	0h	160mV	
3	VBAT_OVP_ALM[3]	R/W	0h	80mV	
2	VBAT_OVP_ALM[2]	R/W	1h	40mV	
1	VBAT_OVP_ALM[1]	R/W	1h	20mV	
0	VBAT_OVP_ALM[0]	R/W	0h	10mV	

Table3. IBAT_OCP Register (Address=02h) [reset=51h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_OCP_DIS	R/W	0h	N/A	0: Enable the IBAT_OCP protection (default) 1: Disable the IBAT_OCP protection
6	IBAT_OCP[6]	R/W	1h	6400mA	BAT Over-Current Protection Setting. When the bat current reaches the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Offset: 0A Range: 0A (b0000000) – 12.7A (b1111111) Default: 8.1A (b1010001)
5	IBAT_OCP[5]	R/W	0h	3200mA	
4	IBAT_OCP[4]	R/W	1h	1600mA	
3	IBAT_OCP[3]	R/W	0h	800mA	
2	IBAT_OCP[2]	R/W	0h	400mA	
1	IBAT_OCP[1]	R/W	0h	200mA	
0	IBAT_OCP[0]	R/W	1h	100mA	

Table4. IBAT_OCP_ALM Register (Address=03h) [reset=50h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_OCP_ALM_DIS	R/W	0h	N/A	0: Enable the IBAT_OCP_ALM protection (default) 1: Disable the IBAT_OCP_ALM protection
6	IBAT_OCP_ALM[6]	R/W	1h	6400mA	BAT Over-Current Alarm Setting. When the bat current reaches the programmed threshold, an INT is sent. Offset: 0A Range: 0A (b0000000) – 12.7A (b1111111) Default: 8A (b1010000)
5	IBAT_OCP_ALM[5]	R/W	0h	3200mA	
4	IBAT_OCP_ALM[4]	R/W	1h	1600mA	
3	IBAT_OCP_ALM[3]	R/W	0h	800mA	
2	IBAT_OCP_ALM[2]	R/W	0h	400mA	
1	IBAT_OCP_ALM[1]	R/W	0h	200mA	
0	IBAT_OCP_ALM[0]	R/W	0h	100mA	

Table5. CONFIG1 Register (Address=04h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table6. CTRL1 Register (Address=05h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_UCP_DIS	R/W	0h	N/A	0: Enable the IBUS_UCP protection (default) 1: Disable the IBUS_UCP protection
6	RESERVED	R/W	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	VBUS_IN_RANGE_DIS	R/W	0h	N/A	0: Enable the VBUS_IN_RANGE protection (default) 1: Disable the VBUS_IN_RANGE protection
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table7. VBUS_OVP Register (Address=06h) [reset=26h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_PD_EN	R/W	0h	N/A	0 = VBUS pull-down disabled (default) 1 = VBUS pull-down enabled
6	VBUS_OVP[6]	R/W	0h	3200mV	VBUS Over-Voltage Protection Setting. When the bus voltage goes above the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. 2:1 mode Offset: 7V Step: 50mV Range: 7V (b0000000) – 13.35V (b1111111) Default: 8.9V (b0100110) 1:1 mode Offset: 3.5V Step: 25mV Range: 3.5V (b0000000) – 6.675V (b1111111) Default: 4.45V (b0100110)
5	VBUS_OVP[5]	R/W	1h	1600mV	
4	VBUS_OVP[4]	R/W	0h	800mV	
3	VBUS_OVP[3]	R/W	0h	400mV	
2	VBUS_OVP[2]	R/W	1h	200mV	
1	VBUS_OVP[1]	R/W	1h	100mV	
0	VBUS_OVP[0]	R/W	0h	50mV	

Table8. VBUS_OVP_ALM Register (Address=07h) [reset=22h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_OVP_ALM_DIS	R/W	0h	N/A	0: Enable the VBUS_OVP protection (default) 1: Disable the VBUS_OVP protection
6	VBUS_OVP_ALM[6]	R/W	0h	3200mV	VBUS Over-Voltage Protection Setting. When the bus voltage goes above the programmed threshold, an INT is sent. 2:1 mode Offset: 7V Step: 50mV Range: 7V (b000000) – 13.35V (b111111) Default: 8.7V (b0100010) 1:1 mode Offset: 3.5V Step: 25mV Range: 3.5V (b000000) – 6.675V (b111111) Default: 4.35V (b0100010)
5	VBUS_OVP_ALM[5]	R/W	1h	1600mV	
4	VBUS_OVP_ALM[4]	R/W	0h	800mV	
3	VBUS_OVP_ALM[3]	R/W	0h	400mV	
2	VBUS_OVP_ALM[2]	R/W	0h	200mV	
1	VBUS_OVP_ALM[1]	R/W	1h	100mV	
0	VBUS_OVP_ALM[0]	R/W	0h	50mV	

Table9. IBUS_OCP Register (Address=08h) [reset=0Dh]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_DIS	R/W	0h	N/A	0: Enable the IBUS_OCP protection (default) 1: Disable the IBUS_OCP protection
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	IBUS_OCP[4]	R/W	0h	4A	Bus Over-Current Protection Setting. When the bus current reaches the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. Offset: 1A Range in 2:1 mode: 1A (b00000) – 8A (b11100) Range in 1:1 mode: 1A (b00000) – 8A (b11100) Default: 4.25A (b01101)
3	IBUS_OCP[3]	R/W	1h	2A	
2	IBUS_OCP[2]	R/W	1h	1A	
1	IBUS_OCP[1]	R/W	0h	500mA	
0	IBUS_OCP[0]	R/W	1h	250mA	

Table10. CONFIG3 Register (Address=09h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table11. TEMP_CTRL Register (Address=0Ah) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSHUT_DIS	R/W	0h	N/A	0 = Enable the thermal shutdown protection (default) 1 = Disable the thermal shutdown protection
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R/W	0h	N/A	
3	TSBUS_FLT_DIS	R/W	0h	N/A	0: Enable the TSBUS fault protection (default) 1: Disable the TSBUS fault protection
2	TSBAT_FLT_DIS	R/W	0h	N/A	0: Enable the TSBAT fault protection (default) 1: Disable the TSBAT fault protection
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table12. TDIE_ALM Register (Address=0Bh) [reset=C8h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TDIE_ALM[7]	R/W	1h	64°C	TDIE temperature alarm threshold. When the TDIE temperature goes above the programmed threshold, an INT is sent. Offset: 25°C Range: 25°C (b00000000) – 152.5°C (b11111111) Default: 125°C (b11001000)
6	TDIE_ALM[6]	R/W	1h	32°C	
5	TDIE_ALM[5]	R/W	0h	16°C	
4	TDIE_ALM[4]	R/W	0h	8°C	
3	TDIE_ALM[3]	R/W	1h	4°C	
2	TDIE_ALM[2]	R/W	0h	2°C	
1	TDIE_ALM[1]	R/W	0h	1°C	
0	TDIE_ALM[0]	R/W	0h	0.5°C	

Table13. TSBUS_FLT Register (Address=0Ch) [reset=15h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBUS_FLT[7]	R/W	0h	25%	<p>TSBUS percentage fault threshold. When the TSBUS pin voltage goes below the programmed threshold, an INT is sent and CHG_EN bit is set to '0'.</p> <p>Offset: 0%</p> <p>Range: 0% (b00000000) – 50% (b11111111)</p> <p>Default: 4.1% (b00010101)</p> <p>A TSBUS_TSBAT_ALM interrupt will be sent when TSBUS is within 5%+TSBUS_FLT[7:0]</p>
6	TSBUS_FLT[6]	R/W	0h	12.5%	
5	TSBUS_FLT[5]	R/W	0h	6.25%	
4	TSBUS_FLT[4]	R/W	1h	3.125%	
3	TSBUS_FLT[3]	R/W	0h	1.5625%	
2	TSBUS_FLT[2]	R/W	1h	0.78125 %	
1	TSBUS_FLT[1]	R/W	0h	0.39063 %	
0	TSBUS_FLT[0]	R/W	1h	0.19531 %	

Table14. TSBAT_FLT Register (Address=0Dh) [reset=15h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBAT_FLT[7]	R/W	0h	25%	<p>TSBAT percentage fault threshold. When the TSBAT pin voltage goes below the programmed threshold, an INT is sent and CHG_EN bit is set to '0'.</p> <p>Offset: 0%</p> <p>Range: 0% (b00000000) – 50% (b11111111)</p> <p>Default: 4.1% (b00010101)</p> <p>A TSBUS_TSBAT_ALM interrupt will be sent when TSBAT is within 5%+TSBUS_FLT[7:0]</p>
6	TSBAT_FLT[6]	R/W	0h	12.5%	
5	TSBAT_FLT[5]	R/W	0h	6.25%	
4	TSBAT_FLT[4]	R/W	1h	3.125%	
3	TSBAT_FLT[3]	R/W	0h	1.5625%	
2	TSBAT_FLT[2]	R/W	1h	0.78125 %	
1	TSBAT_FLT[1]	R/W	0h	0.39063 %	
0	TSBAT_FLT[0]	R/W	1h	0.19531 %	

Table15. VAC_CTRL Register (Address=0Eh) [reset=0Ch]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP[2]	R/W	0h	N/A	VAC1 Over-Voltage Protection Setting. When the VAC1 voltage reaches the programmed threshold, ACDRV1 is turned off. 000: 6.5V (default) 001: 10.5V 010: 12V 011: 14V 100: 16V 101-111: 18V
6	VAC1_OVP[1]	R/W	0h	N/A	
5	VAC1_OVP[0]	R/W	0h	N/A	
4	VAC2_OVP[2]	R/W	0h	N/A	VAC2 Over-Voltage Protection Setting. When the VAC2 voltage reaches the programmed threshold, ACDRV2 is turned off. 000: 6.5V 001: 10.5V 010: 12V 011: 14V (default) 100: 16V 101-111: 18V
3	VAC2_OVP[1]	R/W	1h	N/A	
2	VAC2_OVP[0]	R/W	1h	N/A	
1	VAC1_PD_EN	R/W	0h	N/A	When this bit is enabled, it pulls down the VAC1 for t_{VAC_PD} to discharge any bulk cap on VAC1 0: Disable (default) 1: Enable
0	VAC2_PD_EN	R/W	0h	N/A	When this bit is enabled, it pulls down the VAC2 for t_{VAC_PD} to discharge any bulk cap on VAC2 0: Disable (default) 1: Enable

Table16. CTRL2 Register (Address=0Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	REG_RST	R/W	0h	N/A	0 = No register reset (default) 1 = Reset registers to their default values
6	RESERVED	R	0h	N/A	
5	OTG_EN	R/W	0h	N/A	Power path control during OTG mode, when OTG_EN=1, REGN is alive 0: Precondition of ACDRV is VAC_OK 1: Precondition of ACDRV is VBUS_PRESENT
4	CHG_EN	R/W	0h	N/A	0 = Charger disabled (default) 1 = Charger enabled
3	MODE	R/W	0h	N/A	This bit decides the operation mode 0 = 2:1 charger mode (default) 1 = 1:1 charger mode
2	RESERVED	R	0h	N/A	
1	ACDRV1_STAT	R	0h	N/A	External ACFER1-RBFET1 gate driver status 0 = ACDRV1 is OFF (default) 1 = ACDRV1 is ON
0	ACDRV2_STAT	R	0h	N/A	External ACFER2-RBFET2 gate driver status 0 = ACDRV2 is OFF (default) 1 = ACDRV2 is ON

Table17. CTRL3 Register (Address=10h) [reset=80h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	FSW_SET2	R/W	1h	N/A	Set the CP switching frequency 000: 200kHz 001: 300kHz 010: 400kHz 011: 500kHz 100: 600kHz (default) 101: 650kHz 110: 700kHz 111: 750kHz
6	FSW_SET1	R/W	0h	N/A	
5	FSW_SET0	R/W	0h	N/A	
4	WD_TIMEOUT1	R/W	0h	N/A	Watchdog Timeout protection 00: 0.5s (default) 01: 1s 10: 5s 11: 30s
3	WD_TIMEOUT0	R/W	0h	N/A	
2	WD_TIMEOUT_DIS	R/W	0h	N/A	0 = Enable watchdog (default) 1 = Disable watchdog
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table18. CTRL4 Register (Address=11h) [reset=70h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	SET_IBAT_SNS_RE	R/W	0h	N/A	This bit selects the external BAT_SNS resistor value 0: 2mΩ (default) 1: 5mΩ
6	SS_TIMEOUT2	R/W	1h	N/A	Adjustable timeout for IBUS to rise to the IBUS_UCP_RISE_THRESHOLD 000: 6.25ms 001: 12.5ms 010: 25ms 011: 50ms 100: 100ms 101: 400ms 110: 1.5s 111: 10s (default)
5	SS_TIMEOUT1	R/W	1h	N/A	
4	SS_TIMEOUT0	R/W	1h	N/A	
3	IBUS_UCP_FALL_DEGLITCH_SET1	R/W	0h	N/A	This bit sets the deglitch time for IBUS_UCP_FALL 00: 10us (default) 01: 5ms 10: 50ms 11: 150ms
2	IBUS_UCP_FALL_DEGLITCH_SET0	R/W	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table19. CTRL5 Register (Address=12h) [reset=60h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VOUT_OVP_DIS	R/W	0h	N/A	0: Enable the VOUT_OVP protection (default) 1: Disable the VOUT_OVP protection
6	VOUT_OVP1	R/W	1h	N/A	VOUT Over-Voltage Protection Setting. When the VOUT voltage reaches the programmed threshold, an INT is sent and CHG_EN bit is set to '0'. 00: 4.7V 01: 4.8V 10: 4.9V 11: 5.0V (default)
5	VOUT_OVP0	R/W	1h	N/A	
4	FREQ_SHIFT1	R/W	0h	N/A	Adjust FSW for EMI 00 = Nominal frequency 01 = +10% 10 = -10% 11 = Spread spectrum varies frequency +-10%
3	FREQ_SHIFT0	R/W	0h	N/A	
2	RESERVED	R	0h	N/A	
1	MS1	R	0h	N/A	00: Standalone 01: Slave 10: Master 11: Reserved
0	MS0	R	0h	N/A	

Table20. STAT1 Register (Address=13h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_STAT	R	0h	N/A	Indicates a VBAT over-voltage event is occurring
6	VBAT_OVP_ALM_STAT	R	0h	N/A	Indicates the VBAT_OVP_ALM threshold is exceeding
5	VOUT_OVP_STAT	R	0h	N/A	This bit is set when VOUT_OVP is active
4	IBAT_OCP_STAT	R	0h	N/A	Indicates a IBAT over-current event is occurring
3	IBAT_OCP_ALM_STAT	R	0h	N/A	Indicates the IBAT_OCP_ALM threshold is exceeding
2	RESERVED	R	0h	N/A	
1	VBUS_OVP_STAT	R	0h	N/A	Indicates a VBUS over-voltage event is occurring
0	VBUS_OVP_ALM_STAT	R	0h	N/A	Indicates the VBUS_OVP_ALM threshold is exceeding

Table21. STAT2 Register (Address=14h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_STAT	R	0h	N/A	Indicates an IBUS over-current event is occurring
6	RESERVED	R	0h	N/A	
5	IBUS_UCP_FALL_STAT	R	0h	N/A	Indicates an IBUS under-current event is occurring
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	PIN_DIAG_FAIL_STAT	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table22. STAT3 Register (Address=15h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP_STAT	R	0h	N/A	Status of VAC1_OVP. Persists until condition is no longer valid
6	VAC2_OVP_STAT	R	0h	N/A	Status of VAC2_OVP. Persists until condition is no longer valid
5	VBAT_INSERT_STAT	R	0h	N/A	Indicates the VBAT UVLO threshold is exceeding
4	VAC1_INSERT_STAT	R	0h	N/A	Indicates the VAC1 UVLO threshold is exceeding
3	VAC2_INSERT_STAT	R	0h	N/A	Indicates the VAC2 UVLO threshold is exceeding
2	VBUS_PRESENT_STAT	R	0h	N/A	Indicates the VBUS PRESENT threshold is exceeding
1	ACRB1_CONFIG_STAT	R	0h	N/A	0: ACDRV1 pin is tied to GND 1: ACDRV1 pin is not tied to GND
0	ACRB2_CONFIG_STAT	R	0h	N/A	0: ACDRV2 pin is tied to GND 1: ACDRV2 pin is not tied to GND

Table23. STAT4 Register (Address=16h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	ADC_DONE_STAT	R	0h	N/A	Indicates the ADC conversion is complete in 1-shot mode only.
6	SS_TIMEOUT_STAT	R	0h	N/A	Soft-start timeout status
5	TSBUS_TSBAT_ALARM_STAT	R	0h	N/A	Indicates the TSBUS or TSBAT alarm threshold is exceeding
4	TSBUS_FLT_STAT	R	0h	N/A	Indicates a TSBUS over-temp event is occurring
3	TSBAT_FLT_STAT	R	0h	N/A	Indicates a TSBAT over-temp event is occurring
2	TSHUT_STAT	R	0h	N/A	Thermal shutdown status. This register is 1 until the event no longer persists.
1	TDIE_ALM_STAT	R	0h	N/A	Indicates the TDIE alarm threshold is exceeding
0	WD_TIMEOUT_STAT	R	0h	N/A	Watchdog timeout status

Table24. STAT5 Register (Address=17h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	CP_SWITCHING_STAT	R	0h	N/A	0: Charge-pump is not switching 1: Charge-pump is switching
5	RESERVED	R	0h	N/A	
4	VBUS_ERRORHI_STAT	R	0h	N/A	This bit shows the current status of VBUS, and is '0' only when the event is not happening.
3	VBUS_ERRORLO_STAT	R	0h	N/A	This bit shows the current status of VBUS, and is '0' only when the event is not happening.
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table25. FLAG1 Register (Address=18h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_FLAG	R	0h	N/A	
6	VBAT_OVP_ALM_FLAG	R	0h	N/A	
5	VOUT_OVP_FLAG	R	0h	N/A	
4	IBAT_OCP_FLAG	R	0h	N/A	
3	IBAT_OCP_ALM_FLAG	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	VBUS_OVP_FLAG	R	0h	N/A	
0	VBUS_OVP_ALM_FLAG	R	0h	N/A	

Table26. FLAG2 Register (Address=19h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_FLAG	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	IBUS_UCP_FALL_FLAG	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	PIN_DIAG_FAIL_FLAG	R	0h	N/A	Pin diagnostic fail flag. CPLY short and CDRV short/open will be checked before switch. An INT is sent when this event happens and is cleared when read. This bit is not maskable.
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table27. FLAG3 Register (Address=1Ah) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP_FLAG	R	0h	N/A	
6	VAC2_OVP_FLAG	R	0h	N/A	
5	VBAT_INSERT_FLAG	R	0h	N/A	
4	VAC1_INSERT_FLAG	R	0h	N/A	
3	VAC2_INSERT_FLAG	R	0h	N/A	
2	VBUS_PRESENT_FLAG	R	0h	N/A	
1	ACRB1_CONFIG_FLAG	R	0h	N/A	
0	ACRB2_CONFIG_FLAG	R	0h	N/A	

Table28. FLAG4 Register (Address=1Bh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	ADC_DONE_FLAG	R	0h	N/A	
6	SS_TIMEOUT_FLAG	R	0h	N/A	
5	TSBUS_TSBAT_ALM_FLAG	R	0h	N/A	
4	TSBUS_FLT_FLAG	R	0h	N/A	
3	TSBAT_FLT_FLAG	R	0h	N/A	
2	TSHUT_FLAG	R	0h	N/A	
1	TDIE_ALM_FLAG	R	0h	N/A	
0	WD_TIMEOUT_FLAG	R	0h	N/A	

Table29. FLAG5 Register (Address=1Ch) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	CP_SWITCHING_FLAG	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	VBUS_ERRORHI_FLAG	R	0h	N/A	
3	VBUS_ERRORLO_FLAG	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table30. MASK1 Register (Address=1Dh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_OVP_MASK	R/W	0h	N/A	
6	VBAT_OVP_ALM_MASK	R/W	0h	N/A	
5	VOUT_OVP_MASK	R/W	0h	N/A	
4	IBAT_OCP_MASK	R/W	0h	N/A	
3	IBAT_OCP_ALM_MASK	R/W	0h	N/A	
2	RESERVED	R	0h	N/A	
1	VBUS_OVP_MASK	R/W	0h	N/A	
0	VBUS_OVP_ALM_MASK	R/W	0h	N/A	

Table31. MASK2 Register (Address=1Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_OCP_MASK	R/W	0h	N/A	
6	RESERVED	R	0h	N/A	
5	IBUS_UCP_FALL_MASK	R/W	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	PIN_DIAG_FAIL_MASK	R/W	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table32. MASK3 Register (Address=1Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_OVP_MASK	R/W	0h	N/A	
6	VAC2_OVP_MASK	R/W	0h	N/A	
5	VBAT_INSERT_MA SK	R/W	0h	N/A	
4	VAC1_INSERT_MA SK	R/W	0h	N/A	
3	VAC2_INSERT_MA SK	R/W	0h	N/A	
2	VBUS_PRESENT_ MASK	R/W	0h	N/A	
1	ACRB1_CONFIG_ MASK	R/W	0h	N/A	
0	ACRB2_CONFIG_ MASK	R/W	0h	N/A	

Table33. MASK4 Register (Address=20h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	ADC_DONE_MASK	R/W	0h	N/A	
6	SS_TIMEOUT_MA SK	R/W	0h	N/A	
5	TSBUS_TSBAT_AL M_MASK	R/W	0h	N/A	
4	TSBUS_FLT_MAS K	R/W	0h	N/A	
3	TSBAT_FLT_MASK	R/W	0h	N/A	
2	TSHUT_MASK	R/W	0h	N/A	
1	TDIE_ALM_MASK	R/W	0h	N/A	
0	WD_TIMEOUT_MA SK	R/W	0h	N/A	

Table34. MASK5 Register (Address=21h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	CP_SWITCHING_MASK	R/W	0h	N/A	
5	RESERVED	R	0h	N/A	
4	VBUS_ERRORHI_MASK	R/W	0h	N/A	
3	VBUS_ERRORLO_MASK	R/W	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	RESERVED	R	0h	N/A	

Table35. PART_INFO Register (Address=22h) [reset=41h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	Device ID7	R	0h	N/A	0x41
6	Device ID6	R	0h	N/A	
5	Device ID5	R	0h	N/A	
4	Device ID4	R	0h	N/A	
3	Device ID3	R	0h	N/A	
2	Device ID2	R	0h	N/A	
1	Device ID1	R	0h	N/A	
0	Device ID0	R	0h	N/A	

Table36. ADC_CTRL Register (Address=23h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	ADC_EN	R/W	0h	N/A	Enable ADC 0 = Disabled 1 = Enabled
6	ADC_RATE	R/W	0h	N/A	0 = Continuous conversion 1 = One-shot
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	IBUS_ADC_DIS	R/W	0h	N/A	0: Enable Conversion (default) 1: Disable Conversion
0	VBUS_ADC_DIS	R/W	0h	N/A	0: Enable Conversion (default) 1: Disable Conversion

Table37. ADC_FN_DISABLE Register (Address=24h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_ADC_DIS	R/W	0h	N/A	0: Enable Conversion (default) 1: Disable Conversion
6	VAC2_ADC_DIS	R/W	0h	N/A	
5	VOUT_ADC_DIS	R/W	0h	N/A	
4	VBAT_ADC_DIS	R/W	0h	N/A	
3	IBAT_ADC_DIS	R/W	0h	N/A	
2	TSBUS_ADC_DIS	R/W	0h	N/A	
1	TSBAT_ADC_DIS	R/W	0h	N/A	
0	TDIE_ADC_DIS	R/W	0h	N/A	

Table38. IBUS_ADC1 Register (Address=25h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	IBUS ADC LSB: 2.5mA
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBUS_ADC[11]	R	0h	N/A	
2	IBUS_ADC[10]	R	0h	N/A	
1	IBUS_ADC[9]	R	0h	N/A	
0	IBUS_ADC[8]	R	0h	N/A	

Table39. IBUS_ADC0 Register (Address=26h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBUS_ADC[7]	R	0h	N/A	IBUS ADC LSB: 2.5mA
6	IBUS_ADC[6]	R	0h	N/A	
5	IBUS_ADC[5]	R	0h	N/A	
4	IBUS_ADC[4]	R	0h	N/A	
3	IBUS_ADC[3]	R	0h	N/A	
2	IBUS_ADC[2]	R	0h	N/A	
1	IBUS_ADC[1]	R	0h	N/A	
0	IBUS_ADC[0]	R	0h	N/A	

Table40. VBUS_ADC1 Register (Address=27h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VBUS ADC LSB: 3.75mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VBUS_ADC[11]	R	0h	N/A	
2	VBUS_ADC[10]	R	0h	N/A	
1	VBUS_ADC[9]	R	0h	N/A	
0	VBUS_ADC[8]	R	0h	N/A	

Table41. VBUS_ADC0 Register (Address=28h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBUS_ADC[7]	R	0h	N/A	VBUS ADC LSB: 3.75mV
6	VBUS_ADC[6]	R	0h	N/A	
5	VBUS_ADC[5]	R	0h	N/A	
4	VBUS_ADC[4]	R	0h	N/A	
3	VBUS_ADC[3]	R	0h	N/A	
2	VBUS_ADC[2]	R	0h	N/A	
1	VBUS_ADC[1]	R	0h	N/A	
0	VBUS_ADC[0]	R	0h	N/A	

Table42. VAC1_ADC1 Register (Address=29h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VAC1 ADC LSB: 5mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VAC1_ADC[11]	R	0h	N/A	
2	VAC1_ADC[10]	R	0h	N/A	
1	VAC1_ADC[9]	R	0h	N/A	
0	VAC1_ADC[8]	R	0h	N/A	

Table43. VAC1_ADC0 Register (Address=2Ah) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC1_ADC[7]	R	0h	N/A	VAC1 ADC LSB: 5mV
6	VAC1_ADC[6]	R	0h	N/A	
5	VAC1_ADC[5]	R	0h	N/A	
4	VAC1_ADC[4]	R	0h	N/A	
3	VAC1_ADC[3]	R	0h	N/A	
2	VAC1_ADC[2]	R	0h	N/A	
1	VAC1_ADC[1]	R	0h	N/A	
0	VAC1_ADC[0]	R	0h	N/A	

Table44. VAC2_ADC1 Register (Address=2Bh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VAC2 ADC LSB: 5mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VAC2_ADC[11]	R	0h	N/A	
2	VAC2_ADC[10]	R	0h	N/A	
1	VAC2_ADC[9]	R	0h	N/A	
0	VAC2_ADC[8]	R	0h	N/A	

Table45. VAC2_ADC0 Register (Address=2Ch) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VAC2_ADC[7]	R	0h	N/A	VAC2 ADC LSB: 5mV
6	VAC2_ADC[6]	R	0h	N/A	
5	VAC2_ADC[5]	R	0h	N/A	
4	VAC2_ADC[4]	R	0h	N/A	
3	VAC2_ADC[3]	R	0h	N/A	
2	VAC2_ADC[2]	R	0h	N/A	
1	VAC2_ADC[1]	R	0h	N/A	
0	VAC2_ADC[0]	R	0h	N/A	

Table46. VOUT_ADC1 Register (Address=2Dh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VOUT ADC LSB: 1.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VOUT_ADC[11]	R	0h	N/A	
2	VOUT_ADC[10]	R	0h	N/A	
1	VOUT_ADC[9]	R	0h	N/A	
0	VOUT_ADC[8]	R	0h	N/A	

Table47. VOUT_ADC0 Register (Address=2Eh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VOUT_ADC[7]	R	0h	N/A	VOUT ADC LSB: 1.25mV
6	VOUT_ADC[6]	R	0h	N/A	
5	VOUT_ADC[5]	R	0h	N/A	
4	VOUT_ADC[4]	R	0h	N/A	
3	VOUT_ADC[3]	R	0h	N/A	
2	VOUT_ADC[2]	R	0h	N/A	
1	VOUT_ADC[1]	R	0h	N/A	
0	VOUT_ADC[0]	R	0h	N/A	

Table48. VBAT_ADC1 Register (Address=2Fh) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	VBAT ADC LSB: 1.25mV
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	VBAT_ADC[11]	R	0h	N/A	
2	VBAT_ADC[10]	R	0h	N/A	
1	VBAT_ADC[9]	R	0h	N/A	
0	VBAT_ADC[8]	R	0h	N/A	

Table49. VBAT_ADC0 Register (Address=30h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	VBAT_ADC[7]	R	0h	N/A	VBAT ADC LSB: 1.25mV
6	VBAT_ADC[6]	R	0h	N/A	
5	VBAT_ADC[5]	R	0h	N/A	
4	VBAT_ADC[4]	R	0h	N/A	
3	VBAT_ADC[3]	R	0h	N/A	
2	VBAT_ADC[2]	R	0h	N/A	
1	VBAT_ADC[1]	R	0h	N/A	
0	VBAT_ADC[0]	R	0h	N/A	

Table50. IBAT_ADC1 Register (Address=31h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	IBAT ADC LSB: 3.125mA
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	IBAT_ADC[11]	R	0h	N/A	
2	IBAT_ADC[10]	R	0h	N/A	
1	IBAT_ADC[9]	R	0h	N/A	
0	IBAT_ADC[8]	R	0h	N/A	

Table51. IBAT_ADC0 Register (Address=32h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	IBAT_ADC[7]	R	0h	N/A	IBAT ADC LSB: 3.125mA
6	IBAT_ADC[6]	R	0h	N/A	
5	IBAT_ADC[5]	R	0h	N/A	
4	IBAT_ADC[4]	R	0h	N/A	
3	IBAT_ADC[3]	R	0h	N/A	
2	IBAT_ADC[2]	R	0h	N/A	
1	IBAT_ADC[1]	R	0h	N/A	
0	IBAT_ADC[0]	R	0h	N/A	

Table52. TSBUS_ADC1 Register (Address=33h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	TSBUS_ADC[9]	R	0h	50%	
0	TSBUS_ADC[8]	R	0h	25%	

Table53. TSBUS_ADC0 Register (Address=34h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBUS_ADC[7]	R	0h	12.5%	TSBUS pin voltage as a percentage of VOUT TSBUS percentage = TSBUS_ADC [9:0] * 0.09766%
6	TSBUS_ADC[6]	R	0h	6.25%	
5	TSBUS_ADC[5]	R	0h	3.125%	
4	TSBUS_ADC[4]	R	0h	1.5625%	
3	TSBUS_ADC[3]	R	0h	0.78125 %	
2	TSBUS_ADC[2]	R	0h	0.39063 %	
1	TSBUS_ADC[1]	R	0h	0.19531 %	
0	TSBUS_ADC[0]	R	0h	0.09766 %	

Table54. TSBAT_ADC1 Register (Address=35h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	TSBAT_ADC[9]	R	0h	50%	
0	TSBAT_ADC[8]	R	0h	25%	

Table55. TSBAT_ADC0 Register (Address=36h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TSBAT_ADC[7]	R	0h	12.5%	TSBAT pin voltage as a percentage of VOUT TSBAT percentage = TSBAT_ADC [9:0] * 0.09766%
6	TSBAT_ADC[6]	R	0h	6.25%	
5	TSBAT_ADC[5]	R	0h	3.125%	
4	TSBAT_ADC[4]	R	0h	1.5625%	
3	TSBAT_ADC[3]	R	0h	0.78125 %	
2	TSBAT_ADC[2]	R	0h	0.39063 %	
1	TSBAT_ADC[1]	R	0h	0.19531 %	
0	TSBAT_ADC[0]	R	0h	0.09766 %	

Table56. TDIE_ADC1 Register (Address=37h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	RESERVED	R	0h	N/A	
6	RESERVED	R	0h	N/A	
5	RESERVED	R	0h	N/A	
4	RESERVED	R	0h	N/A	
3	RESERVED	R	0h	N/A	
2	RESERVED	R	0h	N/A	
1	RESERVED	R	0h	N/A	
0	TDIE_ADC[8]	R	0h	128°C	

Table57. TDIE_ADC0 Register (Address=38h) [reset=00h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	TDIE_ADC[7]	R	0h	64°C	DIE temperature = TDIE_ADC [8:0] * 0.5°C
6	TDIE_ADC[6]	R	0h	32°C	
5	TDIE_ADC[5]	R	0h	16°C	
4	TDIE_ADC[4]	R	0h	8°C	
3	TDIE_ADC[3]	R	0h	4°C	
2	TDIE_ADC[2]	R	0h	2°C	
1	TDIE_ADC[1]	R	0h	1°C	
0	TDIE_ADC[0]	R	0h	0.5°C	

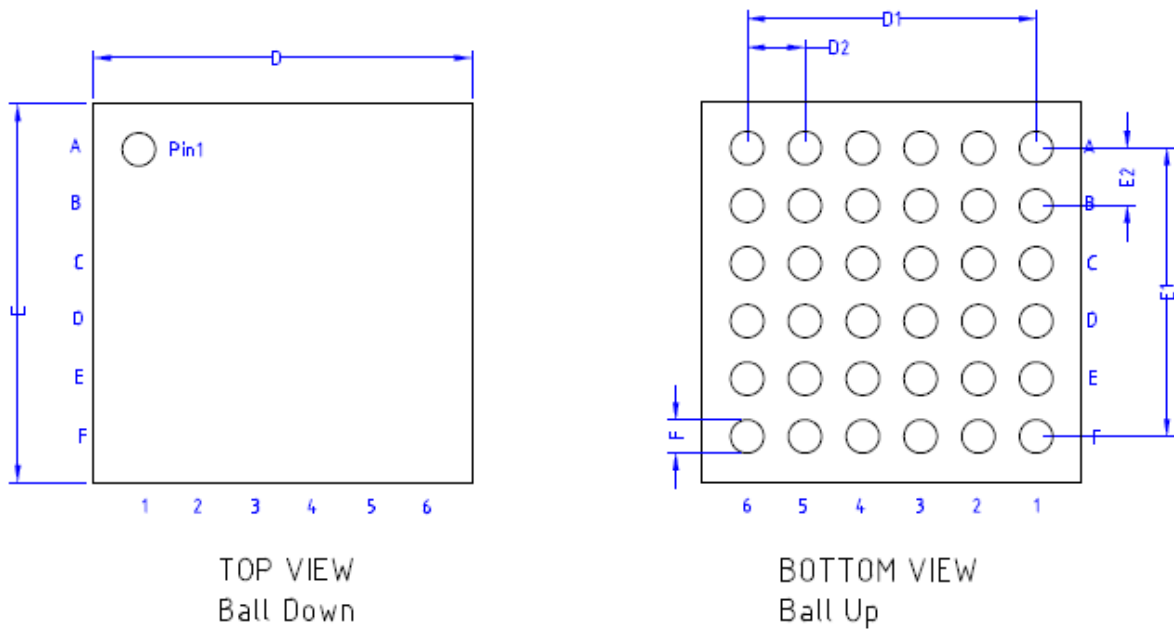
Table58. CTRL6 Register (Address=40h) [reset=05h]

Bit	Field	Type	Default value @POR	Bit Value	Notes
7	POR_FLAG	R	0h	N/A	Indicate a POR event has ever happened
6	ACDRV_MANUAL_EN	R/W	0h	N/A	0 = Auto-mode (default) 1 = Manual-mode
5	ACDRV1_EN	R/W	0h	N/A	0 = Disable ACDRV1 (default) 1 = Enable ACDRV1
4	ACDRV2_EN	R/W	0h	N/A	0 = Disable ACDRV2 (default) 1 = Enable ACDRV2
3	IBUS_UCP_RISE_FLAG	R	0h	N/A	IBUS under-current threshold rising flag. An INT is sent when this occurs, and is cleared upon read.
2	IBUS_UCP_RISE_MASK	R/W	1h	N/A	IBUS under-current threshold rising /INT mask 0: Not masked 1: Masked
1	VOUT_OK_CHG_FLAG	R	0h	N/A	Indicates the VOUT_TH_CHG_EN threshold has been exceeded. An INT is sent when this occurs and is cleared upon read
0	VOUT_OK_CHG_MASK	R/W	1h	N/A	0 = Not Masked; 1 = Masked

Table59. PMID2OUT_OVP_UVP (Address=42h) [reset=6Ch]

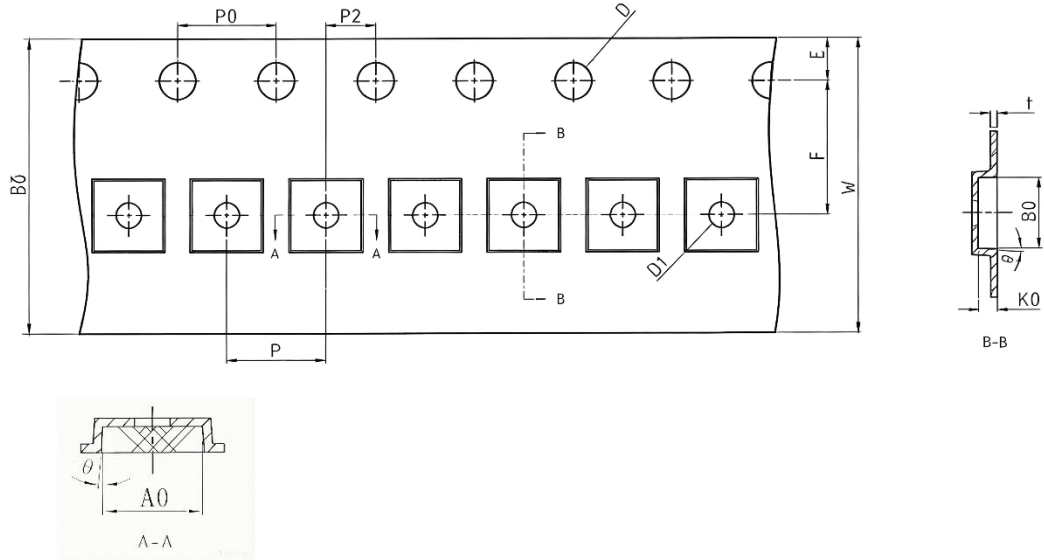
Bit	Field	Type	Default value @POR	Bit Value	Notes
7	PMID2OUT_UVP2	R/W	0h	-100mV	PMID/2-VOUT UVP is used to protect input short. Offset: -50mV Range: -50mV (b000) ~ -225mV (b111) Default: -125mV (b011)
6	PMID2OUT_UVP1	R/W	1h	-50mV	
5	PMID2OUT_UVP0	R/W	1h	-25mV	
4	PMID2OUT_OVP2	R/W	0h	200mV	PMID/2-VOUT OVP is used to protect output short. Offset: 150mV Range: 150mV (b000) ~ 500mV (b111) Default: 300mV (b011)
3	PMID2OUT_OVP1	R/W	1h	100mV	
2	PMID2OUT_OVP0	R/W	1h	50mV	
1	PMID2OUT_UVP_F LAG	R	0h	N/A	PMID/2-VOUT under-voltage flag. An INT is sent and CHG_EN bit is set to '0' when this event happens. This bit is cleared when read.
0	PMID2OUT_OVP_F LAG	R	0h	N/A	PMID/2-VOUT over-voltage flag. An INT is sent when this event happens, and is cleared when read.

MECHANICAL DATA



Unit:mm				
	NO.	Mean	Tolerance	
Top Thickness	A	0.575	± 0.0405	
Ball Height+UBM Thickness	A1	0.216	± 0.023	
Wafer/Grinding Thickness	A2	0.319	± 0.0125	
Backside Coating Thickness	A3	0.040	± 0.005	
Pkg Die Size	X	D	2.685	± 0.025
	Y	E	2.685	± 0.025
Ball diameter	F	0.265	± 0.020	
Ball Pitch	D1	2.000	NA	
	D2	0.400	NA	
	E1	2.000	NA	
	E2	0.400	NA	

TAPE INFORMATION



Item	W	P	Ao	Bo	Ko	t	θ
Size (mm)	12.00 +0.30/-0.10	4.00±0.10	2.82±0.05	2.82±0.05	0.74±0.05	0.25±0.03	5° TYP

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