

SC25042Q

1 Descriptions

The SC25042Q high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

2 Features

ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant

Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase

Ringing suppression reduces signal ringing in a larger topologies network

Suitable for 12 V and 24 V systems

Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)

V_{IO} input on SC25042AQ allows for direct interfacing with 3 V to 5V microcontrollers

Available in SOP8 package and leadless DFN8 package (3.0 mm × 3.0 mm) with improved Automated Optical Inspection (AOI) capability

AEC-Q100 qualified

3 Applications

Automotive and Transportation

All devices support highly loaded CAN networks

4 Device Information

ORDER NUMBER	FUNCTION	PACKAGE	BODY SIZE
SC25042ASQSEER	With V _{IO}	SOP8	4.9mm x 3.9mm x 1.75mm
SC25042BSQSEER	Only V _{CC}	SOP8	4.9mm x 3.9mm x 1.75mm
SC25042ADQDDJR	With V _{IO}	DFN8	3mm x 3mm x 0.85mm
SC25042BDQDDJR	Only V _{CC}	DFN8	3mm x 3mm x 0.85mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
0.0.0	2025/02/12	New	1.Draft version
0.0.1	2025/06/16	Page 9	1. Leakage current
0.0.2	2025/07/28	Page 2	1.FUNCTION

6 Typical Application Circuit

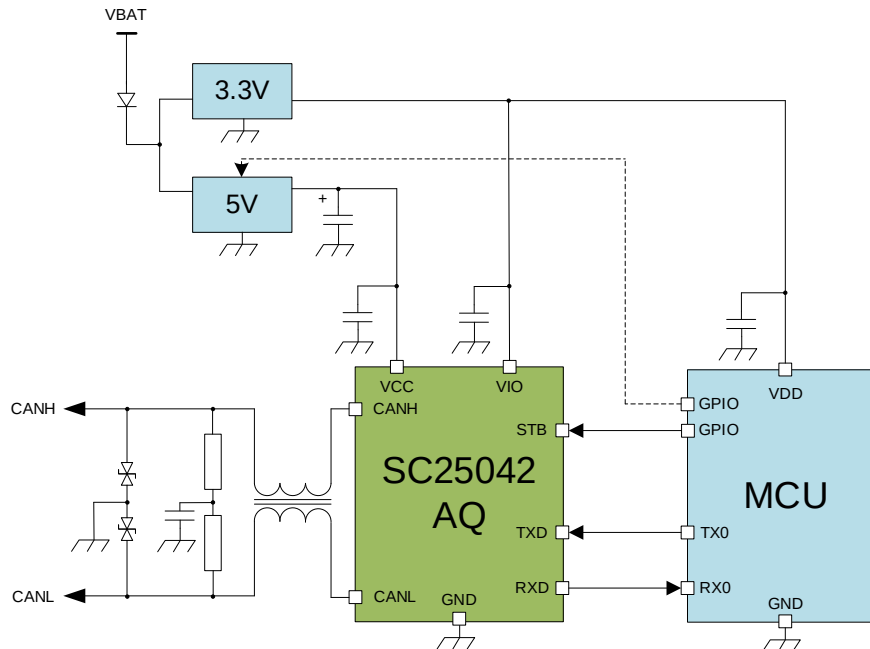


Figure 6-1. Typical SC25042AQ with a 3.3V microcontroller

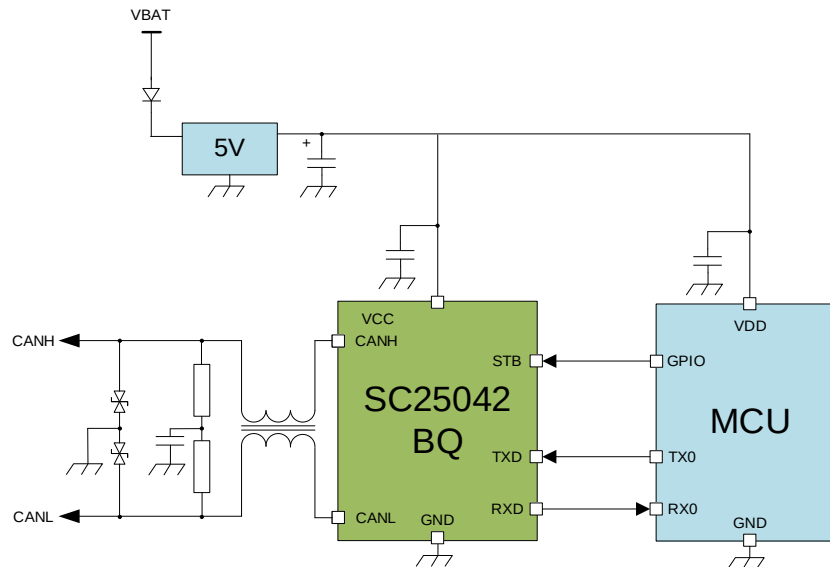
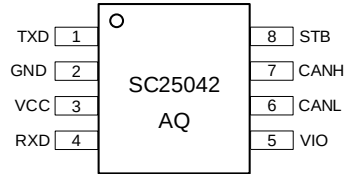
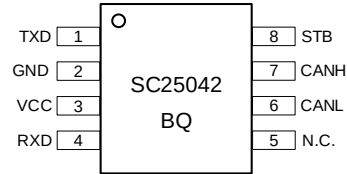
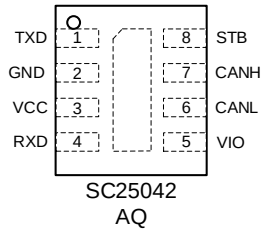
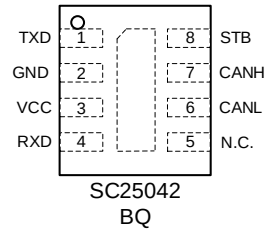


Figure 6-2. Typical SC25042BQ with a 5V microcontroller

7 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	TXD	I	transmit data input; inputs data (from the CAN controller) to be written to the bus lines
2	GND	G	ground
3	VCC	P	supply voltage input
4	RXD	O	receive data output; outputs data read from the bus lines (to the CAN controller)
5	VIO	P	supply voltage input for I/O level adapter in
	N.C.	—	not connected in
6	CANL	AIO	LOW-level CAN bus line
7	CANH	AIO	HIGH-level CAN bus line
8	STB	I	Standby mode control input; active-HIGH

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER			MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	voltage on pin x	pins CANH and CANL	-58	+58	V
		on any other pin	-0.3	+7	V
V _(CANH-CANL)	voltage between pin CANH and pin CANL		-27	+27	V
T _J	Operating junction temperature range		-40	150	°C
T _{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	TEST CONDITIONS	MIN	MAX	UNIT
ESD	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) ⁽¹⁾			
		at pins CANH and CANL	-8	+8	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ ⁽²⁾			
		at pins CANH and CANL	-8	+8	kV
		at any other pin	-4	+4	kV
		Charged Device Model (CDM); field Induced charge; 4 pF ⁽⁴⁾			
		at corner pins	-750	+750	V
V _{trt}	transient voltage	on pins CANH, CANL ⁽⁵⁾			V
		Pulse 1	-100	-	V
		Pulse 2a	-	75	V
		Pulse 3a	-150	-	V
		Pulse 3b	-	100	V
		at any pin	-500	+500	V

(1) According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

(2) According to AEC-Q100-002.

(3) According to AEC-Q100-003.

(4) According to AEC-Q100-011 Rev-C1. The classification level is C4B.

(5) According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V _{CC}	supply voltage	4.5	-	5.5	V
V _{IO}	supply voltage on pin V _{IO}	2.8	-	5.5	V
V _{uvd(stb)} (VCC)	undervoltage detection voltage on pin V _{CC}	3.5	4	4.3	V
V _{uvd(swoff)} (VCC)	switch-off undervoltage detection voltage on pin V _{CC}	2.2	2.4	2.6	V
V _{uvd(swoff)} (VIO)	switch-off undervoltage detection voltage on pin V _{IO}	2.2	2.4	2.6	V
I _{CC}	Standby mode	-	10	15	μA
	Normal mode; bus recessive	2.5	5	10	mA
	Normal mode; bus dominant	20	45	70	mA
I _{IO}	Standby mode; V _{TXD} = V _{IO}	5	-	16.5	μA
	Normal mode				
	recessive; V _{TXD} = V _{IO}	15	80	200	μA
	dominant; V _{TXD} = 0 V	-	350	1000	μA
T _A	Operating ambient temperature	-40		125	°C
T _J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾			Value	UNIT
R _{th(vj-a)}	thermal resistance from virtual junction to ambient	SOP8 package; in free air	145	°C/W
		DFN8 package; in free air	50	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

8.5 Electrical Characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V⁽³⁾; R_L = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC⁽²⁾.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply; pin V _{CC}						
V _{CC}	supply voltage		4.5	-	5.5	V
V _{uvd(stb)} (V _{CC})	undervoltage detection voltage on pin V _{CC}		3.5	4	4.3	V
V _{uvd(swoff)} (V _{CC})	switch-off undervoltage detection voltage on pin V _{CC}		2.2	2.4	2.6	V
I _{CC}	supply current	Standby mode				
		SC25042A; includes I _{IO} ; V _{TXD} = V _{IO} ⁽³⁾	-	10	15	μA
		SC25042B	-	-	5	μA
		Normal mode				
		recessive; V _{TXD} = V _{IO} ⁽³⁾	1	3	10	mA
		dominant; V _{TXD} = 0V	20	45	70	mA
		dominant; V _{TXD} = 0V; short circuit on bus lines; -3 < (V _{CANH} = V _{CANL}) <+18 V	2.5	80	110	mA
I/O level adapter supply; pin V _{IO} ⁽¹⁾						
V _{IO}	supply voltage on pin V _{IO}		2.8	-	5.5	V
V _{uvd(swoff)} (V _{IO})	switch-off undervoltage detection voltage on pin V _{IO}		2.2	2.4	2.6	V
I _{IO}	supply current on pin V _{IO}	Standby mode; V _{TXD} = V _{IO} ⁽³⁾	5	-	16.5	μA
		Normal mode				
		recessive; V _{TXD} = V _{IO} ⁽³⁾	5	15	200	μA
		dominant; V _{TXD} = 0V		150	1000	μA
Standby mode control input; pin STB						
V _{IH}	HIGH-level input voltage	⁽⁴⁾	0.7 V _{IO} ⁽³⁾	-	V _{IO} ⁽³⁾ + 0.3	V

V_{IL}	LOW-level input voltage		-0.3	-	$0.3 V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{IO}^{(3)}$	-1	-	+1	μA
I_{IL}	LOW-level input current	$V_{STB} = 0V$	-15	-	-1	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage	⁽⁴⁾	$0.7 V_{IO}$	-	$V_{IO} + 0.3$	V
V_{IL}	LOW-level input voltage		-0.3	-	$0.3 V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{IO}^{(3)}$	-5	-	+5	μA
I_{IL}	LOW-level input current	$V_{TXD} = 0V$	-260	-150	-30	μA
C_i	input capacitance	⁽⁵⁾	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO} - 0.4V$	-8	-4.5	-1	mA
I_{OL}	LOW-level output current	$V_{RXD} = 0.4V$; bus dominant	2	5	12	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	$V_{TXD} = 0V$; $t < t_{to(dom)TXD}$ $V_{CC} = 4.5 V$ to $5.5 V$				
		pin CANH; $R_L = 50 \Omega$ to 65Ω	2.75	3.5	4.5	V
		pin CANL; $R_L = 50 \Omega$ to 65Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; ⁽⁵⁾ $f_{TXD} = 250 kHz, 1 MHz$ or $2.5 MHz$	$0.9 V_{CC}$		$1.1 V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant: Normal mode; $V_{TXD} = 0 V$; $t < t_{to(dom)TXD}$; $V_{CC} = 4.5 V$ to $5.5 V$				
		$R_L = 45 \Omega$ to 65Ω	1.5	-	3	V
		$R_L = 45 \Omega$ to 70Ω	1.4	-	3.3	V
		$R_L = 2240 \Omega$	1.5	-	5	V
		recessive; no load				
		Normal mode: $V_{TXD} = V_{IO}^{(3)}$	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXD} = V_{IO}^{(3)}$; no load	2	$0.5V_{CC}$	3	V
		Standby mode; no load	-0.1	-	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	$-30 V < V_{CANL} < +30 V$; $-30 V < V_{CANH} < +30 V$				
		Normal mode	0.5	0.7	0.9	V

		Standby mode	0.4	0.7	1.15	V
$V_{\text{rec(RX)}}$	receiver recessive voltage	$-30\text{ V} < V_{\text{CANL}} < +30\text{ V};$ $-30\text{ V} < V_{\text{CANH}} < +30\text{ V}$				
		Normal mode	-4	-	0.5	V
		Standby mode	-4	-	0.4	V
$V_{\text{dom(RX)}}$	receiver recessive voltage	$-30\text{ V} < V_{\text{CANL}} < +30\text{ V};$ $-30\text{ V} < V_{\text{CANH}} < +30\text{ V}$				
		Normal mode	0.9		9.0	V
		Standby mode	1.15		9.0	V
$V_{\text{hys(RX)dif}}$	differential receiver hysteresis voltage	$-30\text{ V} < V_{\text{CANL}} < +30\text{ V};$ $-30\text{ V} < V_{\text{CANH}} < +30\text{ V}$	50	120	200	mV
$I_{\text{O(SC)dom}}$	dominant short-circuit output current	$V_{\text{TXD}} = 0\text{ V}; t < t_{\text{O(dom)TXD}};$ $V_{\text{CC}} = 5\text{ V}$				
		pin CANH; $V_{\text{CANH}} = -15\text{ V to } +40\text{ V}$	-100	-70	-	mA
		pin CANL; $V_{\text{CANL}} = -15\text{ V to } +40\text{ V}$	-	70	100	mA
$I_{\text{O(SC)rec}}$	recessive short-circuit output current	Normal mode; $V_{\text{TXD}} = V_{\text{IO}}^{(3)}$ $V_{\text{CANH}} = V_{\text{CANL}} = -27\text{ V to } +32\text{ V}$	-5	-	+5	mA
I_{L}	leakage current	$V_{\text{CC}} = V_{\text{IO}} = 0\text{ V}$ or $V_{\text{CC}} = V_{\text{IO}} = \text{shorted to ground via } 47\text{ k}\Omega;$ $V_{\text{CANH}} = V_{\text{CANL}} = 5\text{ V}$	-10	-	+10	μA
R_{i}	input resistance	$-2\text{ V} < V_{\text{CANL}} < +7\text{ V};^{(5)}$ $-2\text{ V} < V_{\text{CANH}} < +7\text{ V}$	25	40	50	k Ω
ΔR_{i}	input resistance deviation	$-2\text{ V} < V_{\text{CANL}} < +7\text{ V};^{(5)}$ $-2\text{ V} < V_{\text{CANH}} < +7\text{ V}$	-3	-	+3	%
$R_{\text{i(dif)}}$	differential input resistance	$-2\text{ V} < V_{\text{CANL}} < +7\text{ V};^{(5)}$ $-2\text{ V} < V_{\text{CANH}} < +7\text{ V}$	50	80	100	k Ω
$C_{\text{i(cm)}}$	common-mode input capacitance	⁽⁵⁾	-	-	20	pF
$C_{\text{i(dif)}}$	differential input capacitance	⁽⁵⁾	-	-	10	pF
Temperature detection						
$T_{\text{j(sd)}}$	shutdown junction temperature	⁽⁵⁾	-	175	-	$^{\circ}\text{C}$
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 8-1 and Figure 8-2						
$t_{\text{d(TXD-busdom)}}$	delay time from TXD to bus dominant	Normal mode ⁽⁵⁾	-	65	102.5	ns

$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode ⁽⁵⁾	-	90	102.5	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode ⁽⁵⁾	-	60	127.5	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode ⁽⁵⁾	-	65	127.5	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	versions with V _{IO} pin; Normal mode	60	-	230	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	versions with V _{IO} pin; Normal mode	60	-	230	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)} = 500 \text{ ns}^{(5)}$	435	-	530	ns
		$t_{bit(TXD)} = 200 \text{ ns}^{(5)}$	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)} = 500 \text{ ns}^{(5)}$	400	-	550	ns
		$t_{bit(TXD)} = 200 \text{ ns}^{(5)}$	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)} = 500 \text{ ns}^{(5)}$	-65	-	+40	ns
		$t_{bit(TXD)} = 200 \text{ ns}^{(5)}$	-45	-	+15	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V _{TXD} = 0 V; Normal mode	0.8	3	6.5	ms
$t_{d(stb-norm)}$	standby to normal mode delay time		7	25	47	μs
$t_{wake(busdom)}$	bus dominant wake-up time	⁽⁵⁾	0.5	-	1.8	μs
$t_{wake(busrec)}$	bus recessive wake-up time	⁽⁵⁾	0.5	-	1.8	μs
$t_{to(wake)bus}$	bus wake-up time-out time		0.8	3	6.5	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	⁽⁵⁾	0.5	-	1.8	μs

- (1) Only the SC25042AQ have a V_{IO} pin; all circuitry is connected to V_{CC} in the other variants.
- (2) All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
- (3) Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
- (4) V_{IO} = V_{CC} in non- V_{IO} product variants.
- (5) Guaranteed by design.

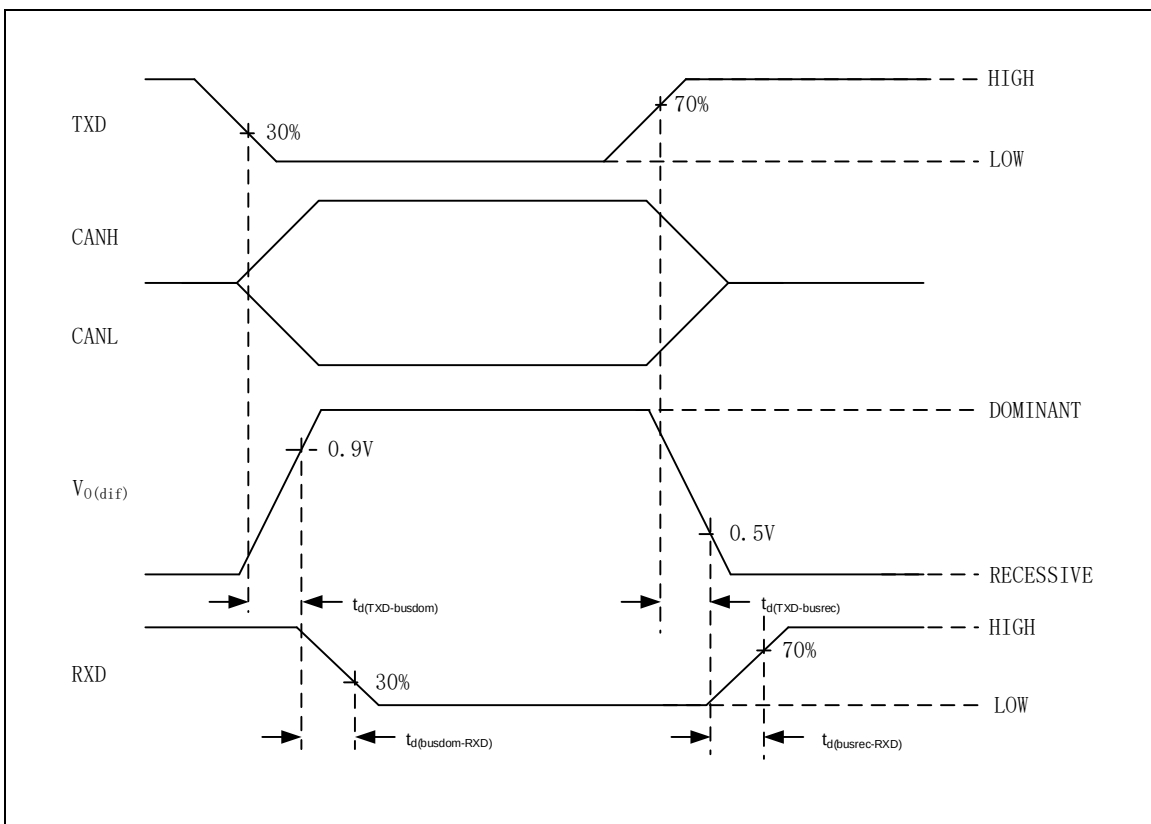


Figure 8-1.

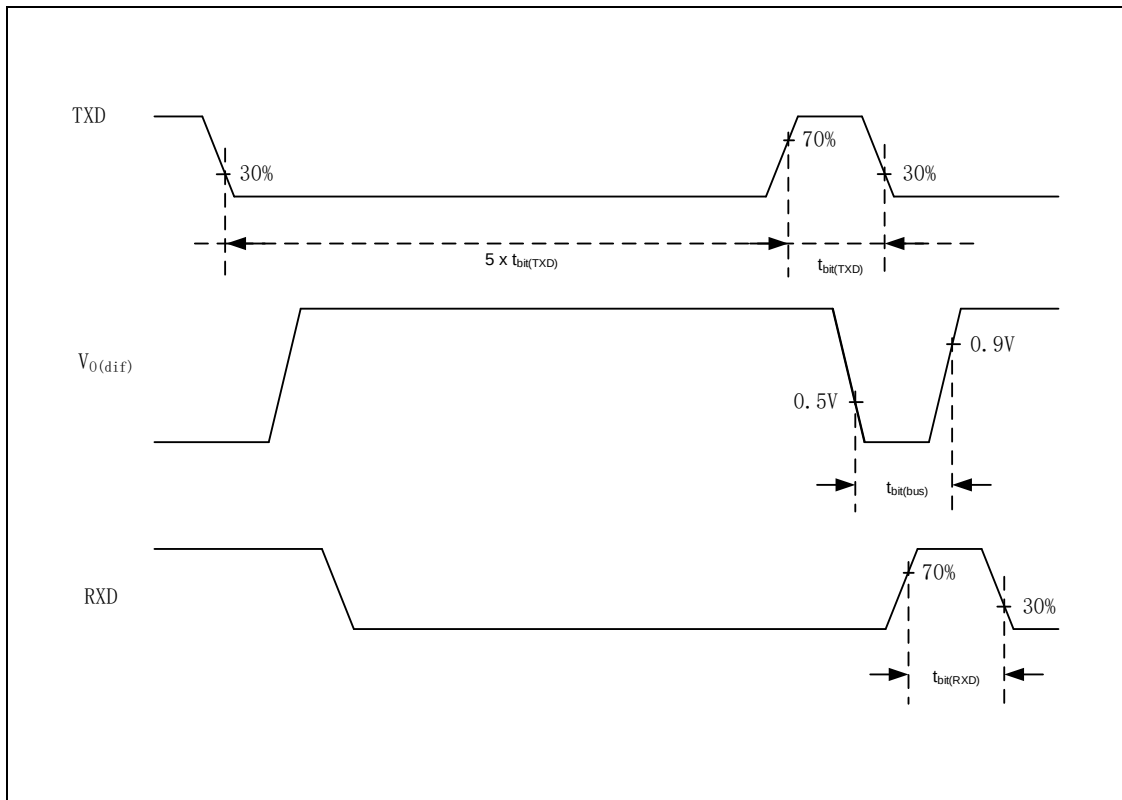
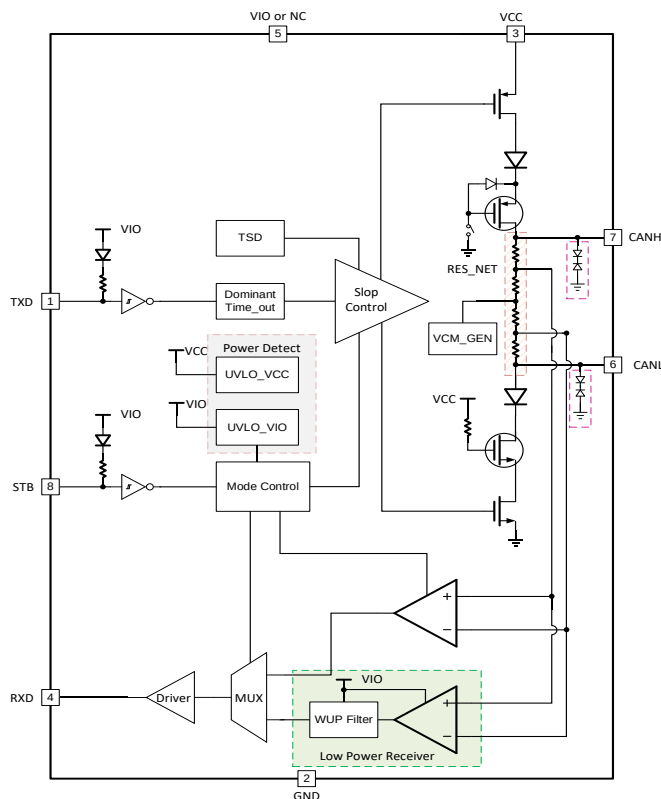


Figure 8-2.

9 Functional Block Diagram



10 Feature Description

10.1 Operating modes

The SC25042Q supports two operating modes, Normal and Standby. The operating mode is selected via pin STB.

Mode	Inputs		Outputs	
	Pin STB	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	Dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	x[1]	Biased to ground	Follows BUS when wake-up detected
				HIGH when no wake-up detected

[1] 'x' = don't care.

•10.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD.

The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

•10.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity.

In Standby mode, the bus lines are biased to ground to minimize system supply current.

The low-power receiver is supplied from V_{IO} (V_{CC} in non- V_{IO} variants) and can detect CAN bus activity even if V_{IO} is the only available supply voltage. Pin RXD follows the bus after a wake-up request has been detected. A transition to Normal mode is triggered when STB is forced LOW

10.2 Remote wake-up(via the CAN bus)

The SC25042Q wakes up from Standby mode when a dedicated wake-up pattern

(specified in ISO 11898-2:2016) is detected on the bus. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

After a wake-up sequence has been detected, the SC25042Q will remain in Standby mode with the bus signals reflected on RXD. Note that dominant or recessive phases lasting less than $t_{ftr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on RXD in Standby mode.(Figure 10-1.)

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The SC25042Q switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} undervoltage is detected ($V_{CC} < V_{UVD(swff)}(V_{CC})$ or $V_{IO} < V_{UVD(swff)}(V_{IO})$;

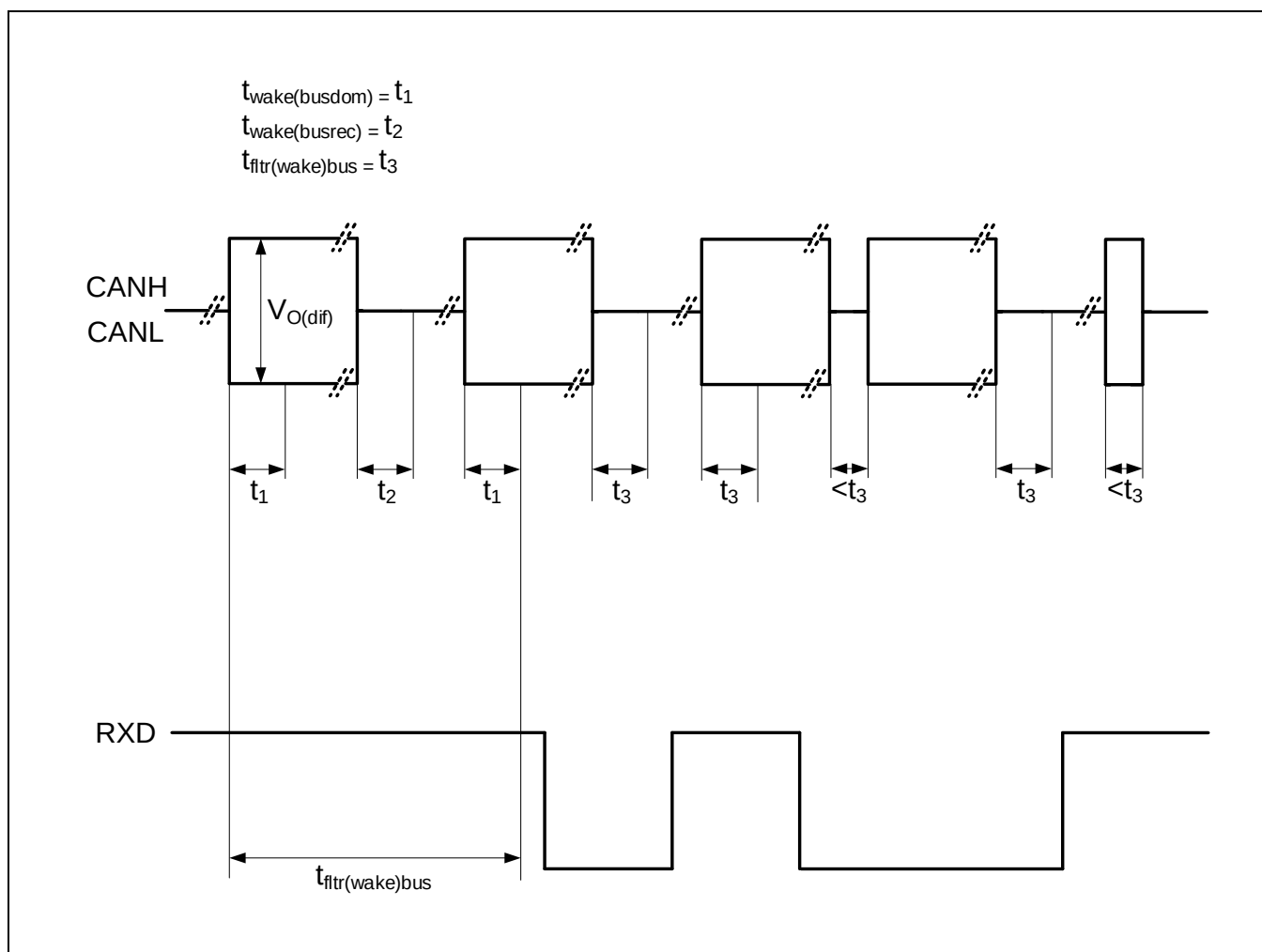


Figure 10-1 Wake-up timing

10.3 Fail-safe features

•10.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{\text{to}(\text{dom})\text{TXD}}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

•10.3.2 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to V_{CC} (V_{IO} for variants with a V_{IO} pin) to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize supply current

•10.3.3 Undervoltage detection on pins V_{CC} and V_{IO}

If V_{CC} drops below the standby undervoltage detection level, $V_{\text{uvd}(\text{stb})}(V_{CC})$, the transceiver switches to Standby mode. The logic state of pin STB is ignored until V_{CC} has recovered.

In versions with a V_{IO} pin, if V_{IO} drops below the switch-off undervoltage detection level $V_{\text{uvd}(\text{swoff})}(V_{IO})$, the transceiver switches off and disengages from the bus (zero load) until V_{IO} has recovered.



In versions without a V_{IO} pin, if V_{CC} drops below the switch-off undervoltage detection level $V_{UVD(swoff)}(V_{CC})$, the transceiver switches off and disengages from the bus (zero load) until V_{CC} has recovered.

•10.3.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers recover once TXD has been reset to HIGH. Including the TXD condition prevents output driver oscillation due to small variations in temperature.

10.4 V_{IO} supply pin

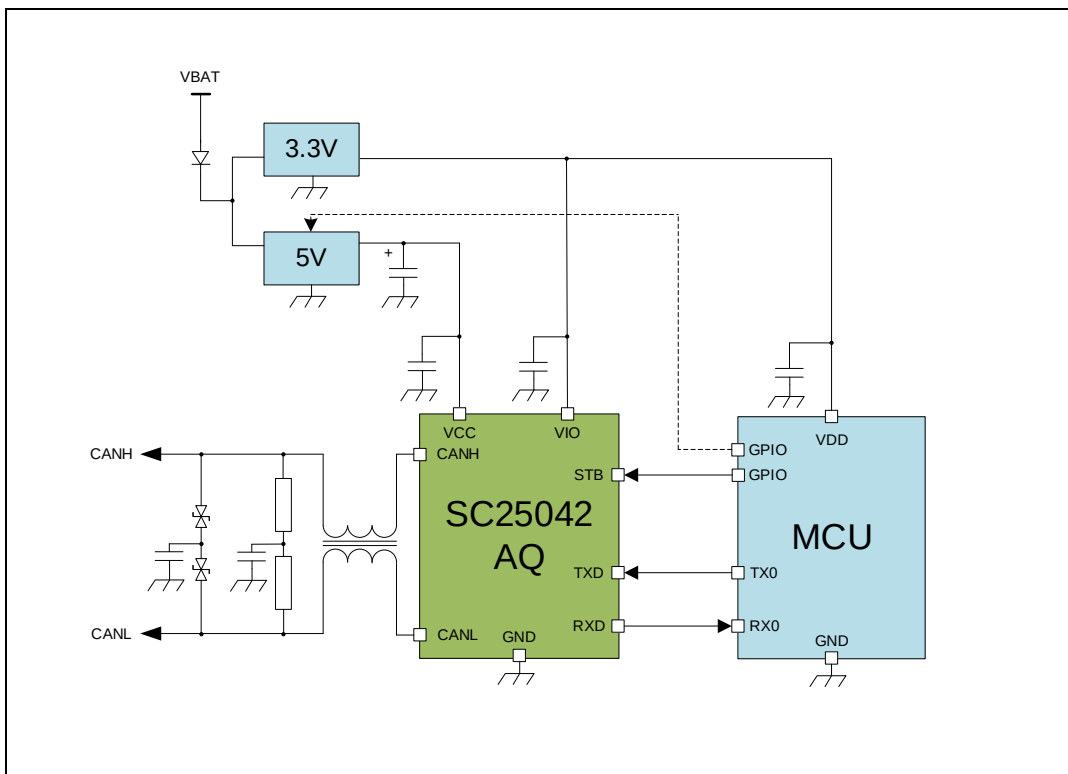
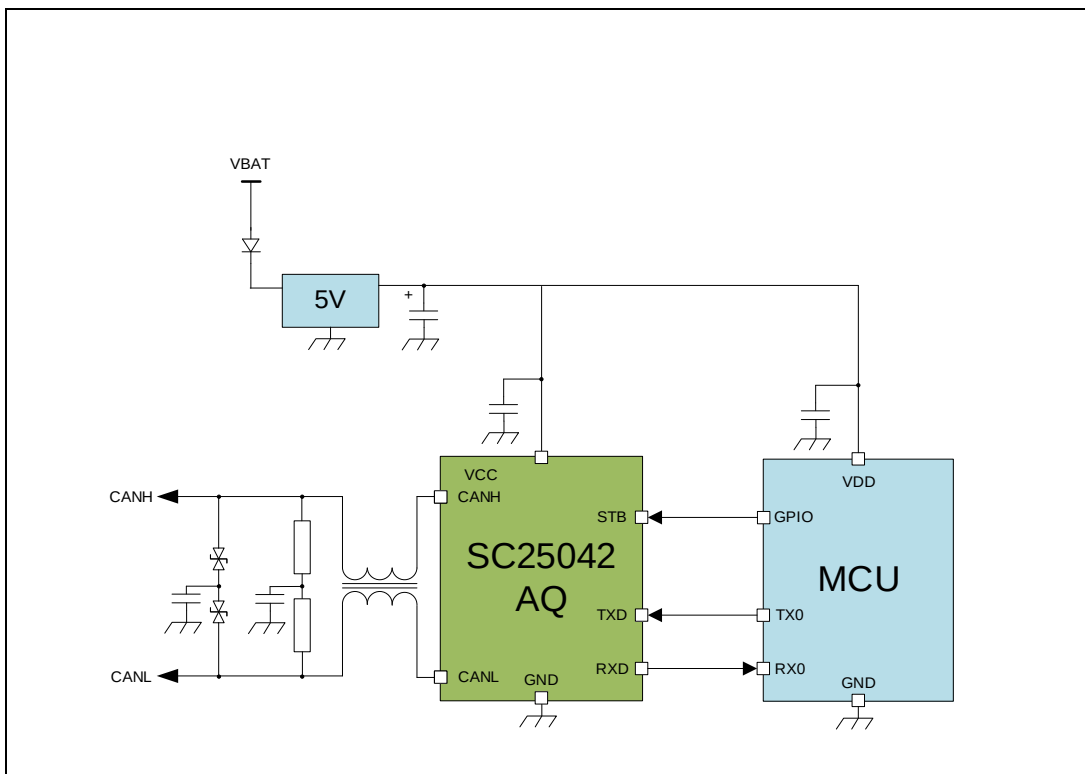
Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver in the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC} .

For variants of the SC25042BQ without a V_{IO} pin, all circuitry is connected to V_{CC} (pin 5 is not bonded). The signal levels of pins TXD, RXD and STB are then compatible with 5 V microcontrollers. This allows the device to interface with both 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.

10.5 Ringing suppression

Due to the situation of multi-node communication, it is easy to cause ringing, which makes data error. The ringing suppression function ensures that information is transmitted correctly.

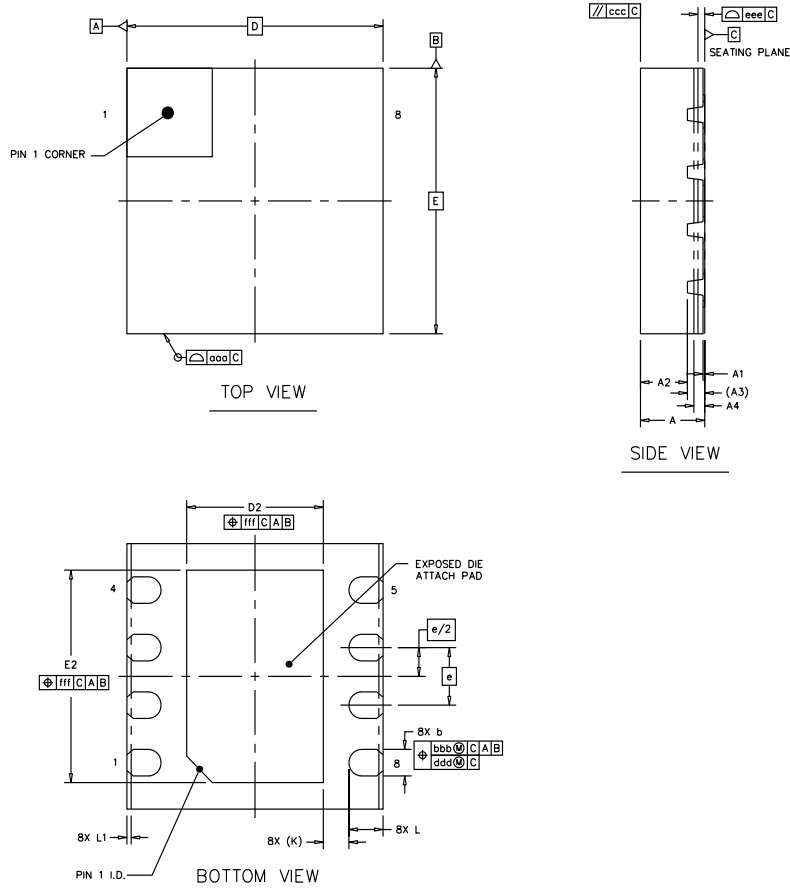
11 Application Information



12 Layout Guide

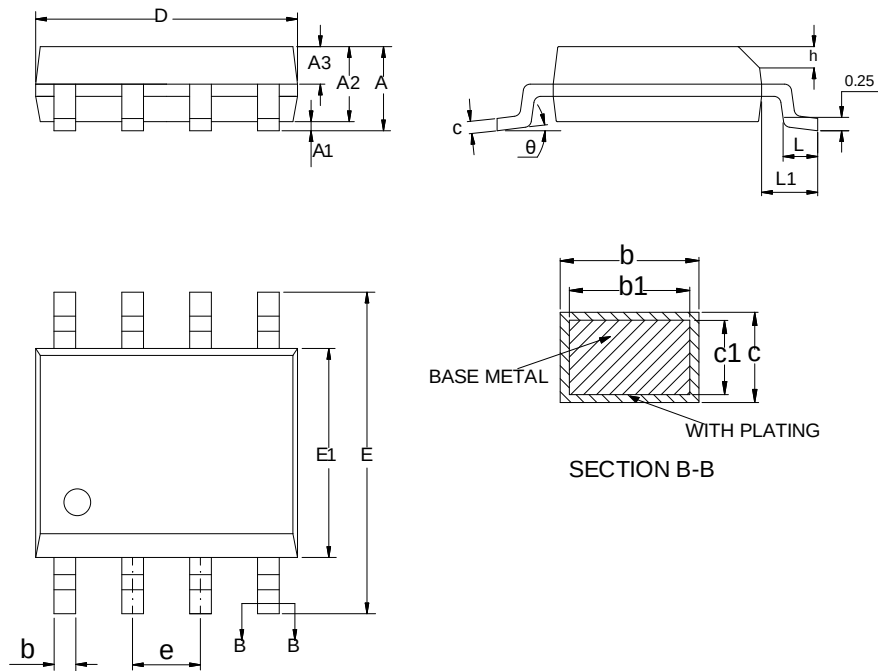
MECHANICAL DATA

DFN 3×3-8L



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D	3 BSC		
	Y	E	3 BSC		
LEAD PITCH		e	0.65 BSC		
EP SIZE	X	D2	1.5	1.6	1.7
	Y	E2	2.3	2.4	2.5
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K	0.3 REF		
PACKAGE EDGE TOLERANCE		ooo	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		
EXPOSED PAD OFFSET		fff	0.1		

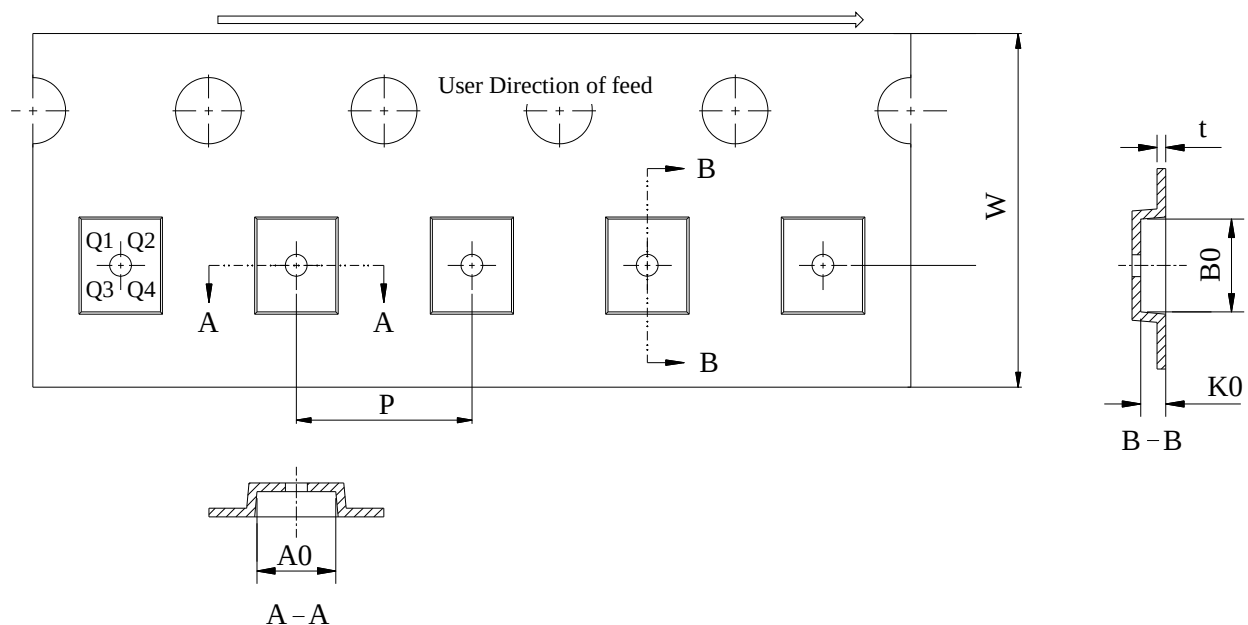
SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

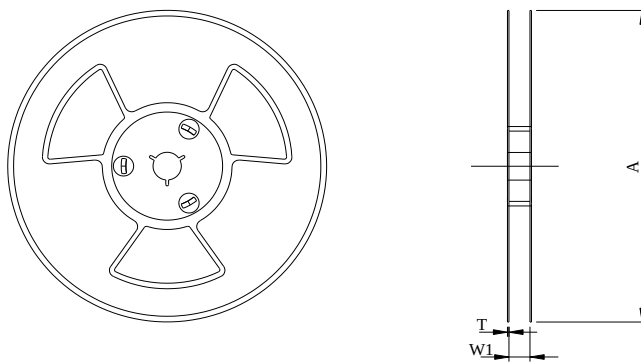
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 ± 0.10	8.00 ± 0.10	6.60 ± 0.10	5.30 ± 0.10	1.90 ± 0.10	0.30 ± 0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330 ± 1	$12.4 +1/-0$	2.1 ± 0.3

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