



High-Efficiency CrM Boost PFC Controller

1 Descriptions

The SC3252 is a Power Factor Correction (PFC) controller with 650V GaN integrated, which is applied to boost converter. It features High performance by using multi-mode control strategy. At heavy load or full load, it operates in Critical conduction Mode (CrM). When load decreases, it operates in Discontinuous Conduction Mode (DCM) with valley switching and lower frequency for high efficiency. And at no load, the IC will operate in Burst Mode to reduce power consumption and minimize audio noise. Using SC3252 together with the Flyback controller and secondary synchronous rectifier controller, high efficiency over full load can be achieved, and extremely low standby power consumption of system can easily meet the efficiency regulations.

Benefit from the SC3252, the PFC stage will obtain nearly unity power factor and sinusoidal line input current with few external components.

SC3252 offers comprehensive protections to prevent the circuit from damage under abnormal conditions.

ESOP-10W package is provided to simplified user's design and reduced system cost

2 Features

- Integrated 650V GaN
- Unity power factor and low THD
- Critical conduction Mode (CrM)
- Boost follow mode
- Valley switching operation with frequency fold-back
- No need for second winding on boost inductor
- High Efficiency and Ultra-low no-load input power
- Burst mode with noise immunity
- Comprehensive Protection
 - VDD under voltage protection
 - Cycle-by-cycle current limit
 - Output over-voltage protection
 - Inductor current CCM protection
 - Over-temperature protection
- VCC Range: from 9 V to 30 V
- ESOP-10W package

3 Applications

- USB-PD chargers
- AC-DC adapters for Portable Devices
- Desktop computing and TV/Monitor
- LED drivers
- Industrial and communication power supplies
- Power tools chargers
- E-bike chargers



4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3252SDER	ESOP-10W	10.3mm x 9.9mm x 1.6mm

SC3252 Functional Table

ORDER NUMBER	SC3252
Package	ESOP-10W
Boost Follow Mode	Y
ZCD OVP	N
Brown In/Out	Y
PFC EN Function	N

Y: The feature is enabled;

N: The feature is disabled;



5 Typical Application Circuit

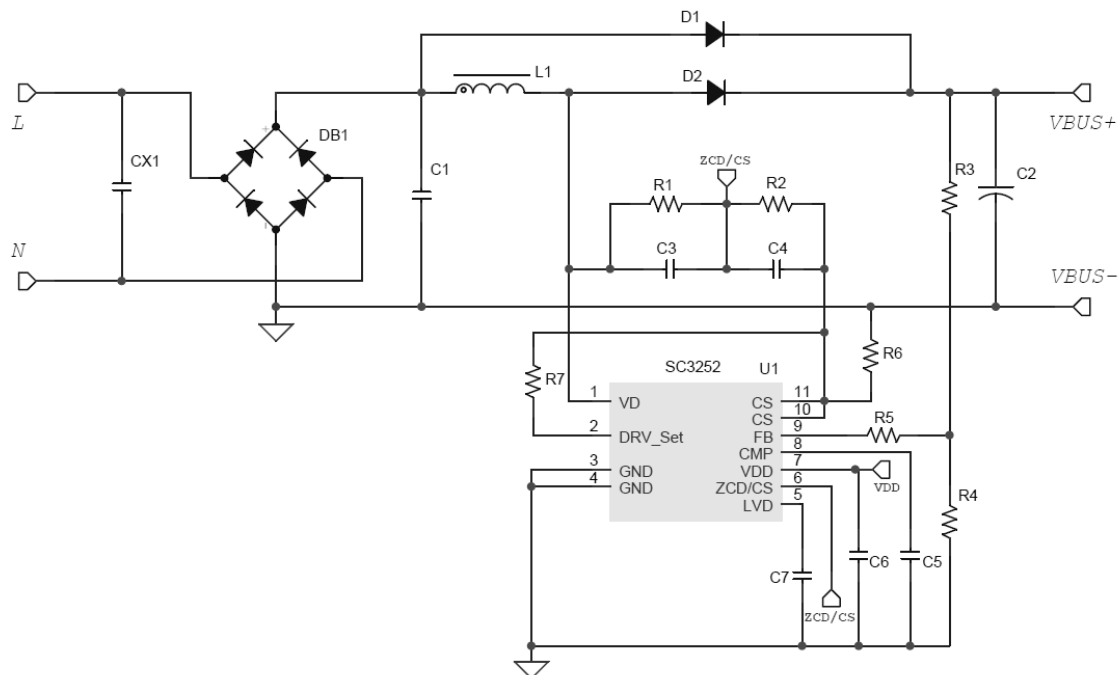
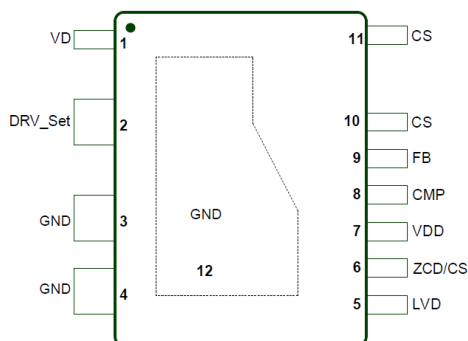


Fig. 1 Typical application circuit



6 Terminal Configuration and Functions



TOP VIEW (ESOP-10W)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VD	PWR	Internal GaN FET drain terminal.
2	DRV_Set	I/O	This pin connects to a resistor to adjust sink/source current.
3、4、12	GND	PWR	Power Ground. All GND Pin must be electrically connected to Power Ground.
5	LVD	PWR	Internal GaN FET voltage stress protection. It is recommended to retain a ceramic capacitor (NC) position, which connects directly through pins 4-5.
6	ZCD/CS	I	Current Sense. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation. Voltage Sense. The ZCD voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage.
7	VDD	PWR	Power Supply.
8	CMP	I/O	Compensated net.
9	FB	I	Voltage feedback.
10、11	CS	O	Internal GaN FET source terminal. These pins connect to a current-sense resistor to sense the GaN current.



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

ITEM	DESCRIPTION	MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	VD, max to GND ($V_{LVD}>20V$ and 2Pin connect to the GND)		650	V
	VD, max to GND ($V_{LVD}<20V$ or 2Pin not connect to the GND)		30	V
	LVD, max to GND		30	V
	VDD to GND	-0.3	+33	V
	DRV to GND	-0.3	+18	V
	DRV_Set to LVD	-30	0	V
	Other Pins to GND	-0.3	+6.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾ (All pins except VD、DRV_Set、LVD、CS)	-2	+2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-1	+1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe

7.3 Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD to GND	VDD voltage range to GND	9		30	V
VD to GND	VD voltage range to GND	0		650	V
LVD to GND	LVD voltage range to GND	0		30	V
DRV_Set to LVD	DRV_Set voltage range to LVD	-30		0	V
Others to GND	Other pins voltage range to GND	0		5.0	V
C_{VDD}	VDD Capacitor	4.7		22	μF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C



7.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		ESOP-10W	UNIT
θ_{JA}	Junction to ambient thermal resistance	32.5	θ_{JA}
θ_{JC}	Junction to case resistance	16	θ_{JC}

7.5 Electrical Characteristics

VDD=15V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Supply (VDD)					
V _{DDON}	VDD on threshold voltage		10.70		V
V _{DDOFF}	VDD off threshold voltage		8.85		V
I _{VDDST}	VDD start up current	V _{VDD} < V _{DDON} - 0.1V	25		μA
I _{VDDFAULT}	Hold up current in fault mode		130		μA
I _{VDDBT}	Burst mode current	V _{COMP} < 0.3V	130		μA
I _{VDDQ}	Operating current	V _{VDD} = 12V, No PWM, DRV pin floating	0.5		mA
I _{VDD50k}	Operating current	V _{VDD} = 12V, 50kHz, DRV pin floating	0.68		mA
Gate Driver (DRV) for MOSFET					
V _{OL}	Driver output low voltage	VDD=15V, I _{DRV} =20mA		0.5	V
V _{OH}	Driver output high voltage	VDD=15V	12.5		V
T _R	DRV rising time	CL = 1nF, 1.5V to 9V	130		ns
T _F	DRV falling time	CL = 1nF, 9V to 1.5V	22		ns
Feedback Voltage (VFB)					
V _{FBREF}	Feedback voltage reference		2.5		V
V _{FBOVP1}	FB fast stop OVP		2.7		V
K _{FBOVP2} ⁽¹⁾	FB fast stop OVP2 Voltage Ratio in Boost follow Mode	V _{FBOVP2} / V _{FBREF}	120		%
R _{FBOVP}	The discharge resistor in CMP	FB OVP trigger	4.7		kΩ
V _{FBUVP}	VFB under voltage protection		0.4		V
V _{FBUVP_HYS} ⁽¹⁾	VFB under voltage protection hysteresis		0.1		V
I _{FBDN}	VFB pin sink current		45		nA
I _{FBLowLINE}	VFB pin source current	Boost follow Mode	7.5		μA
Compensation (CMP)					
G _{GM1}	Compensates for amplification gain		60		μS
I _{CMPsORMAX}	CMP maximum source current		46		μA
I _{CMPsINKMAX}	CMP maximum sink current		125		μA
V _{CMPBSTIN}	Burst Mode voltage threshold		0.3		V
V _{CMPBSTHYS}	Burst Mode voltage hysteresis		80		mV
V _{CMPCLAMP}	Clamp voltage of CMP		3.3		V



Zero Voltage Detection and Current Sense (ZCD/CS)				
T _{ZCDBLK}	Zero current detection blanking time		500	ns
V _{ZCDH}	Zero current detect voltage threshold		7.0	mV
V _{ZCDHYS}	ZCD voltage hysteresis		7.0	mV
I _{ZCDOPENDET}	ZCD pin sink current		37	nA
V _{CSOCP1}	Cycle by cycle current limited		0.405	V
T _{LEBOCP1}	OCP1 leading edge blanking time		450	ns
V _{CSOCP2}	Current limited level 2		0.61	V
T _{LEBOCP2}	OCP2 leading edge blanking time		260	ns
T _{OCPDT1}	OCP2 delay time		500	μs
T _{OCPDT2}	OCP2 trigger 2 times delay time		1	ms
V _{ZCDBIN}	ZCD brown in DC voltage		0.280	V
V _{ZCDBIN_HYS}	ZCD brown in DC voltage hysteresis		38	mV
T _{BOUT}	Delay time of brown out protection		50	ms
T _{MAXOFF}	Maximum off time		260	μs
V _{ZCDHLINE}	ZCD voltage threshold of high line		0.650	V
V _{ZCDLLINE}	ZCD voltage threshold of low line		0.620	V
T _{MAXONL}	Maximum on-time at low line		12.80	μs
T _{MAXONH}	Maximum on-time at high line		4.4	μs
GaN Section				
R _{DS_ON}	Drain-source On-state Resistance	V _{GS} = 8V, I _D = 4A, T _J = 25 °C	180	mΩ
		V _{GS} = 8V, I _D = 4A, T _J = 150 °C	360	mΩ
C _{OSS}	Output capacitance	V _{GS} = 0V, V _{DS} = 400V; f = 1MHz	45	pF
C _{ISS}	Input capacitance		165	pF
C _{RSS}	Reverse capacitance		27	pF
Internal Over-Temperature Protection (OTP)				
OTP _H ⁽¹⁾	OTP Temperature		145	°C
OTP _{HYS} ⁽¹⁾	OTP Hysteresis		24	°C

(1) Guaranteed by design.



7.6 Typical Characteristics

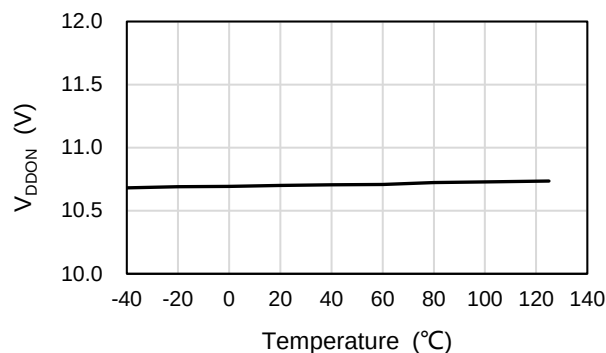


Figure 2. V_{DDON} vs Temperature

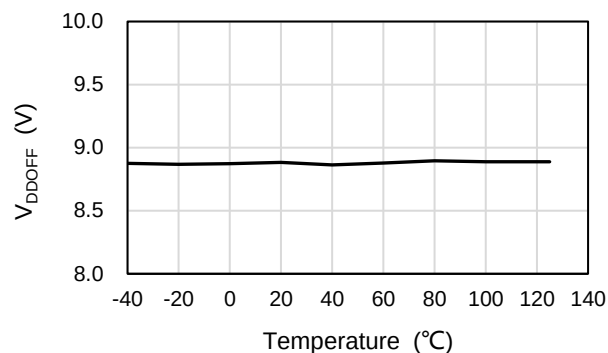


Figure 3. V_{DDOFF} vs Temperature

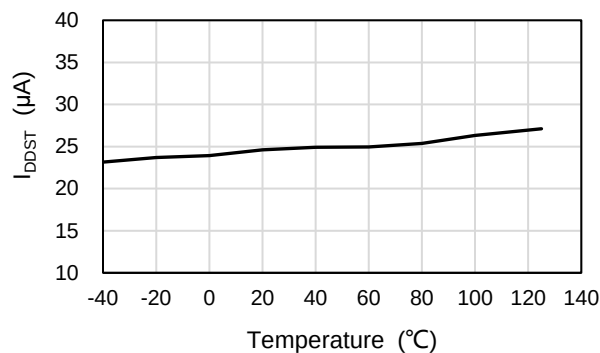


Figure 4. I_{DDST} vs Temperature

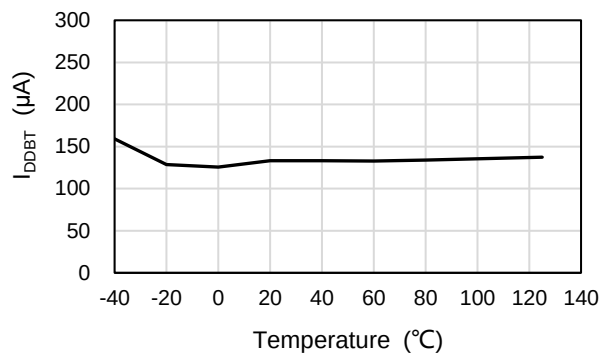


Figure 5. I_{DDBT} vs Temperature

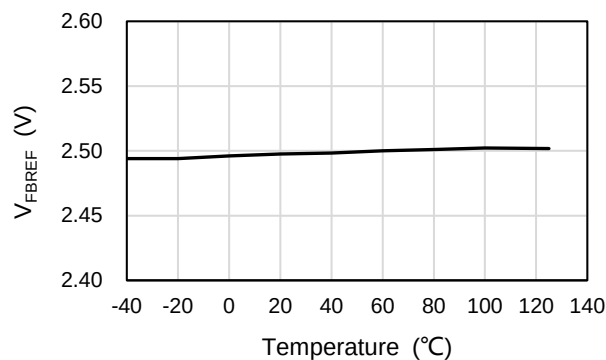


Figure 6. V_{FBREF} vs Temperature

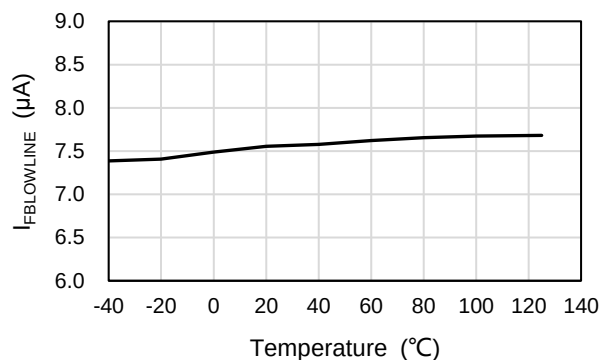


Figure 7. $I_{FBLOWLINE}$ vs Temperature

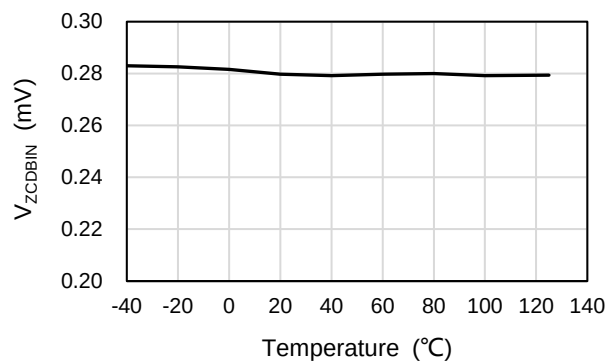


Figure 8. V_{ZCDBIN} vs Temperature

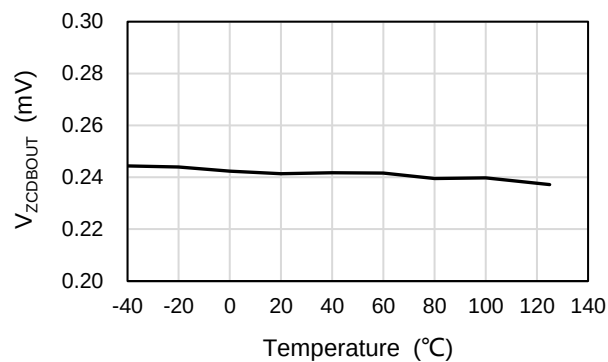


Figure 9. $V_{ZCDBOUT}$ vs Temperature

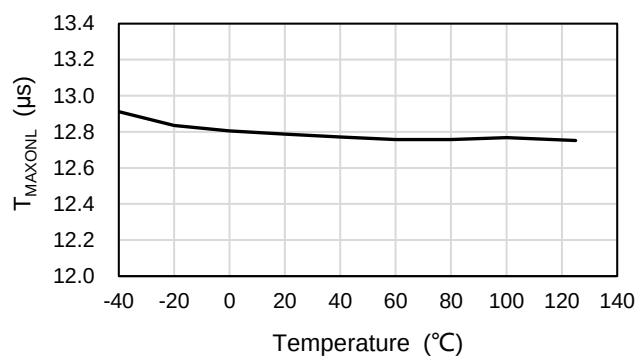


Figure 10. T_{MAXONL} vs Temperature

8 Functional Block Diagram

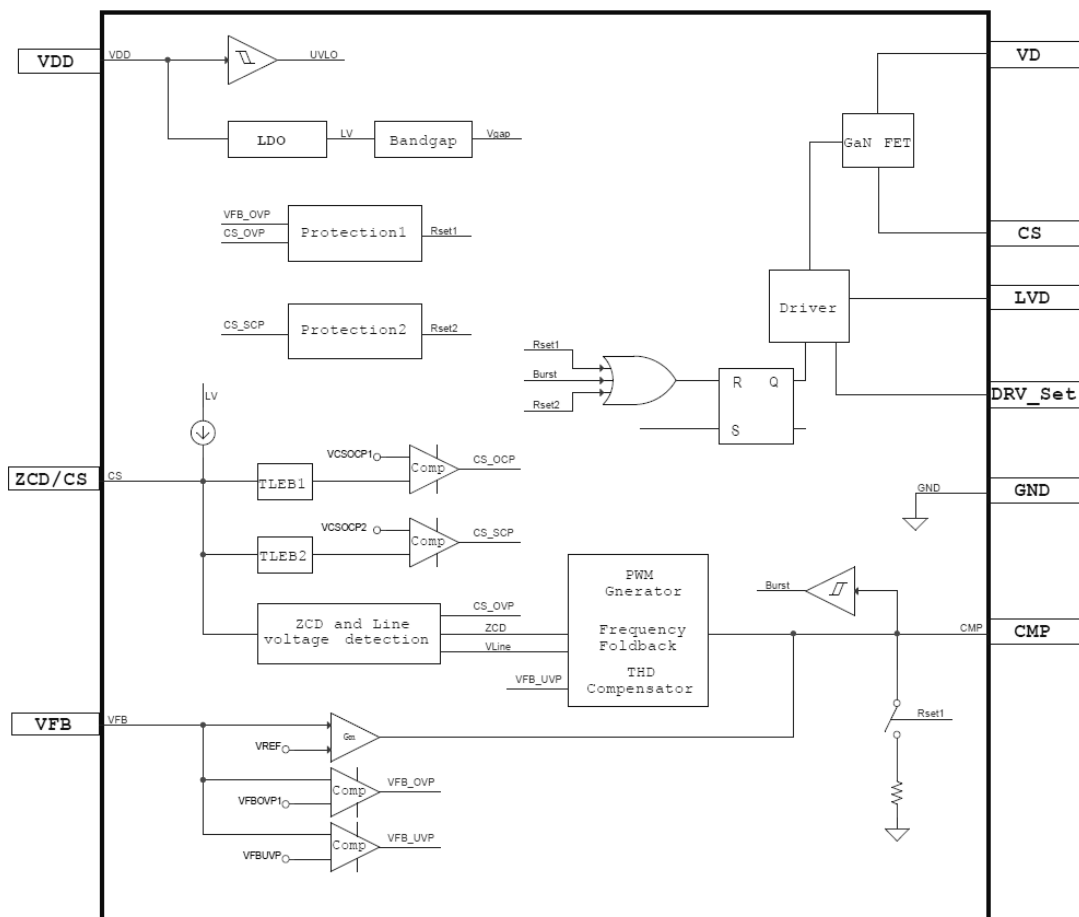


Fig.11 Function Block Diagram

9 Feature Description

The SC3252 controller is designed to optimize the efficiency of Boost PFC stage throughout the load range. For 75w to 120w power system, it followed with the flyback controller SC302x/SC305x and synchronous rectification controller SC350x to provide an isolated AC-DC power system.

The combined power supply is designed to meet tough efficiency and standby power requirements without the need for an auxiliary converter and with no need to switch off the PFC under light load conditions. It allows designers to meet modern green power standards with a simpler and lower system cost of power supply.

The SC3252 controller contains numbers of features designed to maximize operating efficiency across the entire range of Line and Load. Multi-mode control strategy allows SC3252 to operate in Critical conduction Mode (CrM) at heavy power load and then transition into Discontinuous Conduction Mode (DCM) as load decreases without compromising line current harmonics or power factor. Light-load efficiency and standby power are further enhanced by transitioning automatically to a burst mode of operation. During the burst OFF periods, the controller powers down most of its internal circuits to minimize controller power consumption.

The SC3252 controller offers comprehensive protections to prevent the circuit from damage under abnormal conditions, such as cycle-by-cycle current limit, over-current protection, dual independent output over-voltage protection, Line Brown-In, overtemperature protection and supply undervoltage lockout (UVLO).

Due to the high performance of SC3252, the PFC stage will obtain nearly unity power factor and sinusoidal line input current, which can meet mains harmonics requirements such as EN61000-3-2.

The Boost PFC stage can provide relatively stable output voltage during a wide AC input range, which simplifies the design difficulty of LLC or flyback.

9.1 CrM/DCM Operation

The SC3252 controller operates in CrM or DCM with valley turn-on, as shown in figure 4 and figure 5. In this working mode, the switching loss of the system is greatly reduced,

so as to obtain higher efficiency.

The SC3252 samples the information of input voltage and load to match different on-time and frequency, and then determines whether the system works in CrM or DCM.

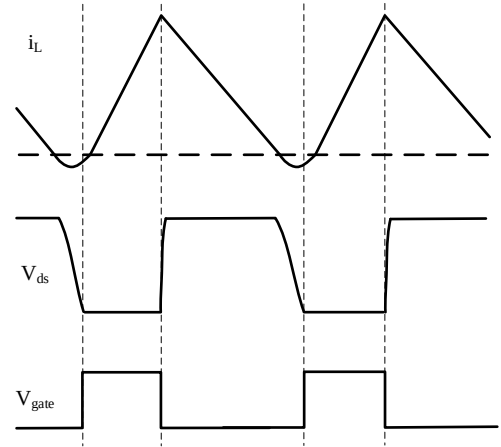


Fig. 12 Valley Switching Operation in CrM

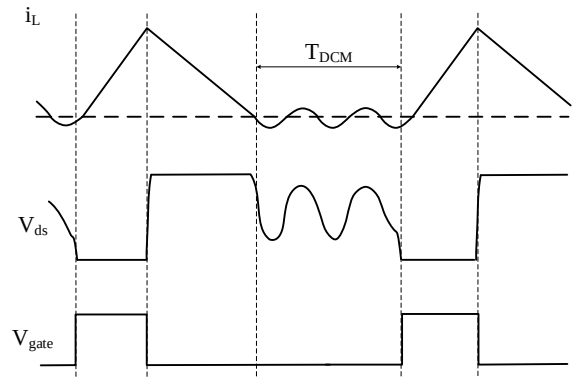


Fig. 13 Valley Switching Operation in DCM

Line current distortion is particularly severe during the transition from the first valley (CrM) to the second valley (DCM) operation while the input voltage is low. In this region, the first valley duration is extended by the clamping action of the power switch body diode. In this region Line current is reduced when switching on the first valley (CrM), because the inductor current is negative at the start of the on period. The reduction in Line current is not observed for second or subsequent valley (DCM) operation because the inductor current starts the on period from zero. The SC3252 optimizes THD by avoiding CrM/DCM transitions across a Line cycle.

9.2 THD Compensation

When the conduction time is relatively constant, the peak value of the inductance current is linear with the input voltage, and the average value of the input current is approximately linear with the peak value. Therefore, the input current can follow the input voltage to realize the unit power factor. Ideally, the input voltage and input current waveform in half line cycle is shown in Figure 6.

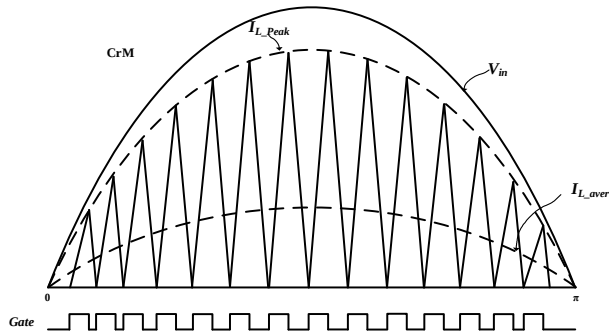


Fig. 14 Ideal Input voltage and input current waveform

Actually, there is a negative inductance current before the GATE on, as shown in fig.4. Therefore, the actual average input current is distorted, as shown in fig.7.

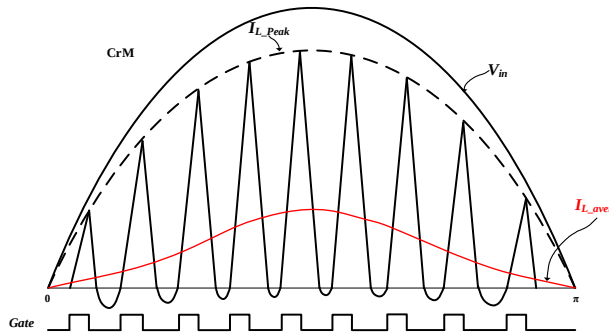


Fig. 15 Actual Input voltage and input current waveform

To achieve better THD, the THD Compensation technology is applied in SC3252. The conduction time (T_{on}) is adaptive during in a half AC cycle. T_{on} at peak of input voltage will be shorter than that at zero-crossing of input voltage.

9.3 Boost Follow Mode

The SC3252 controller detects the AC line voltage by ZCD/CS pin. At low line, IC enters Boost Follow Mode, and FB pin sources 7.5 μ A current, to change output voltage of

PFC stage. When the AC voltage increases to high line, IC exits Boost Follow Mode, and output voltage of PFC stage will change to higher voltage.

9.4 Brown In/Out

The Brown IN/OUT function is implemented through CS/ZCD pin. The average of the MOS drain voltage in each switching cycle represents the instantaneous line voltage. Therefore, the peak line voltage can be detected by the external divider network attached to the ZCD/CS pin. When the average of CS/ZCD pin voltage rises above V_{ZCDBIN} , the IC starts working, and it stops working when the average of CS/ZCD pin voltage decreases below $V_{ZCDBOUT}$.

9.5 VDD UVLO

Supply undervoltage lockout (UVLO) protection ensures that the controller operates only while the supply voltage is in a range that ensures correct operation and adequate Gate drive amplitude for the power switch.

When the VDD voltage is Lower than the V_{DDOFF} threshold voltage for a longer period than a blanking time, the controller will stop switching. The controller then returns to a dormant condition. During this dormant period, the controller consumes a relatively small amount of supply current until it exceeds the V_{DDON} threshold again.

9.6 Over-Current or CCM Protection

Two levels of overcurrent protection are integrated. V_{CSOCP1} is cycle-by-cycle current limiting for overload protection. V_{CSOCP2} is the protection for the case of CCM. When the current in the inductor does not drop to zero at the end of a switching cycle, the peak of the inductor current will be very high in the next cycles, even beyond the cycle-by-cycle current limit. Then the CCM protection will be triggered, and there will be a longer off time to demagnetize the inductive current to zero.

9.7 Output Over-Voltage Protection

The SC3252 controller provides two independent output overvoltage protection strategies to ensure that a single fault does not cause the output voltage to be too high.

FB overvoltage protection: FB pin monitors the output voltage through an external divider network. If the voltage



on this pin is higher than V_{FBOVP1} , it indicates that the output voltage is too high, and the controller immediately turns off the DRV to prevent further increase of the output voltage.

ZCD overvoltage protection: During the conduction of the boost diode, the voltage on the MOSFET is close to the output voltage. The controller monitors the voltage on the MOSFET through an external voltage divider network connected to the ZCD/CS pin. This monitoring provides a second independent method to detect excessive output voltage when the voltage dividers of FB pin is damaged. A fixed blanking period is applied after the falling edge of the DRV waveform to ensure that the comparator is not triggered by the induced spike at the leading edge of the drain waveform.

When the voltage of ZCD pin is higher than the threshold voltage of internal comparator for three consecutive cycles, ZCD overvoltage protection is triggered, and DVR is closed immediately for 1ms.

9.8 On-Chip OTP

An internal OTP circuit is embedded inside to provide the worst-case protection for SC3252. When the chip temperature rises higher than the OTP_H , the controller will be disabled and works in the failure mode until the chip is cooled down below the hysteresis OTP_{HYS} .

9.9 Pin Open/Short Protection

In case CS/ZCD pin is floating or short to GND, ZCD Brown-Out Protection will be triggered and DRV will turn off to protect the power circuit.

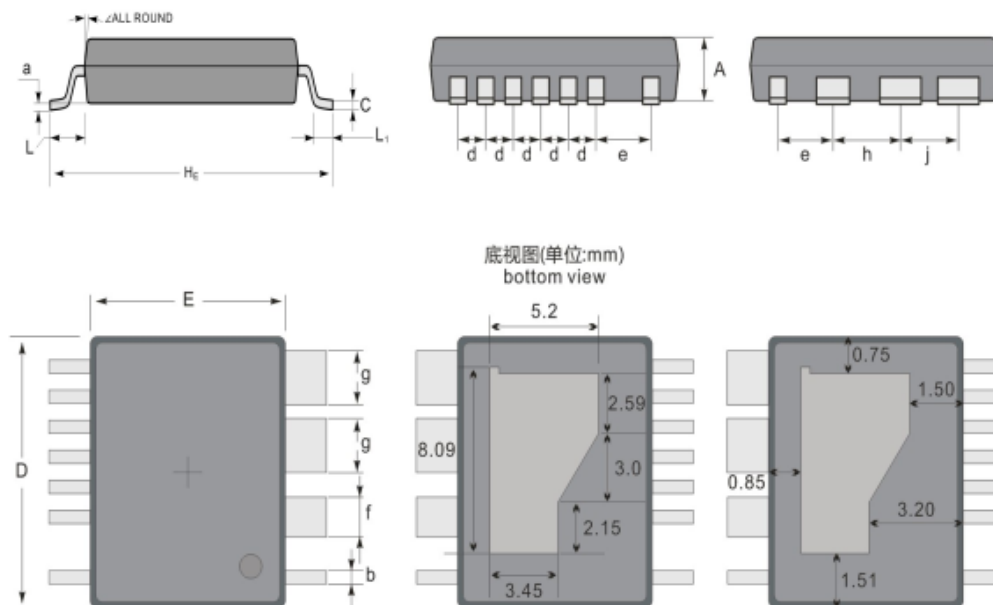
In case FB pin is floating or short to GND, FB Under Voltage Lock-Out Protection will be triggered, and IC will be shut down.

Further application information and PCB layout guidance is provided in document **SC325x Application Note**.



MECHANICAL DATA

ESOP-10W (2.92mmx2.80mmx1.25mm)



Unit		A	C	D	E	HE	L	L1	a	b	d	e	f	g	h	j	∠
mm	max	1.7	0.30	10.1	7.7	10.4	1.5	0.8	0.2 (ref)	0.45	1.32	2.59	1.25	1.96	3.34	2.35	7°
	typ	1.6	0.25	9.9	7.5	10.3	1.4	/		0.40	1.27	2.54	1.20	1.91	3.29	2.30	
	min	1.5	0.20	9.7	7.3	10.2	1.3	0.4		0.35	1.22	2.49	1.15	1.86	3.24	2.25	
mil	max	67	12	398	303	409	59	31	8 (ref)	18	52	102	49	77	131	93	
	typ	63	10	390	295	406	55	/		16	50	100	47	75	130	91	
	min	59	8	382	287	402	51	16		14	48	98	45	73	128	89	