Dual-Ouputs 6-A Buck Converter with Integrated DCP Scheme

1 Description

The SC8112A is a synchronous dual-output ports buck converter with a wide input voltage from 4.6V to 36V. The SC8112A regulates the output voltage at a fixed 5V or customized voltage by setting the divider resistor. It also provides high accurate output current limit. The converter enters Constant Current (CC) Mode in case any of the two output channels reaches the setting current limit. The total output power can be programmed by a resistor, which makes it easy for constant power (CP) control.

The SC8112A adopts programmable line drop compensation, programmable frequency setting with minimum external components. It also integrates automatic DCP mode and Type-C current mode, so that a USB controller can be saved. With minimum external components, maximum functions can be achieved for user's different applications.

The SC8112A also supports full protections including under voltage protection, over voltage protection, short circuit protection and auto-restart, over temperature protection.

The SC8112A adopts 32 pin QFN 5x5 package

2 Features

- Wide input operating voltage from 4.6V to 36V
- 11mΩ/27mΩ Low Rdson Internal Power MOSFETs
- Max output capacity with 5V/6A
- Almost 100% duty cycle operation
- Low quiescent current
- High side output current sense
- Programmable output power limit
- Programmable line drop compensation
- Supports 1.4ms output over-current debounce to meet Apple over-current requirement
- Build-in DP/DM for BC 1.2 DCP scheme
  - BC1.2 DCP Mode
  - Divider Mode
  - 1.2V/1.2V Mode
- Build-in USB Type-C 3A Current Mode Controller
- PFM Operation
- Adjustable frequency 80kHz to 600kHz
- Hiccup and auto-restart
- Full protection of UVLO, OVP, OCP, OTP

3 Applications

- Car Charger
- Multi-Ports Wall Charger
- Hub
- Industrial applications

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8112AQDJR	32 pin QFN	5 mm x 5 mm x 0.75 mm

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

5 Typical Application Circuit

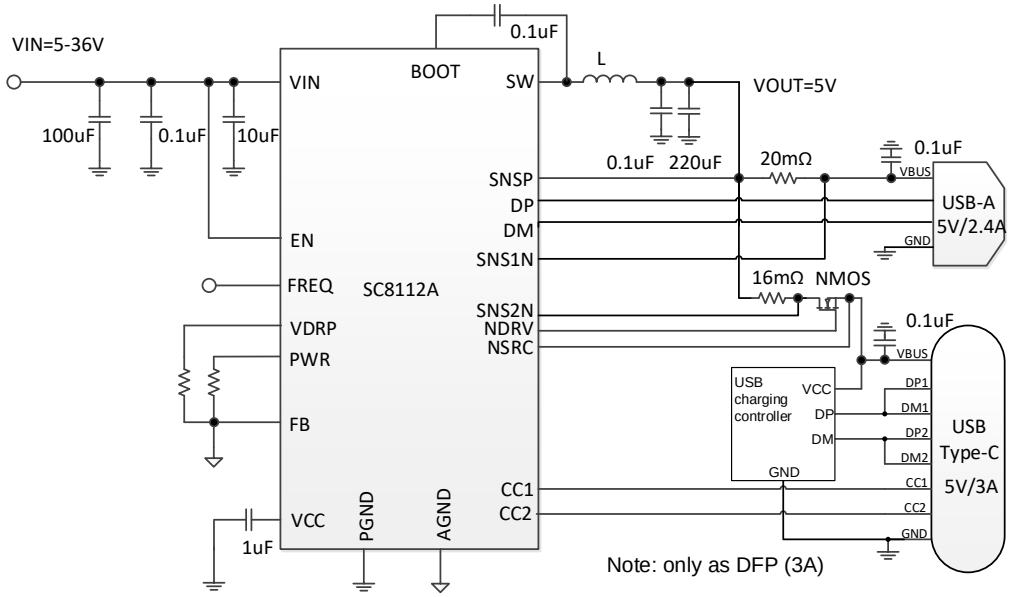


Figure. 1 Typical Application Circuit for Generic Charging Port.

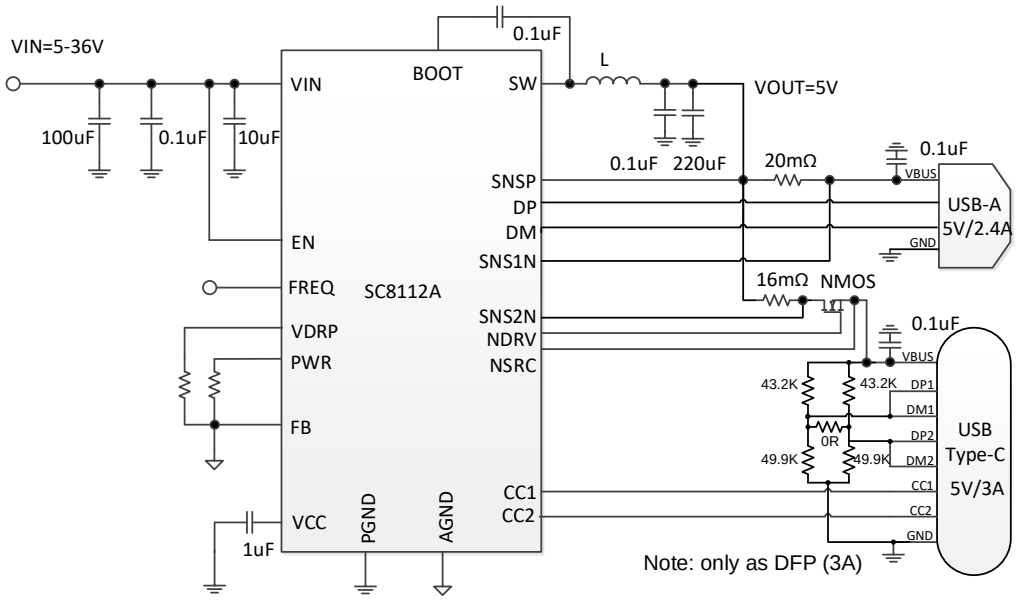


Figure. 2 Typical Application Circuit for Dedicated Charging Port

Note:

For some devices which use DP/DM as charging control interface, an additional USB charging controller IC is recommended for generic purpose charging port. As shown in figure 1, this application has the best compatibility.

For dedicated adapter or charger, we recommend using resistors divider or just short DP/DM to configure the type-c USB port as shown in figure 2. For example, shorting DP/DM for android devices and using resistors for Apple device. Keeping DP/DM floating is also allowed to the most devices which support USB Type-C Downstream Facing Port (DFP).

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

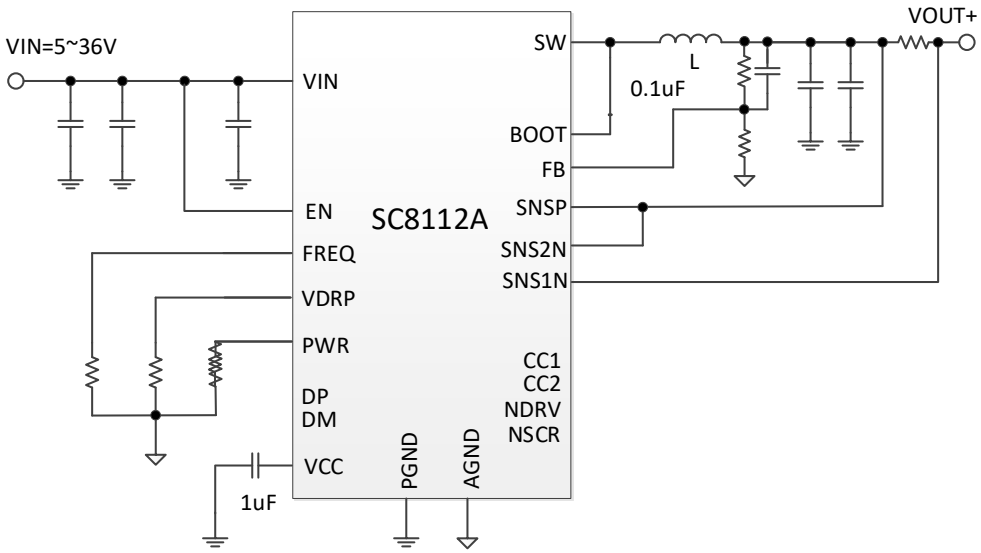
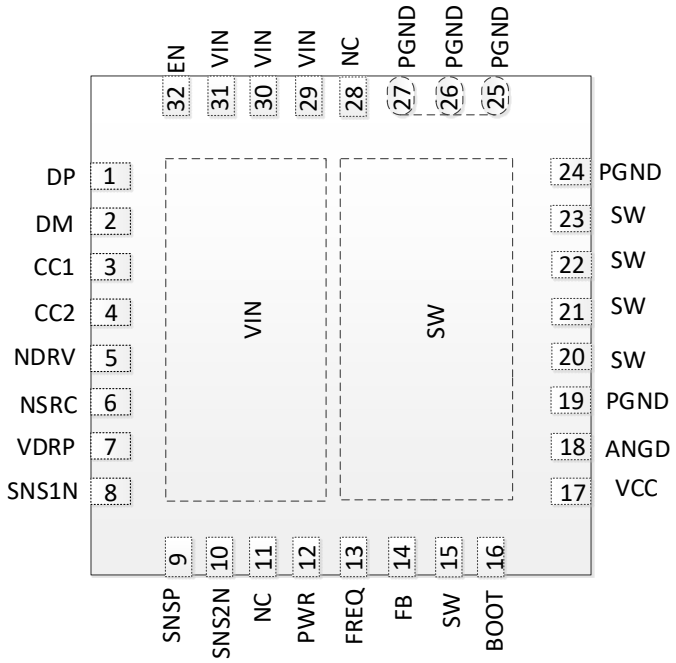


Figure.3 Typical Application Circuit with general purpose BUCK converter

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

6 Terminal Configuration and Functions



QFN 32 Package Reference

(Top View)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	DP	I/O	D+ data line to USB connector, used for hand-shaking with portable devices.
2	DM	I/O	D- data line to USB connector, used for hand-shaking with portable devices.
3	CC1	I/O	Configuration Channel 1 to USB Type-C connector.
4	CC2	I/O	Configuration Channel 2 to USB Type-C connector.
5	NDRV	O	Gate signal for isolated Type-C NMOS
6	NSRC	O	Source signal for isolated Type-C NMOS
7	VDRP	O	Line drop compensation configuration pin. Setting the line compensation slope by connecting a resistor to AGND
8	SNS1N	I	Negative end of output 1 current sense amplifier.
9	SNSP	I	Positive end of output current sense amplifier/ Output voltage sense.
10	SNS2N	I	Negative end of output 2 current sense amplifier.

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

11	NC		Keeping floating（This pin is connected to VIN from internal metal frame）
12	PWR	I	Output power limit pin. Setting the output power limit by connecting a resistor to AGND
13	FREQ	I	The operation frequency is programmed by a resistor between this pin and AGND.
14	FB	I	Output voltage feedback. Connect the center of two divider resistor to program the output voltage. Output voltage be configured for fixed 5.1V with FB pin connected to AGND.
15, 20~23	SW	PWR	Switching node.
16	BOOT	PWR	Connect a capacitor between BT and SW to bootstrap a voltage to provide the bias for high side MOSFET driver.
17	VCC	PWR	Output of internal regulator to provide 5.2V voltage for the bias voltage of internal gate drivers. Connect a 1 μF ceramic capacitor from VCC to PGND pin.
18	AGND	I/O	Analog Ground.
19, 24~27	PGND	PWR	Power ground.
28	NC		Keeping floating（This pin is connected to SW from internal metal frame）
29~31	VIN	I	Input node of Buck. Connect a 10 μF ceramic capacitor from VIN to PGND pin.
32	EN	I	Enable logic input. Logic high level enables the device and logic low level disables the device.

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage range at terminals (2)	VIN, EN , SNS1N, SNS2N, SNSP	-0.3	42	V
	SW	-1	42	V
	FB, DP1, DM1, DP2, DM2, VCC, MODE, FREQ, PWR, VDRP,	-0.3	6.5	V
	BOOT	-0.3	50	V
Temperature Range	Operating Junction, T_J	-40	150	°C
	Storage temperature range, T_{stg}	-65	150	°C
	Continuous power dissipation (TA=25°C), P_D (3)		3.2	W
	Junction to ambient thermal resistance, $T_{\Theta JA}$ (3)	39		°C/W
	Junction to case (top) thermal resistance, $T_{\Theta JC}$ 3)	18		°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) Measured on JESD51-7, 4-layer PCB.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage(2) for DP/DM pin	-8	8	kV
	Human body model (HBM) ESD stress voltage for other pins	-1	1	kV
	Charged device model (CDM) ESD stress voltage (3)	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	5		32	V
V_{OUT}	Output voltage range		5.1		V
C_{IN}	Input Capacitance	30	100		µF
C_{OUT}	Output capacitance	80	220	680	µF
f_{SW}	Operating frequency range	80	120	600	kHz
T_J	Operating junction temperature	-40		125	°C

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

7.4 Electrical Characteristic

T_J= 25°C and V_{IN} = 12V, V_{OUT} = 5.1V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Operating voltage		4.6		36	V
V_{IN_UVLO}	Under voltage lockout threshold	Rising edge		4.35	4.5	V
		Falling edge		4.2	4.4	V
I_Q	Quiescent current into VIN	EN= high, no switching		400		μA
I_{SD}	Shutdown current into VIN	EN = low		3	4	μA
OUTPUT						
V_{OUT}	Operating voltage		3		36	V
		FB connected to GND	5.05	5.1	5.15	V
V_{FB_REF}	FB reference voltage		1.208	1.22	1.232	V
R_{UI}	Upper divider resistor of internal FB	FB connected to GND		78		kΩ
I_{VDRP_max}	Max Line drop compensation current			1.5		μA
V_{Drop_max}	Max internal Line drop compensation	FB connected to GND		120		mV
VCC AND DRIVER						
V_{CC}	VCC clamp voltage		4.9	5.2	5.5	V
I_{VCC_LIM}	VCC current limit	V_{CC} = 5.2V	40			mA
DT1	Dead time for HD off to LD on	V_{CC} = 5.2V		25		ns
DT2	Dead time for LD off to HD on	V_{CC} = 5.2V		25		ns
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	VCC=5.2V		27		mΩ
	Low-side MOSFET on-resistance	VCC=5.2V		11		mΩ
CURRENT LIMIT						
I_{LIM_Peak}	Internal peak current limit		9			A
V_{LIM_OUT}	Output current limit threshold	RSNS=20mΩ	52.4	54	56.6	mV
T_{D_OC}	Debounce time of output overcurrent	RSNS=20mΩ	1.1	1.4	1.7	ms
SWITCHING FREQUENCY						
f_{SW}	Switching frequency		80		600	kHz
		R_{FREQ} = Floating		120		kHz
SOFT START						
t_{SS}	Internal soft-start time	VOUT from 10% to 90%		5	8	ms
BC1.2 DCP MODE						
R_{DPM_short}	DP/DM short resistor		5	10	20	Ω
DIVIDER MODE						
$V_{DP_divider}$	DP output voltage		2.57	2.75	2.84	V
$V_{DM_divider}$	DM output voltage		2.57	2.75	2.84	V

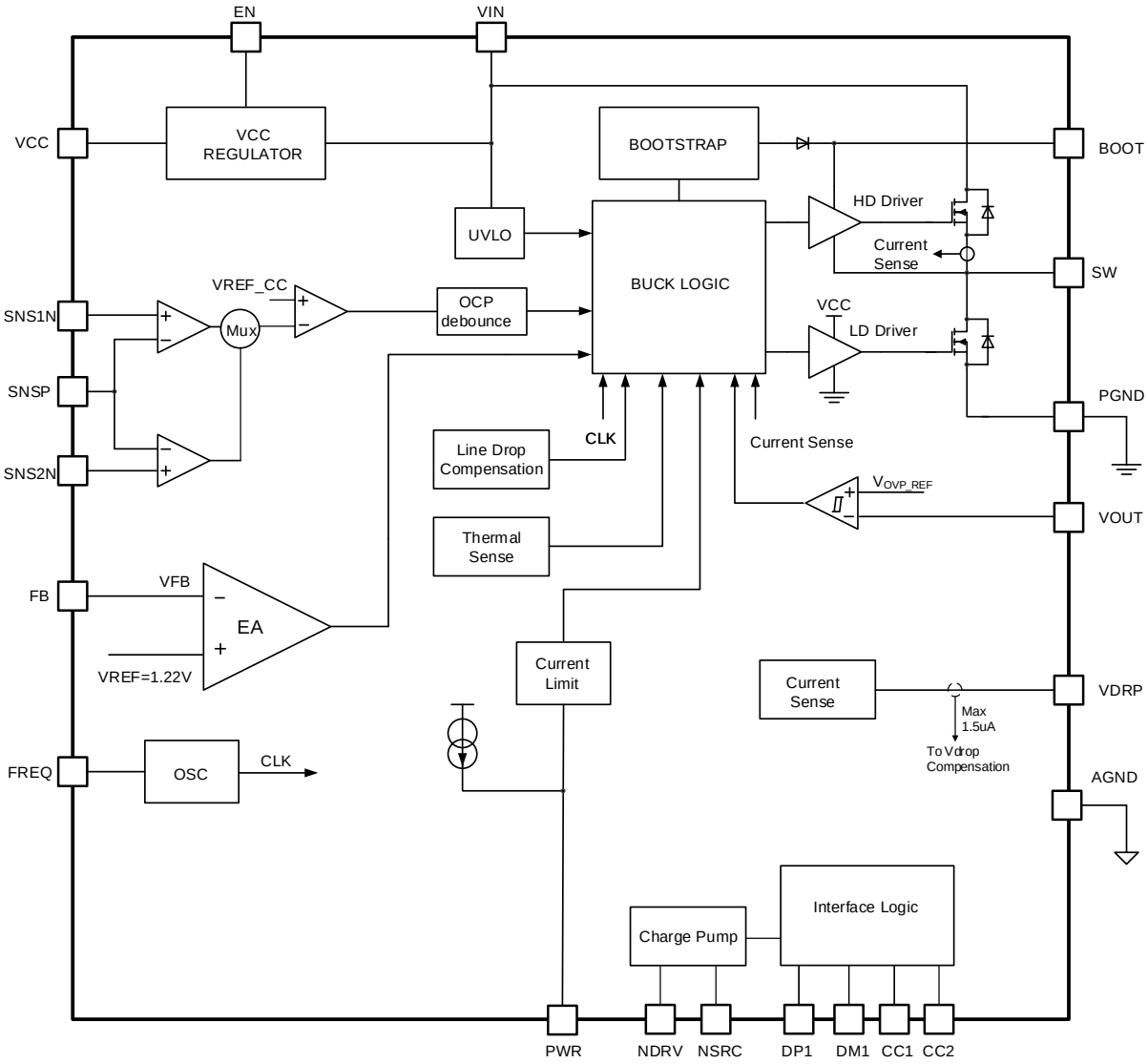
Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

$Z_{DP_divider}$	DP output impedance		24	30	36	kΩ
$Z_{DM_divider}$	DM output impedance		24	30	36	kΩ
1.2V/1.2V MODE						
$V_{DPM_1.2V}$	DP/DM output voltage		1.1	1.2	1.3	V
$Z_{DP_1.2V}$	DP output impedance		70	100	130	kΩ
$Z_{DM_1.2V}$	DM output impedance		70	100	130	kΩ
LOGIC CONTROL						
V_{EN_R}	EN rising threshold		1.1	1.2	1.35	V
V_{EN_F}	EN falling threshold		0.9	1.0	1.1	V
V_{MODE_L}	MODE logic low voltage		0.4			V
V_{MODE_H}	MODE logic high voltage				1.2	V
PROTECTION						
OVP	Output over voltage protection	FB connected to feedback network	108%	110%	112%	
		FB connected to GND	5.5	5.55	5.61	V
V_{HICP}	Hiccup trigger threshold voltage			2.0		V
T_{HICP_ON}	On time of Hiccup Mode	VOUT<2.0V	15	20	25	ms
T_{HICP_OFF}	Off time of Hiccup Mode	VOUT<2.0V	400	500	600	ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature (1)			165		°C
	Thermal shutdown hysteresis (1)			15		°C

(1) Guarantee by design

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

8 Functional Block Diagram



Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

9 Detailed Description

The SC8112A is a dual-output synchronous buck converter with a wide input voltage range. The SC8112A is configured to provide a fixed 5-V or customized output voltage programmed by FB pin. Each channel offers max 3A continuous output capacity with ±5% current limit accuracy.

The SC8112A operates in a fixed frequency current mode control to regulate the output voltage in Constant Voltage (CV) mode. If output current reaches its limit, the SC8112A enters Constant Current (CC) mode while output voltage drops. If the output current still goes larger, SC8112A enters hiccup as short circuit protection when output voltage is lower than 2V. The line drop compensation, power limitation and operating frequency are programmable for different user's application. The internal loop compensation simplifies the design process and save the external components. The SC8112A works in PFM mode, high efficiency can be achieved in light load condition.

9.1 Feature Description

9.1.1 Enable and Programmable UVLO

The SC8112A has an enable control pin EN: pulling it high enables the IC and pulling it low disables the IC. Connect EN to VIN for automatic startup. EN pin is connected to GND internally with a typical 800kΩ resistor to avoid uncertain status if EN pin is floating.

EN pin can also be reused for VIN under voltage protection. Connecting the center tape of the divider resistors between VIN and GND programs the VIN under voltage threshold and restart voltage, as shown in Figure. 4

The VIN under voltage threshold can be calculated as the following equation.

$$V_{IN_LOW} = 1.0\text{V} \times \left(1 + \frac{\text{R}_{\text{IN1}}}{\text{R}_{\text{IN2}} \times R_{PD}}(\text{R}_{\text{IN2}} + R_{PD})\right)$$

When the input voltage is higher than the startup threshold, the SC8112A goes back to normal operation.

$$\text{V}_{\text{IN_HIGH}} = 1.2\text{V} \times \left(1 + \frac{\text{R}_{\text{IN1}}}{\text{R}_{\text{IN2}} \times R_{PD}}(\text{R}_{\text{IN2}} + R_{PD})\right)$$

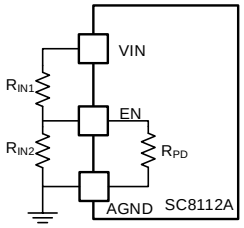


Figure.4 UVLO Threshold Programming

9.1.2 Startup and Shutdown

The SC8112A integrates an internal circuit that controls the ramp up of output voltage during start-up and prevents the converter from the large inrush current. During the startup phase, the internal soft-start circuit increases the voltage on FB pin gradually so that the output voltage slope follows the FB pin voltage slope until the target voltage is reached.

9.1.3 Output Voltage Setting

The SC8112A can be configured for two fixed 5.05V output ports with FB pin connected to GND. The output voltage can also be configured for customized values by using external feedback resistors. The FB status is only detected when IC is powered up, so the FB configuration setting is latched and cannot be changed until SC8112A is powered down and restart again.

If alternative output voltage is required, the following equation can be used to calculate the divider resistor.

$$\text{VOUT} = \text{V}_{FB_REF} \times \left(1 + \frac{\text{R}_U}{\text{R}_D}\right)$$

Where:

V_{FB_REF} = Internal reference voltage 1.22V

R_U and R_D = Resistor divider at FB connected to VOUT and AGND.

9.1.4 Line Drop Compensation

The SC8112A is capable of compensating the output voltage drop, caused by a long trace, to keep a fairly constant load-side voltage. The line drop compensation is adjusted by the internal current source, which sinks a certain current from FB to GND. The current slop can be adjusted by VDRP pin with a resister connected to GND (1.5uA, max).

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

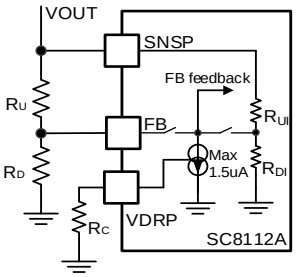


Figure.5 Line Drop Compensation diagram

The compensation voltage is calculated by the following formulas:

$$\Delta V_{OUT} = \frac{2.5\times R_U}{R_C} \times V_{SENSE}$$

$$V_{SENSE} = I_{OUT} \times R_{SENSE}$$

Where:

R_U is the upper resistor of FB divider. The maximum compensation voltage: $\Delta V_{OUT-MAX} = 1.5 \times R_U$ .For FB pin connected to GND application, R_{UI} is 78 KΩ and the maximum compensation voltage $\Delta V_{OUT-MAX}$ is 117mV.

R_C =VDRP setting resistor.

V_{SENSE} is the output current sampling voltage (54mV, max).In dual outputs application, the device selects the larger one to compensate the line drop.

I_{OUT} = output voltage

R_{SENSE} = output current sampling resistor

Here are 2 typical applications with different R_C:

Example 1, FB pin connected to GND application:

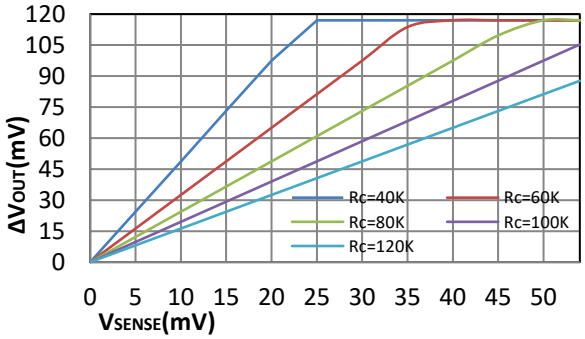


Figure.6 ΔV_{OUT} vs. V_{SENSE}(R_{UI}=78 KΩ)

Example 2, FB pin is set with 100K upper resistor:

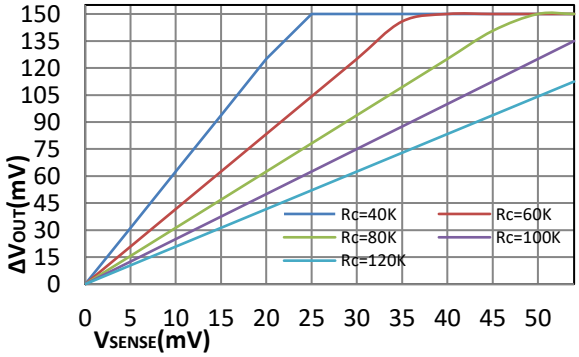


Figure.7 ΔV_{OUT} vs. V_{SENSE}(R_U=100 KΩ)

Using proper R_C/R_U user can set the compensation slop and the maximum amplitude. The line drop compensation amplitude increases linearly as the load current increasing.

9.1.5 Switching Frequency

The switching frequency can be set by a resistor between FREQ pin and GND. Figure.8 shows the relationship between operating frequency and resistor value.

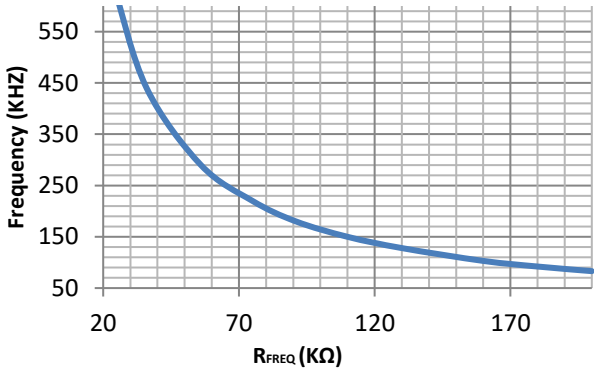


Figure.8 Switching Frequency vs. Setting Resistor

For minimal external components and simplifying the design process, the SC8112A also supports 120-kHz operating frequency if FREQ pin is floating.

9.1.6 Output Power Limit

The output power limit function helps customer to control the total power delivery of the system. Especially in the application of fast charge, the total power delivery should be same even though the VOUT is different. Due to this function, the output current limit can be different according to different output voltage.

The output power limit can be set by connecting a resistor between PWR pin and GND. The following table shows the relationship between output power limit and the resistor.

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Table. 1 Relationship between R-PWR and power limit

R_{PWR} (KΩ)	0	56	68	82	100	120
P_{OUT} (typ.) (W)	Disabled	38	31	26	21	18

If the output power limit function is not needed, tie the PWR pin to ground directly, the maximum output power is limited by internal peak current limit or the programmed output current limit loop.

9.1.7 Constant Voltage / Constant Current Mode

SC8112A operates either in CV (constant voltage) mode or CC (constant current) mode and automatically changes from CV to CC smoothly. In CV mode, SC8112A regulates the output voltage. As long as output current limit threshold is reached, SC8112A enters CC mode and the output voltage drops while output current is clamped at the setting values.

SC8112A both monitors the two output ports current limit. In case either of the two outputs current reaches setting current limit, SC8112A enters CC mode.

The current limit can be set by the current sensing resistors by the following equation.

$$I_{LIM_OUT} = \frac{54mV}{RSNS}$$

Where, RSNS is the value of current sense resistor.

Usually, the BC1.2 mode limit is set at 2.7A by default with an external sensing resistor RSNS=20mΩ. When the voltage drop across the sensing resistor gets higher than 54mV, the internal over current timer will be activated. After 1.4ms if the voltage drop is still higher than 54mV, the IC stops switching and goes into over current protection phase. Table 2 shows recommended RSNS and corresponding current limit setting.

Table. 2 Relationship between RSNS and current limit

RSNS	Output Current Limit
16mΩ	3.375A
20mΩ	2.7A

9.1.8 Under-Voltage Lockout (UVLO)

The UVLO function protects the chip from operating at insufficient power supply. The chip disables all the function if input voltage in lower than 4.0V and it doesn't start up again until input voltage is higher than 4.2V.

9.1.9 Output Over-Voltage Protection

SC8112A adopts an output over-voltage protection (OVP) with ±1% accuracy. When FB pin is connected to GND, in case the output voltage is higher than 5.55V, the buck converter stops switching until OVP status is removed. When FB is connected with two divider resistors, OVP is triggered in case the FB voltage is higher than 110% normal reference voltage.

9.1.10 Short Circuit Protection and Hiccup

The SC8112A integrates a hiccup mode which is triggered once the output voltage is lower than 2V. In hiccup mode, SC8112A periodically stops switching for 500ms and then tries to restart with output current increasing to current limit for 20ms. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate the thermal issue and to protect the converter. Once the short-circuit condition is removed, SC8112A exits hiccup mode and goes back to normal operation.

9.1.11 Over Temperature Protection

The over temperature protection (OTP) prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165 ℃, SC8112A is shut down. When the temperature drops below threshold (typically 150℃), the chip is enabled again.

9.1.12 Charging Port Controller

The SC8112A integrates a USB type-A port dedicated charging port controller. It can detect the type of the attached phone, and automatically support below common charging protocols:

1. USB battery charging specification, revision 1.2 (BC1.2)

2. Chinese Telecommunication Industry Standard YD/T 1591-2009

3. The divider mode for Apple device (DP = 2.7V, DM = 2.7V)

4. The 1.2V/1.2V Mode for Samsung device

9.1.13 Type C Controller

The SC8112A integrates a USB Type-C Downstream Facing Port (DFP) controller. It acts as a DFP/Source device, and monitors the Type-C Configuration Channel (CC) lines to determine when an USB device is attached. If an Upstream Facing Port (UFP) or Sink device is attached, the SC8112A turns on the power switch automatically which controlled by NDSRC and NDRV pin with soft-start so to apply power to

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

USB-C port. Then it advertises its 3A current source capability through CC line.

Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

10 Application Information

10.1 Input and Output Capacitor Selection

The input current of the Buck converter is discontinuously and the input capacitor should be carefully selected. At least 30μF input capacitor is required for small input voltage ripple and stability. The input capacitor can be electrolytic, tantalum or ceramic. MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60 μF X5R or X7R capacitors with higher voltage rating than operating voltage with margin is recommended. A 10μF ceramic capacitor must be placed close to IC's VIN pin, to improve the high frequency performance (stability and EMI radiation).

To avoid input hot swapping spike, a low ESR aluminum electrolytic or solid capacitor is recommend to suppress the input voltage spike. Aluminum solid capacitor is highly recommended to improve efficiency.

The input voltage ripple caused by the capacitance can be calculated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The output capacitor is recommended to be larger than 80μF.

The output voltage ripple is estimated as the following equation

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \times (1 - \frac{V_{OUT}}{V_{IN}})$$

If electrolytic or tantalum capacitor is used, low ESR capacitor is recommended and 10μF ceramic capacitor is needed in parallel.

10.2 Inductor Selection

For better power limit regulation, a larger inductance is recommend to make sure the system operates in CCM mode at the max load, especially the max VIN and the max VOUT. The min inductance is calculated as follows:

$$L \geq \frac{V_{OUT}}{2I_{OUT} \times f_{SW}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so around 10mΩ n DCR is recommended for the first selection. If the current is relatively small, high DCR inductor can be selected. But if switch current is high, just like around 10A, then select the lowest DCR inductor as much as possible because 10mΩ DCR also causes 1W power loss.

The inductor saturation current I_{SAT} should be higher than input / output current with sufficient margin.

10.3 PCB Layout Guide

For best performance, PCB layout should be carefully designed to avoid instability, noise and EMI. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI. For a BUCK converter, the critical loop area is showed in figure 9:

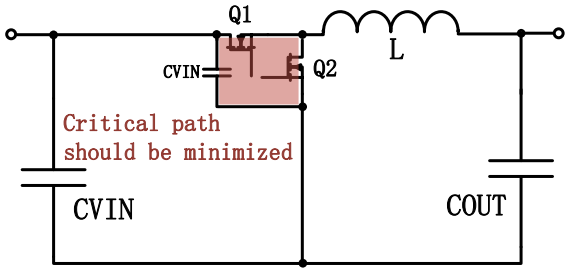


Figure.9 Minimizing the critical path helps mitigate EMI

Here shows some guidelines for reference:

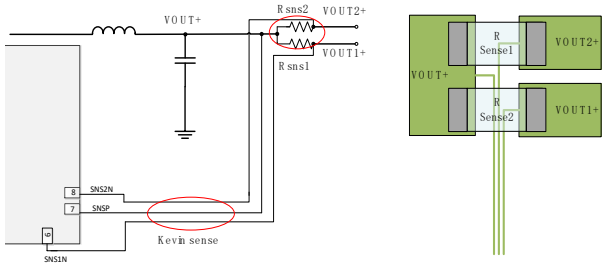
1) The input capacitor (CVIN, 10uF, MLCC) should be close to IC to minimize the critical path area and make sure the current flows through the CVIN first, then VIN pin.

2) The VCC capacitor (CVCC, 1uF, MLCC) should be close to VCC pin and connected to PGND pin directly, to avoid noise and instability.

3) The power limit resistor and line drop compensation resistor (R-PWR) are sensitive, it should be close to the corresponding pin (keep away from switching node) and connected to AGND pin directly.

4) The FB feedback resistor should be close to FB pin and be away from switching node. A feed-forward capacitor is highly recommended to prevent instability.

5) The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing)



Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

Figure.10 Current sense

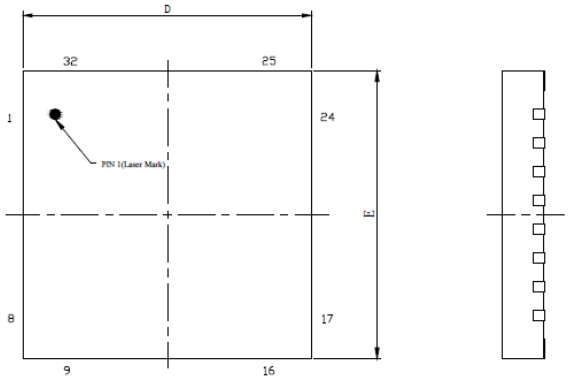
6) The RC snubber is connected between SW and PGND to absorb switching noise. The snubber should be close to SW and GND pin and minimize the loop area to optimize EMI.

7) The boot capacitor should be close to SW and BOOT pin

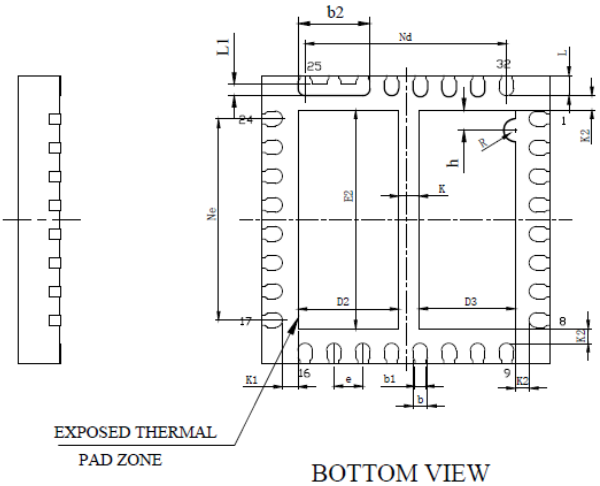
Copyright © 2026, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

MECHANICAL DATA

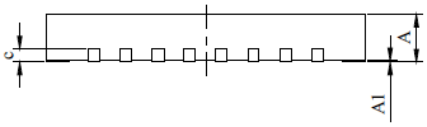
QFN32L (0505 x 0.75)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

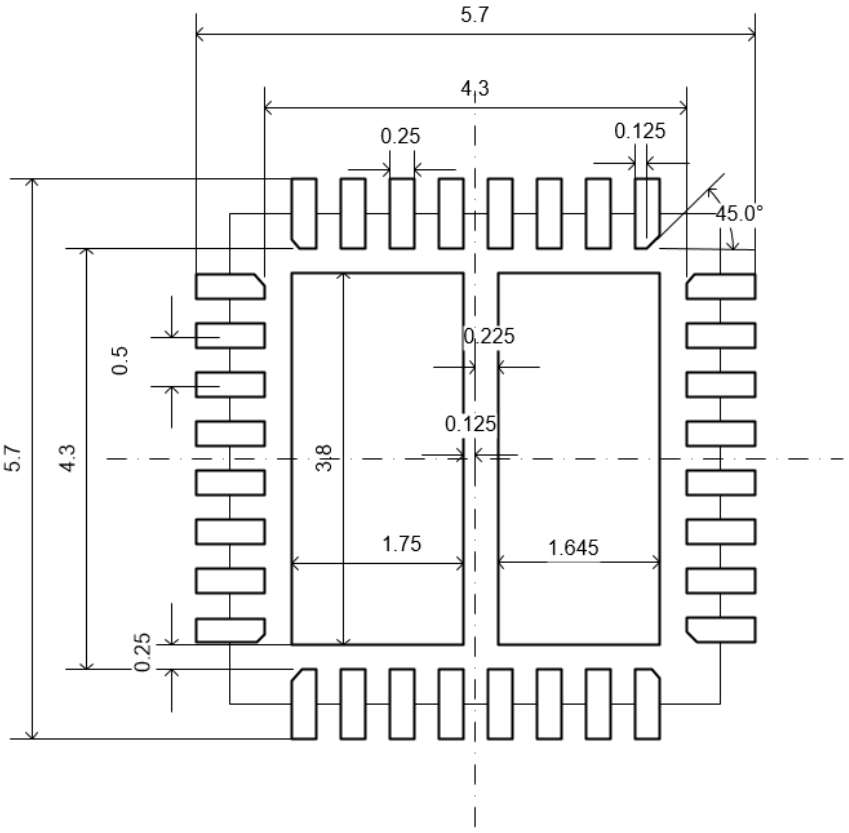
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
b2	1.20	1.25	1.30
c		0.203REF	
D	4.90	5.00	5.10
D2	1.65	1.75	1.85
D3	1.575	1.675	1.775
e		0.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
Ne		3.50BSC	
L	0.30	0.35	0.40
L1	0.15	0.20	0.25
K	0.30	0.35	0.40
K1	0.225	0.275	0.325
K2	0.20	0.25	0.30
R		0.20REF	
h		0.35REF	

DATASHEET DRAFT CONFIDENTIAL

Copyright © 2020, Southchip Semiconductor Technology (Shanghai) Co., Ltd.

RECOMMENDED FOOTPRINT

Example Board Layout



NOTES:

A. All linear dimensions are in millimeters
B. Publication IPC-7351 is recommended for alternate designs
C. Using any array of heat-sinking vias to connect the exposed pad to the PCB power plane. If the PCB has multiple copper layers, these thermal vias must also be connected to inner layer heat-spreading planes.
D. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DATASHEET CHIP

Copyright © 2020, Southchip Semiconductor Technology (Shanghai) Co., Ltd.