

SC77120AQ Single Channel 20-mΩ Smart High Side Driver with Advanced Protections and Diagnostics

1 Descriptions

The SC77120AQ is a fully-protected single channel smart high side driver qualified in automotive grade. Full diagnostics and high accuracy current sense of channel enable intelligent control of the load even in harsh conditions. It integrates one 20mΩ MOSFET in a compact package size with advanced protections of load current limitation, dynamic thermal swing shutdown, absolute thermal shutdown. Auto-restart or fault latch-off mode in over temperature events can be configured by an external /FaultRST pin. Besides, it features chip junction temperature and supply voltage sense output to monitor the driver status more precisely. A multiplexed pin delivers proportional current sense, chip junction temperature, supply voltage sense signals and fault indications in Normal Operation Mode.

2 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C4B
- Single Channel 20mΩ Smart High-Side Driver with Full Diagnostics
 - 16-pins, Auto-restart or Fault Latch-off Mode, Channel Fault Diagnosis, Proportional Load Current, T_j and V_s Sense Output
- Operating Junction Temperature: -40 to 150°C
- Wide Operating Voltage from 4 to 28V with Load Dump Withstand Voltage up to 40V
- Ultra Low Standby Current < 500 nA
- Input Control, 3.3 V and 5 V Logic Compatible
- Multiplexed Analog Signals Sensing Output, including
 - Proportional Load Current of Channel
 - Power Supply Voltage
 - Chip Junction Temperature
- High Accuracy Current Sense:
 - ±5% @ 5A
 - ±5% @ 3A
 - ±12% @ 0.1A
 - ±20% @ 0.05A
 - ±65% @ 0.01A
- Electrical Transient Disturbance Immunity Certification of ISO7637-2 and ISO16750-2
- Advanced Protections:
 - Short to GND Protection by Internal Current Limit
 - Dynamic Thermal Swing Shutdown and Absolute Thermal Shutdown with Auto-restart
 - Configurable Fault Latch-off Mode for Both Thermal Swing Shutdown and Absolute Thermal Shutdown Events
 - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
 - Loss of GND and Loss of Battery Protection
 - Under Voltage Lockout (UVLO) Protection
- Diagnostics:
 - Overload and Short to Ground Detection in Normal Operation Mode
 - Open Load and Short to Battery Detection in OFF-State

3 Applications

- High Side Power Driver for Sub-module
- Power Switch for Automotive Lamp
- High Side Relays and Solenoids
- General Resistive, Inductive and Capacitive Loads

4 Device Information

ORDER NUMBER	DISCRIPTION	PACKAGE	BODY SIZE
SC77120AQSHER	<ul style="list-style-type: none"> Auto-restart or Fault Latch-off Mode Channel Fault Diagnosis Output Proportional Load Current, T_J and V_s Sense Output 	eSSOP-16	5.2mm x 3.9 mm x 1.4mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
1.0	2024.10	New	Initial Release.
1.0.1	2025.09	5~9	1. " V_{sense_TC} "@-40°C Updated (Min./Max.:2.16/2.44 → 2.2/2.4) 2. " V_{sense_TC} "@25°C Updated (Min./Max.:1.77/2.04 → 1.8/2.0) 3. " V_{sense_TC} "@125°C Updated (Min./Typ./Max.:1.18/1.3/1.54 → 1.2/1.32/1.5) 4. " V_{sense_Vs} " Updated (Min./Typ./Max.:3.14/3.24/3.34 → 3.17/3.23/3.32) 5. " $t_{D,ON}$ " Updated (Min./Max. :10μs/120μs → 35μs/95μs) 6. " $t_{D,OFF}$ " Updated (Min./Typ./Max.:40μs/140μs/200μs → 20μs/70μs/150μs) 7. " dV/dt_{ON} " Updated (Min./Typ./Max.:0.1V/μs / 0.3V/μs / 0.5V/μs → 0.3V/μs / 0.45V/μs / 0.6V/μs) 8. " dV/dt_{OFF} " Updated (Min./Typ./Max.:0.1V/μs / 0.3V/μs / 0.5V/μs → 0.3V/μs / 0.45V/μs / 0.7V/μs) 9. " t_{skew} " Updated (Min./Max. :-150μs/50μs → Min./Max. :-100μs/100μs)
1.0.2	2025.09	5~9	" t_{Latch_RST} " Updated (Min./Typ./Max.:3μs/10μs/20μs → 60μs/80μs/90μs)
1.0.3	2026.03	10-22	Update the function description in the datasheet.

6 Typical Application Circuit

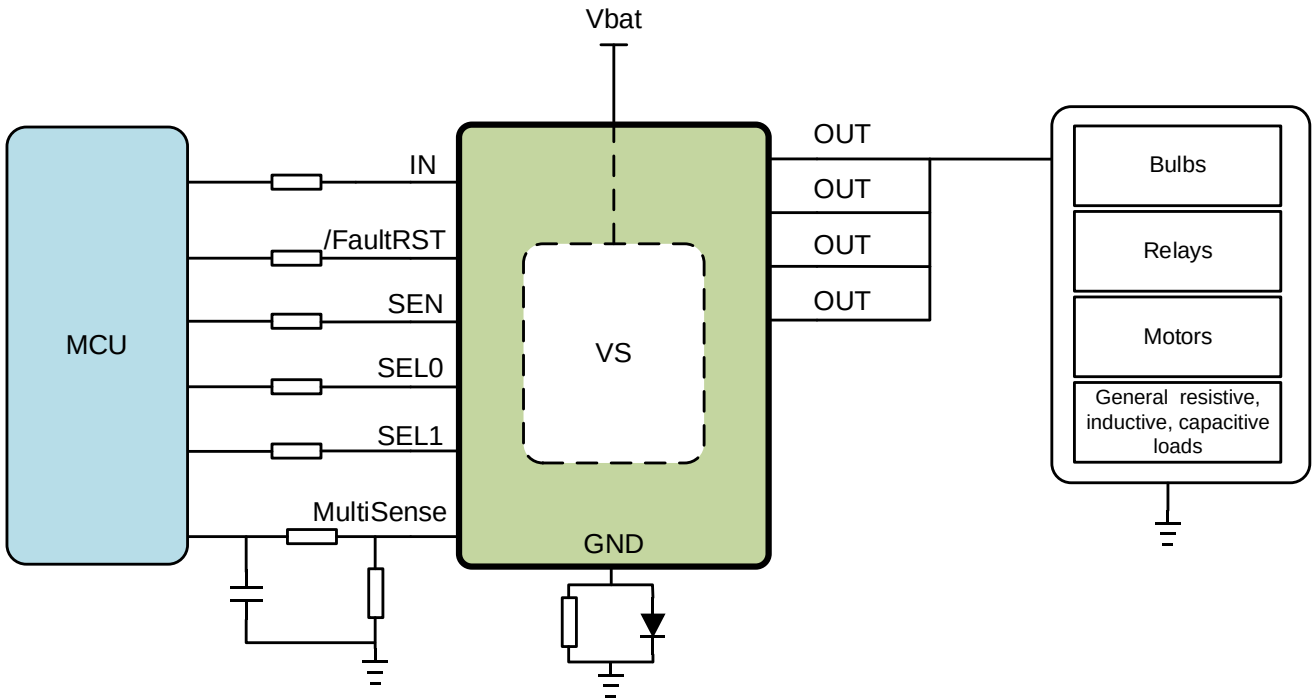


Figure 6-1. Typical Application Circuit

7 Terminal Configuration and Functions

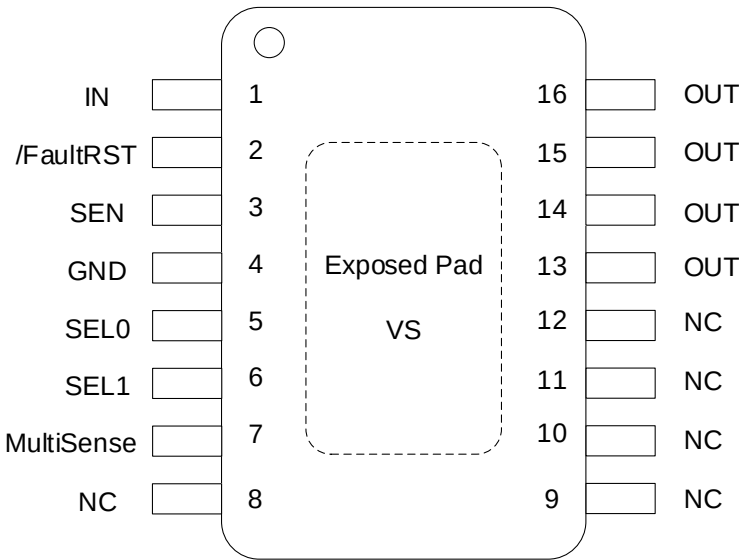


Figure 7-1. Configuration Diagram (Top View)

Table 7-1. Suggested Connections for Unused and Not Connected Pins

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	IN	I	Input pin of the Channel. Active high to turn on.
2	/FaultRST	I	Latch fault if it's set high; clear fault or keep auto-restart if it's set low.
3	SEN	I	Diagnosis enable pin. Active high.
4	GND	-	Ground connection.
5	SEL0	I	SEL bit 0 for diagnosis multiplexer selection.
6	SEL1	I	SEL bit 1 for diagnosis multiplexer selection.
7	MultiSense	O	Multiplexed sense output. It delivers proportional current sense , chip junction temperature , supply voltage sense signals and fault indications
8	NC	-	Not connected.
9	NC	-	Not connected.
10	NC	-	Not connected.
11	NC	-	Not connected.
12	NC	-	Not connected.
13	OUT	O	Output of Channel.
14	OUT	O	Output of Channel.
15	OUT	O	Output of Channel.
16	OUT	O	Output of Channel.
Exposed Pad	VS	I	Power supply connection.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	UNIT
Voltage range at Terminals ⁽²⁾	Supply Voltage ⁽³⁾	-0.3	40	V
	Reverse Polarity Voltage with External Blocking Diode ⁽⁴⁾	-18		V
	Supply Voltage for Short Circuit Protection ⁽⁷⁾		18	V
	Voltage on IN, SEN, SELx, and /FaultRST Pins	-0.3	7	V
	Voltage on Multisense Pin	-2.7	7	V
Current range at Terminals ⁽²⁾	DC Current on OUT Pin	-3.5	Internally limited	A
	Current on GND Pin	-50 -250 ⁽⁵⁾	20	mA
	Current on IN, SEN, SELx, /FaultRST Pins	-30	2	mA
	Current on Multisense Pin	-2	30	mA
f _{IN,MAX}	PWM Frequency on IN Pin		2	kHz
E _{AS}	Inductive Load Switch-off Energy Dissipation, Single Pulse ⁽⁶⁾		25	mJ
T _A	Operating Ambient Temperature Range	-40	125	°C
T _J	Operating Junction Temperature Range	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Supply voltage to withstand 40V load dump test for 400ms, according to ISO 16750-2:2010 Test B
- (4) Reverse polarity condition: t < 60 s, reverse current < I_{OUT,REV1}, GND pin 4.7kΩ resistor in parallel with diode.
- (5) For limited time range: t < 120s
- (6) Test condition: V_S = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-μm Cu, 2- × 35-μm Cu. 600-mm² thermal pad copper area.

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human Body Model (HBM) ESD Stress Voltage ⁽²⁾	All Pins	-4	4	kV
	Charged Device Model (CDM) ESD Stress Voltage ⁽³⁾	All Pins	-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per AEC-Q100-002. The human-body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each terminal.
- (3) Level listed above is the passing level per AEC-Q100-011.

8.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V_S	Voltage on VS pin	5		28	V
V_{IH}	Input Logic High on IN, SEN, SELx, and /FaultRST Pins	2.1		5.5	V
V_{IL}	Input Logic Low on IN, SEN, SELx, and /FaultRST Pins	0		0.9	V
$I_{OUT,NOM}$	Nominal DC load current		5		A
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		eSSOP-16	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance ⁽²⁾	32.2	°C/W
$R_{\theta JC(top)}$	Junction to case(top) thermal resistance	21.9	°C/W
$R_{\theta JC(bottom)}$	Junction to case(bottom) thermal resistance	1.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.4	°C/W

(1) Measured on JE5D51-7, 4-layer PCB.

(2) The thermal data is based on JEDEC standard high-K profile – JE5D 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

8.5 Electrical Characteristics

-40°C < T_J < 150°C and 5V < V_S < 28V unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE					
$V_{S,NOM}$	Nominal Operating Voltage	5	13.5	28	V
$V_{S,EXT}$	Extended Operating Voltage	4		5	V
		R_{ON} and switching characteristics may increase compared to those in $V_{S,NOM}$, but protection functions are still operative.			
$V_{S,UVR}$	Undervoltage Restart	3.5	3.7	4	V
$V_{S,UVF}$	Undervoltage Shutdown	3	3.2	3.5	V
$V_{S,UVhys}$	Undervoltage Shutdown Hysteresis		0.5		V
OPERATING CURRENT					



I _{S_ON}	Supply Current for No Load, No Diagnosis	V _S =13.5V, V _{IN} =5V, V _{FR} =V _{SEN} = V _{SEL0,1} = 0 V; I _{OUT} = 0 A	2	3	mA	
I _{GND_ON}	I _q in ON-state with All Channels Active	V _S =13.5V, V _{IN} =V _{SEN} =5V, V _{FR} = V _{SEL0,1} = 0 V; I _{OUT} = 3 A		3	mA	
I _{S_STBY}	Supply Current in Standby Mode	V _S =13.5V; V _{IN} = V _{SEN} = V _{FR} =V _{SEL0,1} = V _{OUT} = 0 V, T _J = 25°C		0.5	uA	
		V _S =13.5V; V _{IN} =V _{SEN} =V _{FR} =V _{SEL0,1} =V _{OUT} =0 V, T _J = 125°C		3	uA	
I _{L_OFF}	Output Leakage Current in OFF-state	V _S =13.5V; V _{IN} =V _{SEN} =V _{FR} =V _{SEL0,1} = V _{OUT} = 0 V; T _J = 25°C	0.01	0.5	uA	
		V _S =13.5V; V _{IN} =V _{SEN} =V _{FR} =V _{SEL0,1} = V _{OUT} = 0 V; T _J =125°C		3	uA	
t _{D_STBY}	Blanking Time into Standby Mode	V _S =13.5V, V _{SEN} =5V to 0V, V _{IN} = V _{OUT} = V _{FR} = V _{SEL0,1} = 0 V	12.5		ms	
POWER STAGE						
R _{ON}	ON-state Resistance	V _S =13.5V, I _{OUT} = 2A, T _J = 25°C	18	26	mΩ	
		V _S =13.5V, I _{OUT} = 2A, T _J = 150°C		40	mΩ	
I _{LIMH}	Current Limit	V _S = 5~18 V	40	50	60	A
I _{LIML} ⁽¹⁾	Current Limit during Thermal Cycling	V _S = 13 V; T _R < T _J < T _{SD}	20			A
V _{DS,CLP}	Drain to source internal clamp voltage	I _{OUT} = 2 A, L=6mH, T _J = -40°C	38			V
		I _{OUT} = 2 A, L=6mH, T _J = 25~150°C	42	48	52	V
OUTPUT DIODE CHARACTERISTICS						
V _{OUT,F}	Drain to Source Diode Voltage	V _{IN} =0, I _{OUT,REV} =3A	0.7			V
I _{OUT,REV} ⁽¹⁾	Continuous Reverse Current when Reverse Polarity	t < 60 s, V _S = 13.5 V, GND pin 4.7kΩ resistor in parallel with diode. T _J = 25°C	4			A
I _{OUT,INV} ⁽¹⁾	Continuous Inverse Current When V _{OUT} > V _S + V _{OUT,F}	t < 60 s, V _S = 13.5 V, T _J = 25°C	3			A
LOGIC INPUT (IN, SEN, SELx, /FaultRST)						
V _{IH}	Input Logic High		2.1			V
V _{IL}	Input Logic Low			0.9		V
V _{I_HYS}	Input Logic Hysteresis		170			mV
I _{IH}	High Level Pull-down Current	V _{IH} =2.1V		10		uA
I _{IL}	Low Level Pull-down Current	V _{IL} =0.9V	1	10		uA
DIAGNOSTICS						

I _{LOSS,GND}	Output Leakage Current when Loss of Ground		100			uA
V _{OL,OFF}	Open Load Detection Threshold in OFF-state (Vout-GND)	V _{SEN} =5V, V _{IN} =0V, V _{SEL1} =0V, V _{SEL0} =0V	2	3	4	V
I _{OL,OFF}	OFF-state Output Sink Current with Open Load	V _S =13.5 V, V _{SEN} =5V, V _{IN} = 0 V, V _{OUT} =4V	-100			uA
t _{D_OL,IN}	OFF-state Diagnostic Delay Time from Falling Edge of Input	V _S =V _{OUT} =13.5V, V _{SEN} =5V, V _{SEL0,1} =0, V _{IN} =5V to 0V	350	500	700	us
t _{D_OL,VO}	OFF-state Diagnostic Delay Time from Rising Edge of Vout	V _S =13.5V, V _{SEN} =5V, V _{IN} = V _{SEL0,1} =0 V, V _{OUT} =0V to 4V	150 250			us
t _{D_OL,SEN}	OFF-state Diagnostic Delay Time from Rising Edge of SEN	V _S =13.5V, V _{IN} =V _{SEL0,1} =0 V, V _{OUT} =4V, V _{SEN} =0V to 5V	150 250			us
T _{SD} ⁽¹⁾	Thermal Shutdown Temperature		170			°C
T _R ⁽¹⁾	Thermal Shutdown Flag Reset Temperature		145			°C
T _{SW} ⁽¹⁾	Thermal Swing Shutdown Threshold	T _J = - 40 °C, V _s =13.5V	60			°C
T _{HYS} ⁽¹⁾	Hysteresis for Resetting the Thermal Shutdown and Swing		20			°C
t _{Latch_RST}	Deglitch Time for Reset Fault	V _{SEN} =5V, V _{IN} =5V, V _{SEL0,1} =0V, Latched fault triggered, then V _{FR} = 5V to 0V	60	80	90	us
Multiple SENSE Functions						
K _{SNS}	Ratio of Current Sense		3000			
dK _{SNS} /K _{SNS}	Accuracy of Current Sense (I _{CS} × K _{SNS} – I _{OUT}) /I _{OUT} × 100	I _{OUT} = 0.01A	-65 65			%
		I _{OUT} = 0.05A	-20 20			
		I _{OUT} = 0.1A	-12 12			
		I _{OUT} = 3A	-5 5			
		I _{OUT} = 5A	-5 5			
V _{SENSE_SAT}	SENSE Saturation Voltage	V _S = 7 V; R _{SENSE} = 2.5kΩ; V _{SEN} = 5 V; V _{IN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 9 A;	4.8			V
I _{SENSE_SAT}	SENSE Saturation Current	V _S = 7 V; V _{SENSE} = 4V; V _{IN} = 5 V; V _{SEN} = 5 V; V _{SEL0} = 0 V; V _{SEL1} = 0 V; I _{OUT} = 9 A;	4			mA
V _{CS,H}	Fault High Voltage of SENSE	V _S ≥ 7V	5	5.5	6	V
		5V≤V _S <7V	4.3	6		V

$I_{CS,H}$	Fault Current of SENSE	$V_S \geq 7V, V_{SENSE} = 4.3V$	10	mA
V_{SENSE_TC}	SENSE Output Voltage Proportional to T_J	$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$		
		$V_{SEN} = 5V; V_{SEL0} = 0V; V_{SEL1} = 5V; V_{IN} = 0V; R_{SENSE} = 1k\Omega; T_J = -40^\circ C$	2.2 2.3 2.4	V
		$V_{SEN} = 5V; V_{SEL0} = 0V; V_{SEL1} = 5V; V_{IN} = 0V; R_{SENSE} = 1k\Omega; T_J = 25^\circ C$	1.8 1.9 2	V
		$V_{SEN} = 5V; V_{SEL0} = 0V; V_{SEL1} = 5V; V_{IN} = 0V; R_{SENSE} = 1k\Omega; T_J = 125^\circ C$	1.2 1.32 1.5	V
dV_{SENSE_TC} / dT	Temperature Coefficient	$T_J = -40^\circ C$ to $150^\circ C$	-6.0	mV/ $^\circ C$
V_{SENSE_VS}	SENSE Output Voltage Proportional to V_S	$V_{SENSE_VS} = V_S / 4$		
		$V_S = 13V; V_{SEN} = 5V; V_{SEL0} = 5V; V_{SEL1} = 5V; V_{IN} = 0V; R_{SENSE} = 1k\Omega$	3.17 3.23 3.32	V
$I_{SNS,LEAK1}$	Leakage Current of SENSE in Diagnostic Disable State	$V_{SEN}=0V, V_{IN}=5V, I_{OUT}=3A, V_{SENSE}=0V, T_J=125^\circ C$	0.5	μA
$I_{SNS,LEAK2}$	Leakage Current of SENSE in Diagnostic Enable State	$V_{SEN}=5V, V_{IN}=5V, I_{OUT}=0A, V_{SENSE}=0V, T_J=125^\circ C$	6	μA
$t_{SNS,ON1}$	Current SENSE Settling Time from SEN Rising Edge	$V_{IN} = 5V, I_{OUT} \geq 1A. V_{SEN}$ from 0 to 5 V. V_{SENSE} to 90% of sense value, $R_{SENSE} = 1k\Omega$	20	μs
$t_{SNS,OFF1}$	Current SENSE Settling Time from SEN Falling Edge	$V_{IN} = 5V, I_{OUT} \geq 1A. V_{SEN}$ from 5 to 0 V. V_{SENSE} to 10% of sense value, $R_{SENSE} = 1k\Omega$	20	μs
$t_{SNS,ON2}$	Current SENSE Settling Time from IN Current Rising Edge	$V_{SEN}=5V, I_{OUT} \geq 1A. V_{IN}$ from 0 to 5 V. V_{SENSE} to 90% of sense value, $R_{SENSE} = 1k\Omega$	150	μs
$t_{SNS,OFF2}$	Current SENSE Settling Time from IN Falling Edge	$V_{SEN} = 5V, I_{OUT} \geq 1A. V_{IN}$ from 5 to 0 V. V_{SENSE} to 10% of sense value, $R_{SENSE} = 1k\Omega$	20	μs
$t_{SNS,ON3}$	V_{SENSE_TC} Settling Time from Rising Edge of SEN	$V_{SEN} = 0V$ to $5V; V_{SEL0} = 0V; V_{SEL1} = 5V; R_{SENSE} = 1k\Omega$	20	μs
$t_{SNS,OFF3}$	V_{SENSE_TC} Disable Delay Time from Falling Edge of SEN	$V_{SEN} = 5V$ to $0V; V_{SEL0} = 0V; V_{SEL1} = 5V; R_{SENSE} = 1k\Omega$	20	μs
$t_{SNS,ON4}$	V_{SENSE_VS} Settling Time from Rising Edge of SEN	$V_{SEN} = 0V$ to $5V; V_{SEL0} = 5V; V_{SEL1} = 5V; R_{SENSE} = 1k\Omega$	60	μs
$t_{SNS,OFF4}$	V_{SENSE_VS} Disable Delay Time from Falling Edge of SEN	$V_{SEN} = 5V$ to $0V; V_{SEL0} = 5V; V_{SEL1} = 5V; R_{SENSE} = 1k\Omega$	20	μs

$t_{D_CS\to TC}$	SENSE Transition Delay from Stable Current Sense to TC sense	$V_S=13.5V$, $V_{IN} = 5V$; $V_{SEN} = 5V$; $V_{SEL0} = 0V$; $V_{SEL1} = 0V$ to $5V$; $I_{OUT} = 1.5A$; $R_{SENSE} = 1k\Omega$	60	us
$t_{D_TC\to CS}$	SENSE Transition Delay from TC sense to Stable Current Sense	$V_S=13.5V$, $V_{IN} = 5V$; $V_{SEN} = 5V$; $V_{SEL0} = 0V$; $V_{SEL1} = 5V$ to $0V$; $I_{OUT} = 1.5A$; $R_{SENSE} = 1k\Omega$	20	us
$t_{D_TC\to VS}$	SENSE Transition Delay from TC sense to Vs sense	$V_S=13.5V$, $T_J = 125^\circ C$; $V_{SEN} = 5V$; $V_{SEL1} = 5V$; $V_{SEL0} = 0V$ to $5V$; $R_{SENSE} = 1k\Omega$	20	us
$t_{D_VS\to TC}$	SENSE Transition Delay from Vs sense to TC sense	$V_S=13.5V$, $T_J = 125^\circ C$; $V_{SEN} = 5V$; $V_{SEL1} = 5V$; $V_{SEL0} = 5V$ to $0V$; $R_{SENSE} = 1k\Omega$	20	us
Switching Characteristics				
t_{D_ON}	Turn-on Delay Time	V_{IN} rising edge to $V_{OUT} = 20\% * V_S$, $V_S=13.5V$, $R_L=4.3\Omega$, $T_J = 25^\circ C$	35 65 95	us
t_{D_OFF}	Turn-off Delay Time	V_{IN} falling edge to $V_{OUT} = 80\% * V_S$, $V_S=13.5V$, $R_L=4.3\Omega$, $T_J = 25^\circ C$	20 70 150	us
dV/dt_{ON}	Turn-on Slew Rate	V_{OUT} from 20% to 80%, $T_J = 25^\circ C$	0.3 0.45 0.6	V/us
dV/dt_{OFF}	Turn-off Slew Rate	V_{OUT} from 80% to 20%, $T_J = 25^\circ C$	0.3 0.45 0.7	V/us
t_{skew}	Pulse Skew $t_{Pd_rise}-t_{Pd_fall}$	$V_S=13.5V$, $R_L=4.3\Omega$, $T_J = 25^\circ C$ t_{Pd_rise} : V_{IN} rising edge to $V_{OUT} = 80\% * V_S$ t_{Pd_fall} : V_{IN} falling edge to $V_{OUT} = 20\% * V_S$	-100 100	us

(1) Parameter guaranteed by design and characterization; not subject to production test.

8.6 Typical Characteristics

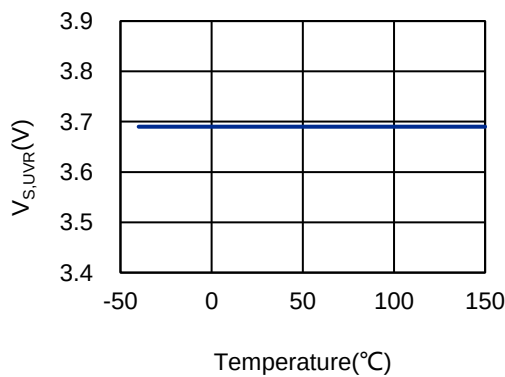


Figure 8-1. $V_{S,UVR}$ vs T_A

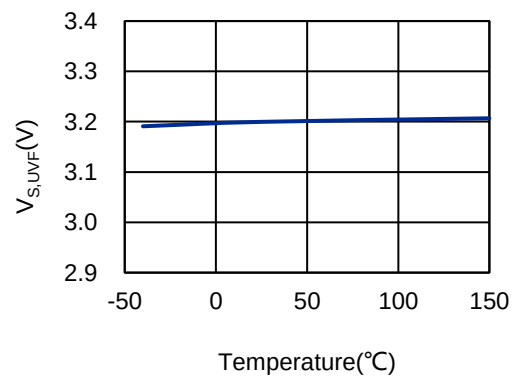


Figure 8-2. $V_{S,UVF}$ vs T_A

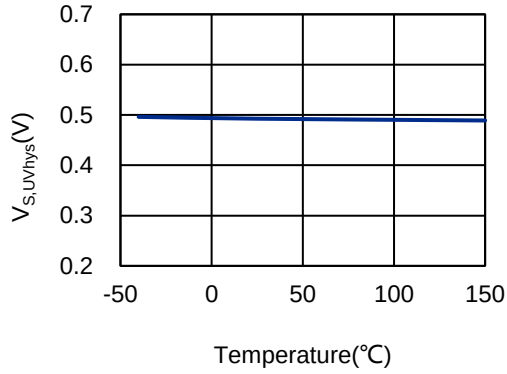


Figure 8-3. $V_{S,UVhys}$ vs T_A

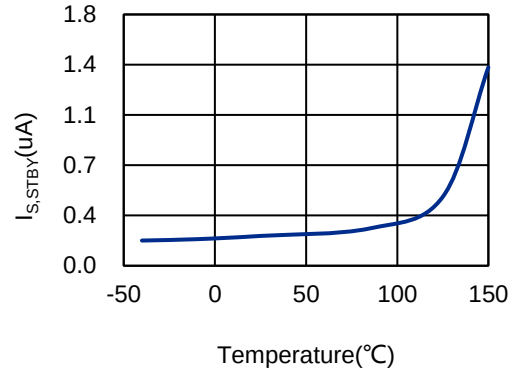


Figure 8-4. $I_{S,STBY}$ vs T_A

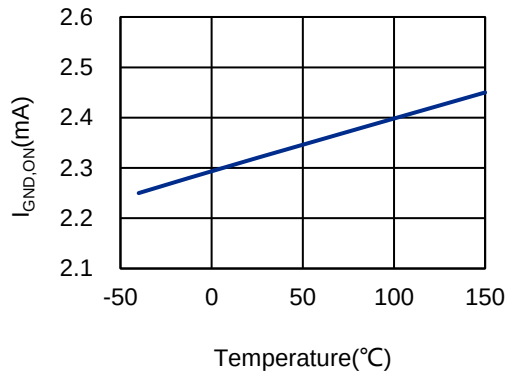


Figure 8-5. $I_{GND,ON}$ vs T_A

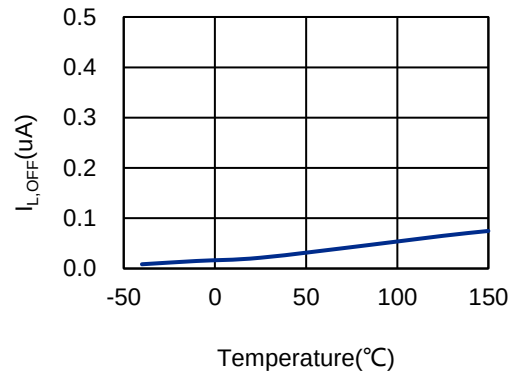


Figure 8-6. $I_{L,OFF}$ vs T_A

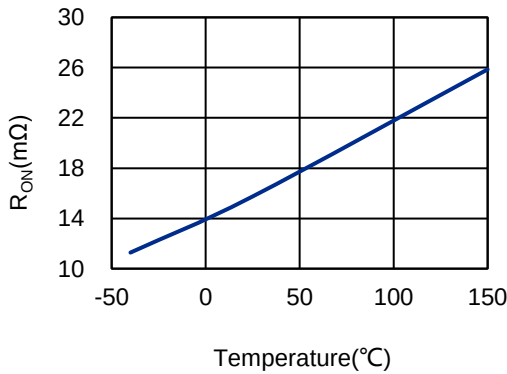


Figure 8-7. R_{ON} vs T_A

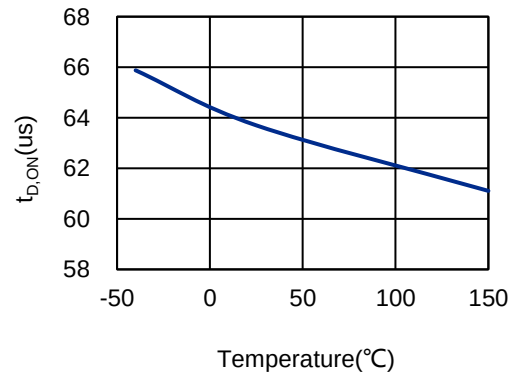


Figure 8-8. $t_{D,ON}$ vs T_A

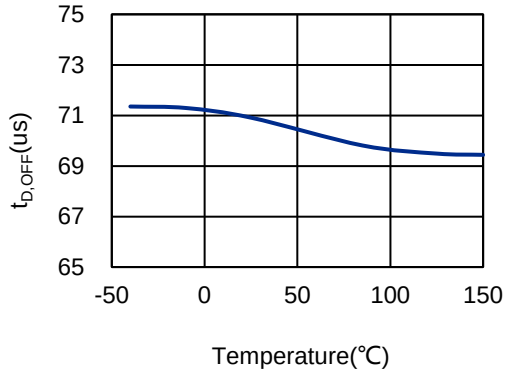


Figure 8-9. $t_{D,OFF}$ vs T_A

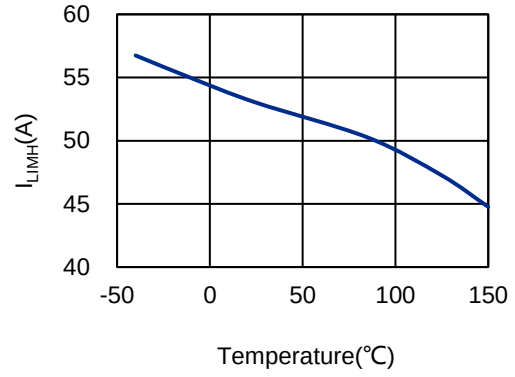


Figure 8-10. I_{LIMH} vs T_A

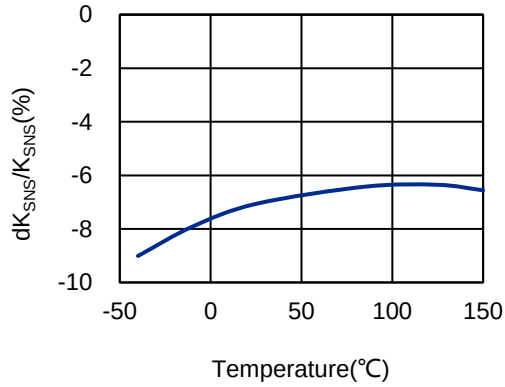


Figure 8-11. dK_{SNS} / K_{SNS} vs T_A ($I_{OUT} = 0.01A$)

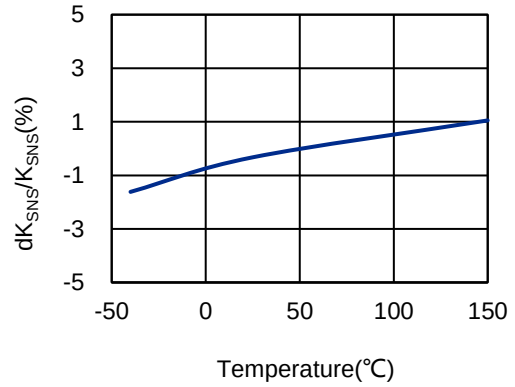


Figure 8-12. dK_{SNS} / K_{SNS} vs T_A ($I_{OUT} = 5A$)

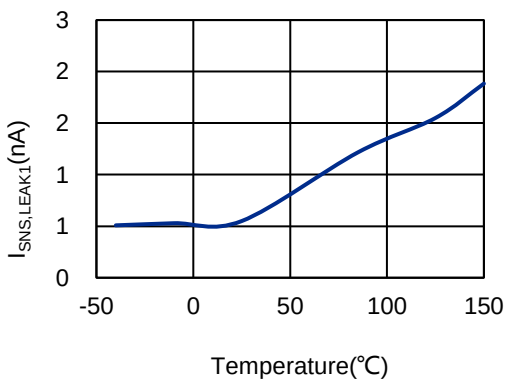


Figure 8-13. $I_{SNS,LEAK1}$ vs T_A

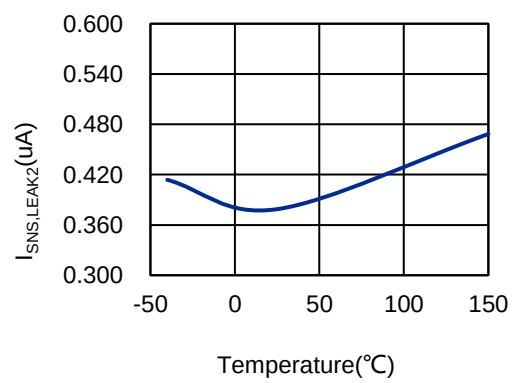


Figure 8-14. $I_{SNS,LEAK2}$ vs T_A

9 Functional Block Diagram

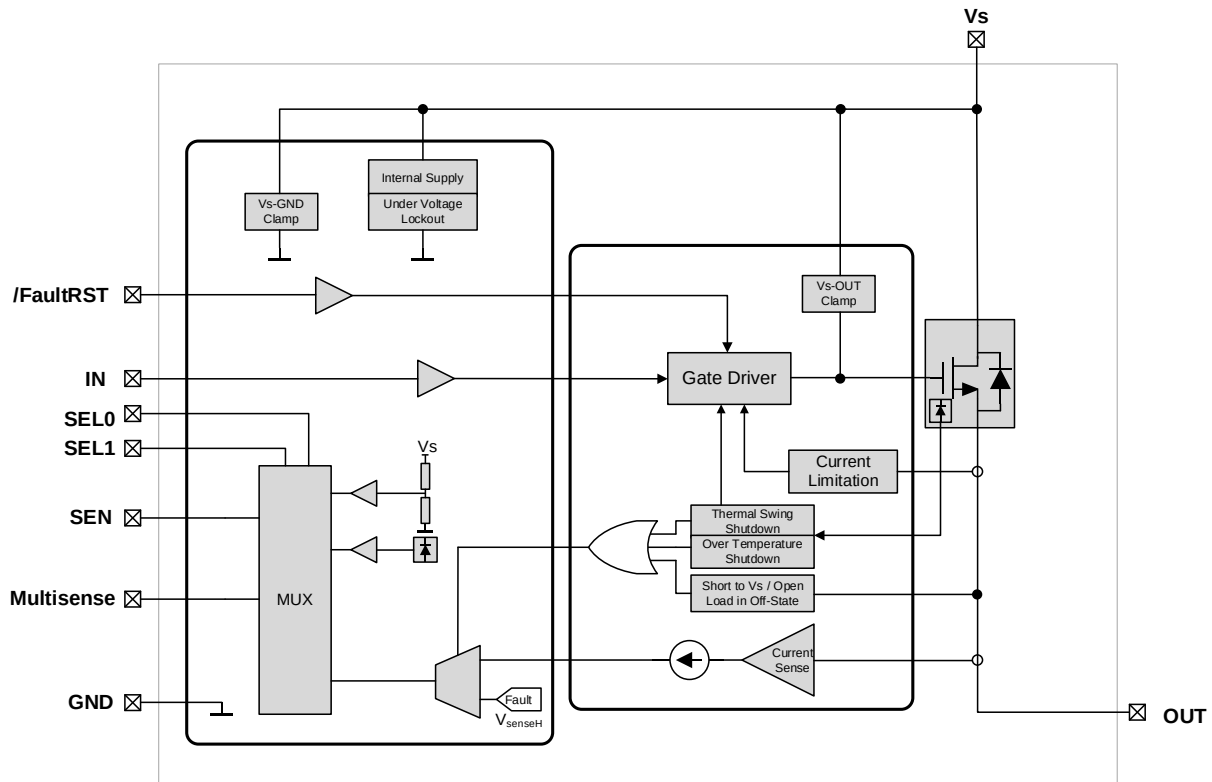


Figure 9-1. Functional Block Diagram

10 Feature Description

10.1 Operating States Diagram

The device has two operating states called 'Normal Operation Mode' and 'Standby Mode', which are decided by input logic signal status and deglitch time, shown as below.

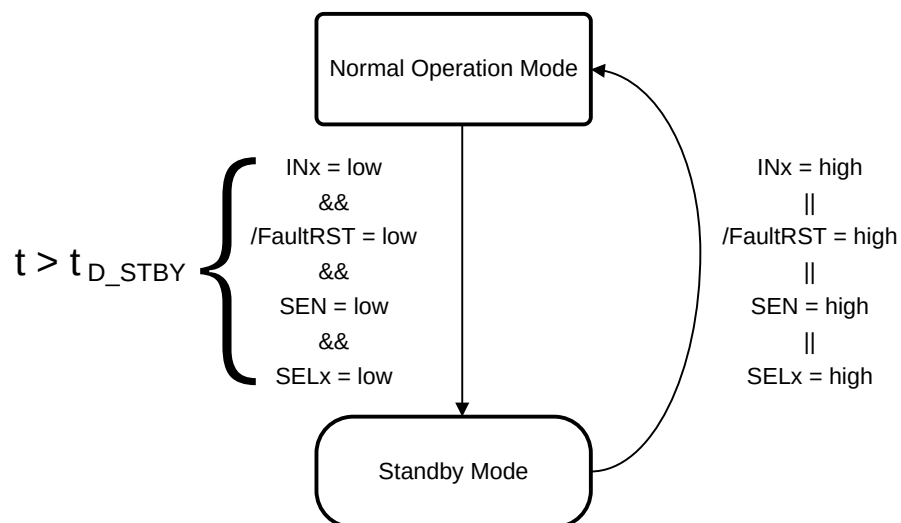


Figure 10-1. Operating States Diagram

10.2 Power Stages

10.2.1 Switching Resistive Loads

When switching resistive loads, the switching time and slew rates are shown in Figure 10-2.

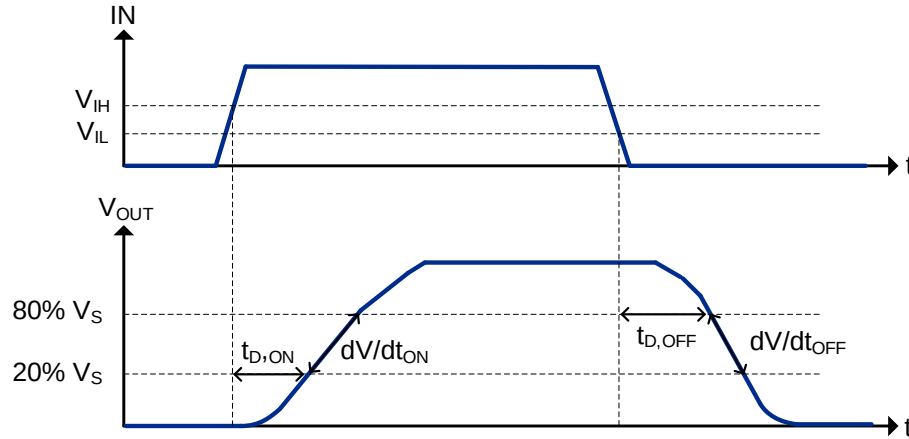


Figure 10-2. Switching Resistive Loads

10.2.2 Switching Inductive Loads

When turning OFF inductive loads with high-side driver, the output voltage V_{OUT} drops to a negative potential, because the inductance tends to maintain the current flow. To prevent the device from damage due to overvoltage, a voltage clamp mechanism is implemented. The clamping mechanism limits the negative output voltage to a safe value. Figure 10-3 shows a concept drawing of implementation.

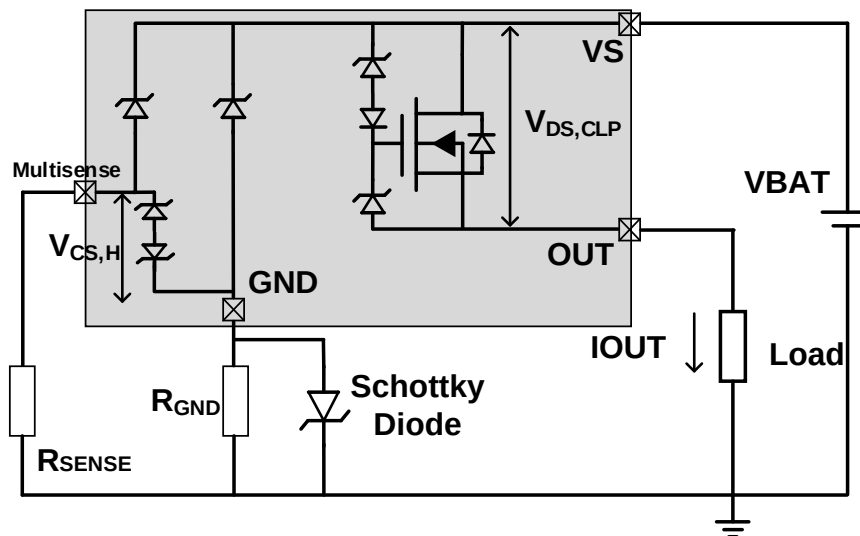


Figure 10-3. Output Clamp Diagram

10.3 MultiSense timings

10.3.1 Current sense mode

MultiSense timings of Current sense mode are shown in Figure 10-4.

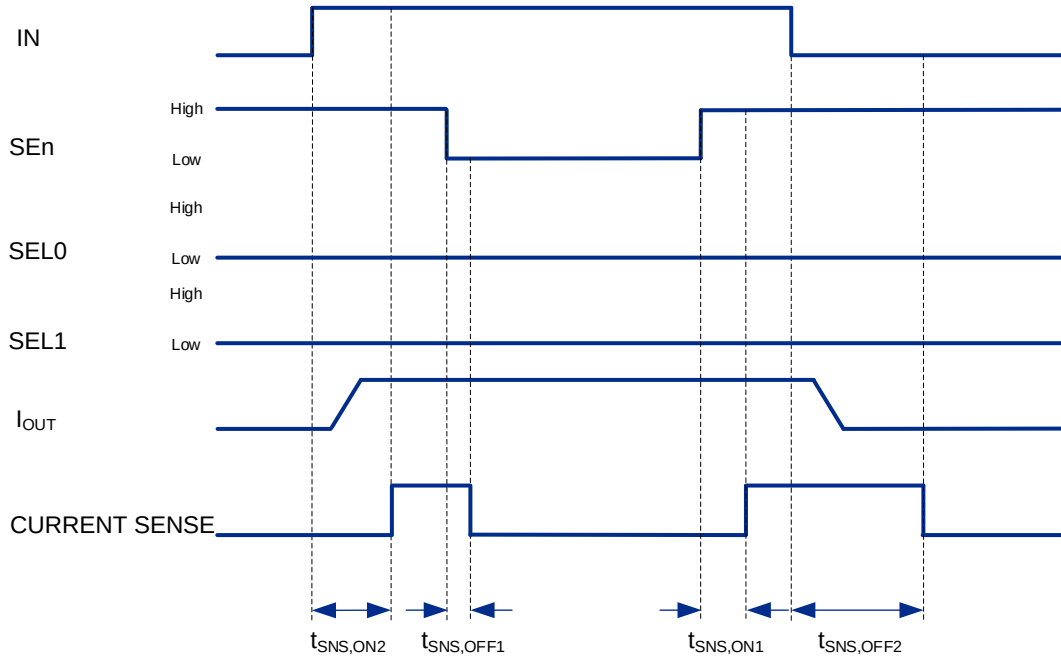


Figure 10-4. MultiSense Timings of Current Sense Mode

10.3.2 Chip temperature and Vs sense mode

MultiSense timings of Chip temperature and Vs sense mode are shown in Figure 10-5

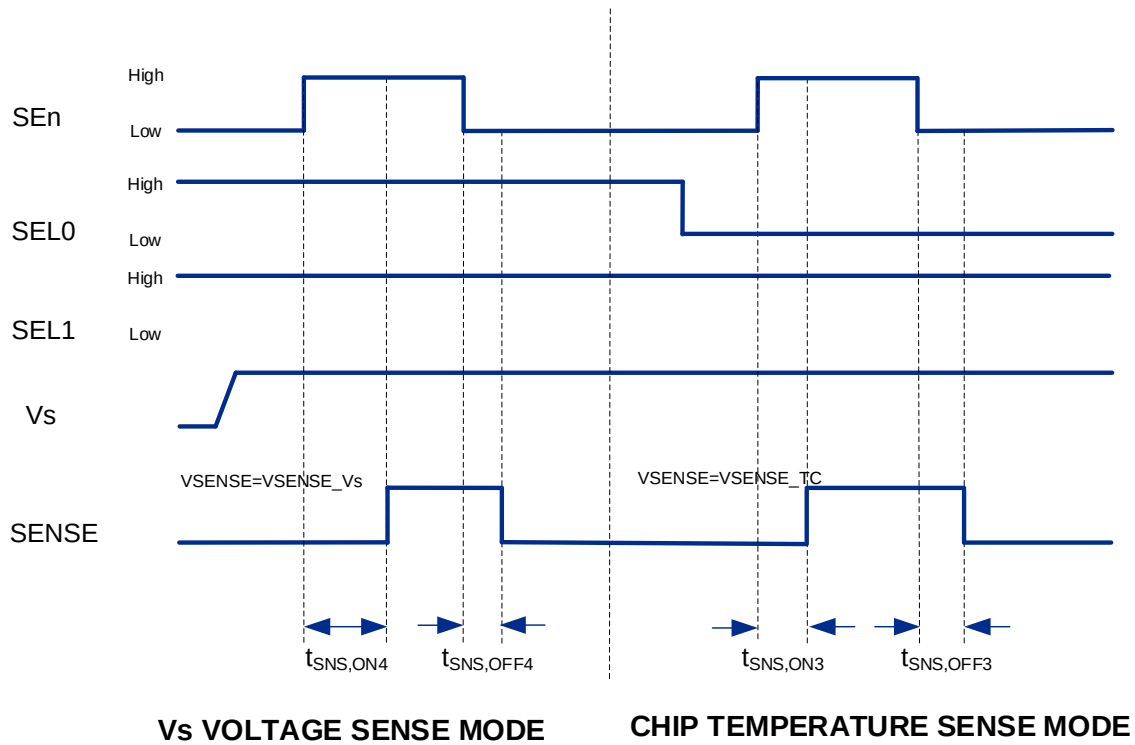


Figure 10-5. MultiSense Timings of Chip Temperature and Vs Sense Mode

10.4 Protections

10.4.1 Overload Protection

The device features protection against overload and short circuit to ground. Its overload threshold decreases as junction temperature rises: at high temperatures, the overload threshold is reduced to prevent device damage. When the supply voltage V_S exceeds 20V-24V, the overload detection current decreases to I_{LIML} as shown in Figure 10-6.

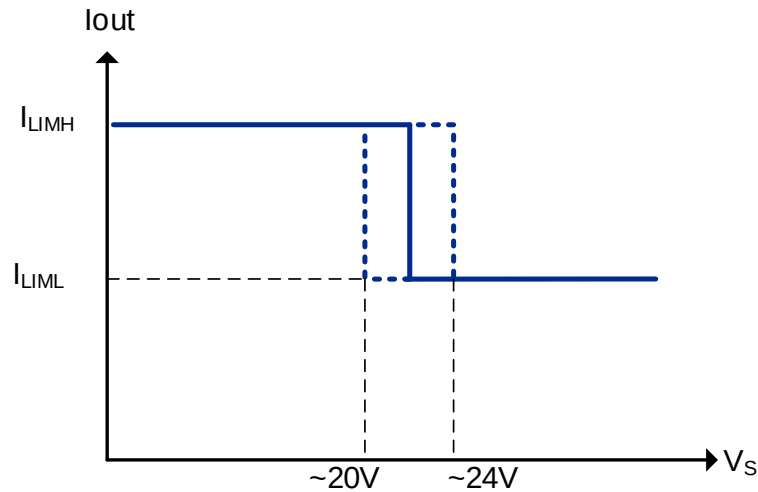


Figure 10-6. The Overload Detection Current Decrease to I_{LIML}

Once the load current meets or exceeds the applicable overload threshold, the output channel is switched off. The channel is allowed to restart, according to the Auto-retry strategy is shown in Figure 10-7.

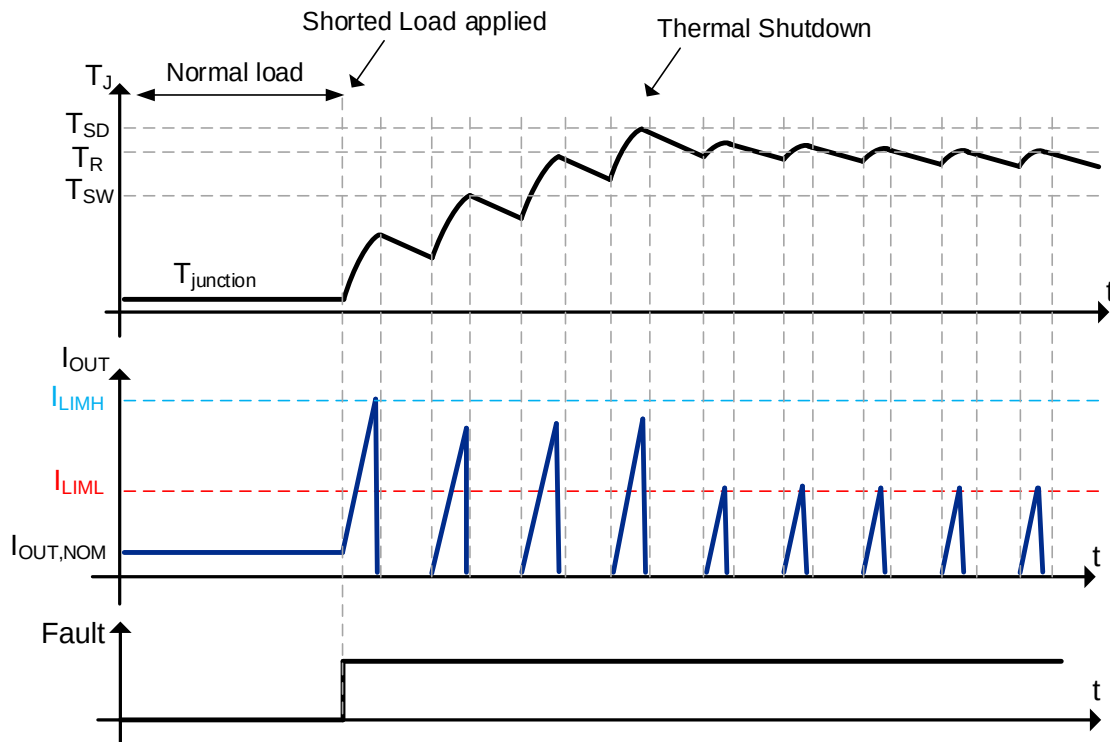


Figure 10-7. Auto-retry Strategy

10.4.2 Undervoltage Protection

Undervoltage protection monitors the supply voltage (V_S). If V_S drops below the minimum undervoltage threshold ($V_{S,UVF}$), the output is turned off regardless of the input status. As soon as V_S is above the operative threshold ($V_{S,UVR}$), the channel is switched ON again as shown in Figure 10-8.

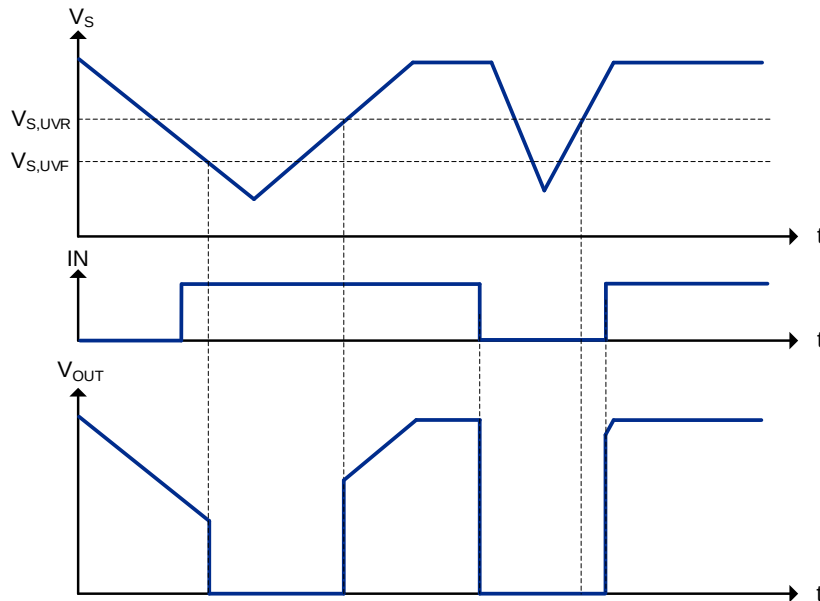


Figure 10-8. V_S Undervoltage Protection

10.4.3 Loss of Ground Protection

In the event of Loss of Ground, the device automatically switches off the power MOSFET, ensuring no current flows into the load. It is recommended to connect a resistor between any logic pins and the microcontroller to ensure the channel switches OFF.

Note: In case any logic pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.

10.4.4 Thermal Swing Shutdown

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing T_{SW} through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level. According to the voltage level on the $/\text{FaultRST}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($/\text{FaultRST} = \text{Low}$) or remains off ($/\text{FaultRST} = \text{High}$). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

10.4.5 Thermal Shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 170°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $/\text{FaultRST}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($/\text{FaultRST} = \text{Low}$) or remains off ($/\text{FaultRST} = \text{High}$).

10.5 Multiplexed Output of Multisense Pin

- Normal output: current sense, chip junction temperature T_J , V_S power supply.
- Fault indication: over load, short to ground, TSW/TSD, open load or short to V_S in OFF-state.

Table 10-1. Multiplexed Output.

Condition			MUX Channel	Multisense Output			
SEN	SEL1	SEL0		Normal Mode	Over Load	Off-State Diagnostic	Negative Output
L	X	X	/	Hi-Z			
H	L	L	Channel Diagnostic	$I_{CS} = I_{out} / K$	H	L	L
H	L	H	/	Hi-Z	H	L	H
H	H	L	Chip Junction Temperature	$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$			
H	H	H	Vs power supply	$V_{SENSE_VS} = V_s / 4$			

10.6 Truth Table of Protections and Diagnostics

Table 10-2. Truth Table of Protections and Diagnostics.

Mode	Conditions	IN	/FaultRST	SEN	SELx	OUT	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low I_{S_STBY} consumption
Normal	Nominal load current: $T_J < 150\text{ }^{\circ}\text{C}$	L	X	Referring to Table 10-2		L	Referring to Table 10-2	/
		H	L			H		Configured in auto-restart mode
		H	H			H		Configured in latch-off mode
Over Load	Over load current: $T_J > T_{SD}$ or $\Delta T_J > T_{SW}$	L	X	Referring to Table 10-2		L	Referring to Table 10-2	/
		H	L			H		Output restarts with temperature protection hysteresis
		H	H			L		Output latches off
Undervoltage	$V_S < V_{S_UVF}$	X	X	X	X	L	Hi-Z	Restart when $V_S > V_{S_UVR}$
Off-state Diagnostic	Short to V_S	L	X	Referring to Table 10-2		H	Referring to Table 10-2	/
	Open Load	L	X			H		External pull-up required
Negative Output Voltage	Inductive loads turn off	L	X	Referring to Table 10-2		< 0 V	Referring to Table 10-2	/

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This is a very simplified example of an application circuit. The function must be verified in the real application.

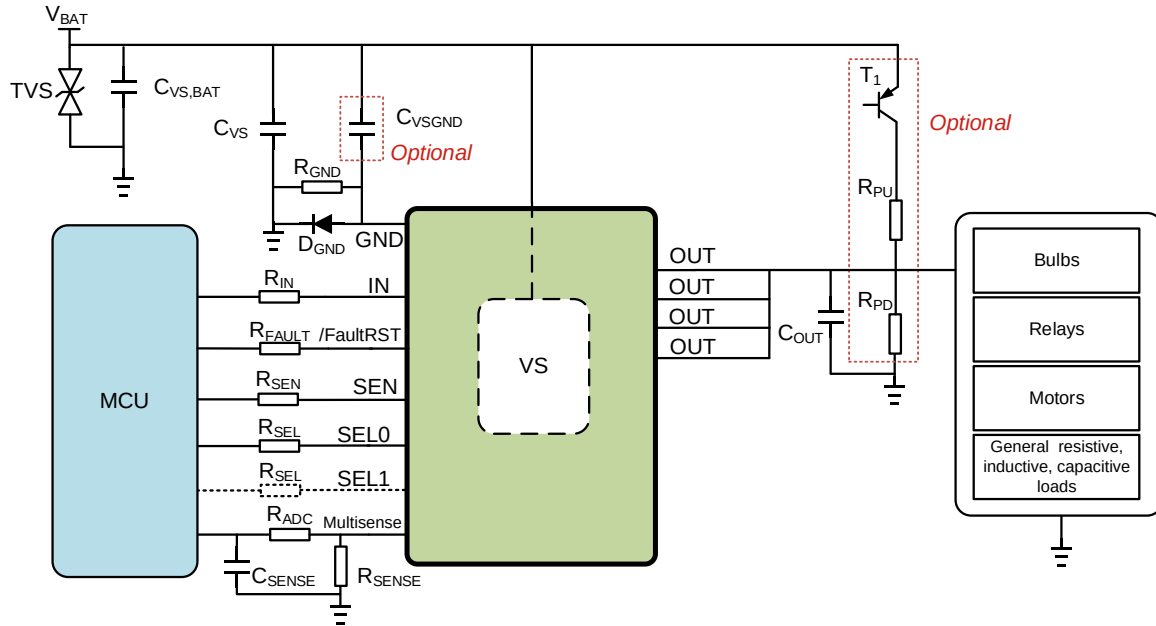


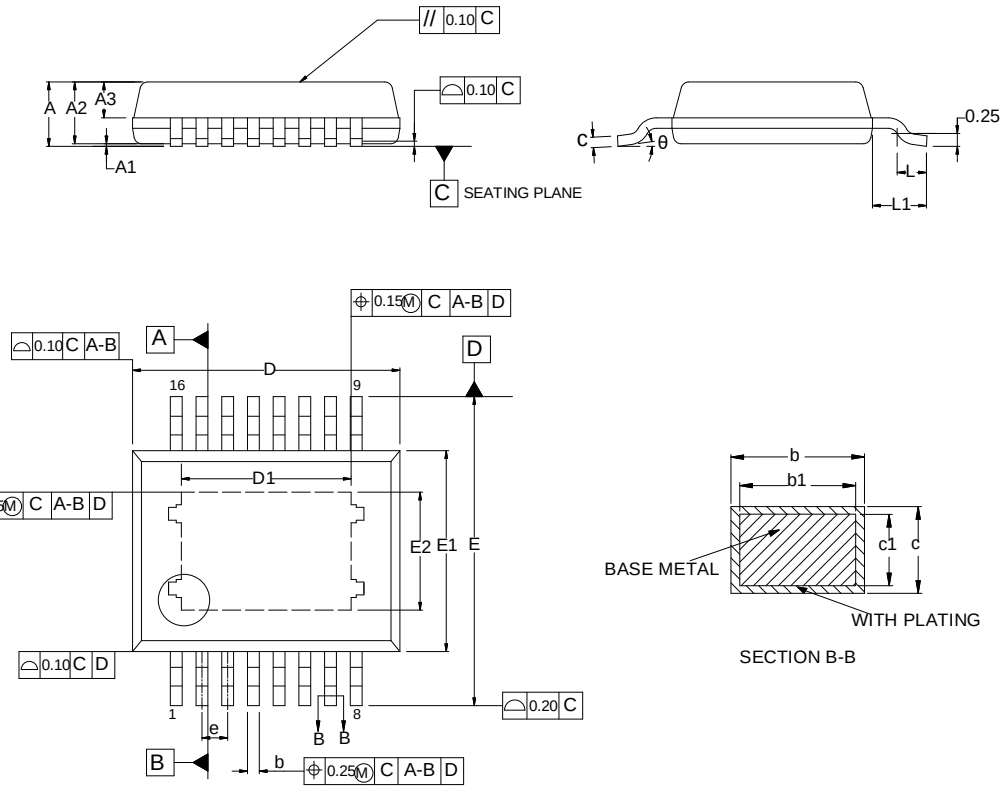
Figure 11-1. Application Diagram

Table 11-1. Suggested Component Values

Reference	Value	Purpose
R _{IN}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{FAULT}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Polarity
R _{SEL}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{SEN}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{PD}	47kΩ	Output pull-down Ensure polarization of the device outputs to distinguish between Open Load and Short to VS in OFF-State
R _{PU}	1.5kΩ	Output pull-up Ensure polarization of the device output during Open Load in OFF-State
C _{OUT}	10nF	Protection of the device output during ESD events
T ₁	-	Switch the battery voltage for Open Load in OFF-State
C _{VS}	100nF	Filtering of voltage spikes on the battery line
C _{VSGND}	47nF	Buffer capacitor for fast transient
TVS	33V	Diode transient voltage suppressor diode
C _{VS,BAT}	-	Filtering / buffer capacitor located at V _{BAT} connector
R _{SENSE}	1.2kΩ	Sense resistor
R _{ADC}	4.7kΩ	Protection of microcontroller ADC input during Overvoltage, Reverse Battery, Loss of Ground
C _{SENSE}	220pF	Sense signal filtering
D _{GND}	-	Reverse polarity protection Schottky diode.
R _{GND}	4.7kΩ	Protection in case of Loss of Battery while driving inductive loads

MECHANICAL DATA

eSSOP-16

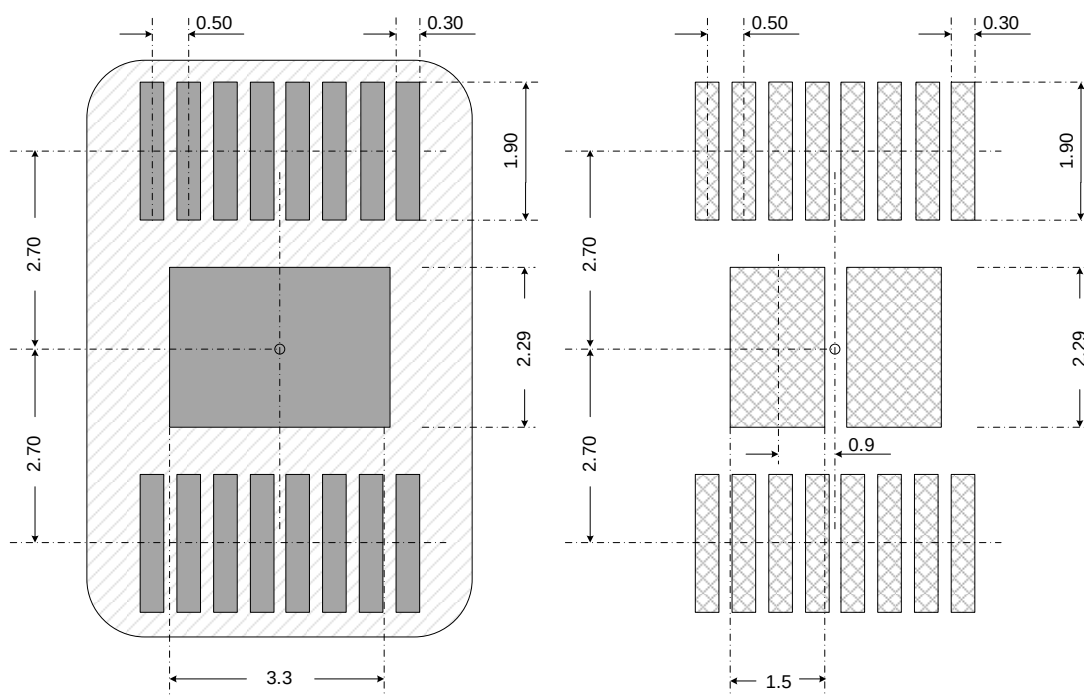


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.40
A1	0.00	—	0.10
A2	1.10	1.20	1.30
A3	0.65	0.70	0.75
b	0.21	—	0.29
b1	0.20	0.23	0.26
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	5.10	5.20	5.30
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.50BSC		
L	0.40	0.57	0.80
L1	1.05REF		
θ	0	—	8°

Size (mm)	E2	D1
U/F Size (mil)		
98*138	2.29±0.30	3.30±0.30

RECOMMENDED FOOTPRINT

eSSOP-16

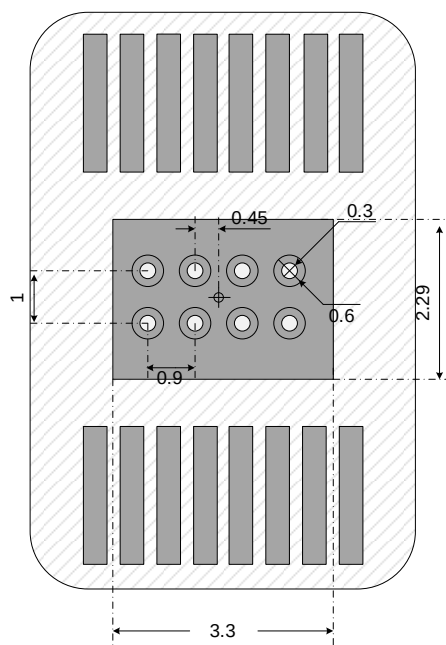


ALL DIMENSIONS ARE IN UNITS MM

Copper

Solder mask

Stencil apertures



ALL DIMENSIONS ARE IN UNITS MM

Copper



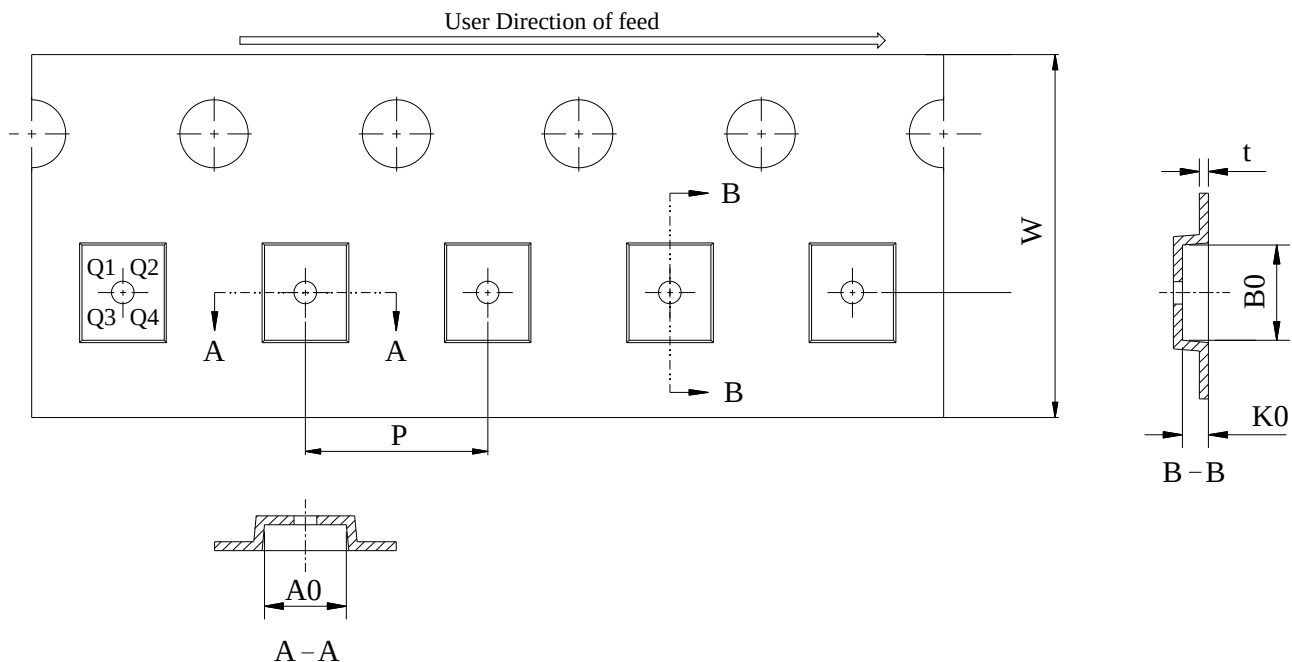
Solder mask



NOTE: Via diameters and positions shall be set according to the actual PCB situation

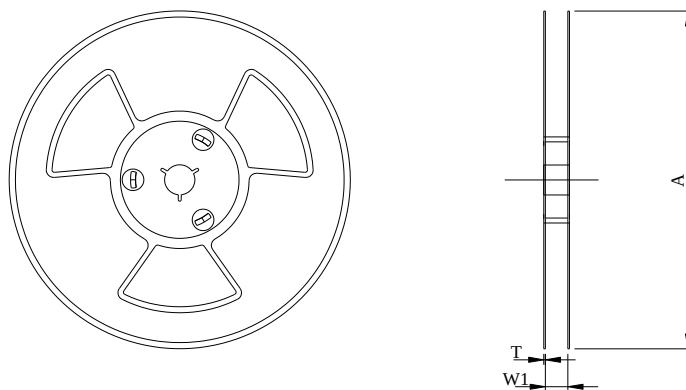
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00+0.30/-0.1	8.00±0.10	6.50±0.10	5.50±0.10	1.75±0.10	0.30±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	12.4 +1/-0	2.1±0.3

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