High Frequency Quasi-Resonant Flyback Controller With GaN Direct Driver

1 Descriptions

SC3023D is a high frequency, quasi-resonant fly-back PWM controller (QR/DCM) with GaN direct driver. The controller with x-cap discharge function integrated high-voltage current source to provide the current during start-up and then turns off during normal operation. The extra low standby power consumption can be obtained.

SC3023D provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. It operates QR and DCM with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

SC3023D provides functions of low start-up current, fast start-up, low standby power consumption. The burst mode with extremely low operation current and significantly reduces standby power consumption to meet the efficiency regulations.

The controller integrates a segmented power supply control circuit, which is especially suitable for applications with a wide output voltage range, reducing power consumption and greatly reducing peripheral devices.

SC3023D integrated the adaptive over current protection (AOCP), which allows controlling the maximum output current from primary-side. The AOCP is specially designed for USB-PD solutions, together with PD controller, such as SC21xx serials. The AOCP can reduce the current stress of secondary synchronous rectification.

The SC3023D offers comprehensive protection to prevent the circuit from damage under abnormal conditions.

Furthermore, the features of frequency jittering and smart driving function can minimize the noise and improve EMI performance.

2 Features

- Integrated GaN direct driver
- Integrated high-voltage startup circuit with brown in/out detection
- Integrated x-cap discharge function
- Internal Soft Start
- Integrated segmented power supply control circuit for extra-wide output range
- Ultra-low operation current @Burst mode/Fault Mode
- Adaptive over current protection
- Adaptive loop gain compensation
- Frequency Jitter for EMI improvement
- Driver capability: 50mA/-500mA
- Valley switching operation @ QR/DCM
- Burst Mode @ Light Load & No Load
- Internal over temperature protection
- Support external NTC for OTP
- Comprehensive Protection
  - VDD over voltage protection
  - VDD under voltage protection
  - Cycle by cycle current limiting
  - Two level over current protection
  - Output over voltage protection
  - Output short protection
  - Over Load protection
- SSOP10 package available

3 Applications

- USB-PD and QC Chargers
- AC-DC adapters for Portable Devices

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4 Device Information

ORDER NUMBER	X-Cap Discharge	PACKAGE	BODY SIZE
SC3023DSGER	N	SSOP10	6.0mm x 4.9mm x 1.55mm

SC3023DXSGER Functional Table

ORDER NUMBER	SC3023D
Maximum Frequency	175KHz
DRV Source Current	+50mA/-500mA
X-Cap Discharge	/
ZCD OVP	A
OLP	A
AOCP	/
Brown In/Out	A
External OTP	A

A: Auto-recovery;

Y: The feature is enabled

/ : The feature is not enabled

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5 Typical Application Circuit

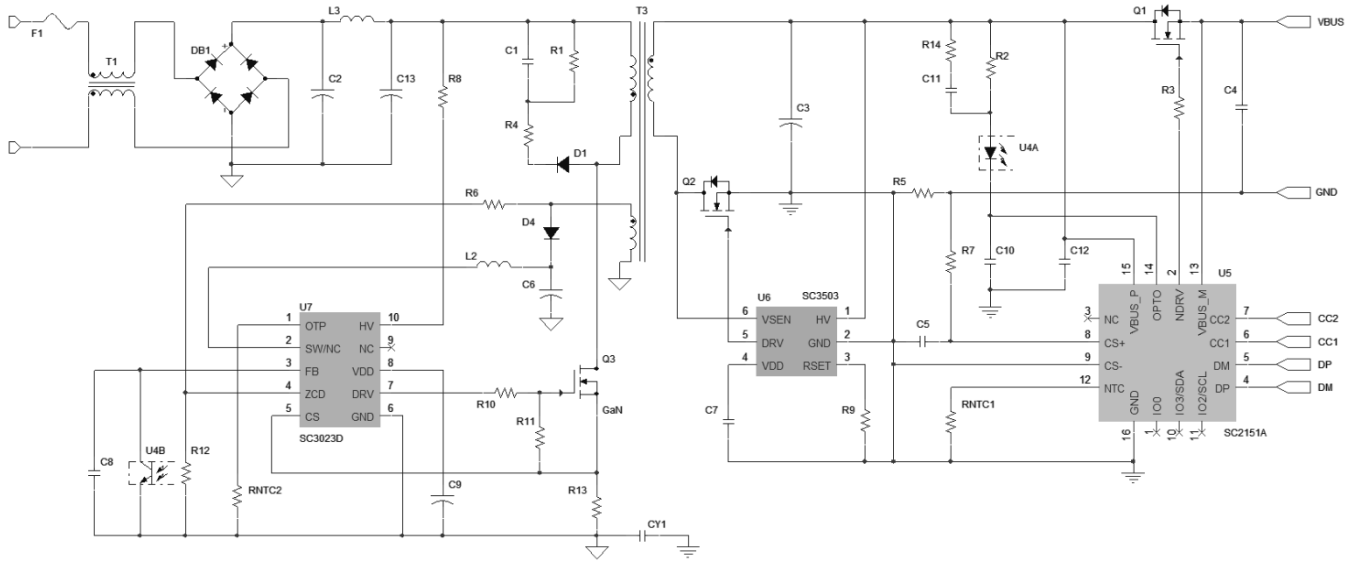

Fig. 1 SC3023D Typical application circuit

6 Terminal Configuration and Functions

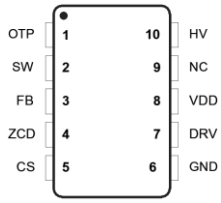

Fig. 2 Top view (SSOP10)

TERMINAL		I/O	DESCRIPTION
SC3023D	NAME		
1	OTP	O	External OTP pin. This pin is typically connected to an NTC resistor.
2	SW	PWR	Booster circuit switch control.
3	FB	I	Secondary side voltage feedback.
4	ZCD	I	Voltage Sense. The ZCD voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage.
5	CS	I	Current Sense. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation.
6	GND	PWR	Power Ground.
7	DRV	O	Output to drive the external power GaN.
8	VDD	PWR	Power Supply.
9	NC		No connection.
10	HV	PWR	Connected to the line via resistors and diodes for startup and x-cap discharge, this pin allows the brown in/out detection as well.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Item	Description	Min.	Typ.	Max.	UNIT
Voltage range at terminals (2)	HV to GND	-0.3		700	V
	VDD、SW to GND	-0.3		+44	V
	DRV to GND	-0.3		+10	V
	Other Pins to GND	-0.3		+6.5	V
T_J	Operating Junction temperature range	-40		150	°C
T_{stg}	Storage temperature range	-65		150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE (1)		SSOP10 (6.0mm x 4.9mm)	UNIT
θ_{JA}	Junction to ambient thermal resistance	150	°C/W
θ_{JC}	Junction to case resistance	40	°C/W

(1) Measured on JESD51-7, 2-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2) (HV pin)	-1	+1	kV
	Human body model (HBM) ESD stress voltage (2) (All pins except HV)	-2	+2	kV
	Charged device model (CDM) ESD stress voltage (3)	-1	+1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.4 Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD to GND	VDD voltage range to GND	10		V_{DDOVP}	V
SW to GND	SW voltage range to GND		V_{DD}+0.7V		V
DRV to CS	DRV voltage range to CS	0		6.5	V
Others to GND	Other pins voltage range to GND	0		5.5	V
C_{VDD}	VDD Capacitor	4.7		22	uF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

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7.5 Electrical Characteristics

VDD=15V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hight Voltage Supply and X-cap Discharge (HV)						
I_{HV_VDD1}	HV Start-up current-1	V_{DD} ≤ 0.5V, V_{HV}>150V			1.0	mA
I_{HV_VDD2}	HV Start-up current-2	V_{DD} = V_{DDON} - 0.5V, V_{HV}>150V		2.9		mA
I_{HVLK}	HV pin leakage current after startup	VDD> V_{DDON}, HV = 400V			15	uA
V_{HVBIN}	Brown-in threshold voltage	DC input voltage	97	105	113	V
V_{HVBOUT}	Brown-out threshold voltage	DC input voltage	84	90	96	V
T_{BOUT}	Debounce time of brown out	V_{TH} < V_{TH_BOUT}		64		ms
T_{XDET}	X-Cap discharge Detection Delay time			80		ms
I_{DHGX}	X-Cap discharge current			5		mA
Voltage Supply (VDD)						
V_{DDON}	VDD on threshold voltage		14.2	15.0	15.8	V
V_{DDOFF}	VDD off threshold voltage		7.9	8.4	8.9	V
$V_{DDHOLDL}$	VDD holding entry point voltage			8.9		V
$V_{DDHOLDH}$	VDD holding exit point voltage			9.7		V
$V_{DDBSTOFF}$	Booster regulation voltage			11.2		V
$V_{DDBSTON}$	The booster circuit starts to work			9.7		V
I_{VDD}	Operating current	Cload = 1nF, Fsw=175KHz		1.6		mA
I_{VDDBT}	Burst mode current	V_{FB} < 0.5V		230	310	uA
$I_{VDDFAULT}$	Hold up current in fault mode			80		uA
T_{DFAULT}	Hold on time in fault mode			2		s
$I_{VDDFAULT1}$	VDD sink current, BO	After T_{DFAULT} 2S		1.6		mA
V_{DDOVP}	VDD OVP			40.0		V
I_{VDDOVP}	VDD OVP sink current	V_{DD} > V_{DDOVP}		5		mA
T_{VDDOVP}	VDD OVP debounce time			160		us
Zero Voltage Detection (ZCD)						
V_{ZCDOVP}	ZCD OVP		4.27	4.45	4.63	V
N_{ZCDOVP}	ZCD OVP debounce counter			4		Cycles
I_{ZCDMAX}	Maximum ZCD Clamp source current		1			mA
$V_{ZCDCLAMP}$	ZCD Clamp voltage	$I_{ZCDCLAMP}$=1.0mA		-120		mV
T_{LEBOVP}	Leading edge blanking time		0.69	0.77	0.85	us
V_{ZCDH}	ZCD valley detection rising edge	V_{DRV} = low		0.40		V
$I_{LINECOMPST}$	Line voltage compensation threshold ZCD clamp current			135		uA
$K_{LINECOMP}$	The ratio of line voltage compensation			0.3		
$R_{LINECOMP}$				2.5		kΩ

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Feedback Voltage (FB)						
V_{FBOPEN}	Open Loop Voltage	I_{FB} = 0		3.0		V
R_{FB}	FB pull-up resistor			10		kΩ
V_{FBOLP}	OLP or FB open loop			2.5		V
T_{FBOLP}	Debounce time of FB open loop protection	V_{FB} > 2.8V		64		ms
V_{FBBST}	FB voltage when DRV stops pulsing		0.4			V
$V_{FBBSTHYS}$	V_{FBBSTH} hysteresis voltage			0.1		V
Current Sense (CS)						
T_{SSCS}	Soft start time of CS threshold	After start up and no trigger protection		4.1		ms
$V_{CSLIMIT}$	Cycle by cycle current limited		0.47	0.495	0.52	V
T_{LEBCBC}	Leading edge blanking time			275		ns
V_{CS_SSCP}	Secondary rectifier short protection			0.9		V
N_{CS_SSCP}	Secondary rectifier short circuit protection debounce counter			3		Cycles
$T_{LEBSSCP}$	Leading edge blanking time			165		ns
V_{CSMIN}	CS minimum voltage			0.1		V
ΔV_{CS}	CS jitter			±5		%
T_{JIT}	CS jitter cycle			240		cycles
Gate Driver (DRV)						
V_{OL}	Driver output low voltage	VDD=15V			0.2	V
V_{OH}	Driver output high voltage	VDD=15V, V_{OH}=V_{DRV}-Vcs	5.5	5.9	6.3	V
$I_{DRVSOURCE}$	DRV maximum source current	V_{DRV} < 1V		100		mA
$I_{DRVSINK}$	DRV maximum sink current	V_{DRV} > V_{OH} - 0.5V		500		mA
T_R	Output rising time 0.5V ~ 5.4V	CL = 1nF		100		ns
T_F	Output falling time 5.4V ~ 0.5V	CL = 1nF		30		ns
External OTP (OTP)						
I_{OTP}	Current source for OTP		95	110	123	uA
V_{OTP}	External OTP trigger voltage		0.47	0.5	0.53	V
T_{OTPP}	External OTP detection period			10		ms
T_{OTPDEB}	OTP debounce time			560		us
Internal Boost Circuit (SW)						
I_{SWOFF}	Boost circuit turn off current			0.1	0.12	A
$T_{SWONMAX}$	Boost maximum on time			1.30		us
$T_{SWOFFMIN}$	Boost minimum off time			0.50		us
Oscillator for Switching Frequency						
F_{SW}	Switching frequency		165	175	185	kHz
F_{SWMIN}	Minimum frequency			25		kHz
T_{OFFMAX}	Maximum off time			35		us
T_{ONMAX}	Maximum on time			25		us

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Internal Over-Temperature Protection (OTP)				
OTP_H	OTP Temperature		140	℃
OTP_{HYS}	OTP Hysteresis		20	℃

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8 Functional Block Diagram

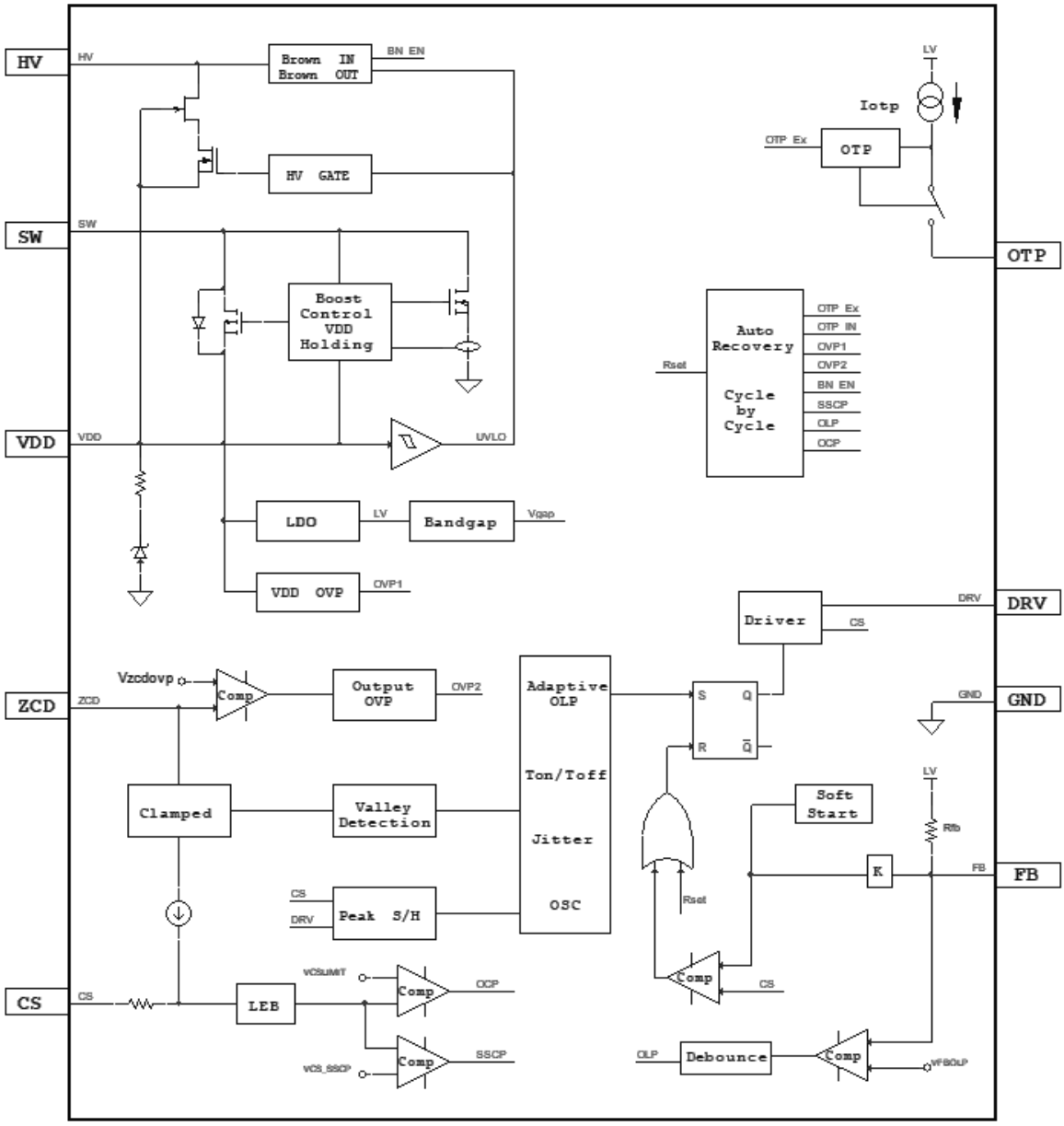

Fig.3 Function Block Diagram

9 Feature Description

SC3023D is designed for USB-PD solutions, together with PD controller, such as SC21xx serials. SC3023D is specifically designed for GaN power systems with GaN direct driver, that is a high frequency, quasi-resonant fly-back PWM controller (QR/DCM).

The controller integrates a boost circuit, which is especially suitable for applications with a wide output voltage range, reducing power consumption and greatly reducing peripheral devices.

SC3023D integrated the adaptive over current protection (AOCP), which allows controlling the maximum output current from primary-side. When PD OC fails, AOCP can reduce the current stress of secondary synchronous rectification to meet the requirements of LPS.

The SC3023D offers comprehensive protection to prevent the circuit from damage under abnormal conditions.

9.1 Start-up

The SC3023D features a HV pin to provide fast start-up. The start-up device will be turned on during start-up and be turned off during normal operation so as to shorten start-up time and to eliminate power loss in this path after start-up.

It also incorporates brownout detection and line removal detection. The HV pin must be connected directly to the ac line in order for the X2 discharge circuit to function correctly. A resistor in series with the pin should be used to protect the pin during EMC or surge testing. A low value resistor should be used 5kΩ to reduce the voltage offset during start−up.

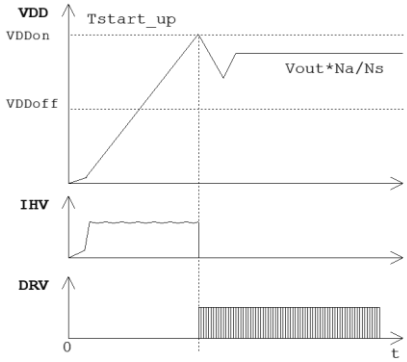

Fig. 3 VDD start-up waveform

An integrated T_{SSCS} soft start is used in the chip to reduce the voltage and current stress. During the soft start-up period, the Vcs threshold gradually rises from 0.1V to 0.5V. Once the secondary side regulation loop is stable, the Vcs is controlled by the feedback loop.

9.2 VDD UVLO

A hysteresis Under Voltage Lock Out (UVLO) comparator is implemented in SC3023D. The turn-on and turn-off thresholds are fixed at V_{DDON} and V_{DDOFF} respectively. This hysteresis ensures that the VDD capacitor can be small enough during start-up. A large hysteresis is essential to ensure the IC work properly during the start-up period, even for a small VDD capacitor.

9.3 VDD Holding Mode

After the system starts, the VDD capacitor can be charged by the auxiliary winding. There are some operation condition changes (load changes, output voltage adjustment, burst mode), may lead the primary side DRV stop working when the output value is higher than the set value. Furthermore, the VDD voltage will be lower than V_{DDOFF} and the system will stop. To avoid this situation, a VDD holding circuitry is designed, which starts working when VDD drops below $V_{DDHOLDL}$ and stops working when VDD rises above $V_{DDHOLDH}$. The working process is shown in below:

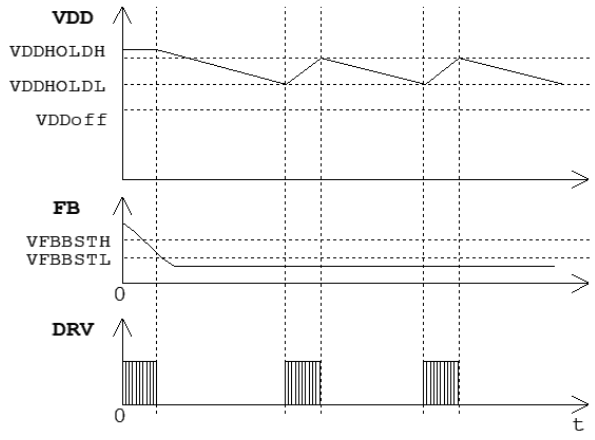

Fig. 4 VDD holding circuitry

9.4 Segmented Power Supply Control Circuit for VDD Power Supply

In some applications with a wide output voltage range, especially for chargers that need to support PPS, the output voltage range is 3.3V ~ 21V. In order to meet the power supply of the SSR controller, additional circuits need to be

added. This makes the circuit complicated and increases system power consumption, which is very unfavorable. The SC3023D integrates a boost circuit, and only needs to add an inductor, which can also guarantee the power supply of VDD under the low output voltage of auxiliary winding. The working process of this circuit is shown below:

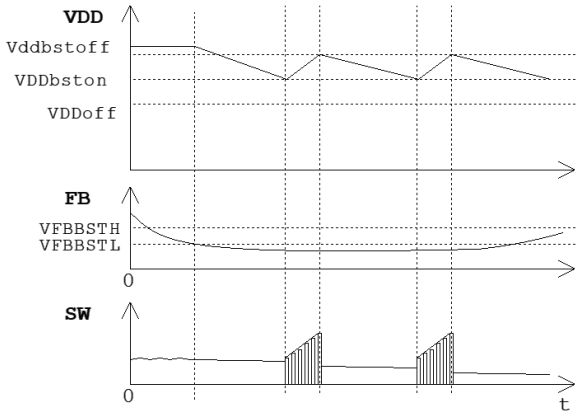

Fig. 5 The Boost Circuit

9.5 Brown IN/OUT Detection and X-Cap Discharge

The Brown IN/OUT function is implemented through HV pin. When HV pin voltage rises above V_{HVBIN}, the IC starts working, and it stops working when HV pin voltage decreases below V_{HVBOUT}. When HV voltage drops below V_{HVBOUT}, a brownout timer is enabled. The controller is disabled if HV voltage doesn't exceed V_{HVBOUT} before brownout timer expires.

SC3023D integrates X-cap discharge function. When detected the voltage on HV pin drops and no rising edge detected after T_{XDET}, it is considered that the AC power is disconnected, and then the X-cap discharge function is enabled. The HV pin generates a source current of 5mA to discharge the X-Cap until the voltage drops to a very low level.

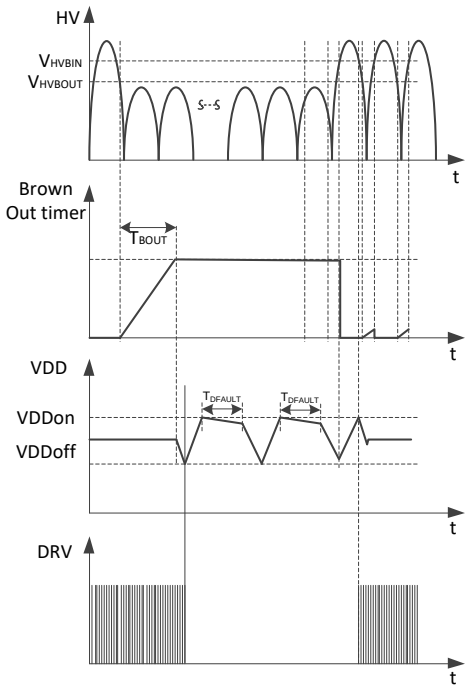

Fig. 6 Brown In/Out detection

9.6 Operation Mode

SC3023D is a high frequency, quasi-resonant fly-back PWM controller (QR/DCM) provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to maximum switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

When the system is under no load or extremely light load, the IC will operate in BURST mode to reduce power dissipation. In this condition, switching loss of the GaN is the main power dissipation. The DRV will be disabled immediately if V_{FB} drops below V_{FBBSTL}. When V_{FB} rises up to V_{FBBSTH}, the DRV starts to pulse again.

When under medium load condition, the system operates in green mode (DCM or QR). The switching frequency will linearly increase from F_{SWMIN} to maximum switching frequency. That means, when load increases, the switching frequency is increased.

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9.7 GaN driver

SC3023D integrates GaN FET direct driver. The high voltage level between Gate and Source of GaN FET is about 6V. The patented drive technology can offset the voltage rise caused by the sampling resistor connected between source of GaN FET and the power ground, so the driver voltage can be constant at 6V. In this way, the peripheral driver devices can be simplified, the efficiency can be maximized, and the reliability is greatly improved.

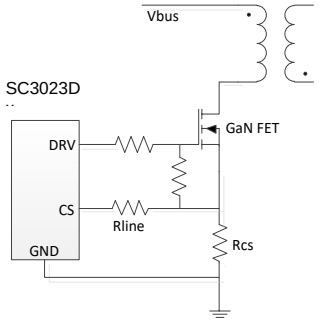

Fig. 7 GaN FET direct driver

9.8 Valley Switching

ZCD pin can detect the freewheel information on the secondary side. In QR mode, when the voltage of ZCD turns to a negative value, it means that after a quarter of the resonant period, the primary GaN can be turned on, and valley opening helps to improve efficiency and improve EMI performance. In order to achieve the best valley opening, it can be achieved by appropriately adjusting T_{DZCD} and T_{DDRV}, where T_{DPG} is an internal fixed delay. T_{DZCD} can be adjusted by connecting a small capacitor in parallel with $R_{ZCDDWON}$. The recommended value is 10 ~ 11pF. T_{DDDRV} can be adjusted by connecting DRV resistors in series.

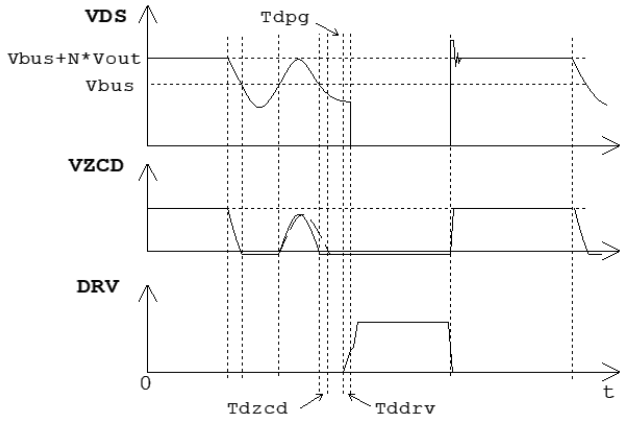

Fig. 7 Valley Switching

9.9 Auto-Recovery after Failure

SC3023D has complete protection functions, such as: VDD over voltage protection, VDD under voltage lock out, two level over current protection, output over voltage protection, output short protection, over Load protection, brown IN/Out with auto-recovery, line voltage over voltage protection. Unless otherwise specified, these protections are auto-recovery. After the protection is triggered, the system enters the protection mode, and the VDD power consumption is reduced. After the T_{DFAULT} delay, the VDD sink current increases until V_{DDOFF}, and VDD starts the restart process. The detailed process is as follows.

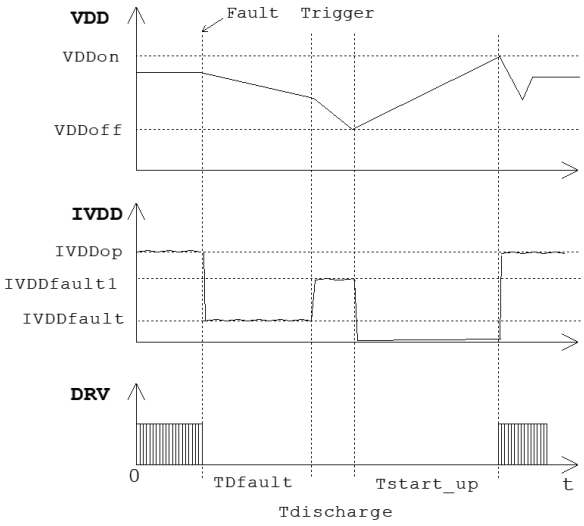

Fig. 8 Auto-Recovery Process

9.10 VDD OVP

When the VDD voltage is higher than the V_{DDOVP} threshold voltage at least T_{VDDOVP}, in the case of a sink current of

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I_{VDDOVP}, DRV will be shut down. The VDD OVP function is an auto-recovery protection.

9.11 ZCD OVP

The auxiliary winding demagnetization voltage V_{AUX} is proportional to the output voltage. V_{ZCD} sensing the V_{AUX} via the divided resistors can be used to sample the output voltage after some blanking time. The output over voltage can be calculated as:

$$\frac{V_{AUX} * R_{ZCD-DOWN}}{R_{ZCD-DOWN} + R_{ZCD-UP}} > V_{ZCDOVP}$$

$$\frac{V_{AUX}}{N_A} = \frac{V_{OUT}}{N_S}$$

The blanking time can ignore the voltage ringing from leakage inductance of transformer. With the increase of V_{FB}, the blanking time is T_{LEBOVP}.

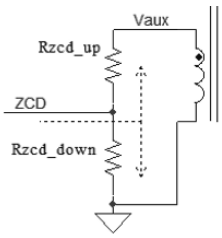

Fig. 9 ZCD Over Voltage Protection

9.12 Over Current Protection

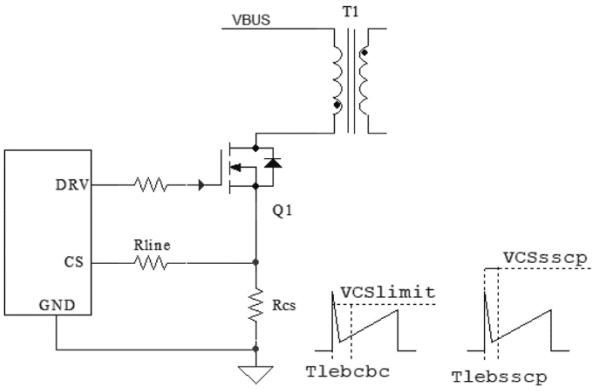

Fig. 10 LEB of OCP

Two levels of overcurrent protection are integrated. One is cycle-by-cycle current limiting for overload protection. V_{CSSSCP} is the fast protection for the case of secondary rectifier rectification shorted. The overcurrent protection and its shielding time are shown in the figure below.

SC3023D integrated the adaptive over current protection (AOCP), which allows controlling the maximum output current from primary-side in width output voltage range.

9.13 Adaptive Over Load Protection (AOLP)

An adaptive over load protection is implemented in the SC3023D. When the voltage of VFB is higher than V_{FBOLP} and lasts for a period of time T_{FBOLP}, overload protection will be triggered. In particular, when the voltage of VFB is higher than V_{FBOLP}, if the peak voltage of ZCD pin is lower than V_{ZCDH}, the delay of T_{FBOLP} will be shortened. When V_{ZCD} is lower than V_{ZCDH}, the coefficient K is less than 1. The AOLP can reduce the power loss when secondary side is shorted.

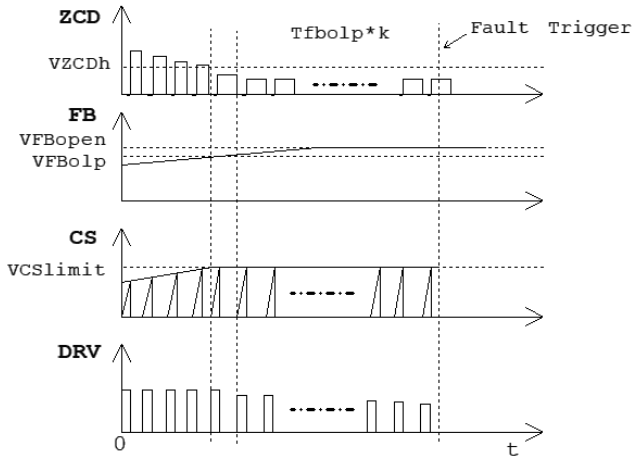

Fig. 11 Adaptive Over Load Protection

9.14 On-Chip OTP

An internal OTP circuit is embedded inside to provide the worst-case protection for SC3023D. When the chip temperature rises higher than the OTP_H, the controller will be disabled and works in the failure mode until the chip is cooled down below the hysteresis OTP_{HYS}.

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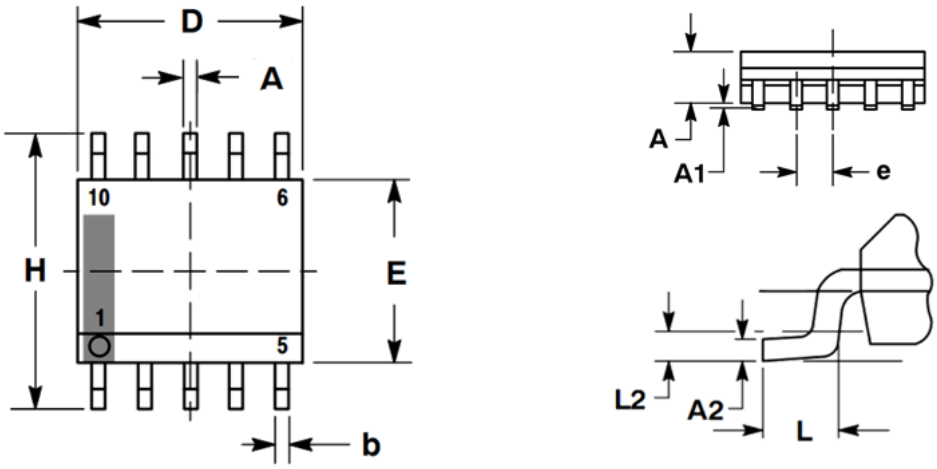
MECHANICAL DATA

SSOP10 (6.0mmx4.9mmx1.55mm)



DIM	Millimeters	
	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A2	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
L	0.40	1.27
L2	0.27 BSC	

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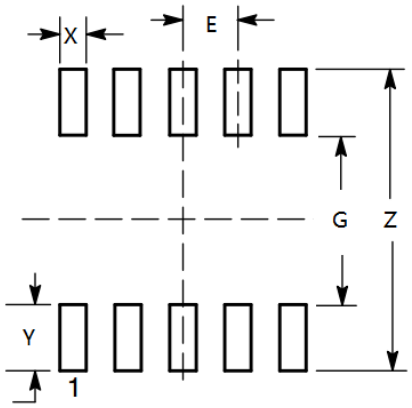
RECOMMENDED FOOTPRINT

Example Board Layout



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)
Value	6.90/0.272	4.40/0.173	0.58/0.023	1.25/0.049	1.00/0.039

NOTES:

A. Publication IPC-7351 is recommended for alternate designs
B. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

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