High-Efficiency CrM Boost PFC Controller

1 Descriptions

The SC3202 is a Power Factor Correction (PFC) controller which is applied to boost converter. It features High performance by using multi-mode control strategy. At heavy load or full load, it operates in Critical conduction Mode (CrM). When load decreases, it operates in Discontinuous Conduction Mode (DCM) with valley switching and lower frequency for high efficiency. And at no load, the IC will operate in Burst Mode to reduce power consumption and minimize audio noise. Using SC3202 together with the flyback controller and secondary synchronous rectifier controller, high efficiency over full load can be achieved, and extremely low standby power consumption of system can easily meet the efficiency regulations.

Benefit from the SC3202, the PFC stage will obtain nearly unity power factor and sinusoidal line input current with few external components.

SC3202 offers comprehensive protections to prevent the circuit from damage under abnormal conditions.

SOT23-6/SOP8 package is provided to simplified user's design and reduced system cost

2 Features

- Unity power factor and low THD
- Critical conduction mode (CrM)
- Valley switching operation with frequency fold-back
- Boost Follow Mode (SC3202A&SC3202C)
- PFC enable (SC3202C)
- High Efficiency and Ultra-low no-load input power
- Burst mode with noise immunity
- Comprehensive Protection
  - VDD under voltage protection
  - Cycle-by-cycle current limit
  - Output over-voltage protection
  - Inductor current CCM protection
  - Over-temperature protection
- VCC Range: from 9 V to 30 V
- SOT23-6/SOP8 package

3 Applications

- USB-PD chargers
- AC-DC adapters for Portable Devices
- Desktop computing and TV/Monitor
- LED drivers
- Industrial and communication power supplies
- Power tools chargers
- E-bike chargers

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4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3202SBER	SOT23-6	2.92mm x 2.80mm x 1.25mm
SC3202ASBER	SOT23-6	2.92mm x 2.80mm x 1.25mm
SC3202CSEER	SOP8	6.00mm x 4.90mm x 1.55mm

SC3202 Functional Table

ORDER NUMBER	SC3202	SC3202A	SC3202C
Package	SOT23-6	SOT23-6	SOP8
Maximum Frequency	320kHz	320kHz	320kHz
Boost Follow	N	Y	Y
ZCD OVP	N	N	N
Brown In/Out	N	N	Y
PFC EN Function	N	N	Y
T_{MAXON}@ Low Line	12.8μs	12.8μs	16.5μs

Y: The feature is enabled;

N: The feature is disabled.

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5 Typical Application Circuit

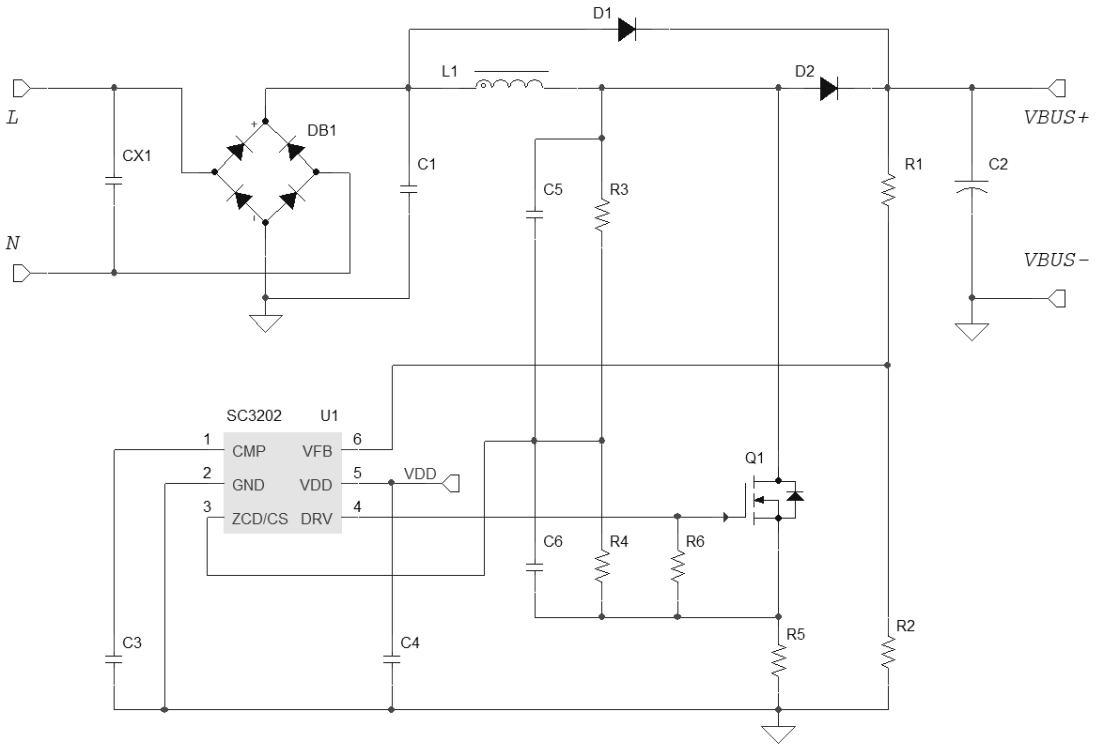


Fig. 1 Typical application circuit of SC3202 (with second winding on boost inductor)

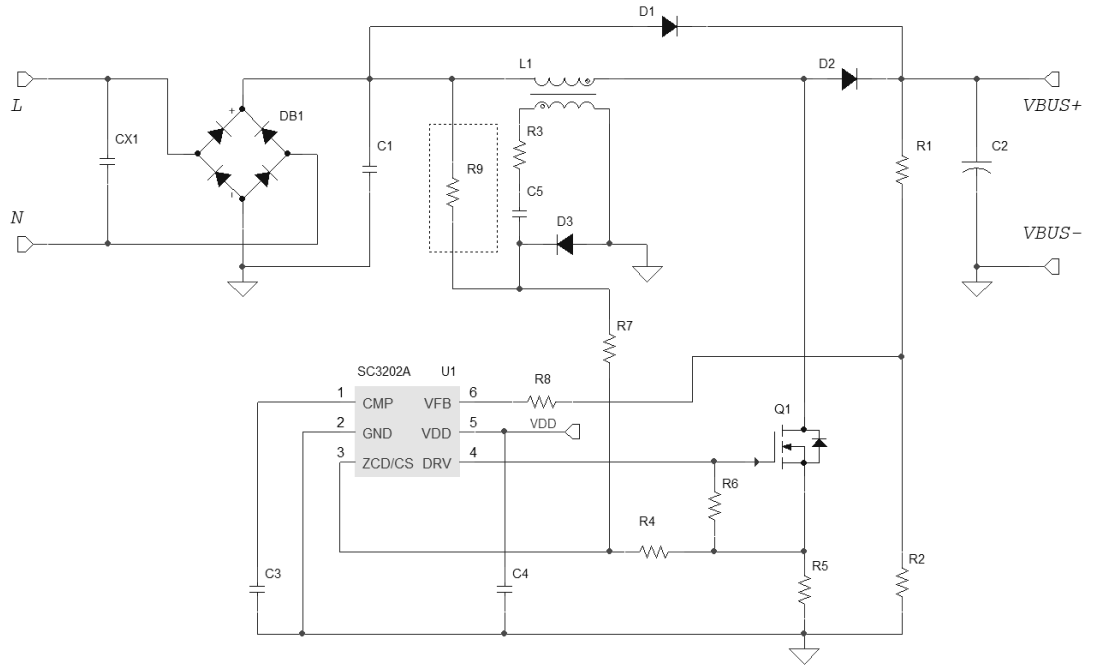


Fig. 2 Typical application circuit of SC3202A (R9 is added)

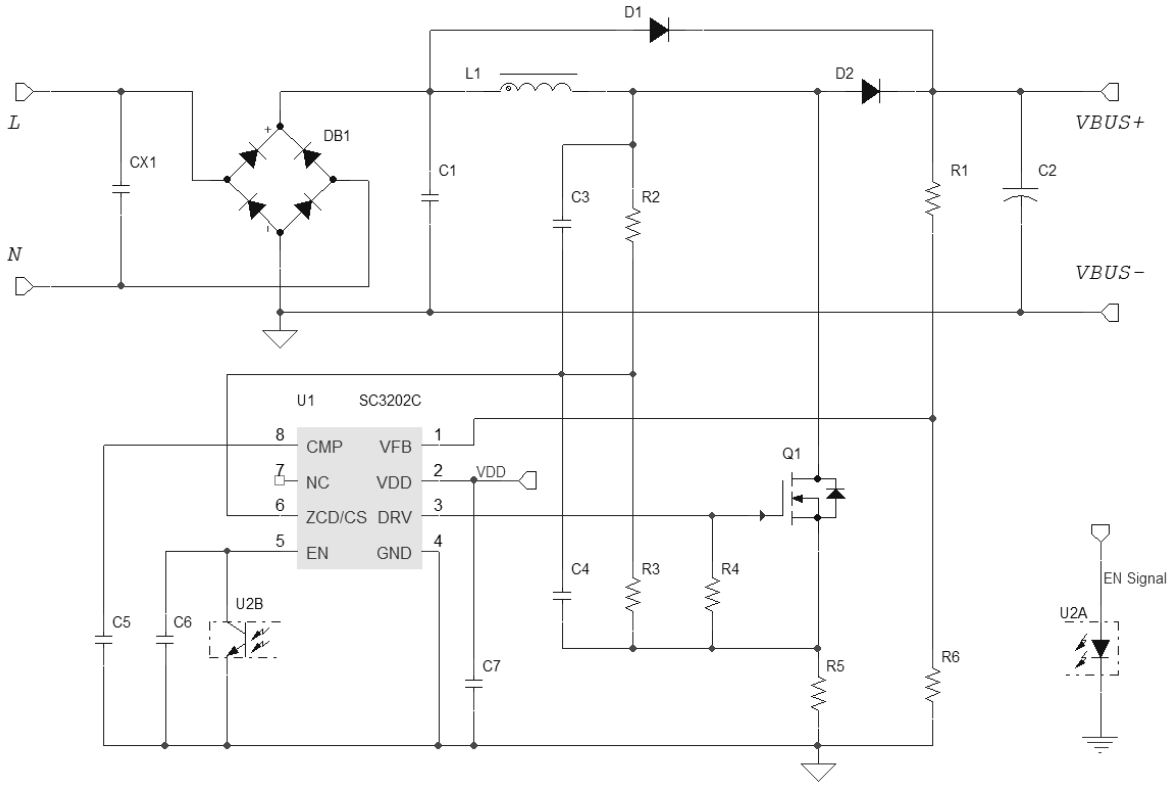
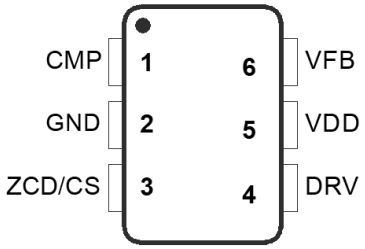
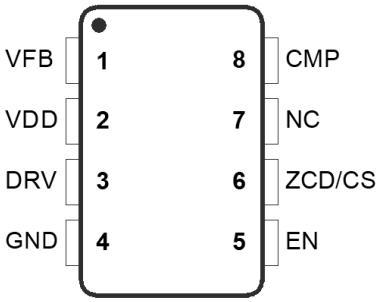


Fig. 3 Typical application circuit of SC3202C (without second winding on boost inductor)

6 Terminal Configuration and Functions



SOT23-6



SOP8(SC3202C Only)

TOP VIEW

TERMINAL			I/O	DESCRIPTION
NUMBER (SOT23-6)	NUMBER (SOP8)	NAME		
1	8	CMP	I/O	Compensated net.
2	4	GND	PWR	Power Ground.
3	6	ZCD/CS	I	Current Sense. This pin connects to a current-sense resistor to sense the MOSFET current for Peak-Current-Mode control for output regulation. Voltage Sense. The ZCD voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage.
4	3	DRV	O	Totem-pole output to drive the external power MOSFET, Maximum Voltage is clamped to 12.5V.
5	2	VDD	PWR	Power Supply.
6	1	VFB	I	Voltage feedback.
	5	EN	O	A high level or open circuit on this pin disables the controller and reduces I_{VDD} current for low standby power.
	7	NC	/	No Connect.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

ITEM	DESCRIPTION	MIN	MAX	Unit
Voltage range at terminals(2)	VDD to GND	-0.3	+33	V
	DRV to GND	-0.3	+18	V
	Other Pins to GND	-0.3	+6.5	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2)	-4	+4	kV
	Charged device model (CDM) ESD stress voltage (3)	-1.5	+1.5	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD to GND	VDD voltage range to GND	9		30	V
DRV to GND	DRV voltage range to GND	0		15	V
Others to GND	Other pins voltage range to GND	0		5.0	V
C_{VDD}	VDD Capacitor	4.7		22	μF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

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7.4 Thermal Information

THERMAL RESISTANCE (1)		SOT23-6	SOP8	UNIT
θ_{JA}	Junction to ambient thermal resistance	220	150	°C/W
θ_{JC}	Junction to case resistance	110	40	°C/W

(1) Measured on JESD51-7, 2-layer PCB.

7.5 Electrical Characteristics

VDD=15V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Supply (VDD)						
V_{DDON}	VDD on threshold voltage		10.20	10.70	11.20	V
V_{DDOFF}	VDD off threshold voltage		8.40	8.85	9.30	V
I_{VDDST}	VDD start up current	$V_{VDD} < V_{DDON}$ - 0.1V		31	50	μA
$I_{VDDFAULT}$	Hold up current in fault mode			130	200	μA
I_{VDDBT}	Burst mode current	V_{COMP} < 0.3V		130	200	μA
I_{VDDQ}	Operating current	V_{VDD} = 12V, No PWM, DRV pin floating		0.5		mA
I_{VDD50k}	Operating current	V_{VDD} = 12V, 50kHz, DRV pin floating		0.68		mA
Gate Driver (DRV) for MOSFET						
V_{OL}	Driver output low voltage	VDD=15V, I_{DRV}=20mA			0.5	V
V_{OH}	Driver output high voltage	VDD=15V	10.0	12.5	15.0	V
T_R	DRV rising time	CL = 1nF, 1.5V to 9V		130		ns
T_F	DRV falling time	CL = 1nF, 9V to 1.5V		22		ns
Feedback Voltage (VFB)						
V_{FBREF}	Feedback voltage reference		2.465	2.5	2.535	V
V_{FBOVP1}	FB fast stop OVP		2.645	2.7	2.755	V
K_{FBOVP2}(1)	FB fast stop OVP2 Voltage Ratio in Boost follow Mode	V_{FBOVP2} / V_{FBREF}		120		%
R_{FBOVP}	The discharge resistor in CMP	FB OVP trigger		4.7		kΩ
V_{FBUVP}	VFB under voltage protection		0.375	0.4	0.425	V
V_{FBUVP_HYS}(1)	VFB under voltage protection hysteresis			0.1		V
I_{FBDN}	VFB pin sink current			45	120	nA
$I_{FBLOWLINE}$	VFB pin source current	Boost follow mode	6.8	7.5	8.2	μA
Compensation (CMP)						
G_{GM1}	Compensates for amplification gain			60		μS
$I_{CMPSORMAX}$	CMP maximum source current			46		μA
$I_{CMPSINKMAX}$	CMP maximum sink current			125		μA
$V_{CMPBSTIN}$	Burst Mode voltage threshold		0.278	0.3	0.322	V
$V_{CMPBSTHYS}$	Burst Mode voltage hysteresis			80		mV

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$V_{CMPCLAMP}$	Clamp voltage of CMP		3.18	3.3	3.42	V
Zero Voltage Detection and Current Sense (ZCD/CS)						
T_{ZCDBLK}	Zero current detection blanking time			500		ns
V_{ZCDH}	Zero current detect voltage threshold			7.0		mV
V_{ZCDHYS}	ZCD voltage hysteresis			7.0		mV
$I_{ZCDOPENDET}$	ZCD pin source current			-128		nA
V_{CSOCP1}	Cycle by cycle current limited		0.385	0.405	0.425	V
$T_{LEBOCP1}$	OCP1 leading edge blanking time			450		ns
V_{CSOCP2}	Current limited level 2		0.58	0.61	0.64	V
$T_{LEBOCP2}$	OCP2 leading edge blanking time			260		ns
T_{OCPDT1}	OCP2 delay time			500		μs
T_{OCPDT2}	OCP2 trigger 2 times delay time			1		ms
V_{ZCDBIN}	ZCD brown in DC voltage	SC3202C	0.263	0.280	0.297	V
V_{ZCDBIN_HYS}	ZCD brown in DC voltage hysteresis	SC3202C		38		mV
T_{BOUT}	Delay time of brown out protection	SC3202C		50		ms
T_{MAXOFF}	Maximum off time			260		μs
$V_{ZCDHLINE}$	ZCD voltage threshold of high line			0.650		V
$V_{ZCDLLINE}$	ZCD voltage threshold of low line			0.620		V
T_{MAXONL}	Maximum on-time at low line	SC3202/SC3202A	12.20	12.80	13.40	μs
		SC3202C	15.90	16.50	17.10	
T_{MAXONH}	Maximum on-time at high line	SC3202/SC3202A		4.4		μs
		SC3202C		5.8		
Enable (EN)						
V_{ENH}	PFC disable voltage threshold	SC3202C	2			V
V_{ENL}	PFC enable voltage threshold	SC3202C			0.6	V
V_{EN_HYS}	PFC enable voltage hysteresis	SC3202C		1.1		V
R_{EN}	Pull-up Resistance	SC3202C		1		MegΩ
T_{EN}	EN Filter time	SC3202C		75		μs
T_{DIS}	DIS Filter time	SC3202C		75		μs
Internal Over-Temperature Protection (OTP)						
OTP_H	OTP Temperature			145		℃
OTP_{HYS}	OTP Hysteresis			24		℃

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7.6 Typical Characteristics

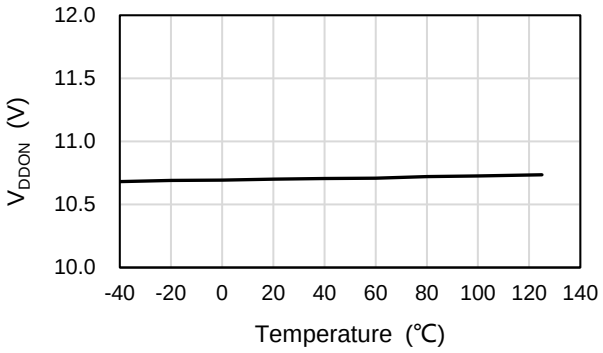

Figure 2. V_{DDON} vs Temperature

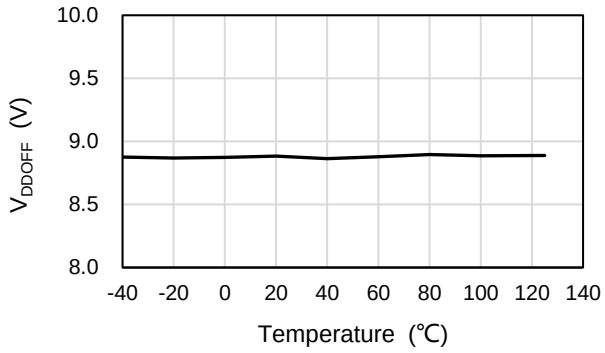

Figure 3. V_{DDOFF} vs Temperature

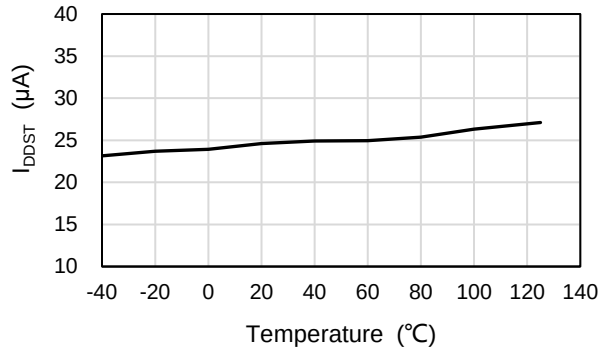

Figure 4. I_{DDST} vs Temperature

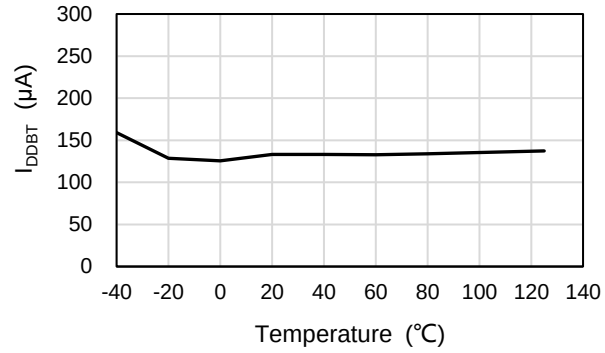

Figure 5. I_{DDBT} vs Temperature

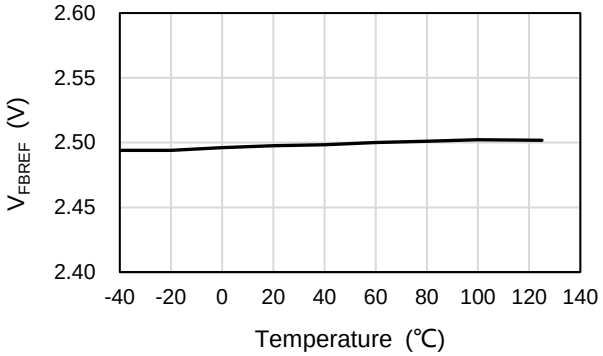

Figure 6. V_{FBREF} vs Temperature

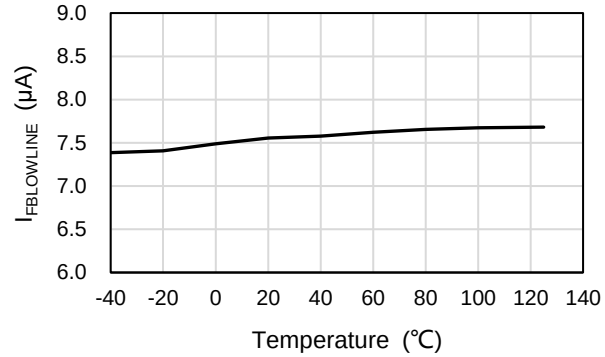

Figure 7. $I_{FBLOWLINE}$ vs Temperature

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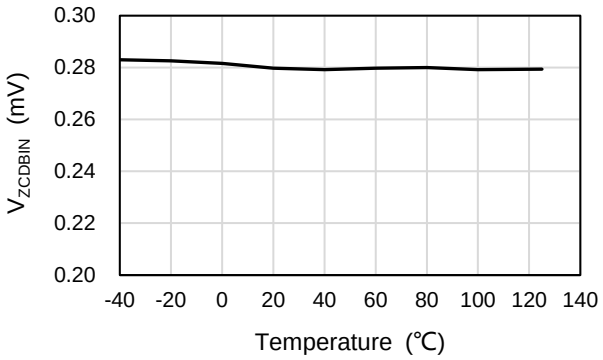

Figure 8. V_{ZCDBIN} vs Temperature

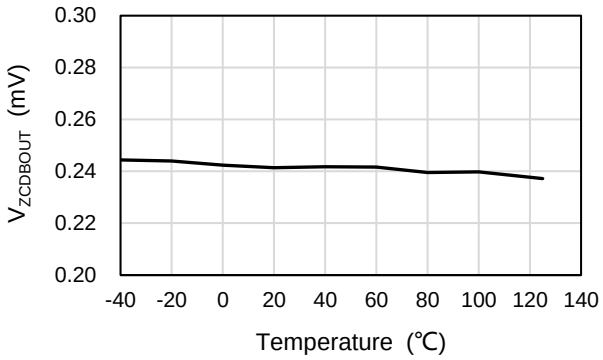

Figure 9. $V_{ZCDBOUT}$ vs Temperature

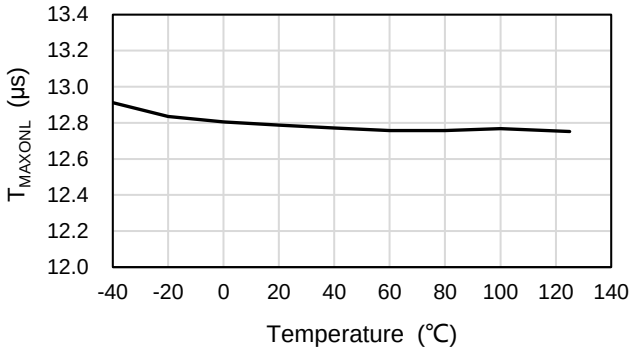

Figure 10. T_{MAXONL} vs Temperature

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8 Functional Block Diagram

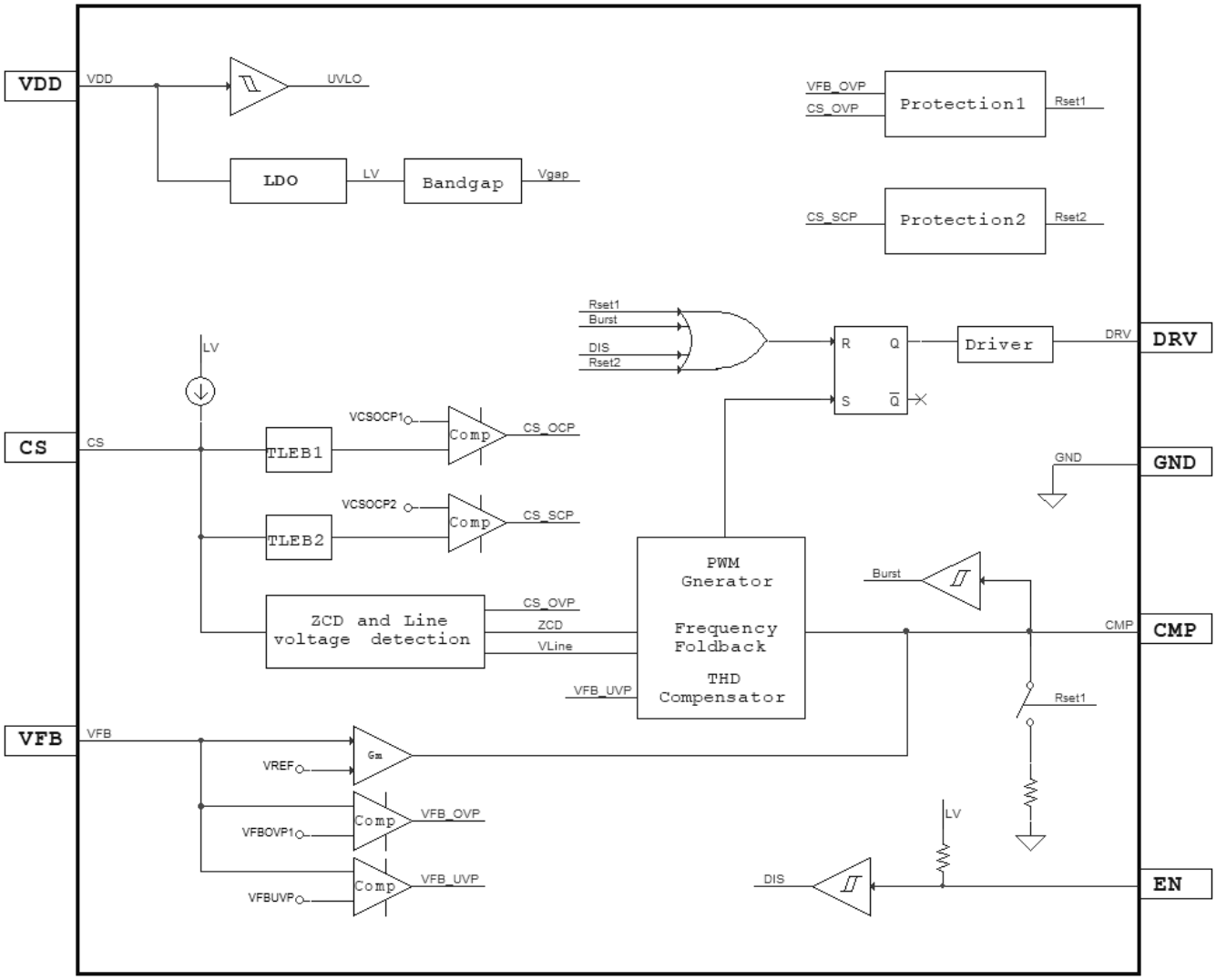

Fig.3 Function Block Diagram

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9 Feature Description

The SC3202 controller is designed to optimize the efficiency of Boost PFC stage throughout the load range. For 75w to 150w power system, it followed with the flyback controller SC302x/SC305x and synchronous rectification controller SC350x to provide an isolated AC-DC power system. For higher power system such as 150w to 300w AC-DC power supply, it can be used together with the LLC controller to provide a complete solution.

The combined power supply is designed to meet tough efficiency and standby power requirements without the need for an auxiliary converter and with no need to switch off the PFC under light load conditions. It allows designers to meet modern green power standards with a simpler and lower system cost of power supply.

The SC3202 controller contains numbers of features designed to maximize operating efficiency across the entire range of Line and Load. Multi-mode control strategy allows SC3202 to operate in Critical conduction Mode (CrM) at heavy power load and then transition into Discontinuous Conduction Mode (DCM) as load decreases without compromising line current harmonics or power factor. Light-load efficiency and standby power are further enhanced by transitioning automatically to a burst mode of operation. During the burst OFF periods, the controller powers down most of its internal circuits to minimize controller power consumption.

The SC3202 controller offers comprehensive protections to prevent the circuit from damage under abnormal conditions, such as cycle-by-cycle current limit, over-current protection, output over-voltage protection, overtemperature protection and supply undervoltage lockout (UVLO).

Due to the high performance of SC3202, the PFC stage will obtain nearly unity power factor and sinusoidal line input current, which can meet mains harmonics requirements such as EN61000-3-2.

The Boost PFC stage can provide relatively stable output voltage during a wide AC input range, which simplifies the design difficulty of LLC or flyback.

9.1 CrM/DCM Operation

The SC3202 controller operates in CrM or DCM with valley turn-on, as shown in figure 4 and figure 5. In this working mode, the switching loss of the system is greatly reduced, so as to obtain higher efficiency.

The SC3202 samples the information of input voltage and load to match different on-time and frequency, and then determines whether the system works in CrM or DCM.

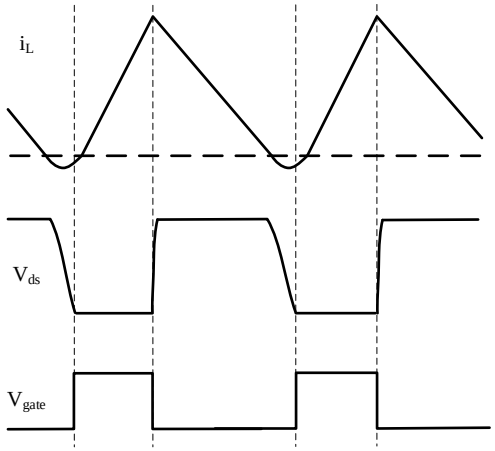

Fig. 4 Valley Switching Operation in CrM

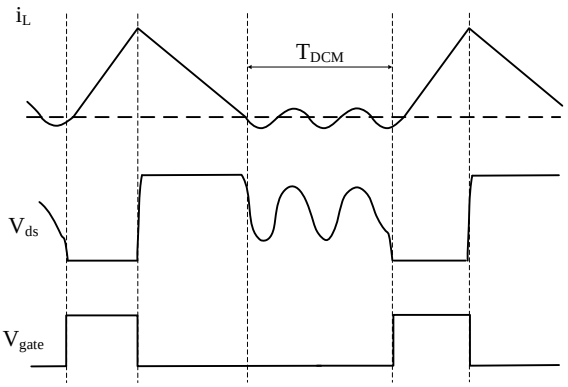

Fig. 5 Valley Switching Operation in DCM

Line current distortion is particularly severe during the transition from the first valley (CrM) to the second valley (DCM) operation while the input voltage is low. In this region, the first valley duration is extended by the clamping action of the power switch body diode. In this region Line current is reduced when switching on the first valley (CrM), because the inductor current is negative at the start of the on period. The reduction in Line current is not observed for second or subsequent valley (DCM) operation because the inductor current starts the on period from zero. The SC3202

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optimizes THD by avoiding CrM/DCM transitions across a Line cycle.

9.2 THD Compensation

When the conduction time is relatively constant, the peak value of the inductance current is linear with the input voltage, and the average value of the input current is approximately linear with the peak value. Therefore, the input current can follow the input voltage to realize the unit power factor. Ideally, the input voltage and input current waveform in half line cycle is shown in Figure 6.

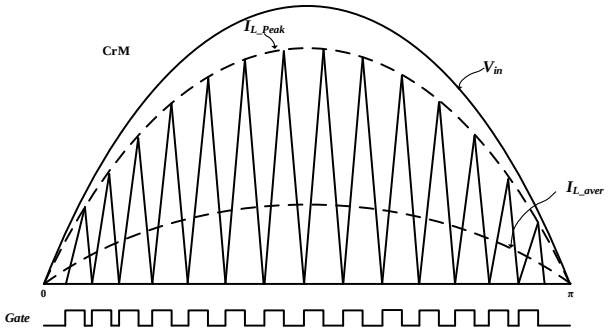

Fig. 6 ideal Input voltage and input current waveform

Actually, there is a negative inductance current before the GATE on, as shown in fig.4. Therefore, the actual average input current is distorted, as shown in fig.7.

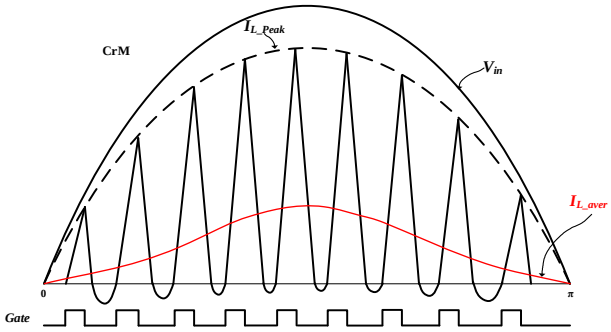

Fig. 7 actual Input voltage and input current waveform

To achieve better THD, the THD Compensation technology is applied in SC3202. The conduction time(Ton) is adaptive during in a half AC cycle. Ton at peak of input voltage will be shorter than that at zero-crossing of input voltage.

9.3 Boost Follow Mode

The SC3202 controller detects the AC line voltage by ZCD/CS pin. At low line, IC enters Boost Follow Mode, and FB pin sources 7.5μA current, to change output voltage of PFC stage. When the AC voltage increases to high line, IC exits Boost Follow Mode, and output voltage of PFC stage will change to higher voltage.

9.4 Brown In/Out

The Brown IN/OUT function is implemented through CS/ZCD pin. The average of the MOS drain voltage in each switching cycle represents the instantaneous line voltage. Therefore, the peak line voltage can be detected by the external divider network attached to the ZCD/CS pin. When the average of CS/ZCD pin voltage rises above V_{ZCDBIN}, the IC starts working, and it stops working when the average of CS/ZCD pin voltage decreases below $V_{ZCDBOUT}$.

9.5 VDD UVLO

Supply undervoltage lockout (UVLO) protection ensures that the controller operates only while the supply voltage is in a range that ensures correct operation and adequate Gate drive amplitude for the power switch.

When the VDD voltage is Lower than the V_{DDOFF} threshold voltage for a longer period than a blanking time, the controller will stop switching. The controller then returns to a dormant condition. During this dormant period, the controller consumes a relatively small amount of supply current until it exceeds the V_{DDON} threshold again.

9.6 Over-Current or CCM Protection

Two levels of overcurrent protection are integrated. V_{CSOCP1} is cycle-by-cycle current limiting for overload protection. V_{CSOCP2} is the protection for the case of CCM. When the current in the inductor does not drop to zero at the end of a switching cycle, the peak of the inductor current will be very high in the next cycles, even beyond the cycle-by-cycle current limit. Then the CCM protection will be triggered, and there will be a longer off time to demagnetize the inductive current to zero.

9.7 Output Over-Voltage Protection

The SC3202 controller provides two independent output overvoltage protection strategies to ensure that a single fault does not cause the output voltage to be too high.

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FB overvoltage protection: FB pin monitors the output voltage through an external divider network. If the voltage on this pin is higher than V_{FBOVP1}, it indicates that the output voltage is too high, and the controller immediately turns off the DRV to prevent further increase of the output voltage.

ZCD overvoltage protection: During the conduction of the boost diode, the voltage on the MOSFET is close to the output voltage. The controller monitors the voltage on the MOSFET through an external voltage divider network connected to the ZCD/CS pin. This monitoring provides a second independent method to detect excessive output voltage when the voltage dividers of FB pin is damaged. A fixed blanking period is applied after the falling edge of the DRV waveform to ensure that the comparator is not triggered by the induced spike at the leading edge of the drain waveform.

When the voltage of ZCD pin is higher than the threshold voltage of internal comparator for three consecutive cycles, ZCD overvoltage protection is triggered, and DVR is closed immediately for 1ms.

9.8 On-Chip OTP

An internal OTP circuit is embedded inside to provide the worst-case protection for SC3202. When the chip temperature rises higher than the OTP_H, the controller will be disabled and works in the failure mode until the chip is cooled down below the hysteresis OTP_{HYS}.

9.9 Pin Open/Short Protection

In case CS/ZCD pin is floating, the voltage of this pin will be pulled up and DRV will turn off to protect the power circuit.·

In case FB pin is floating or short to GND, FB Under Voltage Lock-Out Protection will be triggered, and IC will be shut down.

Further application information and PCB layout guidance is provided in document ***SC320x Application Note***.

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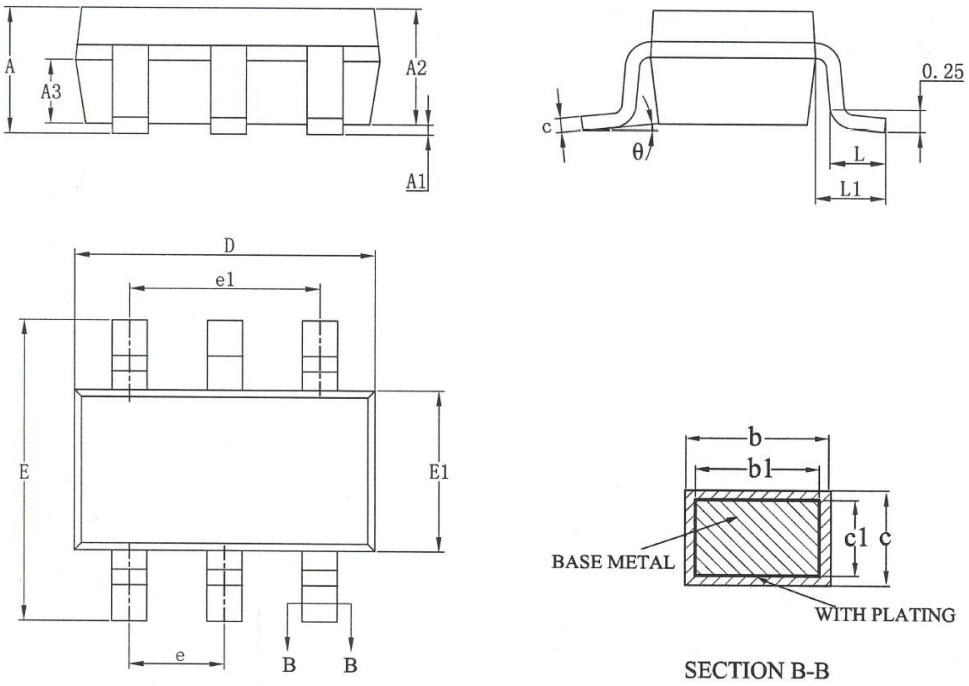
MECHANICAL DATA

SOT23-6 (2.92mmx2.80mmx1.25mm)



SYMBOL	DIMENTIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	——	——	1.25
A1	0.04	——	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	——	0.41
b1	0.32	0.35	0.38
c	0.15	——	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	——	0.60
L1	0.60REF		
θ	0	——	8°

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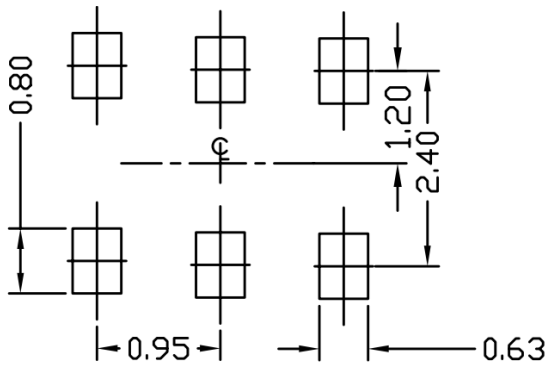
RECOMMENDED FOOTPRINT

Example Board Layout



UNIT: mm

NOTES:

A. Publication IPC-7351 is recommended for alternate designs
B. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

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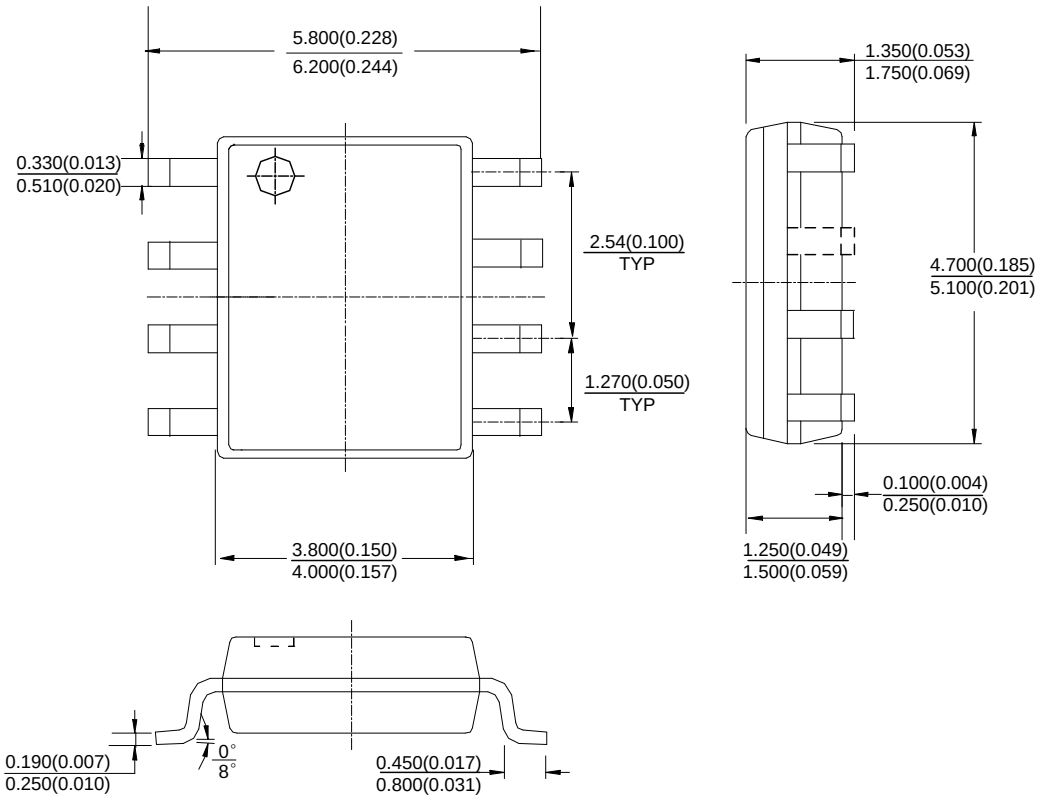
MECHANICAL DATA

SOP8 (6.0mmx4.9mmx1.55mm)



Note: Eject hole, oriented hole and mold mark is optional.

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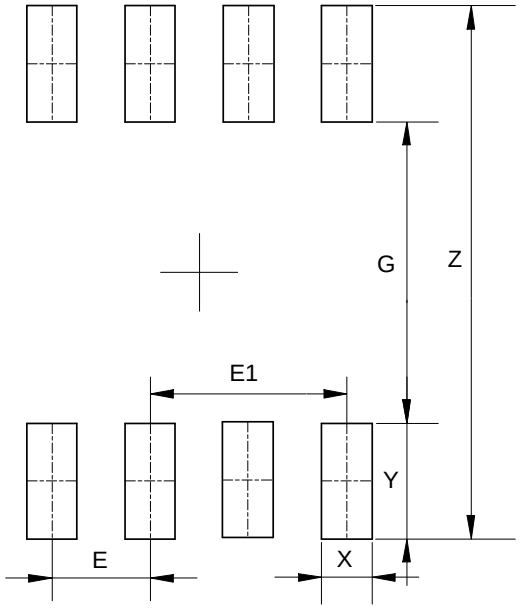
RECOMMENDED FOOTPRINT

Example Board Layout



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)	E1 (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.650/0.026	1.500/0.059	1.270/0.050	2.540/0.100

NOTES:

C. Publication IPC-7351 is recommended for alternate designs
D. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

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