



High Performance Fly-back PWM Controller With GaN Integrated

1 Descriptions

SC3052C is a high performance, multi-mode fly-back PWM controller (CCM/QR/DCM) With GaN Integrated.

SC3052C provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to maximum switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

It provides functions of low start-up current, fast start-up, low standby power consumption. The burst mode with extremely low operation current (240uA) and significantly reduces standby power consumption to meet the efficiency regulations.

The SC3052C offers comprehensive protection to prevent the circuit from damage under abnormal conditions.

Furthermore, the features of frequency jittering and smart driving function can minimize the noise and improve EMI performance.

3 Applications

- USB-PD and QC Chargers
- AC-DC adapters for Portable Devices

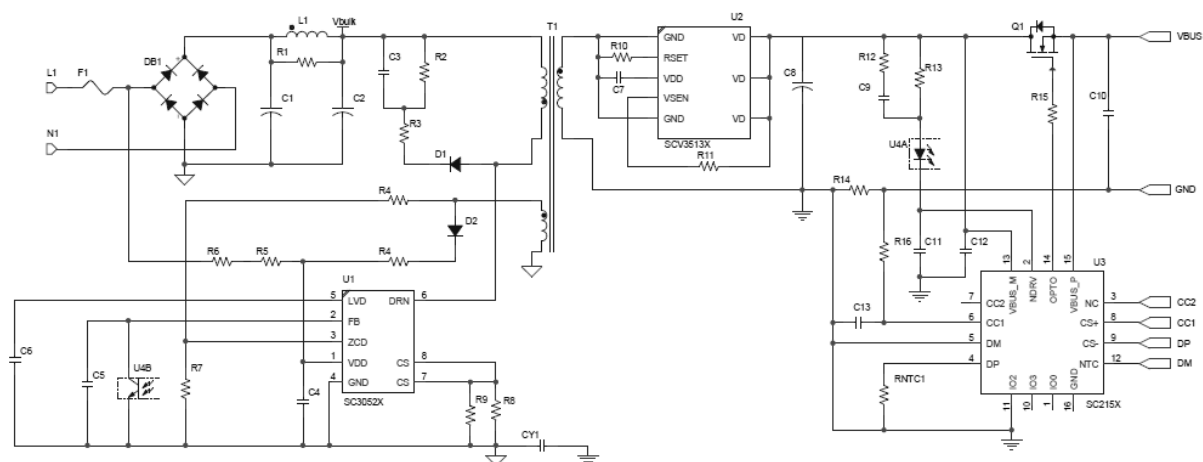
2 Features

- Internal Soft Start
- High Efficiency
 - CCM @ Heavy Load and Low Line
 - Valley switching operation @ Green mode
 - Burst Mode @ Light Load & No Load
- Ultra-low operation current @Burst mode/Fault Mode
- Frequency Jitter for EMI improvement
- Comprehensive Protection
 - VDD over voltage protection
 - VDD under voltage lock out
 - Cycle by cycle current limiting
 - Two level over current protection
 - Output over voltage protection
 - Adaptive output short protection
 - Over Load protection
 - Output UVP protection
 - Brown in/out with auto-recovery
 - Line over voltage protection
- HSOP8 package available

Device Information

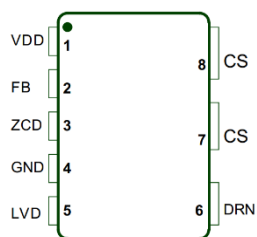
ORDER NUMBER	PACKAGE	BODY SIZE
SC3052CSCER	HSOP8	6.2mmx6mmx1.75mm

4 Typical Application Circuit





5 Terminal Configuration and Functions



HSOP-8 (TOP VIEW)

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VDD	PWR	Power Supply. This pin is typically connected to an external VDD capacitor.
2	FB	I	Secondary side feedback through opto-coupler. A capacitor is needed to connect to GND.
3	ZCD	I	Voltage Sense. The ZCD voltage is used to detect resonant valleys for quasi-resonant switching. This pin detects the output voltage information and diode current discharge time based on the auxiliary winding voltage.
4	GND	PWR	Power Ground.
5	LVD	PWR	Internal PIN. It is recommended to retain a ceramic capacitor position to GND.
6	DRN	PWR	Internal GaN FET drain terminal.
7/8	CS	I	Internal GaN FET source terminal and Current Sense. This pin connects to a current-sense resistor to sense the GaN current for Peak-Current-Mode control for output regulation.



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

Item	Description	Min.	Typ.	Max.	Unit
Voltage range at terminals ⁽²⁾	DRN to GND			700	V
	Transient DRN to GND			800	V
	VDD to GND	-0.3	-	+68	V
	LVD to GND	-0.3	-	+30	V
	ZCD to GND ⁽³⁾	-0.7	-	+6.5	V
	Other Pins to GND	-0.3	-	+6.5	V
T _J	Operating Junction temperature range	-40	-	150	°C
T _{stg}	Storage temperature range	-65	-	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) ZCD allows for -0.7V during repetitive events, t<500ns at 25°C
- (4) DRN allows for surge ratings during non-repetitive Pulse for ≤10ms at 25° C and repetitive off-state spike <300ns, duty cycle<0.01. Limit was extracted from characterization test with cascode device, not measured during production.

6.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	+2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	-1	1	kV

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		HSOP8 (6.2mmx6.0mm)	UNIT
θ _{JA}	Junction to ambient thermal resistance	82.11	°C/W
θ _{JC}	Junction to case resistance	21.59	°C/W

- (1) Measured on JESD51-7, 2-layer PCB.

**6.4 Recommended Operating Conditions**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRN to GND	DRN voltage range to GND	0		700	V
VDD to GND	VDD voltage range to GND	10		V _{DDOVP}	V
ZCD to GND	ZCD voltage range to GND	-0.5		5.5	V
LVD to GND	LVD voltage range to GND	0		25	V
Others to GND	Other pins voltage range to GND	0		5	V
C _{VDD}	VDD Capacitor	2.2		22	μF
T _A	Operating ambient temperature	-40		85	°C
T _J	Operating junction temperature	-40		125	°C



6.5 Electrical Characteristics

VDD=15V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VDD)						
V _{DDON}	VDD on threshold voltage		15.8	16.7	17.4	V
V _{DDOFF}	VDD off threshold voltage		7.4	7.7	8.0	V
V _{DDHOLDL}	VDD holding entry point voltage			8.3		V
V _{DDHOLDH}	VDD holding exit point voltage			8.6		V
I _{ST}	Startup current	VDD < V _{DDON} -1V		9	11	μA
I _{VDD}	Operating current	Clod = 1nF		1		mA
I _{VDDBT}	Burst mode current	V _{FB} < 0.5V		240	270	μA
I _{VDDFAULT}	Hold up current in fault mode			50		μA
T _{FAULT}	Hold on time in fault mode			1		s
I _{VDDFAULT1}	VDD sink current	After T _{FAULT} 1S		1.25		mA
V _{DDOVP}	VDD OVP		58	62	64.5	V
I _{VDDOVP}	VDD OVP sink current	V _{DD} > V _{DDOVP}		3		mA
T _{VDDOVP}	VDD OVP debounce time			160		μs
ZERO VOLTAGE DETECTION (ZCD)						
V _{ZCDOVP2}	ZCD OVP	After T _{ZCDOVP1}	4.2	4.3	4.4	V
N _{ZCDOVP}	ZCD OVP debounce counter			4		Cycles
I _{ZCDMAX}	Maximum ZCD Clamp source current		1			mA
V _{ZCDCLAMP}	ZCD Clamp voltage	I _{ZCDCLAMP} =1.0mA		-180		mV
T _{LEBOVP}	Leading edge blanking time			1.9		μs
V _{ZCDH}	ZCD valley detection rising edge	V _{DRV} = low		0.35		V
I _{ZCDBI}	Line voltage brown in clamp current threshold in ZCD		137	152	168	μA
I _{ZCDBO}	Line voltage brown out clamp current threshold in ZCD		122	136	149	μA
I _{LINEOVP}	Line voltage OVP current threshold in ZCD		616	685	753	μA
T _{ZCDLINEOVP}	Line OVP debounce time	V _{FB} > V _{FBBSTH}		240		ms
T _{DZCDBO}	ZCD brown out debounce time			70		ms
I _{LINECOMPST}	Line voltage compensation threshold ZCD clamp current			200		μA
K _{LINECOMP}	The ratio of line voltage compensation			0.10		/
FEEDBACK VOLTAGE (FB)						
V _{FBOPEN}	Open Loop Voltage	I _{FB} = 0		3		V
R _{FB}	FB pull-up resistor			21	28	kΩ
V _{FBSWMAX}	FB voltage when Maximum Switching frequency is clamped			1.8		V



V_{FBBSTH}	FB voltage when DRV starts pulsing		0.5	0.6	V
$V_{FBBSTHYS}$	V_{FBBSTH} hysteresis voltage		0.1		V
CURRENT SENSE (CS)					
T_{SSCS}	Soft start time of CS threshold		5		ms
$V_{CSLIMIT}$	Cycle by cycle current limited		0.427	0.45	0.472
V_{CSOLP}	CS OLP		0.427	0.45	0.472
$T_{LEB CBC}$	Leading edge blanking time		350		ns
T_{CSOLP}	Debounce time of CS OLP	$V_{CS} > V_{CSOLP}$	70		ms
V_{CS_SSCP}	Secondary rectifier short protection		0.873	0.9	0.927
N_{CS_SSCP}	Secondary rectifier short circuit protection debounce counter		3		Cycles
$T_{LEBSSCP}$	Leading edge blanking time		155		ns
$V_{CSSLOPE}$	Slope compensation		28		mV/ μ s
V_{CSMIN}	CS minimum voltage		0.160		V
ΔV_{CS}	CS jitter		± 5		%
T_{JIT}	CS jitter cycle		480		cycles
GaN FET					
R_{DS_ON}	Drain-source On-state Resistance	$V_{GS} = 0V, I_D = 0.5A, T_j = 25^\circ C$	480	600	720
		$V_{GS} = 0V, I_D = 0.5A, T_j = 150^\circ C$	1285		m Ω
C_{OSS}	Output capacitance	$V_{GS} = 0V, V_{DS} = 400V; f = 100kHz$	3.5		pF
Oscillator for Switching Frequency					
F_{CCM}	CCM switching frequency		100		kHz
K_{QRMAX}	Maximum switching frequency ratio in QR Mode	F_{QRMAX} / F_{CCM}	125		%
F_{SWMIN}	Minimum switching frequency		22	26	kHz
T_{OFFMAX}	Maximum off time	After SS, without ZCD	110		μ s
D_{MAX}	Maximum duty cycle		78		%
Internal Over-Temperature Protection (OTP)					
OTP_H	OTP Temperature		150		$^\circ C$
OTP_{HYS}	OTP Hysteresis		30		$^\circ C$

8 Feature Description

SC3052C is designed for USB-PD solutions, together with PD controller, such as SC21xx series. SC3052C provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to maximum switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

8.1 Start-up

During the startup period, the controller draws a little current I_{VDD} less than 9uA. This allows a high-impedance start-up resistor, which offers a convenient and efficient way to reduce the standby power.

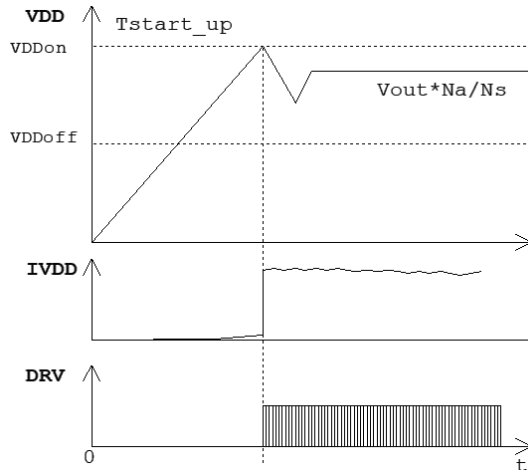


Fig. 2 VDD start-up waveform

The start-up time can be estimated by the following equation:

$$T_{START-UP} \approx \frac{C_{VDD} \cdot V_{DDON}}{V_{BULK}} \cdot R_{STARTUP}$$

Where, C_{VDD} is VDD cap, V_{BULK} is the bulk cap voltage, $R_{STARTUP}$ is the resistor connected between bulk cap positive terminal and VDD cap.

An integrated 5ms soft start is used in the chip to reduce the voltage and current stress. During the soft start-up period, the Vcs threshold gradually rises from 0.1V to 0.45V. Once the secondary side regulation loop is stable, the Vcs is controlled by the feedback loop.

8.2 VDD UVLO

A hysteresis Under Voltage Lock Out (UVLO) comparator is implemented in SC3052C. The turn-on and turn-off thresholds are fixed at 16.6V and 7.5V respectively. This hysteresis ensures that the VDD capacitor can be small enough during start-up. A large hysteresis is essential to ensure the IC work properly during the start-up period, even for a small VDD capacitor.

8.3 VDD Holding Mode

After the system starts, the VDD capacitor can be charged by the auxiliary winding. There are some operation condition changes (load changes, output voltage adjustment, burst mode), may lead the primary side DRV stop working when the output value is higher than the set value. Furthermore, the VDD voltage will be lower than V_{DDOFF} and the system will stop. To avoid this situation, a VDD holding circuitry is designed, which starts working when VDD drops below $V_{DDHOLDL}$ and stops working when VDD rises above $V_{DDHOLDH}$. The working process is shown in below:

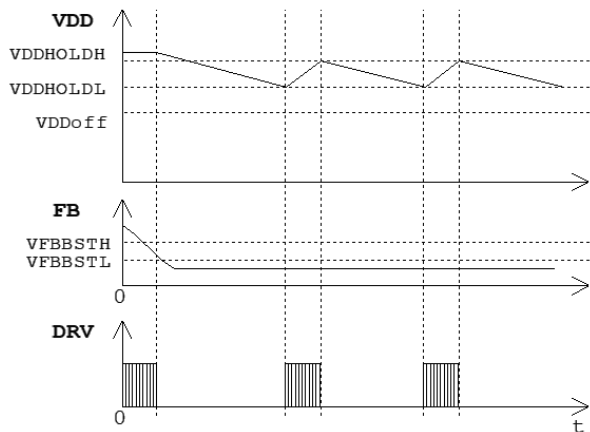


Fig. 3 VDD holding circuitry

8.4 Brown IN/OUT Detection

The ZCD pin is used to monitor the voltage on the Bulk capacitor and perform brown In/Out. Working principle: When the primary switch is turned on, the voltage V_{AUX} on the auxiliary winding is negative. The value of V_{AUX}

is proportional to the line voltage. The clamp circuit built in the ZCD pin clamps the voltage of the ZCD to $V_{ZCDCLAMP}$ through a current source.

The detailed equations are shown as below:

$$\frac{V_{AUX}}{R_{ZCD-UP}} = I_{ZCDCLAP} \text{ and } V_{AUX} = \frac{V_{BULK}}{N_P} * N_{AUX}$$

The V_{AUX} is negatively associated with I_{ZCD} . V_{AUX} is a negative value. When I_{ZCD} is greater than I_{ZCDBI} , the Brown in process is executed and the system starts to work. When the value of I_{ZCD} is less than I_{ZCDBO} and lasts for a certain period of time, the line voltage is considered to be too low and brown out protection is triggered.

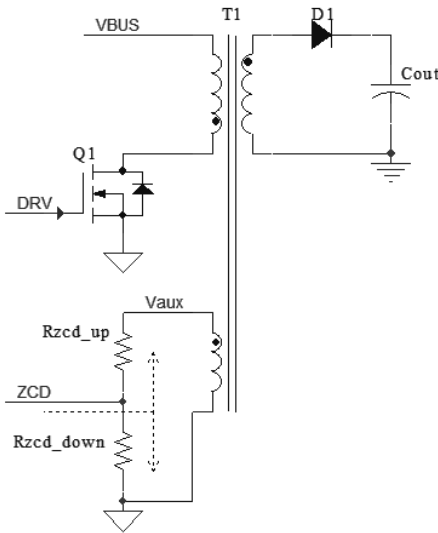


Fig. 4. Brown In/Out detection

8.5 Operation Mode

SC3052C provides an adaptive switching frequency fold-back to achieve higher efficiency in the whole loading range. At heavy load or full load, it operates up to maximum switching frequency. When loading decreases, it operates in green mode with valley switching for high efficiency. And at no load, the IC will operate in Burst mode to reduce power consumption.

When the system is under no load or extremely light load, the IC will operate in BURST mode to reduce power dissipation. In this condition, switching loss of MOSFET is the main power dissipation. The DRV will be disabled immediately if V_{FB} drops below V_{FBBSTL} .

When V_{FB} rises up to V_{FBBSTH} , the DRV starts to pulse again.

When under medium load condition, the system operates in green mode (DCM or QR). The switching frequency will linearly increase from 26kHz to maximum switching frequency. That means, when load increases, the switching frequency is increased.

8.6 Valley Switching

ZCD pin can detect the freewheel information on the secondary side. In QR mode, when the voltage of ZCD turns to a negative value, it means that after a quarter of the resonant period, the primary MOS can be turned on, and valley opening helps to improve efficiency and improve EMI performance. In order to achieve the best valley opening, it can be achieved by appropriately adjusting T_{DZCD} and T_{DDRV} , where T_{DPG} is an internal fixed delay. T_{DZCD} can be adjusted by connecting a small capacitor in parallel with $R_{ZCDDWON}$. The recommended value is 10 ~ 22pF. T_{DDRV} can be adjusted by connecting DRV resistors in series.

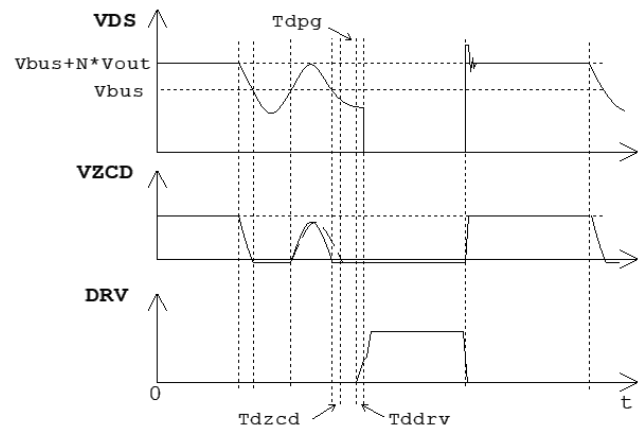


Fig. 5 Valley Switching

8.7 Internal Slope Compensation

A slope compensation circuitry is built-in to simplify the system design. When the switcher is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations.

8.8 Auto-Recovery after Failure

SC3052C has complete protection functions, such as: VDD over voltage protection, VDD under voltage lock out, two level over current protection, output over voltage protection, output short protection, output under voltage protection, over load protection, brown IN/Out with auto-recovery. Unless otherwise specified, these protections are auto-recovery. After the protection is triggered, the system enters the protection mode, and the VDD power consumption is reduced. After the T_{DFault} delay, the VDD sink current increases until V_{DDOFF} , and VDD starts the restart process. The detailed process is as follows.

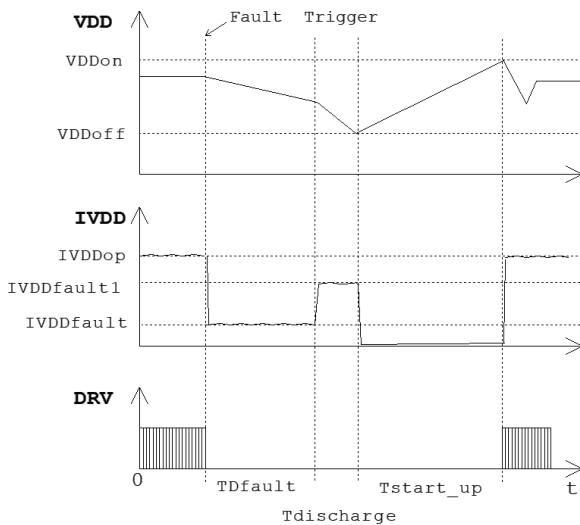


Fig. 6 Auto-Recovery Process

8.9 VDD OVP

When the VDD voltage is higher than the V_{DDOVP} threshold voltage at least T_{VDDOVP} , in the case of a sink current of I_{VDDOVP} , DRV will be shut down. The VDD OVP function is an auto-recovery protection.

8.10 ZCD OVP

The auxiliary winding demagnetization voltage V_{AUX} is proportional to the output voltage. V_{ZCD} sensing the V_{AUX} via the divided resistors can be used to sample

the output voltage after some blanking time. The output over voltage can be calculated as:

$$\frac{V_{AUX} * R_{ZCD-DOWN}}{R_{ZCD-DOWN} + R_{ZCD-UP}} > V_{ZCDOVP}$$

$$\frac{V_{AUX}}{N_A} = \frac{V_{OUT}}{N_S}$$

The blanking time can ignore the voltage ringing from leakage inductance of transformer. With the increase of VFB, the blanking time is from 1.6uS to 2.3uS.

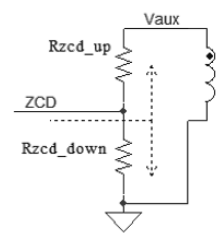


Fig. 7 ZCD Over Voltage Protection

8.11 Over Current Protection

Two levels of overcurrent protection are integrated. One is cycle-by-cycle current limiting for overload protection. V_{CSSSCP} is the fast protection for the case of secondary rectifier rectification shorted. The overcurrent protection and its shielding time are shown in the figure below.

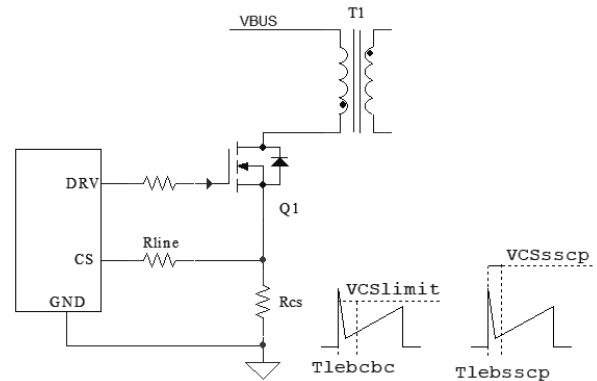
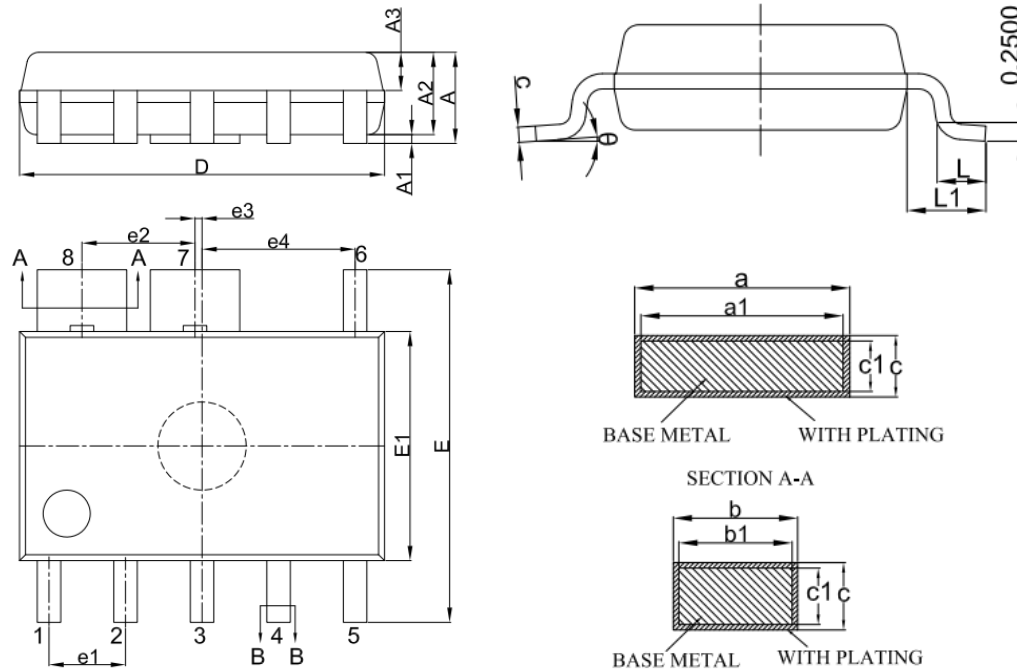


Fig. 8 LEB of OCP



MECHANICAL DATA

HSOP8 (6.2mmx6mmx1.75mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.75
A1	0.1	--	0.25
A2	1.30	1.40	1.50
A3	0.6	0.65	0.70
a	1.50	--	1.58
a1	1.49	1.52	1.55
b	0.38	--	0.46
b1	0.37	0.40	0.43
C	0.20	--	0.24
c1	0.19	0.20	0.21
D	6.10	6.20	6.30
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e1	1.30BSC		
e2	1.92BSC		
e3	0.12BSC		
e4	2.60BSC		
L	0.4	--	0.8
L1	1.05REF		
	0	--	8°