

SC2021PQ AEC-Q100 Type-C/ PD and DPDM Fast Charge Controller

1 Description

SC2021PQ is a Type-C / PD and DPDM fast charge controller for automotive applications. It complies with the latest Type-C and PD 3.1 standards and supports the proprietary high voltage fast charge protocols with dual DPDM interfaces. It targets for the wall adapters, travel adapters and car chargers.

SC2021PQ minimizes external components by integrating USB PD baseband PHY, Type-C detection, dual DPDM PHYs, VBUS discharging paths, VCONN supply, programmable feedback compensation, voltage and current sense, 10-bit high performance ADC, dual 10-bit DACs, NMOS gate driver, I2C interface and protection circuits, which provides cost effective solutions to many applications.

SC2021PQ supports various protection mechanisms including Over Voltage Protection (OVP), Under Voltage Protection (UVP), Over Current Protection (OCP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), DPDM Over Voltage Protection (DPDM OVP), CC Over Voltage Protection (CCOV), VCONN Over Voltage (VCONN OVP), VCONN Over Current (VCONN OCP) and VCONN Short Protection (VCONN SCP), so to effectively ensure stable and reliable operation of system.

The SC2021PQ is available in 32-pin QFN package.

2 Features

- **AEC-Q100**
 - AEC-Q100 Qualified for automotive applications
- **USB Type-C**
 - Support Type-C DFP protocols
 - Support DRP or UFP protocols with external Rd
 - Configurable resistor R_P
- **USB Power Delivery**
 - Support DFP USB PD 3.1 with PPS
 - Hardware BMC transmitter and receiver
 - Full feature physical layer
 - Hardware CRC
 - Hardware reset
 - Integrate PD 3.1 protocol engine
 - Integrate VCONN and support SOP' for e-marker
- **Dual DPDM Fast Charging Interfaces**
 - Integrate 2x firmware controlled DPDM interfaces
 - Support Apple charging, BC1.2, DCP, HVDCCP, FC, AFC
- **Power**
 - Wide operation range: 3V to 22V (26V tolerant)
- **Analog Block**
 - Support OPTO interface for adapter
 - Support FB interface for car charger
 - Dual DACs for CC/CV loop.
 - 10-bit ADC to monitor the voltage / current / DPDM/ other signals
 - Integrated high side current sense amplifier
 - Integrated NMOS gate driver
 - Integrated VBUS discharging paths
 - Integrated temperature sense module
- **Protections**
 - 26V tolerant for CC1 and CC2
 - 12V tolerant for DP and DM
 - On chip OVP, UVP, SCP, VCONN OVP, VCONN OCP, VCONN SCP, OTP, DPDM OVP, CC OVP
- **Package**
 - 32-pin QFN, 4mm x 4mm x 0.75mm

3 Applications

- Wall adapters
- Travel adapters
- Car chargers

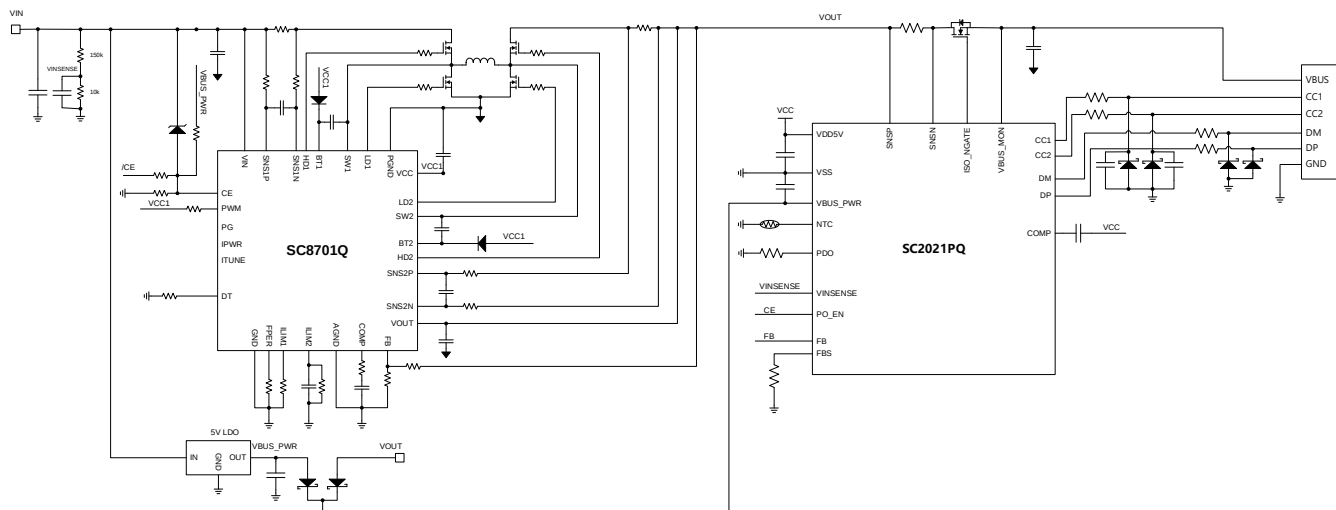
4 Device Information

Part Number	Package	Body Size
SC2021PQQDER	QFN32	4mm x 4mm x 0.75mm



5 Typical Application Diagram

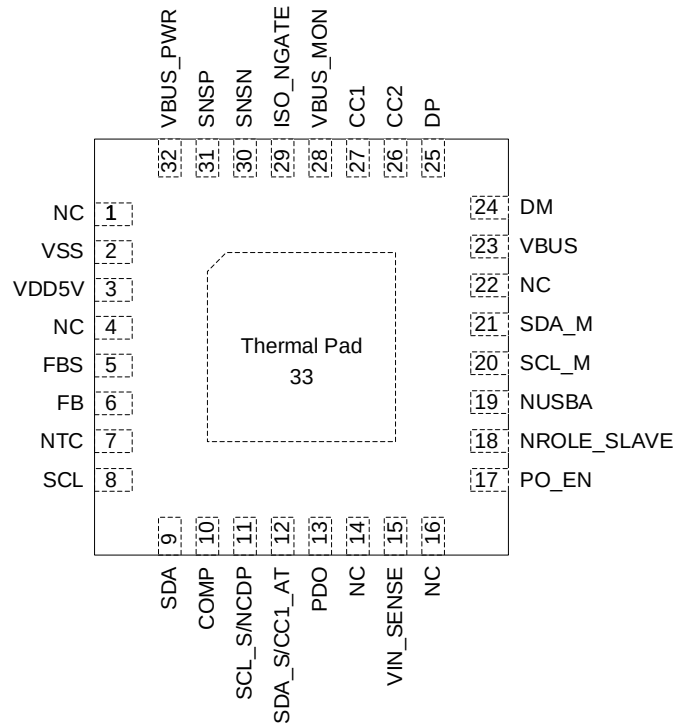
QFN-32 Application-2 Diagram





6 Terminal Configuration and Functions

TOP VIEW of SC2021PQ (QFN-32)



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	NC	-	No connect
2	VSS	I/O	Ground of IC
3	VDD5V	O	Output of 5V LDO. Provide power supply for internal circuits. Connect a 2.2uF capacitor to ground
4	OPTO	I	Current sink output for optocoupler connection
5	FBS	I	This pin is used to set the bias current when FB control is used to adjust the output voltage of power IC. Connect a resistor between this pin and ground. Leave this pin floating if FB control is not used
6	FB	I	If FB control is adopted to adjust the output voltage of the power IC, connect this pin to the feedback divider of the power IC. If FB control is not adopted, leave this pin floating
7	NTC	I	Connect NTC resistor from this pin to GND
8	SCL	i	I2C interface for test, clock line



9	SDA	I/O	I2C interface for test, data line
10	COMP	I/O	If FB control is adopted to adjust the output voltage of the power IC, connect a capacitor to this pin to compensate CC loop
11	SCL_SLAVE	I	I2C slave interface for multi-port application, data line
	NCDP	I/O	BC1.2 function configuration. If CDP function is broadcast on DPDM, connect this pin to GND. If DCP function is broadcast on DPDM, left this pin floating. This configuration is available when NROLE SLAVE connect to GND.
12	SDA_SLAVE	I/O	I2C slave interface for multi-port application, clock line
	CC1_AT	I/O	Plug orient indication. High level indicates that CC1 is attached and low level indicates that CC2 is attached. This configuration is available when I2C_ROLE_SEL connect to GND.
13	PDO	I	Power data object setting pin2. Connect a resistor from this pin to ground for firmware setting the output power, 1K for 30W application, 3K for 45W application, 5K for 60W application, 7K for 65W application and 17K for 65W multi-port application.
14	NC	-	No connect
15	VIN_SENSE	I	VIN voltage sense pin.
16	NC	-	No connect
17	PO_EN	I/O	Power output enable control pin.
18	NROLE_SLAVE	I	I2C role configuration for multi-port application, internal pulled up. I2C mater function is enable by connect this pin to GND and left this pin floating for I2C slave
19	NUSBA	I/O	Type-C or Type-A mode select, internal pulled up. Connect this pin to GND for Type-A mode and left this pin floating for Type-C mode. If SC2021PQ enters Type-C mode, CC function is enabled and NMOS driver is always off other than device attachment is detected. If SC2021PQ enters Type-A mode, CC function is disabled and NMOS driver is always on.
20	SCL_M	I/O	I2C interface for multi-port application. Clock line
21	SDA_M	I/O	I2C interface for multi-port application. Data line
22	NC	-	No connect
23	VBUS	I	Connected to the output of DCDC. It can discharge the output capacitor and could be used to sense VBUS voltage.
24	DM	I/O	DM line of fast charging interface
25	DP	I/O	DP line of fast charging interface
26	CC2	I/O	Type-C configure channel2. It also supports VCONN output
27	CC1	I/O	Type-C configure channel1. It also supports VCONN output
28	VBUS_MON	I	Connected to the VBUS line of the USB Type-C port. It can discharge the output capacitor and could be used to sense VBUS voltage of Type-C port
29	NGATE	O	Load switch (NMOS) driver



30	SNSN	I	Negative input of the internal current sense amplifier. Connect to the high side current sense resistor for the Type-C port
31	SNSP	I	Positive input of the internal current sense amplifier. Connect to the high side current sense resistor for the Type-C port
32	VBUS_PWR	I	IC supply input. It supports more than 100mA discharging capability for the internal VBUS capacitor and could be used to sense VBUS voltage
33	Thermal Pad	-	Connect this pad to VSS



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	ISO_NGATE	-0.3	31	V
	VBUS_PWR, VBUS_MON, SNSP, SNSN, CC1, CC2, VBUS	-0.3	26	V
	DP, DM	-0.3	12	V
	Other pins	-0.3	5.5	V
T _J	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		QFN-16 (4mmX4mm)	UNIT
θ _{JA}	Junction to ambient thermal resistance	52	°C/W
θ _{JC}	Junction to case thermal resistance	23	°C/W

7.3 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	All pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾	All pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V _{BUS_PWR}	VBUS_PWR operation voltage	3.0		22	V
C _{VBUS_MON}	Bulk capacitor at VBUS_MON pin	1		10	μF
C _{VDD5V}	Capacitor at VDD5V pin	2.2			μF
R _{SNS}	Sense resistor between CS+ and CS- pins	3	5	10	mΩ
T _A	Operating ambient temperature	-40		125	°C



T_j	Operating junction temperature	-40		125	°C
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7.5 Electrical Characteristics

$T_j = 25^\circ\text{C}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{BUS_PWR}	VBUS_PWR supply range		3.0		22	V
V _{BUS_PWR_POR}	VBUS_PWR power on threshold	VBUS_PWR rising threshold		2.9	3.0	V
V _{BUS_PWR_UVLO}	VBUS_PWR UVLO threshold	VBUS_PWR falling threshold	2.6	2.7	2.8	V
I _{q_ACT}	Quiescent current in active mode	VBUS_PWR=5V, MCU core is active		12		mA
I _{q_SBY}	Quiescent current in standby mode	VBUS_PWR=5V, standby mode, digital DPDM module wakes up, all analog peripherals enabled		2		mA
5V LDO						
V _{LDO_5V}	5V LDO regulation voltage	VBUS_PWR = 5.5V~20V	4.9	5	5.1	V
V _{LDO_DROP}	5V LDO drop out voltage	V _{BUS_PWR} -V _{LDO5V} , I _{OUT} = 50 mA			150	mV
I _{LDO_LIMIT}	LDO current limit	V _{BUS_PWR} = 5V	90	100	120	mA
DISCHARGE						
I _{DIS_VBUS_PWR}	Discharging current at VBUS_PWR	Register-Programmable	25		150	mA
R _{DCHG_VBUS_MON}	Discharging resistor at VBUS_MON			1	1.4	kΩ
R _{DCHG_VBUSA}	Discharging resistor at VBUSA			1	1.4	kΩ
NMOS GATE DRIVER						
V _{DRV}	Driving voltage	V _{GATE} -V _{VBUS_MON} , V _{BUS_PWR} ≥ 3.3V		5		V
V _{CLAMP_GS}	Driver clamp voltage	V _{GATE} -V _{VBUS_MON}		7		V
R _{DRIVE_UP}	Driver pull up resistance	VBUS_PWR=5V, Register-Programmable	20		200	kΩ
CURRENT SENSE						
G _{CSNS}	Gain of current sense amplifier		19.8	20	20.2	
V _{OCP}	OCP threshold, calculated as I _{BUS} *R _{SNS}			36	37	mV
V _{OCP_DT}	OCP deglitch time			1000		μs
V _{LINE_COMP_MAX}	Max VBUS output voltage compensation		160	200	240	mV
ADC						



V _{ADC_REF}	Reference voltage for ADC		2.249	2.253	2.257	V
N _{ADC}	Resolution		10			Bits
R _{SAMPLE}	ADC sample rate		47.5	50	52.5	ksps
K _{ADC_VBUS_PWR}	Ratio from VBUS_PWR voltage sense		1/10			
K _{ADC_VBUS_MON}	Ratio from VBUS_MON voltage sense		1/10			
K _{ADC_VBUSA}	Ratio from VBUSA voltage sense		1/10			
K _{ADC_CSNS}	Ratio from the output of current sense amplifier		1			
K _{ADC_DPDM}	Ratio from DP1, DP2, DM1, DM2		1/4			
K _{ADC_VDD5V}	Ratio from VDD5V		1/4			
ADC _{VBUS_PWR} , ADC _{VBUS_MON} , ADC _{VBUSA}	Range		3.0	22.46		V
	LSB		22			mV
	Error	VBUS = 3.3V ~ 9V	-50	50		mV
		VBUS = 9V ~ 21V	-100	100		mV
ADC _{DPX} , ADC _{DMX}	Range		0	8.983		V
	LSB		8.78			mV
	Error	Full range	-150	150		mV
ADC _{ADX} , ADC _{CSNS}	Range		0	2.251		V
	LSB		2.2			mV
	Error	Full range	-5	5		mV
INL	Integral non-linearity		-1.0	1.0		LSB
DNL	Differential non-linearity		-1.0	1.0		LSB
FB CV-DAC AND CC-DAC						
V _{FB_VDAC_REF}	FB regulator VDAC reference		1.024			V
V _{FB_VDAC_STEP}	FB VDAC step voltage		1			mV
V _{BUS_PWR_STEP_VOLT_FB}	VBUS_PWR adjust voltage per step via FB	R _{UP} = 20×R _{FBS}	20			mV
I _{FB_SRC}	FB source capability	FB = 2.5V	400			μA
I _{FB_SNK}	FB sink capability	FB = 0.8V	400			μA
V _{DCDC_IDAC_REF}	DCDC regulator IDAC reference		2.244	2.248	2.252	mV
I _{FB_REG_STEP}	Output current regulation per step by DCDC IDAC		10.98			mA
I _{COMP}	Current capability from COMP pin		-4	2		μA
VBUS OVP and UVP						



V _{BUS_PWR_OVP}	VBUS_PWR OVP rising threshold		115	120	125	%
V _{BUS_OVP_HYS}	VBUS_PWR OVP threshold hysteresis, respect to VDAC setting			0	5	%
V _{BUS_PWR_UVP}	VBUS_PWR UVP falling threshold		73	75	77	%
V _{BUS_UVP_HYS}	VBUS_PWR UVP threshold hysteresis, respect to VDAC setting			0	3	%
V _{BUS_SCP_TH}	VBUS_PWR SCP threshold		3.1	3.2		V
t _{MON_SCP}	VBUS_MON SCP deglitch time			0		μs
TYPE-C/ PD PROTOCOLS						
I _{CC_330μA}	CC1/2 pull up current		303.6	330	356.4	μA
R _{CC_open}	CC1/2 open impedance	CC1/2 in disable status	126			kΩ
V _{CC_0P2_th_src}	CC1/2 0.2V comparison threshold	CC1/2 as source	0.15	0.2	0.25	V
V _{CC_0P4_th_src}	CC1/2 0.4V comparison threshold	CC1/2 as source	0.35	0.4	0.45	V
V _{CC_0P66_th_src}	CC1/2 0.66V comparison threshold	CC1/2 as source	0.61	0.66	0.7	V
V _{CC_0P8_th_src}	CC1/2 0.8V comparison threshold	CC1/2 as source	0.75	0.8	0.85	V
V _{CC_1P23_th_src}	CC1/2 1.23V comparison threshold	CC1/2 as source	1.18	1.23	1.28	V
V _{CC_1P6_th_src}	CC1/2 1.6V comparison threshold	CC1/2 as source	1.5	1.6	1.65	V
V _{CC_2P6_th_src}	CC1/2 2.6V comparison threshold	CC1/2 as source	2.45	2.6	2.75	V
V _{TH_CCOVP_RISING}	CCx OVP detection	CCOVP rising threshold		7.2		V
V _{TH_CCOVP_FALLING}	CCx OVP release	CCOVP falling threshold		7.0		V
Z _{Driver}	PD data Tx output impedance		33		75	Ω
V _{Swing}	High level voltage for CC PD data		1.05	1.125	1.2	V
VCONN SWITCH						
V _{VCONN}	VCONN input voltage		3		5.5	V
R _{VCONN}	VCONN switch on resistance	LV ≥ 3.3V			40	Ω
I _{VCONN}	VCONN current capability	VBUS_PWR = 5V		50		mA
I _{VCONN_OCP}	VCONN over current	Rising threshold		70		mA
DPDM PROTOCOL INTERFACES						



R _{SHORT}	DP DM short resistance	VBUS_PWR = 5V ~ 21V	40	Ω
V _{3.3V}	DPDM 3.3V buffer output voltage	VBUS_PWR = 5V ~ 21V	3.2 3.3 3.4	V
V _{2.7V}	DPDM 2.7V buffer output voltage	VBUS_PWR = 5V ~ 21V	2.6 2.7 2.8	V
V _{1.96V}	DPDM 1.96V buffer output voltage	VBUS_PWR = 5V ~ 21V	1.9 2 2.1	V
V _{TH_3V}	VTH3V comparator threshold at DPDM pin	VBUS_PWR = 5V ~ 21V	2.9 3 3.1	V
V _{TH_2.2V}	VTH2.2V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	2.1 2.2 2.3	V
V _{TH_1.35V}	VTH1.35V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	1.25 1.35 1.45	V
V _{TH_0.425V}	VTH0.425V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	0.35 0.425 0.5	V
V _{TH_0.325V}	VTH0.325V comparator threshold at DPDM pin	VBUS_PWR = 3.3V ~ 21V	0.25 0.325 0.4	V
R _{OUT_30k}	Output resistance of DP or DM buffer		24 30 37.5	kΩ
I _{OUT_0P6V}	0.6V current capability, sink/BC1.2, DP/DM		250	μA
R _{DP/DM_DWN}	DP/DM pull down resistance	source/HVDCP, DM	15 20 25	kΩ
R _{DP/DM_LKG}	DP/DM leakage		300 500 800	kΩ
V _{DATA_HIGH}	DP/DM data output high voltage	Slave data output high, VBUS ≥ 3.3V	3 3.3 3.6	V
V _{DATA_LOW}	DP/DM data output low voltage	Slave data output low	0.2	V
I _{OH_DM_3P3V}	3.3V current capability, DM		5	mA
V _{TH_DPDMOV}	Source/DPDM OVP detection	DPDMOVP rising threshold	4.4 4.75 4.95	V
t _{DPDM_OVP}	DPDM over-voltage deglitch time		4	μs
t _{DATA_RISING}	Data output from low to high		0.3 1	μs
t _{DATA_FALLING}	Data output from high to low		0.3 1	μs
t _{UI}	Unit interval time		144 160 176	μs
t _{PING_ST}	Adapter transmit slave ping duration time		2304 2560 2816	μs
t _{PING_SR}	Adapter receive master ping duration		2304 2560 2816	μs
t _{PSR/t_{PST}}	Ping received and transmit ratio		99 100 101	%
t _{AD}	Terminal attach deglitch		450 500 550	μs
t _{DD}	Terminal detach deglitch		0.475 0.5 0.525	ms
PDO SETTING				
V _{PDO_OPEN}	PDO1/PDO2 open voltage		VDD5V	V



INTC	PDO1/PDO2 bias current		97	100	103	μA
GPIO PINS						
V _{IH_GPIO}	Input voltage high threshold	VBUS_PWR = 3.3V ~ 21V, measured as VIO		0.7		V
V _{IL_GPIO}	Input voltage low threshold	VBUS_PWR = 3.3V ~ 21V, measured as VIO	0.3			V
V _{OH_GPIO}	Output high voltage	VBUS_PWR = 6V, apply 4mA sink current from IO pin to GND externally	4.5			V
V _{OL_GPIO}	Output low voltage	VBUS_PWR = 6V, apply 10mA source current from VDD_5V to IO pin externally		0.5		V
V _{PU}	Pull up resistor value at GPIO pin	VBUS_PWR = 3.3V ~ 21V		5.1		k Ω
V _{PD}	Pull down resistor value at GPIO pin	VBUS_PWR = 3.3V ~ 21V		5.1		k Ω
THERMAL SHUTDOWN						
T _{TH}	Thermal shutdown threshold (LDO), SC2021PQ will reset when junction temperature is over T _{TH}	T _{TH} rising	160	180		°C
T _{TH_HYS}	Over temperature hysteresis	T _J falling below T _{TH} - T _{TH_HYS} , SC2021PQ will restart.		15		°C

(1). It is recommended to set VDAC code at least 60 at 3.2V on VBUS.

8 Detailed Description

8.1 Power Supply

SC2021PQ contains an internal high-voltage LDO which supports wide input range. VBUS_PWR is the power supply input pin of internal LDO. It converts voltage on VBUS_PWR to 5V and supplies internal modules.

For applications, VBUS_MON should be connected to the VBUS on USB port, and VBUS_PWR should be connected to internal VBUS node. It is recommended to place a 1μF ceramic capacitor close to the VDD5V pin.

8.2 NMOS Gate Driver

The Type-C and USB PD specifications require the VBUS isolation implementation for the Type-C port. SC2021PQ provides NMOS gate driver to control the isolation MOSFET between the internal VBUS node and the Type-C port. The gate driver is controlled by register bit. The voltage VGS is clamp to 7V. The IC provides 4 different pull-up capabilities from 20kΩ to 200kΩ so to suit different MOSFETs.

8.3 VBUS Discharging Paths

The IC integrates VBUS discharging paths from VBUS_MON, VBUS_PWR and VBUS_A pins to ground respectively. These paths help drain the residual charge on the bulk capacitors to meet the application requirements. The typical equivalent impedance of discharge path on VBUS_MON pin and VBUS_A pin are 1kΩ. Discharging path on VBUS_PWR pin is a constant current from 45mA to 150mA, which can be configured by registers. These discharge paths are activated at detachment or a lower VBUS voltage transition occurring. All discharging paths can be controlled by firmware.

8.4 ADC

In the Type-C, USB PD or other quick charge applications, it is necessary to monitor the VBUS voltage and current. The SC2021PQ integrates a 10-bit Successive Approximation Analog to Digital Converter (SAR ADC) with a reference voltage of 2.253V.

The ADC supports 10-channel input as below. For VBUS_MON, VBUS_PWR and VBUS_A, an internal ratio of 1/10 is built in. The ratio of DPDM and VDD5V channel is 1/4.

Table 1. ADC input channel

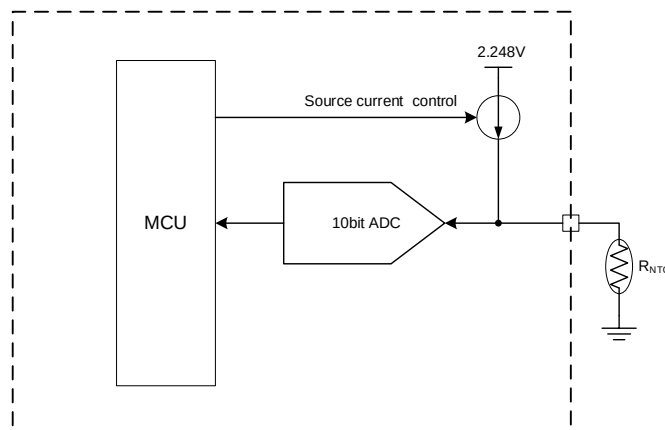
ADC_CH	Input Signal	Note
1	1/10 x VBUS_PWR	With 1/10 internal divider

2	1/10 x VBUS_MON	With 1/10 internal divider
3	VRSNS × 20	The gain of current sense amplifier can be set as 20
4	1/4 x DPx or DMx	With 1/4 internal divider
5	1/4 x VDD5V	With 1/4 internal divider
7	1/10 x VBUS	With 1/10 internal divider

8.5 PDO Setting

SC2021PQ provides a port to support external PDO setting. The PDO pin can source a bias current and can be configured as input of ADC channel. SC2021PQ broadcasts different source capabilities through CC or DPDM by detecting the resistors connected to PDO pins.

As shown in the figure, the NTC pins can be used for temperature detecting. NTC pin outputs current on the R_{NTC}, and the voltage can be sampled by 10-bit ADC. Source current can be configured as 100μA, 20μA or 4μA. The over-temperature protection will be triggered if the voltage is below an over-temperature protection threshold for a programmed time delay.



8.6 CV CC Control Loop for DCDC

Generally, DCDC output voltage and current is controlled through the FB pin, so SC2021PQ integrates another set of voltage and current regulation for DCDC application.

8.7 DPDM Interface

The SC2021PQ contains DPDM interface which can be configured as discharging out port (provider). The DPDM interface is available for USB-A port applications or Type-C port applications. It supports Apple-2.4A, BC1.2 DCP, CDP, FC, AFC, and FCP protocols.

All of the DPDM pins can be configured flexible for different applications. SC2021PQ supports Apple-2.4A mode, which



broadcasts 2.7V voltage on both DP and DM pins with 30kohm output impedance. If 2.4A mode advertisement on DPDM is enabled, it is recommended that VBUS should be able to supply at least 2.4A of current.

SC2021PQ can be also configured as a dedicated charging port (DCP) and charging downstream port (CDP), which complies with the BC1.2 specification. When DCP mode is enabled, SC2021PQ shorts DP and DM pin through a 20ohm resistor.

8.8 CC Interface

The IC can be configured as source only. It presents Rp on CC1 and CC2. CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable. Once an attachment is detected, the IC will apply VBUS voltage and broadcast source capabilities.

Current source presented on CC can be configured to 330μA. Each of the CC pins contains comparators to decide CC_RD and CC_RA attachment.

8.8.1 VCONN Switch

SC2021PQ features a more than 50mA VCONN power with a fixed Overcurrent Protection (OCP) of 70mA.

The IC supports electronically marked cables assembly for more than 3A power delivery. By default, passive cables support up to 3A. The IC can check the cable types through internal CC comparators. If an e-marker cable is detected, the IC supplies the cable with VCONN and communicates with it to check the cable current ratings.

When VCONN switch is turned on, SC2021PQ will continuously monitor current on CC pin. If VCONN output current is above 70mA, VCONN over-current flag will be set, and VCONN switch can be turned off by firmware. SC2021PQ supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

When VCONN switch is turned on, the IC will continuously monitor current on CC pin. VCONN over-current flag will be set if VCONN output current is above 70mA. Once VCONN OCP is triggered, VCONN switch can be turned off by firmware. The IC supports reverse current protection on VCONN switch to avoid damage if CC pin is short to VBUS.

8.9 AC Mode Setting

SC2021PQ supports Type-C mode and Type-A mode output setting. During initial start-up, SC2021PQ pulls up NUSBA pin. To enter Type-A mode, NUSBA should be

connect to GND. The device is latched at Type-A mode until power is recycled. To enter Type-C mode, left NUSBA open.

For Type-A mode, NMOS driver is always on and CC is disable. While for Type-C mode, CC function is enabled and NMOS driver is always off other than device attachment is detected.

8.10 PMAX setting

SC2021PQ supports up to 65W fast charge application. The maximal power delivery could be set by PDO pin. When powers up, SC2021PQ detects the resistance between PDO

pin and GND to config the PMAX. Once the PMAX detection is completed, the configuration will be latched until SC2021PQ is re-powered. In order to ensure this function works well, a 1% precision resistor is required. The detail relationship between resistance and PMAX is as follows.

R _{PDO} / kΩ	PMAX/ W	Output Power Range
1	30	5V3A 9V3A 15V2A 20V1.5A PPS:3.3~11V3A
3.3	45	5V3A 9V3A 15V3A 20V2.5A PPS:3.3~21V2.25A
5.7	60	5V3A 9V3A 15V3A 20V3A PPS:3.3~21V3A
7.7	65	5V3A 9V3A 15V3A 20V3A PPS:3.3~21V3.25A

8.11 Single Port Mode

SC2021PQ could be used for single port application. During initial start-up, SC2021PQ pulls up I2C_ROLE_SEL pin with 5-kΩ resistor to VDD5V. To enter single port mode, connect the NROLE_SLAVE pin to ground. And SC2021PQ will enters multi-port mode if NROLE_SLAVE is left floating. This configuration will be latched until re-powered.

8.12 CDP or DCP Configuration

After single port mode is detect, SC2021PQ detects NUSBA pin to broadcast corresponding protocols. If NUSEBA is connected to GND, then CDP is enabled. And if NUSBA is floating, then DCP is enabled in BC1.2 detection process.

8.13 Plug Orient Indication

When SC2021PQ enters single port mode, SC2021PQ supports CC plug orient indication. If CC1 is attached, CC1_AT pin will output high. While CC1_AT output low when CC2 is attached.



8.14 Protections

8.14.1 OVP, UVP and SCP

The IC monitors the VBUS voltage in real time. Once the voltage exceeds the OVP threshold for a programmed time, the flag is set and an interrupt is generated automatically. It also monitors VBUS voltage for under-voltage protection (UVP). Once VBUS voltage drops below UVP threshold for a programmed time, the UVP flag is set and an interrupt is generated. Once voltage on VBUS drops below 3.2V, Short-Circuit Protection (SCP) will be triggered. An interrupt will be generated and the SCP flag will be set.

8.14.2 Protection for DPDM

The IC supports over-voltage protection of the DP/DM pin. Once it detects any of the DP and DM voltage exceeding 4.75V, the IC will report the over-voltage status and generate an interrupt.

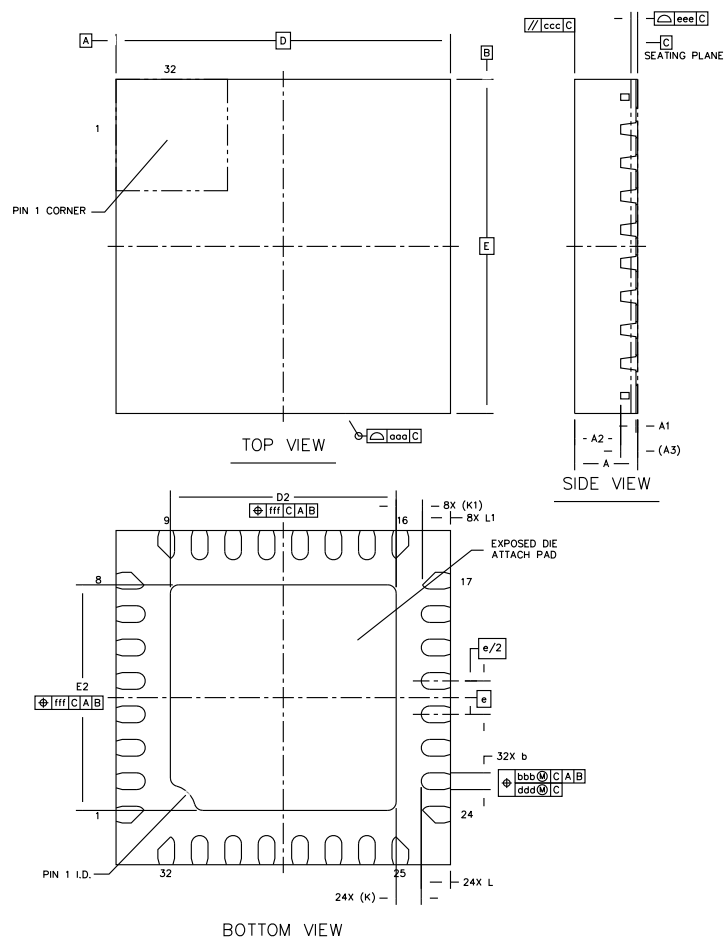
8.14.3 Protection for CC

SC2021PQ continuously monitors CC voltage. Once CC over-voltage detected, SC2021PQ will launch CC Over-Voltage Protection (CC OVP). The CCOVP flag will be set if the voltage on CC1 or CC2 is over 7.2V and will be clear after voltage falls below 7V. The OVP interrupt will be triggered if interrupt enable control bit is set.

If each of the protections including OVP, UVP, SCP is detected, SC2021PQ can drive isolation MOS off by register setting.

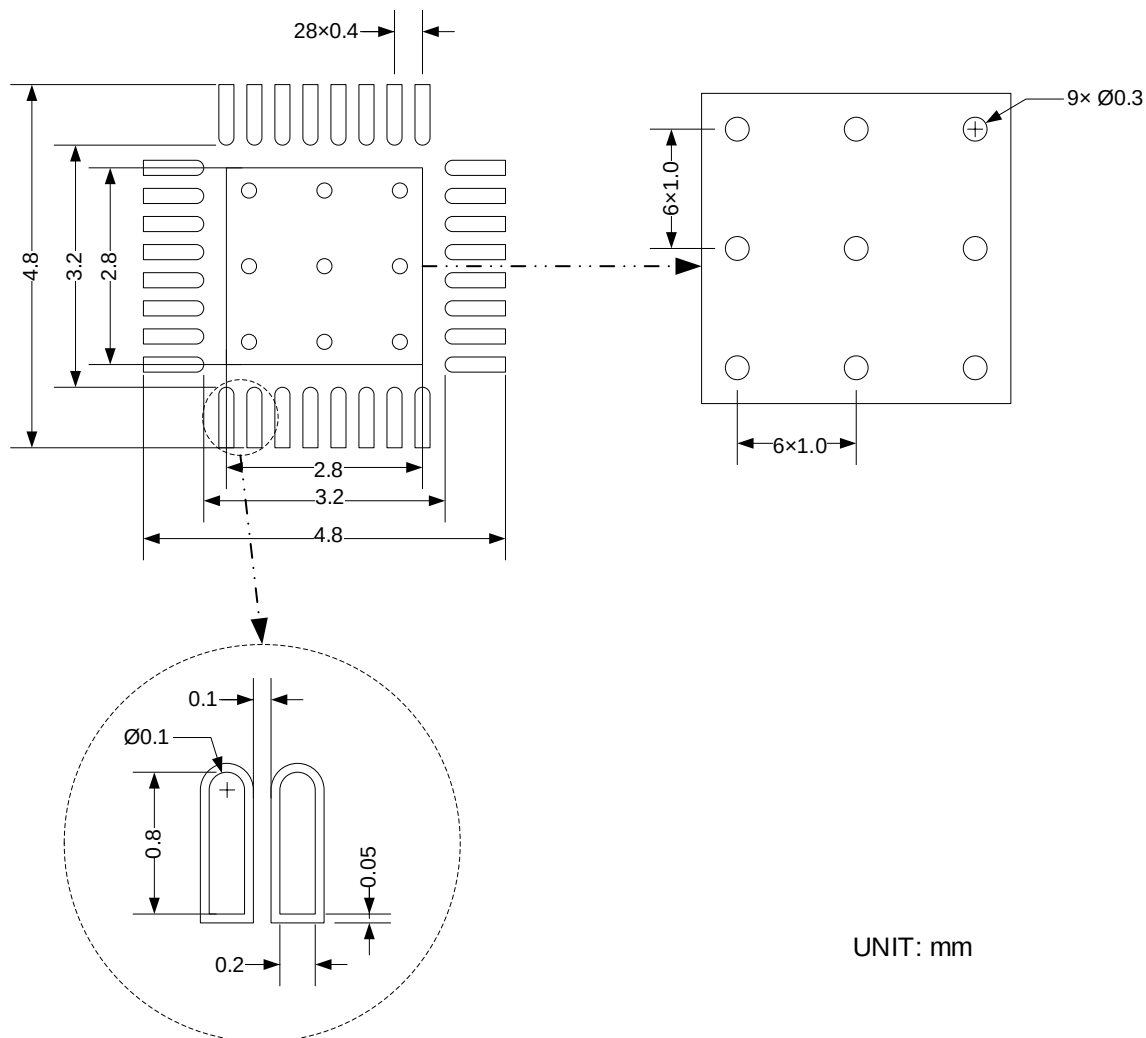
PACKAGE

QFN-32 0404 x 0.75



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	4 BSC		
	Y	E	4 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.235	0.335	0.435
		K	0.3 REF		
LEAD TIP TO EXPOSED PAD EDGE		K1	0.315 REF		
PACKAGE EDGE TOLERANCE		ooo	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
		ddd	0.05		
EXPOSED PAD OFFSET		fff	0.1		

Board Layout Example



UNIT: mm

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