



## SC77708Q 8 Half Bridge Gate Driver

### 1 Descriptions

The SC77708Q is a Multi-MOSFET driver IC dedicated to control up to 16 N-channel MOSFETs. It includes 8 half-bridges for DC motor control applications such as automotive power seat control or other applications.

A 24-bit Serial Peripheral Interface (SPI) is used to configure the SC77708 and to control the half bridges. It also allows the read out of the status registers for diagnostic purpose.

The SC77708 offers a wide range of diagnostic features such as the monitoring of the supply voltage, the charge pump output voltage, temperature warning and over-temperature shutdown. Each gate driver monitors independently its external MOSFET drain-source voltage for fault conditions.

The device is housed in a VQFN-48 with exposed pad supporting lead tip inspection. The package provides a good thermal performance and minimizes the required PCB space.

### 2 Features

- 8 Half-Bridge (HB) gate drivers for external N-channel MOSFETs
- Control of reverse battery protection MOSFET
- Adaptive MOSFET gate control
  - Improved electromagnetic emission
  - Reduced switching losses in PWM mode
- 24-bit Serial Peripheral Interface
- Two current sense amplifiers with configurable gain
  - High-side and low-side capable for protection and diagnosis
- Drain-source monitoring for short circuit detection
- Overtemperature warning and shutdown
- Timeout watchdog
- Detailed off-state diagnostic (open load, short circuit to battery or short circuit to GND) via SPI
- Three PWM inputs
  - High-side and low-side PWM capable
  - Current sense overcurrent for each HB independently
  - Active free-wheeling
  - Up to 25 kHz PWM frequency
- Low current consumption in sleep mode

- Configurable low-side 1-8 brake with short circuit detection in sleep mode and normal mode
- Configurable VS overvoltage detection in sleep mode
- Limp home mode
- Chopping mode for each current sense amplifier
- Leadless power package with support of optical lead tip inspection
- Green Product (RoHS compliant)
- AEC Qualified (Grade 1)

### 3 Applications

- Seat control and extended functions (steering column adjustment, gas pedal adjustment)
- Power lift gate
- Central door lock
- Body control module (cargo cover, washer pump, window lift, rear wiper ...)

### 4 Device Information

| ORDER NUMBER | PACKAGE    | BODY SIZE         |
|--------------|------------|-------------------|
| SC77708QQDAR | 48 pin QFN | 7mm x 7mm x 0.9mm |



## 5 Revision History

| Revision | Date       | Page(s) changed | Changes Description |
|----------|------------|-----------------|---------------------|
| V0.1     | 2024.01.04 | New             | New Spec.           |
| V1.3     | 2025.08.15 | All             | Reg Map Updated     |
|          |            |                 |                     |
|          |            |                 |                     |
|          |            |                 |                     |
|          |            |                 |                     |
|          |            |                 |                     |



## 6 Block diagram

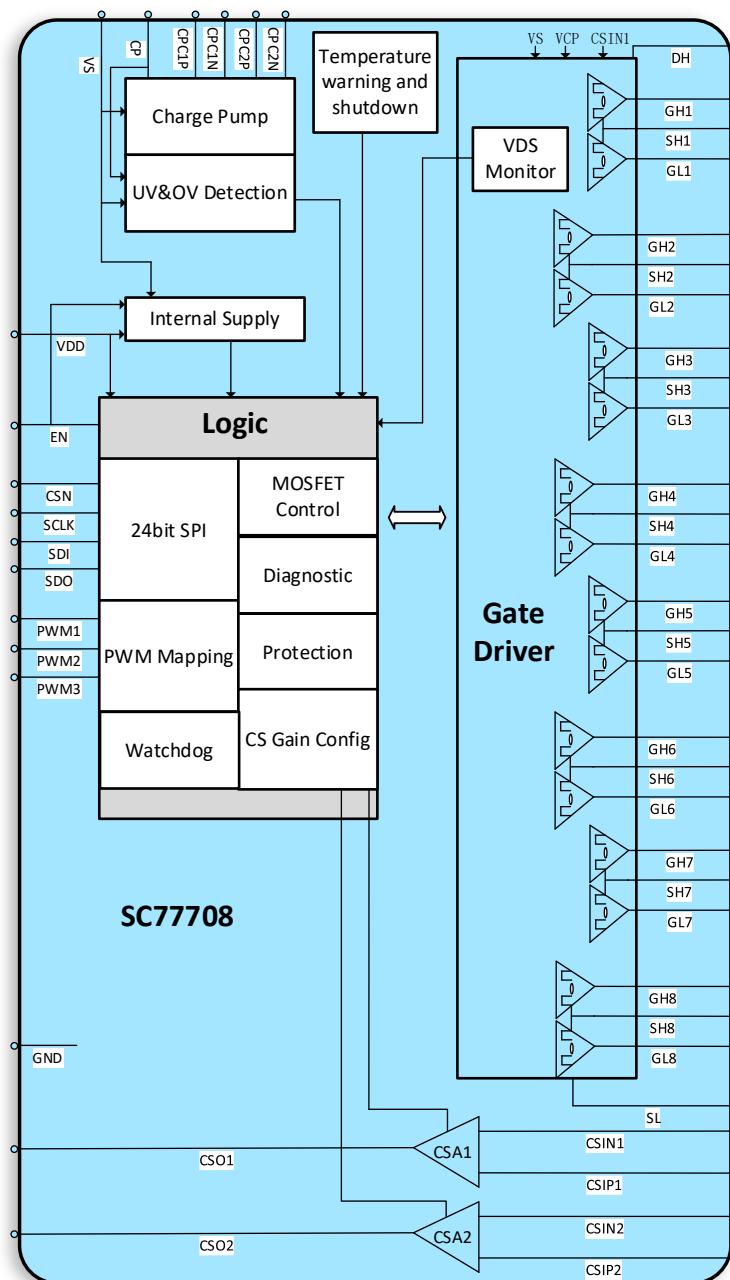


Figure 6-1. Block diagram



## 7 Terminal Configuration and Functions

### TOP VIEW

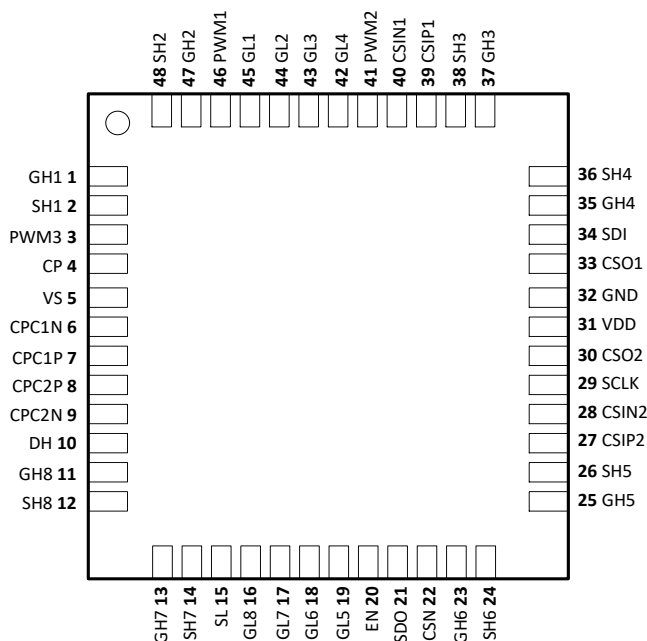


Figure 7-1. PIN Map (Top View)

| TERMINAL |       | I/O | DESCRIPTION                                                                                                                                  |
|----------|-------|-----|----------------------------------------------------------------------------------------------------------------------------------------------|
| NUMBER   | NAME  |     |                                                                                                                                              |
| 1        | GH1   | O   | <b>Gate high-side 1.</b><br>Analog I/O pin to turn on/off high-side MOSFET 1. Connect to the gate of high-side MOSFET 1                      |
| 2        | SH1   | O   | <b>Source high-side 1.</b><br>Connection to source of high-side MOSFET 1.                                                                    |
| 3        | PWM3  | I   | <b>PWM input 3</b>                                                                                                                           |
| 4        | CP    | I   | <b>Charge pump output</b>                                                                                                                    |
| 5        | VS    | I   | <b>Supply Voltage.</b><br>Device supply voltage. Connect this pin to the supply (battery) voltage with a reverse battery protection circuit. |
| 6        | CPC1N | I   | <b>Negative connection to Charge Pump Capacitor 1</b>                                                                                        |
| 7        | CPC1P | I   | <b>Positive connection to Charge Pump Capacitor 1</b>                                                                                        |
| 8        | CPC2P | I   | <b>Positive connection to Charge Pump Capacitor 2</b>                                                                                        |



|    |       |   |                                                                              |
|----|-------|---|------------------------------------------------------------------------------|
| 9  | CPC2N | I | Negative connection to Charge Pump Capacitor 2                               |
| 10 | DH    | I | Drain input for high-sides<br>Input for the drains of high-side MOSFETs.     |
| 11 | GH8   | O | Gate high-side 8                                                             |
| 12 | SH8   | O | Source high-side 8                                                           |
| 13 | GH7   | O | Gate high-side 7                                                             |
| 14 | SH7   | O | Source high-side 7                                                           |
| 15 | SL    | I | Source low-side.<br>Common connection to the source of the low-side MOSFETs. |
| 16 | GL8   | O | Gate low-side 8                                                              |
| 17 | GL7   | O | Gate low-side 7                                                              |
| 18 | GL6   | O | Gate low-side 6                                                              |
| 19 | GL5   | O | Gate low-side 5                                                              |
| 20 | EN    | I | Enable input with internal pull-down                                         |
| 21 | SDO   | O | Serial Data Output                                                           |
| 22 | CSN   | I | Chip Select Not with internal pull-up                                        |
| 23 | GH6   | O | Gate high-side 6                                                             |
| 24 | SH6   | O | Source high-side 6                                                           |
| 25 | GH5   | O | Gate high-side 5                                                             |
| 26 | SH5   | O | Source high-side 5                                                           |
| 27 | CSIP2 | I | Non-Inverting input of the Current Sense Amplifier 2                         |
| 28 | CSIN2 | I | Inverting input of the Current Sense Amplifier 2                             |
| 29 | SCLK  | I | Serial Clock Input with internal pull-down                                   |
| 30 | CSO2  | O | Current Sense Amplifier Output 2                                             |
| 31 | VDD   | I | Logic supply                                                                 |
| 32 | GND   | I | Ground connection                                                            |
| 33 | CSO1  | O | Current Sense Amplifier Output1                                              |
| 34 | SDI   | I | Serial Data Input with internal pull-down                                    |



|    |       |   |                                                                                                                                                        |
|----|-------|---|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 35 | GH4   | O | Gate high-side 4                                                                                                                                       |
| 36 | SH4   | O | Source high-side 4                                                                                                                                     |
| 37 | GH3   | O | Gate high-side 3                                                                                                                                       |
| 38 | SH3   | O | Source high-side 3                                                                                                                                     |
| 39 | CSIP1 | I | Non-inverting input of the Current Sense Amplifier 1                                                                                                   |
| 40 | CSIN1 | I | Inverting input of the Current Sense Amplifier 1. This pin can be used as reference for the high-side MOSFET drain if CSA1 is configured as high-side. |
| 41 | PWM2  | I | PWM input 2                                                                                                                                            |
| 42 | GL4   | O | Gate low-side 4                                                                                                                                        |
| 43 | GL3   | O | Gate low-side 3                                                                                                                                        |
| 44 | GL2   | O | Gate low-side 2                                                                                                                                        |
| 45 | GL1   | O | Gate low-side 1                                                                                                                                        |
| 46 | PWM1  | I | PWM input 1                                                                                                                                            |
| 47 | GH2   | O | Gate high-side 2                                                                                                                                       |
| 48 | SH2   | O | Source high-side 2                                                                                                                                     |
|    | E.P.  | - | Exposed pad<br>For cooling purpose only, do not use as electrical GND.                                                                                 |

Table 7-1 Pin Function Description



## 8 Specifications

### 8.1 Absolute Maximum Ratings

$T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , all voltages with respect to ground, positive current flowing into pin, over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

| PARAMETER                                 |                                                                     | MIN          | MAX          | Unit               |
|-------------------------------------------|---------------------------------------------------------------------|--------------|--------------|--------------------|
| Voltage range at terminals <sup>(2)</sup> | Supply voltage                                                      | -0.3         | 40           | V                  |
|                                           | PWM input voltages (PWMx), ( $ I  < 10\text{ mA}$ )                 | -0.3         | $V_{DD}+0.3$ | V                  |
|                                           | Logic input voltages (SDI, SCLK, CSN, EN), ( $ I  < 10\text{ mA}$ ) | -0.3         | $V_{DD}+0.3$ | V                  |
|                                           | Voltage range and SDO, ( $ I  < 10\text{ mA}$ )                     | -0.3         | $V_{DD}+0.3$ | V                  |
|                                           | Voltage range at CSIPx and CSINx                                    | -8           | 40           | V                  |
|                                           | Differential input voltage range CSIPx - CSINx                      | -8           | 8            | V                  |
|                                           | Voltage range at DH                                                 | -0.3         | 40           | V                  |
|                                           | Voltage range at SL                                                 | -8           | 6            | V                  |
|                                           | Voltage range at SHx                                                | -8           | 48           | V                  |
|                                           | Voltage range at GHx                                                | -8           | 48           | V                  |
|                                           | Voltage range at GLx                                                | -8           | 24           | V                  |
|                                           | Voltage difference between GLx and SL                               | -0.3         | 16           | V                  |
|                                           | Voltage difference between GHx and SHx                              | -1           | 16           | V                  |
|                                           | Voltage range at charge pump pins CP                                | $V_S-0.3$    | $V_S+15$     | V                  |
|                                           | Voltage range at charge pump pins CPC1N, CPC1P, CPC2N, CPC2P        | $V_{CP}-0.3$ | $V_{CP}+0.3$ | V                  |
|                                           | Logic supply voltage                                                | -0.3         | 5.5          | V                  |
|                                           | Voltage at CSOx                                                     | -0.3         | $V_{DD}+0.3$ | V                  |
| $T_J$                                     | Operating junction temperature range                                | -40          | 150          | $^{\circ}\text{C}$ |
| $T_{stg}$                                 | Storage temperature range                                           | -55          | 150          | $^{\circ}\text{C}$ |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

Table 8-1 Absolute maximum ratings

### 8.2 Handling Ratings

| PARAMETER          | DEFINITION                                               |                           | MIN | MAX | UNIT |
|--------------------|----------------------------------------------------------|---------------------------|-----|-----|------|
| ESD <sup>(1)</sup> | Human body model (HBM) ESD stress voltage <sup>(2)</sup> | All pins except VS and DH | -2  | 2   | kV   |



|  |                                                              |                             |      |     |    |
|--|--------------------------------------------------------------|-----------------------------|------|-----|----|
|  |                                                              | VS and DH pins vs GND       | -4   | 4   | kV |
|  | Charged device model (CDM) ESD stress voltage <sup>(3)</sup> | Corner pins                 | -500 | 500 | V  |
|  |                                                              | All pins except corner pins | -750 | 750 | V  |

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Table 8-2 ESD data

### 8.3 Recommended Operating Conditions

| PARAMETER                    |                                           | MIN | TYP | MAX                  | UNIT |
|------------------------------|-------------------------------------------|-----|-----|----------------------|------|
| $V_{S(nor)}$                 | Supply voltage range for normal operation | 6   |     | 28                   | V    |
| $V_{S(ext)}$                 | Extended supply voltage range             | 5.5 |     | 6                    | V    |
| $V_{S(ext)}$                 | Extended supply voltage range             | 28  |     | $V_{SOV\_OFF2(max)}$ | V    |
| $dV_S/dt$                    | Supply voltage transients slew rate       | -10 |     | 10                   | V/us |
| $V_{DD}$                     | Logic supply voltage                      | 3   |     | 5.5                  | V    |
| $V_{SDI}, V_{SCLK}, V_{CSN}$ | SPI logic input voltage                   | 0   |     | $V_{DD}$             | V    |
| $T_A$                        | Operating ambient temperature             | -40 |     | 125                  | °C   |
| $T_J$                        | Operating junction temperature            | -40 |     | 150                  | °C   |

Table 8-3 Recommended operation conditions



## 8.4 Thermal Information

| THERMAL RESISTANCE <sup>(1)</sup> |                                        | QFN-32 (4mm x 4mm) | UNIT |
|-----------------------------------|----------------------------------------|--------------------|------|
| $\Theta_{JA}$                     | Junction to ambient thermal resistance | TBD                | °C/W |
| $\Theta_{JC}$                     | Junction to case resistance            | TBD                | °C/W |

(1) Measured on JESD51-7, 4-layer PCB.

Table 8-4 Thermal data

## 8.5 Electrical Characteristics

$V_S = 6.0\text{ V}$  to  $18\text{ V}$  if  $V_{SOVTH} = 0$ ,  $V_S = 6.0\text{ V}$  to  $28\text{ V}$  if  $V_{SOVTH} = 1$ ;  $V_{DD} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin, unless otherwise noted.

| PARAMETER                                                       | TEST CONDITIONS                                                                                                                                              | MIN | TYP | MAX  | UNIT |
|-----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| <b>CURRENT CONSUMPTION, EN = LOW</b>                            |                                                                                                                                                              |     |     |      |      |
| $I_{SQ}$                                                        | Supply quiescent current<br>$T_j < 85^\circ\text{C}$ , $V_S = 13.5\text{V}$<br>$PASS\_MOD=00b$ , $PASS\_VDS=0b$                                              |     | 3   | 5    | uA   |
| $I_{SQ2}$                                                       | Supply quiescent current<br>$T_j < 85^\circ\text{C}$ , $V_S < 25\text{V}$<br>$PASS\_MOD=00b$ , $PASS\_VDS=0b$                                                |     | 4   | 7    | uA   |
| $I_{SQ\_BRAKE}$                                                 | Additional supply quiescent current, brake enabled<br>$T_j < 85^\circ\text{C}$ , $V_S = 13.5\text{V}$<br>$PASS\_MOD=01b$ or $10b$ or $11b$ or $PASS\_VDS=1b$ |     | 8   | 10.5 | uA   |
| $I_{DD\_Q}$                                                     | Logic Supply quiescent current<br>$T_j < 85^\circ\text{C}$                                                                                                   |     | 0.1 | 2    | uA   |
| $I_{DD\_Q} + I_{SQ}$                                            | Total quiescent current<br>$T_j < 85^\circ\text{C}$ , $V_S = 13.5\text{V}$<br>$PASS\_MOD=00b$ , $PASS\_VDS=0b$                                               |     | 3   | 8    | uA   |
| $t_{DSLEEP}$                                                    | Sleep filter time<br>$BD\_PASS = 0$                                                                                                                          |     | 40  |      | us   |
| $t_{ENL\_FILT}$                                                 | EN Low filter time                                                                                                                                           | 1   |     | 8    | us   |
| $V_{SLEEP\_SET}$                                                | VS for LS1-4 setting                                                                                                                                         |     |     | 5.5  | V    |
| <b>CURRENT CONSUMPTION, EN = HIGH</b>                           |                                                                                                                                                              |     |     |      |      |
| $I_{S1}$                                                        | Supply current<br>$HBxVDSTH = 001b$ , $BD\_PASS = 0$ ,<br>$I_{CP} = 0\text{mA}$                                                                              |     | 59  | 64   | mA   |
| $I_{S4}$                                                        | Supply current<br>$V_S = 6\text{V}$ , $HBxVDSTH = 001b$ ,<br>$BD\_PASS = 0$ , $I_{CP} = 0\text{mA}$                                                          |     | 55  | 60   | mA   |
| $I_{S\_BD\_PASS}$                                               | Supply current<br>$HBxMODE=00b$ , $BD\_PASS = 1$                                                                                                             |     | 40  | 45   | mA   |
| $I_{DD1}$                                                       | Logic supply current<br>SPI not active, CSA1 and CSA2 off,<br>all $I_{PDDiag}$ off, $BD\_PASS=0$                                                             |     | 6.6 | 7.5  | mA   |
| $I_{DD2}$                                                       | Logic supply current<br>All CSA on, $V_{CSOX} = 4.5\text{V}$ , LS shunt,<br>$CCSO = 1$ , $CSAxL = 0$ , $I_{PDDiag}$ off                                      |     | 10  | 11   | mA   |
| <b>VS WITH ACTIVE BRIDGE DRIVER (<math>BD\_PASS = 0</math>)</b> |                                                                                                                                                              |     |     |      |      |
| $V_{SUV\ ON}$                                                   | UV switch ON voltage<br>$V_S$ increasing                                                                                                                     |     |     | 5.5  | V    |
| $V_{SUV\ OFF}$                                                  | UV switch OFF voltage<br>$V_S$ decreasing                                                                                                                    | 4   | 4.5 | 5    | V    |
| $V_{SUV\ HY}$                                                   | UV ON/OFF hysteresis<br>$V_{SUV\ ON} - V_{SUV\ OFF}$                                                                                                         |     | 0.5 |      | V    |
| $V_{SOV\ OFF1}$                                                 | OV switch OFF voltage<br>$V_{SOVTH} = 0$<br>$V_S$ increasing                                                                                                 | 19  |     | 21   | V    |



|                        |                                                  |                                                      |                     |     |      |     |
|------------------------|--------------------------------------------------|------------------------------------------------------|---------------------|-----|------|-----|
| V <sub>SOV ON1</sub>   | OV switch ON voltage<br>VSOVTH = 0               | V <sub>S</sub> decreasing                            | 18                  | 20  | V    |     |
| V <sub>SOV OFF2</sub>  | OV switch OFF voltage<br>VSOVTH = 1              | V <sub>S</sub> increasing                            | 29                  | 31  | V    |     |
| V <sub>SOV ON2</sub>   | OV switch ON voltage<br>VSOVTH = 1               | V <sub>S</sub> decreasing                            | 28                  | 30  | V    |     |
| V <sub>SOV HY</sub>    | OV ON/OFF hysteresis                             | V <sub>SOV ON</sub> - V <sub>SOV OFF</sub>           | 1                   |     | V    |     |
| t <sub>VSUV_FILT</sub> | VS undervoltage filter time                      |                                                      | 7                   | 10  | 13   | us  |
| t <sub>VSOV_FILT</sub> | VS overvoltage filter time                       |                                                      | 7                   | 10  | 13   | us  |
| t <sub>D_CPVSOV</sub>  | CP turn-off delay after VS overvoltage detection |                                                      | 12.8                | 16  | 19.2 | us  |
| VDD                    |                                                  |                                                      |                     |     |      |     |
| V <sub>DD POR</sub>    | VDD Power-On-Reset                               | V <sub>DD</sub> increasing                           | 2.4                 | 2.6 | 2.8  | V   |
| V <sub>DD POFFR</sub>  | VDD Power-Off-Reset                              | V <sub>DD</sub> decreasing                           | 2.3                 | 2.5 | 2.7  | V   |
| V <sub>DD POR HY</sub> | VDD Power-On-Reset Hysteresis                    | V <sub>DD POR</sub> - V <sub>DD POFFR</sub>          |                     | 0.1 |      | V   |
| PWMx, EN               |                                                  |                                                      |                     |     |      |     |
| V <sub>ENH</sub>       | EN high voltage                                  |                                                      | 0.7V <sub>DD</sub>  |     |      | V   |
| V <sub>ENL</sub>       | EN low voltage                                   |                                                      | 0.3V <sub>DD</sub>  |     |      | V   |
| V <sub>ENHY</sub>      | EN hysteresis                                    |                                                      | 0.12V <sub>DD</sub> |     |      | V   |
| R <sub>PD_EN</sub>     | EN pull-down resistor                            |                                                      | 20                  | 40  | 60   | kΩ  |
| V <sub>PWMH</sub>      | PWMx high voltage                                |                                                      | 0.7V <sub>DD</sub>  |     |      | V   |
| V <sub>PWML</sub>      | PWMx low voltage                                 |                                                      | 0.3V <sub>DD</sub>  |     |      | V   |
| V <sub>PWMHY</sub>     | PWMx hysteresis                                  |                                                      | 0.12V <sub>DD</sub> |     |      | V   |
| R <sub>PD_PWMx</sub>   | PWMx pull-down resistor                          |                                                      | 20                  | 40  | 60   | kΩ  |
| CHARGE PUMP            |                                                  |                                                      |                     |     |      |     |
| f <sub>CP</sub>        | Charge Pump Frequency                            |                                                      | 400                 | 450 |      | kHz |
| V <sub>CPmin</sub>     | Output Voltage VCP vs. VS                        | V <sub>S</sub> = 6V, I <sub>CP</sub> = - 6mA         | 8.5                 |     |      | V   |
| V <sub>CP1</sub>       | Regulated output voltage VCP vs. VS, CPSTGA = 0  | 8V < V <sub>S</sub> < 28V, I <sub>CP</sub> = - 12mA  | 11                  | 15  | 17   | V   |
| V <sub>CP2</sub>       | Regulated output voltage VCP vs. VS, CPSTGA = 1  | 18V < V <sub>S</sub> < 28V, I <sub>CP</sub> = - 12mA | 12                  | 15  | 17   | V   |
| t <sub>ON_VCP1</sub>   | Turn-on time, CPSTGA = 0                         | 8V < V <sub>S</sub> < 28V (25%)                      | 10                  | 40  | 80   | us  |
| t <sub>RISE_VCP1</sub> | Rise time, CPSTGA = 0                            | 8V < V <sub>S</sub> < 28V (25%-75%)                  | 10                  | 60  | 100  | us  |
| t <sub>ON_VCP2</sub>   | Turn-on time, CPSTGA = 1                         | 18V < V <sub>S</sub> < 28V (25%)                     | 10                  | 40  | 80   | us  |
| t <sub>RISE_VCP2</sub> | Rise time, CPSTGA = 1                            | 18V < V <sub>S</sub> < 28V (25%-75%)                 | 10                  | 60  | 100  | us  |
| V <sub>CPUV1</sub>     | Charge Pump Undervoltage (referred to VS)        | CPUVTH = 0, VCP falling                              | 5.5                 | 6   | 6.5  | V   |
| V <sub>CPUV2</sub>     | Charge Pump Undervoltage (referred to VS)        | CPUVTH = 1, VCP falling                              | 6.5                 | 7   | 7.5  | V   |



|                      |                                                        |                                                       |     |      |    |    |
|----------------------|--------------------------------------------------------|-------------------------------------------------------|-----|------|----|----|
| $V_{\text{CPSO DS}}$ | Automatic switch over dual to single stage charge pump | CPSTGA = 1                                            | 18  | 19.5 | 21 | V  |
| $V_{\text{CPSO SD}}$ | Automatic switch over single to dual stage charge pump | CPSTGA = 1                                            | 15  | 16.5 | 18 | V  |
| $V_{\text{CPSO HY}}$ | Charge pump switch over hysteresis                     | CPSTGA = 1, $V_{\text{CPSO DS}} - V_{\text{CPSO SD}}$ | 3   |      |    | V  |
| $t_{\text{CPUV}}$    | Charge Pump Undervoltage Filter Time                   |                                                       | 51  | 64   | 77 | us |
| $I_{\text{CPOC1}}$   | Charge pump minimum output current                     | $V_S = 13.5 \text{ V}$ , CPSTGA = 0                   | -12 |      |    | mA |
| $I_{\text{CPOC2}}$   | Charge pump minimum output current                     | $V_S = 18 \text{ V}$ , CPSTGA = 1                     | -12 |      |    | mA |

Table 8-5 Electrical parameter

$V_S = 6.0 \text{ V}$  to  $18 \text{ V}$  if  $\text{VSOVTH} = 0$ ,  $V_S = 6.0 \text{ V}$  to  $28 \text{ V}$  if  $\text{VSOVTH} = 1$ ;  $V_{\text{DD}} = 3.0 \text{ V}$  to  $5.5 \text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ,  $V_{\text{CP}} > V_S + 8.5 \text{ V}$ , all voltages with respect to ground, positive current flowing into pin. Positive current flowing into pin except for  $I_{\text{GLx}}$  and  $I_{\text{GHx}}$  unless otherwise noted.

| PARAMETER            |                                                                       | TEST CONDITIONS                                                                                                  | MIN                  | TYP  | MAX                | UNIT |
|----------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|----------------------|------|--------------------|------|
| COMPARATORS          |                                                                       |                                                                                                                  |                      |      |                    |      |
| V <sub>SHH</sub>     | SHx High Threshold                                                    |                                                                                                                  | V <sub>S</sub> - 2.5 |      | V <sub>S</sub> - 2 | V    |
| V <sub>SHL</sub>     | SHx Low Threshold                                                     | Referred to GND                                                                                                  | 2                    |      | 2.5                | V    |
| t <sub>SHx</sub>     | SHx comparator delay                                                  |                                                                                                                  | 5                    |      | 30                 | ns   |
| MOSFET DRIVER OUTPUT |                                                                       |                                                                                                                  |                      |      |                    |      |
| V <sub>GH1</sub>     | High Level Output Voltage<br>GHx vs. SHx and GLx vs. SL,<br>CPSTGA= 0 | V <sub>S</sub> > 8 V, C <sub>Load</sub> = 10 nF, I <sub>CP</sub> = - 12 mA                                       | 10                   |      | 12                 | V    |
| V <sub>GH3</sub>     | High Level Output Voltage<br>GHx vs. SHx and GLx vs. SL,<br>CPSTGA= 0 | V <sub>S</sub> > 6 V, C <sub>Load</sub> = 10 nF, I <sub>CP</sub> = - 6 mA                                        | 7                    |      |                    | V    |
| V <sub>GH4</sub>     | High Level Output Voltage<br>GHx vs. SHx and GLx vs. SL,<br>CPSTGA= 1 | V <sub>S</sub> > 18 V, C <sub>Load</sub> = 10 nF<br>I <sub>CP</sub> = - 12 mA                                    | 10                   |      | 12                 | V    |
| I <sub>CHG0</sub>    | Discharge current                                                     | I <sub>CHG</sub> = 0 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≤ V <sub>GS(ON)1</sub>            | 0.4                  | 1    | 1.6                | mA   |
| I <sub>CHG6</sub>    | Discharge current                                                     | I <sub>CHG</sub> = 6 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≤ V <sub>GS(ON)1</sub>            | 5                    | 8    | 11                 | mA   |
| I <sub>CHG6</sub>    | Discharge current                                                     | I <sub>CHG</sub> = 14 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≤ V <sub>GS(ON)1</sub>           | 21                   | 30   | 38.4               | mA   |
| I <sub>CHG30</sub>   | Discharge current                                                     | I <sub>CHG</sub> = 30 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≤ V <sub>GS(ON)1</sub>           | 72                   | 96   | 120                | mA   |
| I <sub>DCHG0</sub>   | Discharge current                                                     | I <sub>DCHG</sub> = 0 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≥ V <sub>GS(OFF)1</sub>          | -1.6                 | -1   | -0.4               | mA   |
| I <sub>DCHG6</sub>   | Discharge current                                                     | I <sub>DCHG</sub> = 6 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≥ V <sub>GS(OFF)1</sub>          | -13                  | -9.4 | -5.8               | mA   |
| I <sub>DCHG14</sub>  | Discharge current                                                     | I <sub>DCHG</sub> = 14 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≥ V <sub>GS(OFF)1</sub>         | -41                  | -32  | -23                | mA   |
| I <sub>DCHG30</sub>  | Discharge current                                                     | I <sub>DCHG</sub> = 30 <sub>D</sub> , C <sub>Load</sub> = 10 nF, V <sub>GS</sub> ≥ V <sub>GS(OFF)1</sub>         | -119                 | -95  | -71                | mA   |
| R <sub>GGND</sub>    | Passive discharge resistance<br>between GHx/GLx and GND               |                                                                                                                  | 10                   | 20   | 30                 | kΩ   |
| R <sub>SHGND</sub>   | Resistor between SHx and GND                                          |                                                                                                                  | 10                   | 20   | 30                 | kΩ   |
| R <sub>ONCCP</sub>   | Low RDSON mode                                                        | V <sub>S</sub> = 13.5 V, V <sub>CP</sub> = V <sub>S</sub> + 14 V, I <sub>CHG</sub> = I <sub>DCHG</sub> = 31(max) | 22                   |      | 40                 | Ω    |



| GATE DRIVERS DYNAMIC PARAMETERS |                                              |                                   |     |      |      |    |
|---------------------------------|----------------------------------------------|-----------------------------------|-----|------|------|----|
| $V_{GS(ON)1}$                   | External MOSFET gate-to-source voltage - ON  | $V_S \geq 8V$<br>$ICHGx \leq 14D$ | 7   |      |      | V  |
| $V_{GS(ON)2}$                   | External MOSFET gate-to-source voltage - ON  | $V_S \geq 8V$<br>$ICHGx \geq 15D$ | 6   |      |      | V  |
| $V_{GS(OFF)1}$                  | External MOSFET gate-to-source voltage - OFF | $IDCHGx \leq 14D$                 |     | 2    |      | V  |
| $V_{GS(OFF)2}$                  | External MOSFET gate-to-source voltage - OFF | $IDCHGx \geq 15D$                 |     | 5    |      | V  |
| $t_{PWM\_SYNCH}$                | PWM synchronization delay                    |                                   | 50  | 150  |      | ns |
| $t_{PCHG00}$                    | Pre-charge time                              | TPCHG = 00B                       | 100 | 125  | 150  | ns |
| $t_{PCHG01}$                    | Pre-charge time                              | TPCHG = 01B                       | 200 | 250  | 300  | ns |
| $t_{PCHG10}$                    | Pre-charge time                              | TPCHG = 10B                       | 400 | 500  | 600  | ns |
| $t_{PCHG11}$                    | Pre-charge time                              | TPCHG = 11B                       | 800 | 1000 | 1200 | ns |
| $t_{DPCHG00}$                   | Pre-discharge time                           | TDPCHG = 00B                      | 100 | 125  | 150  | ns |
| $t_{DPCHG01}$                   | Pre-discharge time                           | TDPCHG = 01B                      | 200 | 250  | 300  | ns |
| $t_{DPCHG10}$                   | Pre-discharge time                           | TDPCHG = 10B                      | 400 | 500  | 600  | ns |
| $t_{DPCHG11}$                   | Pre-discharge time                           | TDPCHG = 11B                      | 800 | 1000 | 1200 | ns |

Table 8-6 Gate Driver Parameter

$V_S = 6.0V$  to  $18V$  if  $V_{SOVTH} = 0$ ,  $V_S = 6.0V$  to  $28V$  if  $V_{SOVTH} = 1$ ;  $V_{DD} = 3.0V$  to  $5.5V$ ,  $T_j = -40^\circ C$  to  $150^\circ C$ ,  $V_{CP} > V_S + 8.5V$ , all voltages with respect to ground, positive current flowing into pin. Positive current flowing into pin except for  $I_{GLx}$  and  $I_{GHx}$  unless otherwise noted.

| PARAMETER                          |                                    | TEST CONDITIONS                                | MIN  | TYP  | MAX  | UNIT |
|------------------------------------|------------------------------------|------------------------------------------------|------|------|------|------|
| WATCHDOG                           |                                    |                                                |      |      |      |      |
| T <sub>WDPER1</sub>                | Watchdog period 1                  | WDPER = 0                                      | 40   | 50   | 60   | ms   |
| T <sub>WDPER2</sub>                | Watchdog period 2                  | WDPER = 1                                      | 160  | 200  | 240  | ms   |
| OFF-STATE OPEN LOAD DIAGNOSIS      |                                    |                                                |      |      |      |      |
| I <sub>PUDiag</sub>                | Pull-up diagnosis current          |                                                | -420 | -330 | -240 | uA   |
| I <sub>PDDiag</sub>                | Pull-down diagnosis current        |                                                | 1000 | 1500 | 2000 | uA   |
| I <sub>Diag_ratio</sub>            | Diagnosis current ratio            | Ratio I <sub>PDDiag</sub> /I <sub>PUDiag</sub> | 2.5  | 4.5  |      |      |
| DRAIN SOURCE MONITORING THRESHOLD  |                                    |                                                |      |      |      |      |
| V <sub>VDSMONTH0</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 000B                           | 0.12 | 0.15 | 0.18 | V    |
| V <sub>VDSMONTH1</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 001B                           | 0.16 | 0.2  | 0.24 | V    |
| V <sub>VDSMONTH2</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 010B                           | 0.2  | 0.25 | 0.3  | V    |
| V <sub>VDSMONTH3</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 011B                           | 0.24 | 0.3  | 0.36 | V    |
| V <sub>VDSMONTH4</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 100B                           | 0.32 | 0.4  | 0.48 | V    |
| V <sub>VDSMONTH5</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 101B                           | 0.4  | 0.5  | 0.62 | V    |
| V <sub>VDSMONTH6</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 110B                           | 0.48 | 0.6  | 0.72 | V    |
| V <sub>VDSMONTH7</sub>             | Drain-source monitoring thresholds | HBxVDSTH[2:0] = 111B                           | 1.6  | 2    | 2.4  | V    |
| DRAIN-SOURCE MONITORING BLANK TIME |                                    |                                                |      |      |      |      |
| t <sub>DSMON_BLK0</sub>            | DS monitoring blank time           | TBLANKx[2:0] = 000B                            | 500  | 625  | 850  | ns   |
| t <sub>DSMON_BLK1</sub>            | DS monitoring blank time           | TBLANKx[2:0] = 001B                            | 0.8  | 1    | 1.2  | us   |



|                                                                                                                                       |                                                                                          |                                                   |                |      |      |            |
|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|---------------------------------------------------|----------------|------|------|------------|
| $t_{DSMON\_BLK2}$                                                                                                                     | DS monitoring blank time                                                                 | TBLANKx[2:0] = 010B                               | 1              | 1.25 | 1.5  | us         |
| $t_{DSMON\_BLK3}$                                                                                                                     | DS monitoring blank time                                                                 | TBLANKx[2:0] = 011B                               | 1.2            | 1.5  | 1.8  | us         |
| $t_{DSMON\_BLK4}$                                                                                                                     | DS monitoring blank time                                                                 | TBLANKx[2:0] = 100B                               | 1.6            | 2    | 2.4  | us         |
| $t_{DSMON\_BLK5}$                                                                                                                     | DS monitoring blank time                                                                 | TBLANKx[2:0] = 101B                               | 2.4            | 3    | 3.6  | us         |
| $t_{DSMON\_BLK6}$                                                                                                                     | DS monitoring blank time                                                                 | TBLANKx[2:0] = 110B                               | 3.2            | 4    | 4.8  | us         |
| $t_{DSMON\_BLK7}$                                                                                                                     | DS monitoring blank time                                                                 | TBLANKx[2:0] = 111B                               | 12.8           | 16   | 19.2 | us         |
| <b>DRAIN-SOURCE MONITORING FILTER TIME</b>                                                                                            |                                                                                          |                                                   |                |      |      |            |
| $t_{DSMON\_FILT0}$                                                                                                                    | DS monitoring filter time                                                                | TFVDS[1:0] = 00B                                  | 0.4            | 0.5  | 0.85 | us         |
| $t_{DSMON\_FILT1}$                                                                                                                    | DS monitoring filter time                                                                | TFVDS[1:0] = 01B                                  | 0.8            | 1    | 1.4  | us         |
| $t_{DSMON\_FILT2}$                                                                                                                    | DS monitoring filter time                                                                | TFVDS[1:0] = 10B                                  | 1.6            | 2    | 2.4  | us         |
| $t_{DSMON\_FILT3}$                                                                                                                    | DS monitoring filter time                                                                | TFVDS[1:0] = 11B                                  | 2.4            | 3    | 3.6  | us         |
| <b>CROSS-CURRENT PROTECTION TIME</b>                                                                                                  |                                                                                          |                                                   |                |      |      |            |
| $t_{HBxCCP0}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 000B                              | 300            | 375  | 450  | ns         |
| $t_{HBxCCP1}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 001B                              | 500            | 625  | 750  | ns         |
| $t_{HBxCCP2}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 010B                              | 1              | 1.25 | 1.5  | us         |
| $t_{HBxCCP3}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 011B                              | 1.2            | 1.5  | 1.8  | us         |
| $t_{HBxCCP4}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 100B                              | 1.6            | 2    | 2.4  | us         |
| $t_{HBxCCP5}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 101B                              | 2.4            | 3    | 3.6  | us         |
| $t_{HBxCCP6}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 110B                              | 3.2            | 4    | 4.8  | us         |
| $t_{HBxCCP7}$                                                                                                                         | Cross current protection time                                                            | THBxCCP [2:0] = 111B                              | 12.8           | 16   | 19.2 | us         |
| <b>Bridge driver passive mode: BD_PASS = 1 and all HBxMODE[1:0] = 00B or 11B, or EN = Low or <math>V_{DD} &lt; V_{DD\_POR}</math></b> |                                                                                          |                                                   |                |      |      |            |
| $V_{SOV\_PASS\_OFF}$                                                                                                                  | Passive VS overvoltage                                                                   | $V_S$ increasing PASS_MOD=10B                     | 28             | 31.5 | 35   | V          |
| $V_{SOV\_PASS\_HY}$                                                                                                                   | Passive VS overvoltage hysteresis                                                        |                                                   | 1              | 2.5  | 4    | V          |
| $R_{PWM3\_OD}$                                                                                                                        | PWM3 open drain resistance                                                               |                                                   | 4              | 5.5  | 7    | k $\Omega$ |
| $t_{ON\_BD\_PASS}$                                                                                                                    | Passive turn-on time                                                                     | Cap = 10 nF, $V_{Cap}$ = 5 V, $V_S > 8$ V         |                | 4.5  | 10   | us         |
| $t_{OFF\_BD\_PASS}$                                                                                                                   | Passive Turn-off time                                                                    | Cap = 10 nF, $V_{Cap}$ down to 1.5 V, $V_S > 8$ V |                | 0.7  | 2    | us         |
| $V_{GLX\_BRAKE}$                                                                                                                      | Passive LS gate voltage                                                                  | $V_{GLx} - V_{SL}$ , x = 1 to 4, $V_S > 8$ V      | 5              |      | 10   | V          |
| $t_{BLK\_BD\_PASS}$                                                                                                                   | Passive turn-on blank time                                                               |                                                   | 10             | 20   | 30   | us         |
| $V_{PWM1H\_BD\_PASS}$                                                                                                                 | PWM1 high voltage, bridge driver passive                                                 |                                                   | 0.5            | 1.3  | 2    | V          |
| $t_{DSMON\_FILT\_BD\_PASS}$                                                                                                           | Passive VDS filter time                                                                  |                                                   | 0.5            | 1    | 2    | us         |
| $V_{VDSMON\_BD\_PASS}$                                                                                                                | Passive drain-source monitoring thresholds                                               | PASS_VDS=1B                                       | 0.3            | 0.6  | 0.9  | V          |
| <b>CURRENT SENSE AMPLIFIER</b>                                                                                                        |                                                                                          |                                                   |                |      |      |            |
| VCM                                                                                                                                   | Operating common mode input voltage range referred to GND (CSIPx - GND) or (CSINx - GND) |                                                   | -2             |      | 28   | V          |
| CMRR                                                                                                                                  | Common Mode Rejection Ratio                                                              | DC to 50 kHz, VCM = -2 ... 28 V                   | 69<br>75<br>81 |      |      | dB         |



|                                       |                                                       |                                                                  |                    |                              |                      |            |
|---------------------------------------|-------------------------------------------------------|------------------------------------------------------------------|--------------------|------------------------------|----------------------|------------|
|                                       |                                                       |                                                                  | 81                 |                              |                      |            |
| $t_{SET}$                             | Settling time to 98%                                  |                                                                  | 1500               | 2000                         |                      | ns         |
| $t_{SET\_GAIN}$                       | Settling time to 98% after gain change                | After gain change from CSN rising edge                           |                    | 5000                         |                      | ns         |
| $V_{OS}$                              | Input Offset voltage                                  |                                                                  | -1.5               | 0                            | 1.5                  | mV         |
| $I_{OS1}$                             | Input bias current                                    | $V_{DD}=5V$ & $CSDx = 1$                                         |                    | 80                           |                      | $\mu A$    |
| $I_{OS2}$                             | Input bias current                                    | $V_{DD}=5V$ & $CSDx = 0$                                         |                    | 32                           |                      | $\mu A$    |
| $G_{DIFF10}$                          | Current Sense Amplifier DC Gain (uncalibrated)        | $CSAG = (0,0)$                                                   | 9.9                | 10                           | 10.1                 | V/V        |
| $G_{DIFF20}$                          | Current Sense Amplifier DC Gain (uncalibrated)        | $CSAG = (0,1)$                                                   | 19.8               | 20                           | 20.2                 | V/V        |
| $G_{DIFF40}$                          | Current Sense Amplifier DC Gain (uncalibrated)        | $CSAG = (1,0)$                                                   | 39.6               | 40                           | 40.4                 | V/V        |
| $G_{DIFF80}$                          | Current Sense Amplifier DC Gain (uncalibrated)        | $CSAG = (1,1)$                                                   | 79.2               | 80                           | 80.8                 | V/V        |
| $G_{DRIFT}$                           | Gain drift                                            | Gain drift after calibration                                     | -0.5               |                              | 0.5                  | %          |
| $V_{CSOX}$                            | CSOx single ended output voltage range (linear range) |                                                                  | 0.5                |                              | $V_{DD}-0.5$         | V          |
| $V_{REF\ Unidir}$                     | Reference voltage for unidirectional CSAx             | $CSDx = 0, V_{CSIPx} = V_{CSINx}$                                | -1%                | $V_{DD}/5$                   | +1%                  | V          |
| $V_{REF\ Bidir}$                      | Reference voltage for bidirectional CSAx              | $CSDx = 1, V_{CSIPx} = V_{CSINx}$                                | -1%                | $V_{DD}/5$                   | +1%                  | V          |
| $I_{CSO1}$                            | Output current                                        | $C_{CSO} = 0$                                                    |                    | 2                            | 2.4                  | mA         |
| $I_{CSO2}$                            | Output current                                        | $C_{CSO} = 1$                                                    |                    | 2.4                          | 2.88                 | mA         |
| $t_{SLEW}$                            | Output slew rate                                      | $C_{CSO} = 100pF$                                                | 16                 | 20                           | 24                   | V/us       |
| <b>OUTPUT OF CSA1</b>                 |                                                       |                                                                  |                    |                              |                      |            |
| $R_{IN\_CSO1}$                        | HiZ input resistance                                  | $EN\_CSO\_CFG = 1b$ & $CSO1\_CFG = 10b$                          |                    | 10                           | 50                   | M $\Omega$ |
| <b>LOGIC OUTPUT AND INPUT OF CSA2</b> |                                                       |                                                                  |                    |                              |                      |            |
| $t_{nFAULT}$                          | Fault turn off time                                   | $C_{CSO} = 100pF$                                                |                    | 150                          | 200                  | ns         |
| $t_{DRVOFF}$                          | HB turn off time                                      | $C_{CSO} = 100pF$                                                |                    | 240                          | 300                  | ns         |
| <b>OVERCURRENT DETECTION</b>          |                                                       |                                                                  |                    |                              |                      |            |
| $t_{FOC}$                             | Overcurrent filter time                               | OCxFILT = 00B<br>OCxFILT = 01B<br>OCxFILT = 10B<br>OCxFILT = 11B | 4<br>7<br>40<br>85 | 6<br>10<br>50<br>100         | 8<br>13<br>60<br>115 | $\mu s$    |
| $V_{OCTH1\ Unidir}$                   | OC threshold, unidirectional                          | $CSDx = 0, OCTH[1:0] = 00B$                                      | -4%                | $V_{DD}/2$                   | +4%                  | V          |
| $V_{OCTH2\ Unidir}$                   | OC threshold, unidirectional                          | $CSDx = 0, OCTH[1:0] = 01B$                                      | -4%                | $V_{DD}/2+$<br>$V_{DD}/10$   | +4%                  | V          |
| $V_{OCTH3\ Unidir}$                   | OC threshold, unidirectional                          | $CSDx = 0, OCTH[1:0] = 10B$                                      | -4%                | $V_{DD}/2+2*$<br>$V_{DD}/10$ | +4%                  | V          |
| $V_{OCTH4\ Unidir}$                   | OC threshold, unidirectional                          | $CSDx = 0, OCTH[1:0] = 11B$                                      | -4%                | $V_{DD}/2+3*$<br>$V_{DD}/10$ | +4%                  | V          |
| $V_{OCTH1\ BidirH}$                   | High OC threshold, bidirectional                      | $CSDx = 1, OCTH[1:0] = 00B$                                      | -4%                | $V_{DD}/2+2*$<br>$V_{DD}/20$ | +4%                  | V          |



|                                     |                                       |                          |     |                              |     |    |
|-------------------------------------|---------------------------------------|--------------------------|-----|------------------------------|-----|----|
| V <sub>OCTH2</sub> BidirH           | High OC threshold, bidirectional      | CSDx = 1, OCTH[1:0]= 01B | -4% | $V_{DD}/2+4*$<br>$V_{DD}/10$ | +4% | V  |
| V <sub>OCTH3</sub> BidirH           | High OC threshold, bidirectional      | CSDx = 1, OCTH[1:0]= 10B | -4% | $V_{DD}/2+5*$<br>$V_{DD}/20$ | +4% | V  |
| V <sub>OCTH4</sub> BidirH           | High OC threshold, bidirectional      | CSDx = 1, OCTH[1:0]= 11B | -4% | $V_{DD}/2+6*$<br>$V_{DD}/20$ | +4% | V  |
| V <sub>OCTH1</sub> BidirL           | Low OC threshold, bidirectional       | CSDx = 1, OCTH[1:0]= 00B | -4% | $V_{DD}/2-$<br>$2*V_{DD}/20$ | +4% | V  |
| V <sub>OCTH2</sub> BidirL           | Low OC threshold, bidirectional       | CSDx = 1, OCTH[1:0]= 01B | -4% | $V_{DD}/2-$<br>$4*V_{DD}/10$ | +4% | V  |
| V <sub>OCTH3</sub> BidirL           | Low OC threshold, bidirectional       | CSDx = 1, OCTH[1:0]= 10B | -4% | $V_{DD}/2-$<br>$5*V_{DD}/20$ | +4% | V  |
| V <sub>OCTH4</sub> BidirL           | Low OC threshold, bidirectional       | CSDx = 1, OCTH[1:0]= 11B | -4% | $V_{DD}/2-$<br>$6*V_{DD}/20$ | +4% | V  |
| <b>THERMAL WARNING AND SHUTDOWN</b> |                                       |                          |     |                              |     |    |
| T <sub>JW</sub>                     | Thermal warning junction temperature  |                          | 120 | 140                          | 160 | °C |
| T <sub>JSD</sub>                    | Thermal shutdown junction temperature |                          | 150 | 170                          | 190 | °C |
| T <sub>JHYS</sub>                   | Thermal shutdown hysteresis           |                          |     | 10                           |     | °C |
| t <sub>JW_FILT</sub>                | Thermal warning filter time           |                          | 7   | 10                           | 13  | us |
| t <sub>JSD</sub>                    | Thermal shutdown filter time          |                          | 7   | 10                           | 13  | us |

Table 8-7 Electrical parameter

V<sub>S</sub> = 6.0 V to 18 V if V<sub>SOVTH</sub> = 0, V<sub>S</sub> = 6.0 V to 28 V if V<sub>SOVTH</sub> = 1; V<sub>DD</sub> = 3.0 V to 5.5 V, T<sub>J</sub> = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin.

| PARAMETER                                     |                                           | TEST CONDITIONS                                              | MIN     | TYP | MAX | UNIT |
|-----------------------------------------------|-------------------------------------------|--------------------------------------------------------------|---------|-----|-----|------|
| SPI frequency                                 |                                           |                                                              |         |     |     |      |
| f <sub>SPI,max</sub>                          | Maximum SPI frequency                     |                                                              |         |     | 4   | Mhz  |
| Delay from EN rising edge to first SPI frame  |                                           |                                                              |         |     |     |      |
| t <sub>SET_SPI</sub>                          | SPI interface setup time                  |                                                              |         |     | 150 | us   |
| SPI interface, logic inputs SDI, SCLK, CSN    |                                           |                                                              |         |     |     |      |
| V <sub>IH</sub>                               | High input voltage threshold              |                                                              | 0.7VDD  |     |     | V    |
| V <sub>IL</sub>                               | Low input voltage threshold               |                                                              | 0.3VDD  |     |     | V    |
| V <sub>IHY</sub>                              | Hysteresis of input voltage               |                                                              | 0.12VDD |     |     | V    |
| R <sub>PU_CSN</sub>                           | Pull up resistor at pin CSN               | V <sub>CSN</sub> = 0.7 * V <sub>DD</sub>                     | 20      | 40  | 80  | kΩ   |
| R <sub>PD_SDI</sub> ,<br>R <sub>PD_SCLK</sub> | Pull down resistor at pin SDI, SCLK       | V <sub>SDI</sub> , V <sub>SCLK</sub> = 0.2 * V <sub>DD</sub> | 20      | 40  | 80  | kΩ   |
| C <sub>I</sub>                                | Input capacitance at pin CSN, SDI or SCLK | 0 V < V <sub>DD</sub> < 5.5 V                                |         | 10  |     | pF   |
| Input interface, logic outputs SDO            |                                           |                                                              |         |     |     |      |
| V <sub>SDOH</sub>                             | H-output voltage level                    | I <sub>SDOH</sub> = -1.6 mA                                  | 0.8VDD  |     |     | V    |
| V <sub>SDOL</sub>                             | L-output voltage level                    | I <sub>SDOL</sub> = 1.6 mA                                   | 0.2VDD  |     |     | V    |
| I <sub>SDOLK</sub>                            | Tri-state Leakage Current                 |                                                              | -10     |     | 10  | uA   |
| C <sub>SDO</sub>                              | Tri-state input capacitance               | V <sub>CSN</sub> = V <sub>DD</sub> ;                         | 10      |     | 15  | pF   |



|                             |                                                 |                                               |                                             |    |
|-----------------------------|-------------------------------------------------|-----------------------------------------------|---------------------------------------------|----|
|                             |                                                 | $0\text{ V} < V_{\text{SDO}} < V_{\text{DD}}$ |                                             |    |
| <b>Data input timing</b>    |                                                 |                                               |                                             |    |
| $t_{\text{pCLK}}$           | SCLK Period                                     |                                               | 250                                         | ns |
| $t_{\text{SCLKH}}$          | SCLK High Time                                  |                                               | $0.45t_{\text{pCLK}}$ $0.55t_{\text{pCLK}}$ | ns |
| $t_{\text{SCLKL}}$          | SCLK Low Time                                   |                                               | $0.45t_{\text{pCLK}}$ $0.55t_{\text{pCLK}}$ | ns |
| $t_{\text{BEF}}$            | SCLK Low before CSN Low                         |                                               | 125                                         | ns |
| $t_{\text{lead}}$           | CSN Setup Time                                  |                                               | 250                                         | ns |
| $t_{\text{lag}}$            | SCLK Setup Time                                 |                                               | 250                                         | ns |
| $t_{\text{BEH}}$            | SCLK Low after CSN High                         |                                               | 125                                         | ns |
| $t_{\text{SDI\_setup}}$     | SDI Setup Time                                  |                                               | 100                                         | ns |
| $t_{\text{SDI\_hold}}$      | SDI Hold Time                                   |                                               | 50                                          | ns |
| $t_{\text{rIN}}$            | Input Signal Rise Time at pin SDI, SCLK, CSN    |                                               | 50                                          | ns |
| $t_{\text{fIN}}$            | Input Signal Fall Time at pin SDI, SCLK, CSN    |                                               | 50                                          | ns |
| $t_{\text{DMODE}}$          | Delay time from EN falling edge to standby mode |                                               | 6                                           | us |
| $t_{\text{CSNH}}$           | Minimum CSN High Time                           |                                               | 3                                           | us |
| <b>Data output timing</b>   |                                                 |                                               |                                             |    |
| $t_{\text{rSDO}}$           | SDO Rise Time                                   |                                               | 250                                         | ns |
| $t_{\text{fSDO}}$           | SDO Fall Time                                   |                                               | $0.45t_{\text{pCLK}}$ $0.55t_{\text{pCLK}}$ | ns |
| $t_{\text{ENSDO}}$          | SDO Enable Time after CSN falling edge          |                                               | $0.45t_{\text{pCLK}}$ $0.55t_{\text{pCLK}}$ | ns |
| $t_{\text{DISSDO}}$         | SDO Disable Time after CSN rising edge          |                                               | 125                                         | ns |
| $\text{duty}_{\text{SCLK}}$ | Duty cycle of incoming clock at SCLK            |                                               | 250                                         | ns |
| $t_{\text{VASDO5}}$         | SDO Valid Time for $V_{\text{DD}} = 5\text{V}$  |                                               | 250                                         | ns |

## 9 Feature Description

### 9.1 Power supply

The Multiple MOSFET Driver IC requires two power supplies:  $V_{\text{S}}$  and  $V_{\text{DD}}$ .

$V_{\text{DD}}$  supplies the I/O buffers (including the SPI pins) and the internal voltage regulator for the logic.  $V_{\text{DD}}$  allows the flexibility of a 3.3 V or a 5.0 V logic interface.

$V_{\text{S}}$  supplies the charge pump for the MOSFET gate drivers. The  $V_{\text{S}}$  pin must be connected to the battery through a reverse battery protection.

Both supplies are separated so that the information stored in the logic remains intact in the event of voltage drop on  $V_{\text{S}}$ .  $V_{\text{DD}}$  and  $V_{\text{S}}$  should be decoupled with ceramic capacitors connected close to the supply and ground planes.



## 9.2 Operation modes

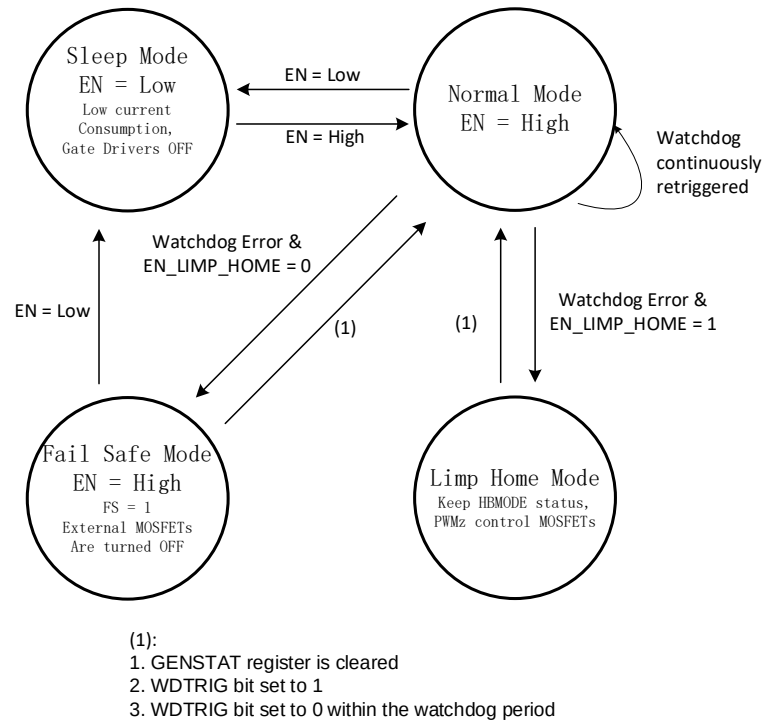


Figure 9-1. State diagram

### 9.2.1 Normal mode

The SC77708 enters Normal Mode by setting EN pin to High and waiting for the SPI setup time  $t_{SET\_SPI}$ .

In normal mode, the MOSFET gate drivers are enabled and can be configured through the SPI interface, provided that the voltages applied to  $V_{DD}$  and  $V_S$  are within the operating range. The watchdog must be retriggered correctly in order to stay in Normal Mode.

### 9.2.2 Sleep mode

The SC77708 enters Sleep Mode by setting EN pin to Low. The transition to the sleep mode is delayed by  $t_{DSLEEP}$  in order to actively turn-off the external MOSFETs. In this mode, the internal regulator and the internal circuitry are deactivated, and the SPI registers are reset. The current consumption of  $V_{DD}$  is reduced to  $I_{DD\_Q}$ . The current consumption of  $V_S$  is reduced to  $I_{SQ}$  or  $I_{SQ} + I_{SQ\_BRAKE}$ .

The  $V_S$  current consumption is  $I_{SQ}$  if:

- **PASS\_MOD** = 00B and **PASS\_VDS** = 0B while entering sleep mode or  $V_S$  has recovered from a voltage below  $V_{SLEEP\_SET}$  (i.e.  $V_S$  has ramped up from a voltage below  $V_{SLEEP\_SET}$  or  $V_S$  has dropped below  $V_{SLEEP\_SET}$ )

The  $V_S$  current consumption is  $I_{SQ} + I_{SQ\_BRAKE}$  if:

- **PASS\_MOD** = 01B, 10B, 11B or **PASS\_VDS** = 1B before entering sleep mode and  $V_S$  never drops below  $V_{SLEEP\_SET}$  after entering sleep mode

The internal resistors  $R_{GGND}$  between GHx/GLx and GND are activated to discharge the gate of the external MOSFETs.

*Note: If EN is set to Low for a duration shorter than ( $t_{ENL\_FLT}$ , 8  $\mu s$  max.), and EN is set to High again, then device does not go in sleep mode and the registers are not reset. The half-bridges are reactivated according to the settings of the control registers when EN is High.*



### 9.2.3 Fail Safe Mode

In case of watchdog error, the device enters Fail Safe Mode, FS bit is set and the external MOSFETs are actively discharged with the static discharge current during the max. configured tHBxCCP active. Then the bridge driver is set to passive mode (the passive discharge path is activated, all external MOSFETs are latched off, and the charge pump is deactivated). To resume Normal Mode the microcontroller must execute the following sequence:

1. Clear **GENSTAT** register.
2. Write **WDTRIG** bit to 1 (**GENCTRL1**) within the watchdog period.
3. Write **WDTRIG** bit to 0 within the watchdog period3).

In fail safe mode, the control registers are frozen to their default value, at the exception of **WDTRIG**, **CCSO**, **PASS\_VDS**, **PASS\_MOD**, **CSA1L**, **CSA2L**. Any write command (except for **WDTRIG** bit) or clear command (except for **GENSTAT**) will be discarded in this mode and sets SPIE bit (Global status byte).

A clear command to **GENSTAT** in fail safe mode does not reset any failure flag reported by this status register. The control and status registers can be read in this mode before the start of the exit sequence without **SPIE** bit being set.

### 9.2.4 Limphome Mode

In some cases, MCU can not to work and occur watchdog timeout, but some half-bridges need to keep work state (static or pwm).

If **EN\_LIMP\_HOME** = 1 (**LIMP\_HOME**, **REG\_BNAK**=1), when watchdog is timeout, SC77708 will enter limphome mode, and the behavior of HBx depends on **LIMP\_HBx** and **LIMP\_PWMz** (**LIMP\_HOME**, **REG\_BNAK**=1)

| LIMP_HBx | LIMP_PWMz | Behavior of HBx            |
|----------|-----------|----------------------------|
| 0b       | x         | OFF                        |
| 1b       | 0b        | Depends on HBMODEx         |
| 1b       | 1b        | PWM if PWMz mapping to HBx |

Table 9-1 HBx behavior in limphome mode

## 9.3 Reset behavior

The following events trigger a Power On Reset:

#### V<sub>DD</sub> undervoltage reset:

If  $V_{DD} < V_{DD\ PoffR}$  the digital block is deactivated and the outputs are switched off. The digital block is reset once  $V_{DD} > V_{DD\ POR}$ . Then **NPOR** bit (negated power-on reset bit, see Global status byte) is reset to 0 to report the reset condition.

#### Reset on EN pin:

If the EN pin is pulled low, the logic content is reset and the device enters sleep mode. Once the device enters Normal Mode (after  $t_{SET\_SPI}$  with EN = high and  $V_{DD} > V_{DD\ POR}$ ), the **NPOR** bit is reset to 0 to report the reset condition.

**NPOR** is set to 1 when **GENSTAT** is cleared.



## 9.4 Charge pump

A dual-stage charge pump supplies the gate drivers for the high-side and low-side MOSFETs. It requires three external capacitors connected between CPC1N and CPC1P, CPC2N and CPC2P, VS and CP.

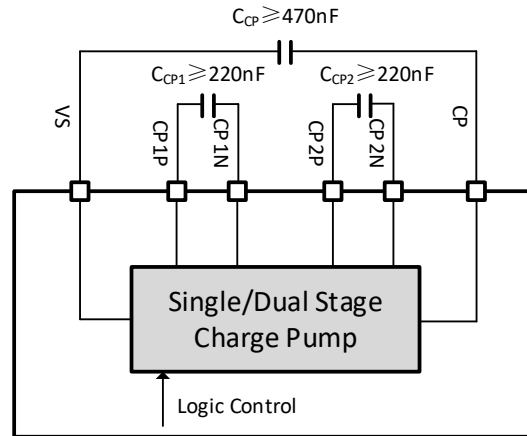


Figure 9-2 Charge pump

**CPSTGA** = 0 (**GENCTRL2**), the device operates with the dual-stage charge pump.

If **CPSTGA** = 1 (**GENCTRL2**), the device switches automatically to single-stage or dual-stage charge pump automatically:

- If  $V_S > V_{CP50DS}$ : the SC77708 switches from a dual-stage to a single-stage charge pump.
- If  $V_S < V_{CP50SD}$ : the SC77708 switches from single-stage to dual-stage charge pump.

The operation with the single-stage charge pump could reduce the current consumption from the VS pin.

## 9.5 Frequency modulation

A modulation of the charge pump frequency can be activated to reduce the peak emission. The modulation frequency can be selected based on the resolution bandwidth of the peak detector during EMC testing.

The modulation frequency is set by the control bit **FMODE** in **GENCTRL1**

- **FMODE** = 0: No modulation.
- **FMODE** = 1: Modulation frequency = 15.6 kHz (default).

## 9.6 Current sense amplifier chopping mode

When the motor is started, a large impulse current occur, which may trigger overcurrent protection and cause motor startup failure. In chopping mode, when  $|I_{CSOX}| > I_{chopx}$ , corresponding half bridges turn off, and after a constant time **CSx\_TOFF** (refer to **CHOPPING\_TOFF1** & **CHOPPING\_TOFF2**), the corresponding half bridge retry turn on. Chopping mode can be used for motor soft-start or const current output.

## 9.7 Half bridge parallel mode

In normal mode, one PWM can only map one half bridge (refer to **PWMSET**), if one PWM mapping multiple half bridge will trigger **HBxPWME** error. In half bridge parallel mode (**EN\_PWM\_HB\_IND** = 1, refer to **HB\_EN\_CFG**), **HBx** can select any PWMz by configuring **PWM\_HBx** (refer to **PWM\_HB**).



## 10 Floating gate drivers

The SC77708 integrates sixteen floating gate drivers capable of controlling a wide range of n-channel MOSFETs. They are configured as eight high-sides and low-sides, building eight half-bridges. This section describes the MOSFET control by the gate drivers.

After power-on reset, the bridge driver is in passive mode (default value of BD\_PASS = 1 and all HBxMODE=00B). Refer to Chapter 10.4 and Chapter 10.5.

The bridge driver is in active mode by setting BD\_PASS to 0. Chapter 10.1, Chapter 10.2 and Chapter 10.3 describes the static and PWM control in active mode.

**Attention:** It is highly recommended to have all HBxMODE bits set to 00B or 11B before setting BD\_PASS to 0 in order to avoid wrong drain-source overvoltage detection.

| EN   | BD_PASS | HBxMODE[1:0]           | Gate driver | Comment                             |
|------|---------|------------------------|-------------|-------------------------------------|
| High | 0       | x                      | Active      |                                     |
| High | 1       | One HBxMODE=01B or 10B | Active      | Equivalent to EN=High and BD_PASS=0 |
| High | 1       | All HBxMODE=00B or 11B | Passive     |                                     |
| Low  | x       | x                      | Passive     |                                     |

Table 10-1 Operating modes of the gate driver

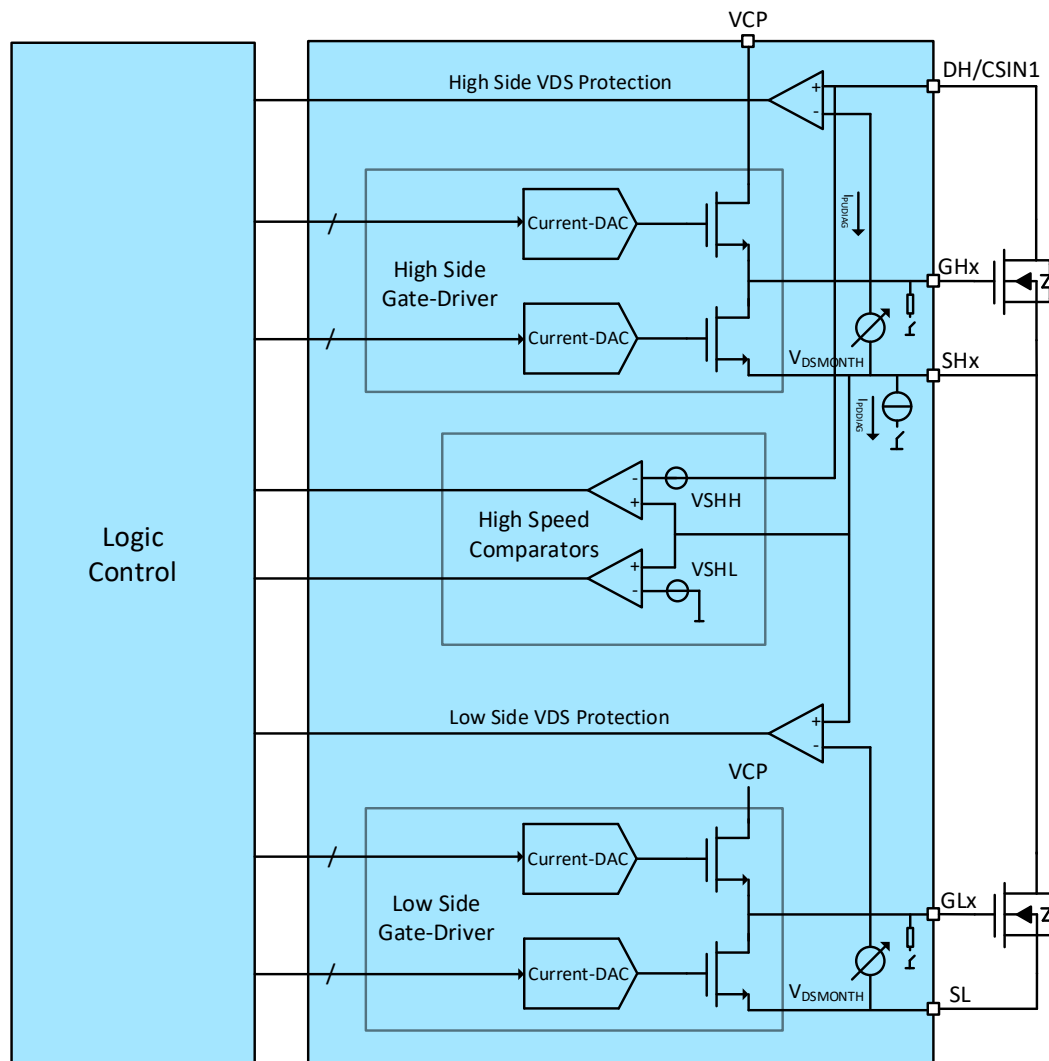


Figure 10-1 Block diagram - Gate driver for one half-bridge

## 10.1 MOSFET control with bridge driver in active mode (BD\_PASS = 0 and EN = High)

Depending on the configuration bits HBxMODE[1:0], each high-side and low-side MOSFETs can be:

- deactivated
- activated (statically, no PWM)
- activated in PWM mode (**PWMSET**)

| HBMODE[1:0] | Configuration of HSx/LSx                                          |
|-------------|-------------------------------------------------------------------|
| 00b         | LSx and HSx MOSFET are actively kept OFF                          |
| 01b         | LSx MOSFET is ON (static or pwm), HSx MOSFET is actively kept OFF |
| 10b         | HSx MOSFET is ON (static or pwm), LSx MOSFET is actively kept OFF |



|     |                                          |
|-----|------------------------------------------|
| 11b | LSx and HSx MOSFET are actively kept OFF |
|-----|------------------------------------------|

Table 10-2 Half-bridge mode selection

## 10.2 Static activation with bridge driver in active mode (BD\_PASS = 0)

In this section, we consider the static activation of the high-side and low-side MOSFET of the half-bridge x, x = 1...8. For the setting of a high-side or low-side in the static or PWM operation.

If HBx is not mapped to any activated PWM channel, the low-side or high-side MOSFET of HBx is statically activated (no PWM) by setting HBxMODE[1:0] to respectively (0,1) or (1,0).

The configured cross-current protection and the Drain-Source overvoltage blank times for the Half-Bridge x are noted  $t_{HBxCCP\_ACT}$  and  $t_{HBxBLANK\_ACT}$ .

The charge and discharge currents applied to the static controlled Half-Bridge x are noted ICHGSTx (**ST\_ICHG**).

IHARDOFF is the maximum current that the gate drivers can sink. It corresponds to the discharge current when IDCHGx[4:0] = 31D (**PWM\_IDCHG\_ACT**). This current is used to keep a MOSFET off, when the opposite MOSFET of the same half-bridge is being turned on. This feature avoids parasitic cross-current conduction.

ICHGSTx is the current sourced, respectively sunk, by the gate driver to turn-on the high-side x or low-side x. ICHGSTx is configured in the control register **ST\_ICHG**.

| ICHGSTx[3:0] | Charge Current (mA) | Discharge Current (mA) | Deviation to Typ Value |
|--------------|---------------------|------------------------|------------------------|
| 0000b        | 1.0                 | 1.0                    | ±60%                   |
| 0001b        | 2.0                 | 2.8                    | ±60%                   |
| 0010b        | 4.5                 | 5.7                    | ±60%                   |
| 0011b        | 8.0                 | 9.4                    | ±38%                   |
| 0100b        | 12.5                | 14.2                   | ±38%                   |
| 0101b        | 17.8                | 19.7                   | ±38%                   |
| 0110b        | 23.9                | 26.0                   | ±38%                   |
| 0111b        | 30.0                | 32.0                   | ±28%                   |
| 1000b        | 37.1                | 39.5                   | ±28%                   |
| 1001b        | 44.3                | 46.8                   | ±28%                   |
| 1010b        | 52.3                | 54.7                   | ±28%                   |
| 1011b        | 60.2                | 62.5                   | ±28%                   |
| 1100b        | 68.3                | 70.6                   | ±28%                   |
| 1101b        | 76.8                | 78.5                   | ±28%                   |



|       |      |      |      |
|-------|------|------|------|
| 1110b | 86.0 | 87.0 | ±28% |
| 1111b | 96.0 | 95.0 | ±25% |

Table 10-3 Static charge and discharge currents

I<sub>HOLD</sub> is the hold current used to keep the gate of the external MOSFETs in the desired state. This parameter is configurable with the **I<sub>HOLD</sub>** control bit in **GENCTRL2**.

If **I<sub>HOLD</sub>** = 0:

- the MOSFETs are kept ON with the current I<sub>CHG8</sub> (12.5 mA typ.)
- the MOSFETs are kept OFF with the current I<sub>DCHG8</sub> (14.2 mA typ.)

If **I<sub>HOLD</sub>** = 1:

- the MOSFETs are kept ON with the current I<sub>CHG12</sub> (23.9 mA typ.)
- the MOSFETs are kept with the current I<sub>DCHG12</sub> (26.0 mA typ.)

The static discharge current is applied to turn off the MOSFETs when the bridge driver is in active mode when the following failures occur:

- VS undervoltage/overvoltage
- Overtemperature
- VDS overvoltage
- Charge pump undervoltage
- Overcurrent if OCEN = 1

### 10.2.1 Static activation of a high-side MOSFET

#### Turn-on with cross-current protection

If LSx is ON (HBxMODE[1:0] = 01B), before the activation of HSx (HBxMODE[1:0] = 10B) then the high-side MOSFET is turned on after a cross-current protection time:

- after the CSN rising edge and for the duration  $t_{HBxCCP\_ACT}$ :
  - the high-side MOSFET is kept OFF with the current -I<sub>CHGSTx</sub>
  - the gate of the low-side MOSFET is discharged with the current -I<sub>CHGSTx</sub>
- at the end of  $t_{HBxCCP\_ACT}$  and for the duration  $t_{HBxBLANK\_ACT} + t_{FVDS}$ :
  - the gate of the high-side MOSFET is charged with the current I<sub>CHGSTx</sub>
  - low-side MOSFET is kept OFF with the current -I<sub>HARDOFF</sub> (hard off phase)
- at the end of  $t_{FVDS}$ :
  - the drive current of the high-side MOSFET is reduced to I<sub>HOLD</sub>
  - the drive current of the low-side MOSFET is set to -I<sub>HOLD</sub>

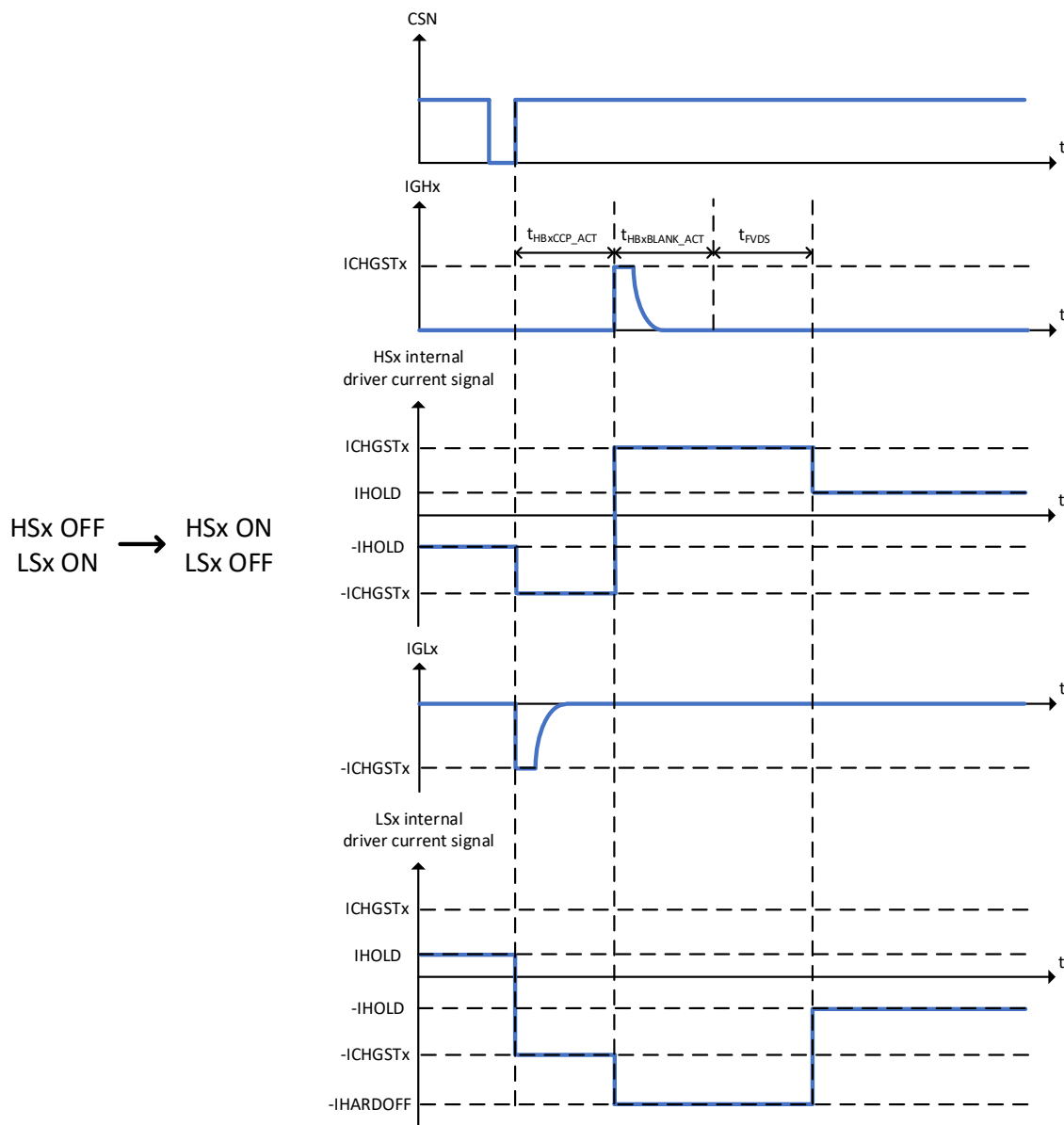


Figure 10-2 Turn-on of a high-side MOSFET with cross-current protection

**Turn-on without cross-current protection**

If LSx is OFF ( $HBxMODE[1:0] = 00B$ ), before the activation of HSx ( $HBxMODE[1:0] = 10B$ ), then the high-side MOSFET is turned on without cross-current protection:

- after the CSN rising edge and for a duration  $t_{HBxBLANK\_ACT} + t_{FVDS}$ :
  - the gate of the high-side MOSFET is charged with the current ICHGSTx
  - the low-side MOSFET is kept OFF with the current -IHARDOFF
- at the end of  $t_{FVDS}$ :
  - the drive current of the high-side MOSFET is reduced to IHOLD



– the drive current of the low-side MOSFET is set to -IHOLD

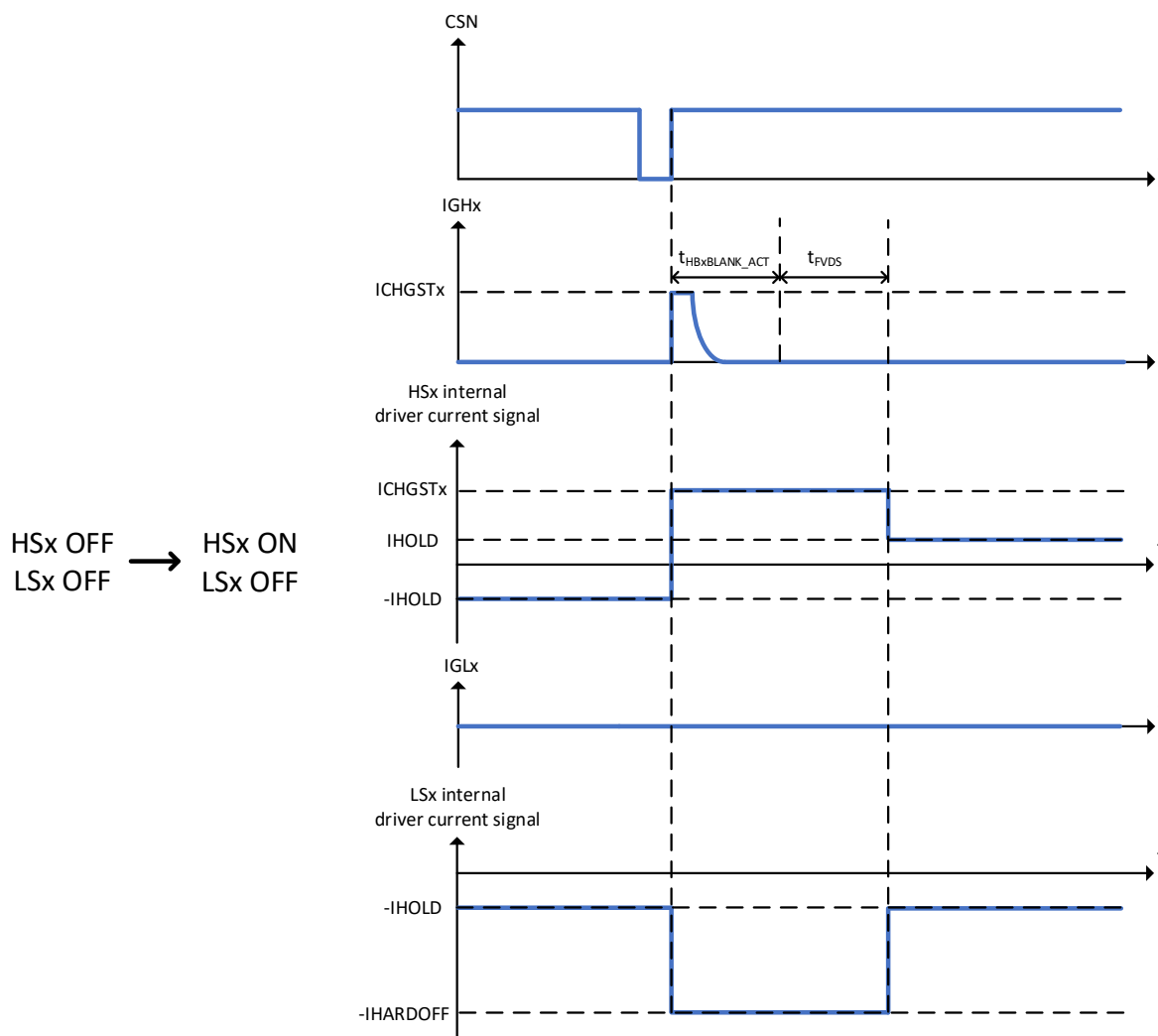


Figure 10-3 Turn-on of a high-side MOSFET without cross-current protection

### 10.2.2 Static activation of a low-side MOSFET

The description of the static activation of a low-side x differs from the description of Chapter 10.2.1 only by exchanging high-side x and low-side x.

### 10.2.3 Turn-off of the high-side and low-side MOSFETs of a half-bridge

When the SC77708 receives a SPI to turn-off both the high-side and low-side MOSFETs of the half-bridge x ( $HBxMODE[1:0] = (0,0)$  or  $(1,1)$ ):

- the gate of HSx and LSx are discharged with the current -ICHGSTx for the duration  $t_{HBxCCP\_ACT}$
- at the end of  $t_{HBxCCP\_ACT}$ , the drive current of HSx and LSx are reduced to -IHOLD

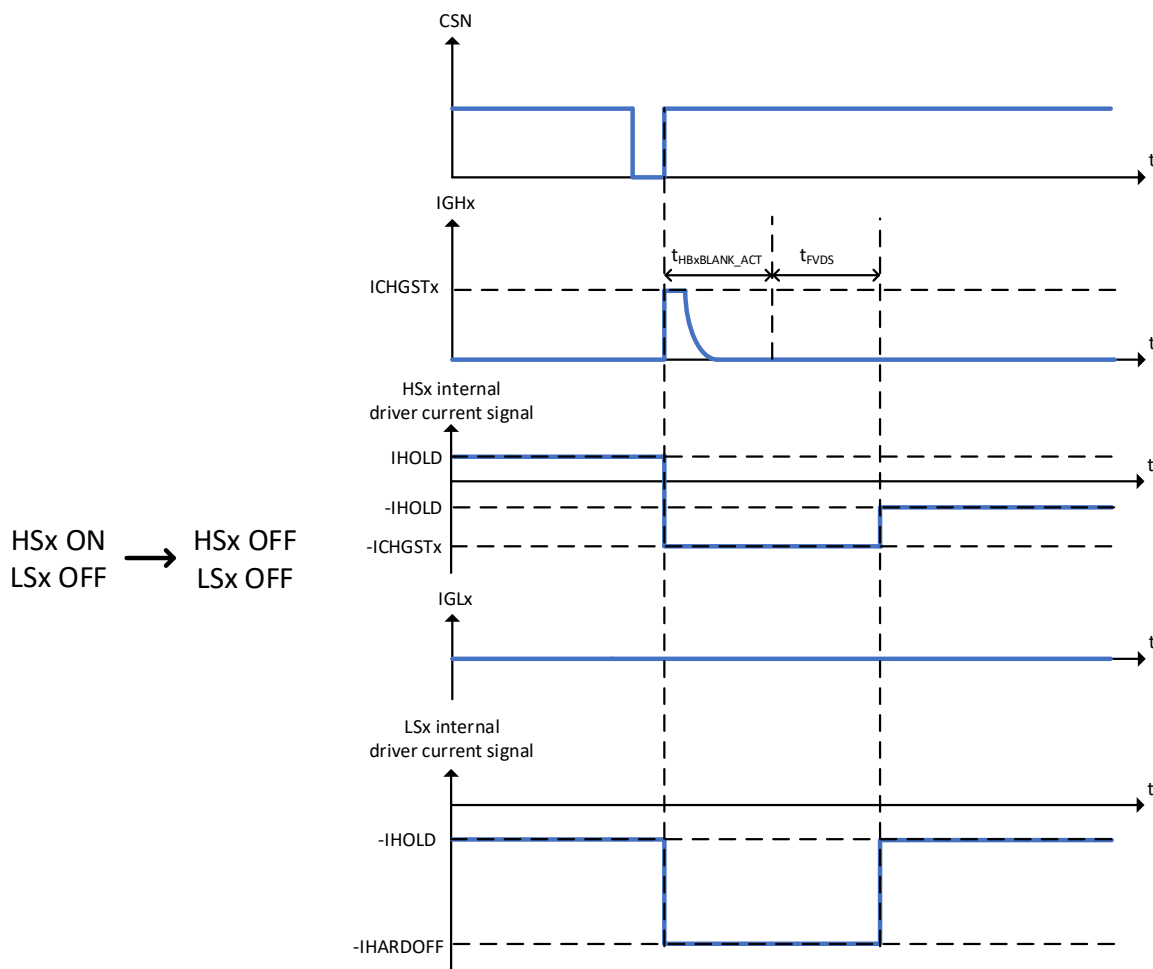


Figure 10-4 Turn-off of the high-side and low-side MOSFETs of a half-bridge

### 10.3 PWM operation with bridge driver in active mode (BD\_PASS = 0)

The SC77708 integrates three PWM channels. The pins PWM1, PWM2 and PWM3 provide the PWM signal for each PWM channel. One half-bridge can be mapped to one of the PWM channels according to the settings of the control registers HBMODE and PWMSET:

- PWMxEN in PWMSET, enables or disables the PWM channel x
- The control bits PWMx\_HB[2:0] in PWMSET select the half-bridge
- The control bits HBMODE[1:0] (HBMODE) of the half-bridge selected by PWMx\_HB[2:0] configures the low-side or the high-side MOSFET in PWM mode

Example: the following commands set to map the low-side of HB3 to the PWM channel 2 (start sequence with PWM):

1. Set HB3MODE[1:0] to (0,0): HB3 is in high impedance
2. Set PWM2\_HB[2:0] to (0,1,0) and set PWM2EN to 1 (HB3 stays in high impedance, independently from the signal present at the PWM2 pin)
3. Set HB3MODE[1:0] to (0,1): PWM2 is applied to the low-side of HB3



| PWMx_EN | PWMx_HB | HByMODE | PWMx channel setting                |
|---------|---------|---------|-------------------------------------|
| 0       | x       | x       | no PWM operation                    |
| x       | x       | 00b     | no PWM operation on selected HB     |
| x       | x       | 11b     | no PWM operation on selected HB     |
| 1b      | 000b    | 01b     | Low-side of HB1 is mapped to PWMx   |
| 1b      | 001b    | 01b     | Low-side of HB2 is mapped to PWMx   |
| 1b      | 010b    | 01b     | Low-side of HB3 is mapped to PWMx   |
| 1b      | 011b    | 01b     | Low-side of HB4 is mapped to PWMx   |
| 1b      | 100b    | 01b     | Low-side of HB5 is mapped to PWMx   |
| 1b      | 101b    | 01b     | Low-side of HB6 is mapped to PWMx   |
| 1b      | 110b    | 01b     | Low-side of HB7 is mapped to PWMx   |
| 1b      | 111b    | 01b     | Low-side of HB8 is mapped to PWMx   |
| 1b      | 000b    | 10b     | High-side of HB1 is mapped to PWMx  |
| 1b      | 001b    | 10b     | High -side of HB2 is mapped to PWMx |
| 1b      | 010b    | 10b     | High -side of HB3 is mapped to PWMx |
| 1b      | 011b    | 10b     | High -side of HB4 is mapped to PWMx |
| 1b      | 100b    | 10b     | High -side of HB5 is mapped to PWMx |
| 1b      | 101b    | 10b     | High -side of HB6 is mapped to PWMx |
| 1b      | 110b    | 10b     | High -side of HB7 is mapped to PWMx |
| 1b      | 111b    | 10b     | High -side of HB8 is mapped to PWMx |

Table 10-4 PWM channel settings

1) x = 1...3

2) the half-bridge y is selected by the PWMx\_HB[2:0] bits

*Note: An SPI error is reported if one half-bridge is mapped to several activated PWM channels. In this case the external MOSFETs of the impacted half-bridge are turned-off and the corresponding status bit (HBxPWME) of the **HBVOUT\_PWMERR** register is set.*

### 10.3.1 Determination of the active and free-wheeling MOSFET

An active free-wheeling is automatically implemented when a half-bridge is activated in PWM mode to reduce the power dissipation of the free-wheeling (FW) MOSFET: If the active MOSFET is OFF, the opposite (freewheeling) MOSFET of the same half-bridge is actively turned on.

If **EN\_GEN\_CHECK** = 0: the PWM MOSFET is considered as the active MOSFET and the opposite MOSFET of the same half-





– during the pre-discharge phase, the gate of the PWM MOSFET mapped to the PWM channel  $x$ ,  $x = 1 \dots 3$ , is discharged with the configured current  $IPCHG_{INIT}$  (Refer to **PWM\_PCHG\_INIT** and Chapter 10.3.4.2)

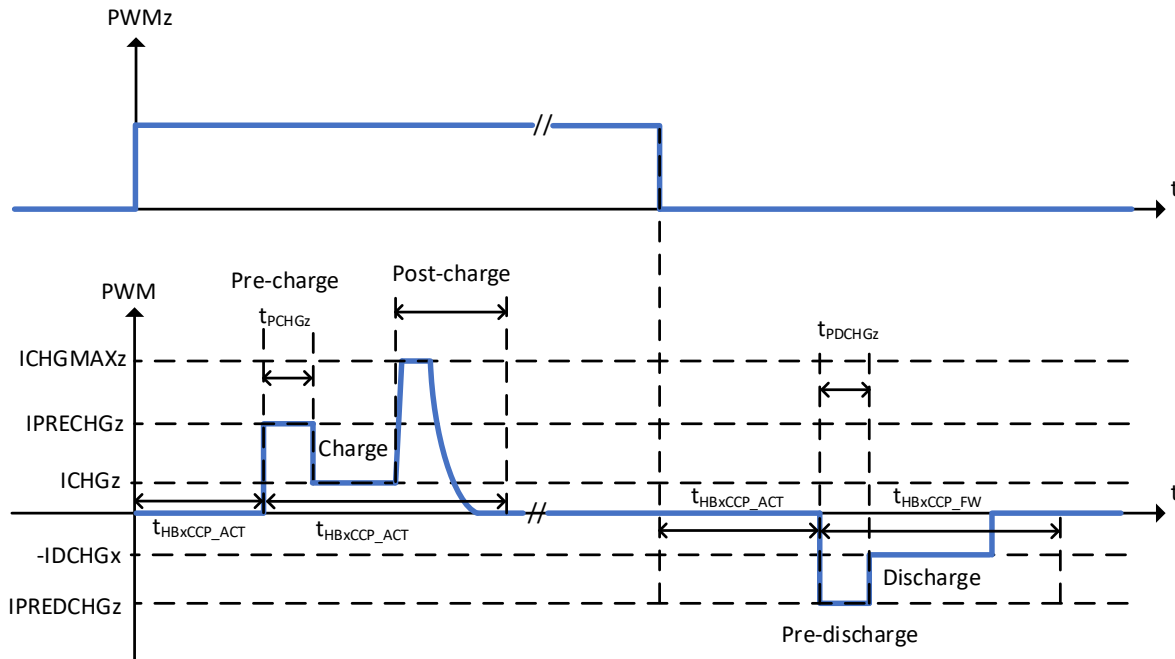


Figure 10-9 PWM overview showing pre-charge, pre-discharge and post charge phases,  $AGC[1:0] = 10B$  or  $11B$ ,  $POCHGDIS = 1B$ .

### 10.3.3 PWM operation with adaptive gate control

This section describes the MOSFETs control during high-side or low-side PWM operation when the adaptive gate control is enabled ( $AGC[1:0] = (1,0)$  or  $(1,1)$ ,  $GENCTRL2$ ).

*Note: Unless otherwise specified, the description of the regulation of the pre-charge and pre-discharge currents are applicable for Refer to Chapter 10.3.1 for the definition of the active and of the freewheeling MOSFET according to the setting of AGC.*

The SC77708 adapts the pre-charge current, respectively the pre-discharge current, in order to match the effective turn-on delay ( $t_{DON}$ ) and turn-off delay ( $t_{DOFF}$ ) to the configured values.

The configured turn-on and turn-off delays of the respective PWM MOSFETs are set by the registers **TDON\_OFF1**, **TDON\_OFF2**, **TDON\_OFF3**.

The effective turn-on and turn-off delays of the respective active MOSFETs are read out from the status registers **EFF\_TDON\_OFF1**, **EFF\_TDON\_OFF2**, **EFF\_TDON\_OFF3**.

#### 10.3.3.1 High-side PWM with adaptive gate control, motor operating as load

The following section describes the MOSFET control when the PWM signal is applied to the high-side MOSFET of one half-bridge while the motor operates.

*Assumption: the PWM channel  $z$ ,  $z = 1,2$  or  $3$ , is applied to the high-side MOSFET of the half-bridge  $x$ ,  $x = 1 \dots 8$ .*

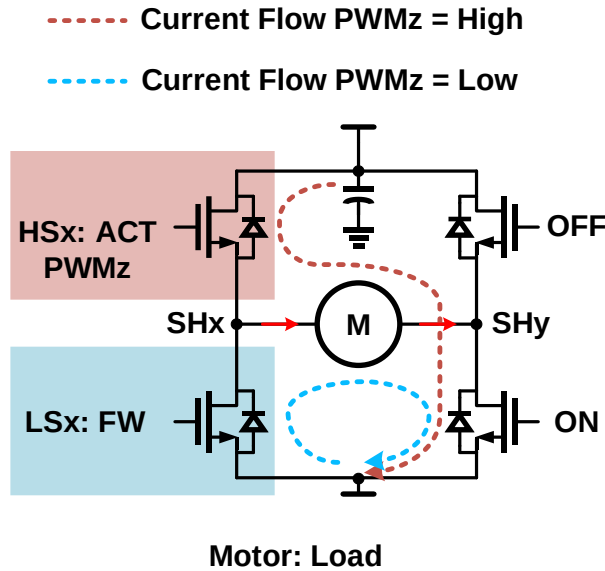


Figure 10-10 PWM channel z is mapped to high-side x, motor operating as load.

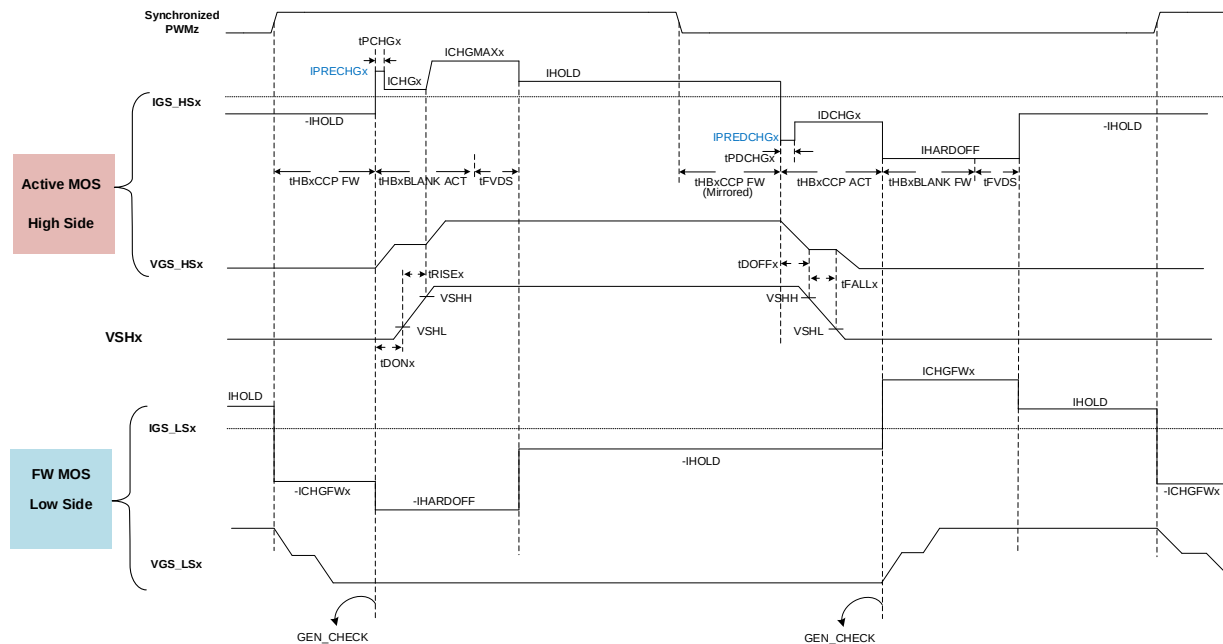


Figure 10-11 Adaptive turn-on and turn-off, high-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as load.

### Adaptive turn-on during high-side PWM

The turn-on of the high-side MOSFET is done in four phases:

- 1. Cross-current protection phase:** The cross-current protection  $t_{HBxCCP\ FW}$  starts at the rising edge of the internal PWMz signal1). During  $t_{HBxCCP\ FW}$ , the low-side MOSFET x is turned off with the discharge current  $ICHGFWx$ , while the high-side MOSFET x is kept off.
- 2. Pre-charge:** Once  $t_{HBxCCP\ FW}$  has elapsed, the gate of the high-side MOSFET x is pre-charged with the current  $IPRECHGz$  for a duration  $tPCHGz$ .  $IPRECHGz$ 2) is an internal parameter, which is self-adaptive (see next phase).
- 3. Charge:** After  $tPCHGz$ , the charge current is decreased from  $IPRECHGz$  down to  $ICHGz$ . The effective  $tDONz$  is measured and



compared to the configured tDONz for the automatic adaptation of IPRECHGz (see Adaptive control of pre-charge current). The charge phase ends up when  $V_{SHx}$  reaches  $V_{SHH}$ .

4. **Post-charge:** After the charge phase, the control signal for the charge current of HSx is increased by one current step every 62.5 ns typ. to ICHGMAXx.

*Note: The postcharge phase is deactivated by setting **POCHDIS** to 1. Refer to **GENCTRL2**.*

### Adaptive control of pre-charge current

Refer to Chapter 11.3.6 for information on the pre-discharge currents.

The pre-charge current IPRECHGz is a self-adaptive parameter if AGC[1:0] = (1,0) or (1,1) (see **GENCTRL2**). It is applied during  $t_{PCHGz}$  (see **TPRECHG**). The SC77708 adapts IPRECHGz to match the effective tDONz to the configured value. IPRECHGz is clamped between ICHG0 (1 mA typ.) and ICHGMAXz (see **PWM\_ICHGMAX\_CCP\_BLK3\_ACT**). IPRECHGz is initialized to min (IPCHGINITz, ICHGMAXz) (refer to **PWM\_PCHG\_INIT**) when the SC77708 receives an SPI command setting PWMz\_EN to 1 (see **PWMSET**).

The following adaptive schemes can be selected:

AGCFILT = 0 (**GENCTRL2**): No filter is applied

- If the effective tDONz is longer than the configured tDONz, then IPRECHGz is increased during the next pre-charge phase.
- If the effective tDONz is shorter than the configured tDONz, then IPRECHGz is decreased during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (Chapter 11.3.6) if the control bit **IPCHGADT** in the control register **GENCTRL1** is set to 0 respectively 1.

AGCFILT = 1: The filter is applied

- If the effective tDONz of the last two PWM cycles are longer than the configured tDONz, then IPRECHGz is increased during the next pre-charge phase.
- If the effective tDONz of the last two PWM cycles are shorter than the configured tDONz, then IPRECHGz is decreased during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps (Chapter 10.3.6) if the control bit **IPCHGADT** in the control register **GENCTRL1** is set to 0 respectively 1.
- If none of the two cases are applicable, then IPRECHGz is unchanged during the next pre-charge phase.

### Adaptive turn-off during high-side PWM

The turn-off of the high-side MOSFET is done in four phases:

1. Turn-off delay time for symmetrization of the PWM signal: The turn-off of HSx is delayed by  $t_{HBxCCP\ FW}$  after the falling edge of the internal PWMz signal1), in order to compensate the distortion caused by the cross-current protection time at turn-on.
2. Pre-discharge: once  $t_{HBxCCP\ FW}$  for symmetrization has elapsed, the gate of the high-side MOSFETx is pre-discharged with the current - IPREDCHGz for a duration  $t_{DPCHGz}$ . IPREDCHGz is a device internal parameter, which is self-adaptive (See next phase).
3. Discharge: After  $t_{PREDCHGz}$ , the pre-discharge current is decreased in absolute value from IPREDCHGz down to IDCHGz. The effective tDOFF3) is measured and compared to the configured tDOFFz for the automatic adaptation of IPREDCHGz. The discharge phase ends up at expiration of  $t_{HBxCCP\ active}$  for cross-current protection.
4. Cross-current protection phase: The cross-current protection is concurrent to the pre-discharge and discharge of the high-side MOSFET. The cross-current protection phase starts when the turn-off delay for symmetrization ends up. It has the duration  $t_{HBxCCP\ active}$ . During  $t_{HBxCCP\ active}$ , the low-side MOSFETx is kept OFF. When  $t_{HBxCCP\ active}$  has elapsed, the gate of the low-side MOSFET x is charged with the current ICHGFWz until the end of  $t_{FVDS}$ , provided that  $V_{SHx} < V_{SHL}$ .



### Adaptive control of pre-discharge current

Refer to Chapter 10.3.6 for information on the pre-discharge currents.

The pre-discharge current IPREDCHGz is a self-adaptive parameter if AGC[1:0] = (1,0) or (1,1) (see **GENCTRL2**).

The SC77708 adapts the IPREDCHGz to match the measured  $t_{DOFFz}$  to the configured value.

IPREDCHGz is clamped between IDCHG0 (1 mA typ.) and ICHGMAXz (see **PWM\_ICHGMAX\_CCP\_BLK3\_ACT**).

IPREDCHGz is initialized to min (IPDCHGINITz, ICHGMAXz) (refer to **PWM\_PDCHG\_INIT**) when the SC77708 receives a SPI command setting PWMz\_EN to 1 (see PWMSET).

The pre-discharge current is increased or decreased by one, respectively by two current steps (Chapter 11.3.6) if the control bit IPCHGADT in the control register GENCTRL1 is set to 0 respectively 1.

The following adaptive schemes can be selected:

AGCFILT = 0 (**GENCTRL2**): No filter is applied

- If the effective  $t_{DOFFz}$  is longer than the configured  $t_{DOFFz}$ , then IPREDCHGz is increased during the next pre-discharge phase
- If the effective  $t_{DOFFz}$  is shorter than the configured  $t_{DOFFz}$ , then IPREDCHGz is decreased during the next pre-discharge phase
- The pre-charge current is increased or decreased by one, respectively by two current steps (Chapter 10.3.6) if the control bit IPCHGADT in the control register GENCTRL1 is set to 0 respectively 1.

AGCFILT = 1: The filter is applied

- If the effective  $t_{DOFFz}$  of the last two PWM cycles are longer than the configured  $t_{DOFFz}$ , then IPREDCHGz is increased during the next pre-charge phase.
- If the effective  $t_{DOFFz}$  of the last two PWM cycles are shorter than the configured  $t_{DOFFz}$ , then IPREDCHGz is decreased during the next pre-charge phase.
- If none of the two cases are applicable, then IPREDCHGz is unchanged during the next pre-charge phase.
- The pre-charge current is increased or decreased by one, respectively by two current steps if the control bit IPCHGADT is set to 0 respectively 1.

#### 10.3.3.2 Low-side PWM with adaptive gate control, motor operating as load

The following section describes the MOSFET control when the PWM signal is applied to the low-side MOSFET of one half-bridge.

Assumption: the PWM channel z, z = 1,2 or 3, is applied to the low-side MOSFET of the half-bridge x, x = 1 ... 8.



----- Current Flow PWMz = High

----- Current Flow PWMz = Low

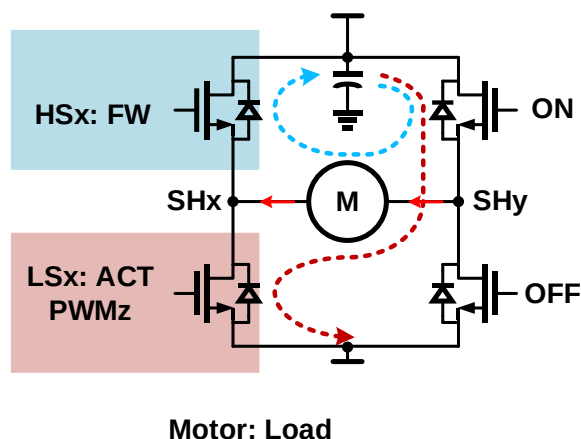


Figure 10-12 PWM Channel z is mapped to low-side x, motor operating as load.

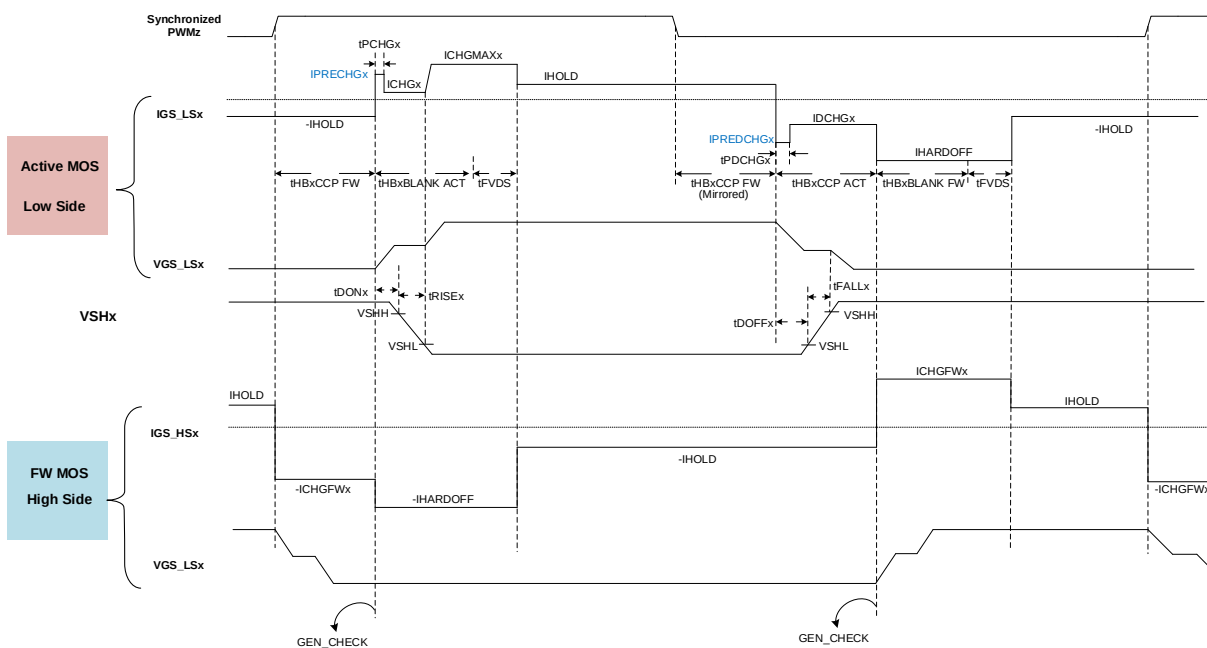


Figure 10-13 Adaptive turn-on and turn-off, low-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as load.

The description of the control of the PWM half-bridge differs from the description of Chapter 11.3.3.1 only by exchanging high-side x and low-side x and the thresholds  $V_{SHH}$  and  $V_{SHL}$ .

### 10.3.3.3 High-side PWM with adaptive gate control, motor operating as generator

The control scheme during high-side PWM in generator mode is equivalent to low-side MOSFET in load mode with the complementary signal of the external PWM input. The turn-on, turn-off delay times and the rise and fall times are applied and measured for the active MOSFET.

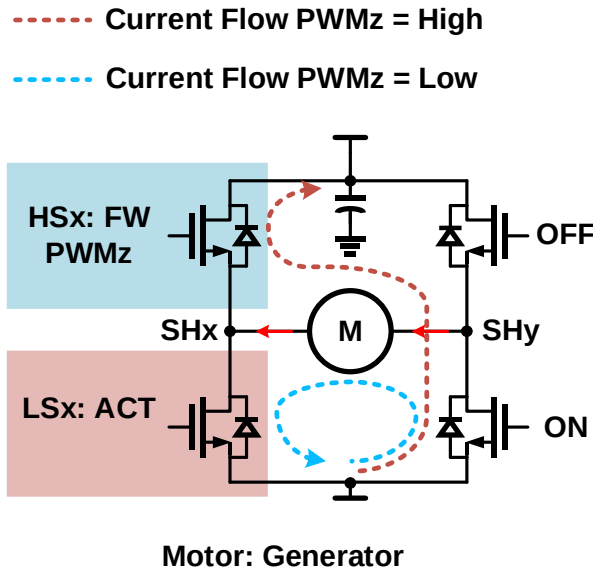


Figure 10-14 PWM Channel z is mapped to high-side x, motor operating as generator.

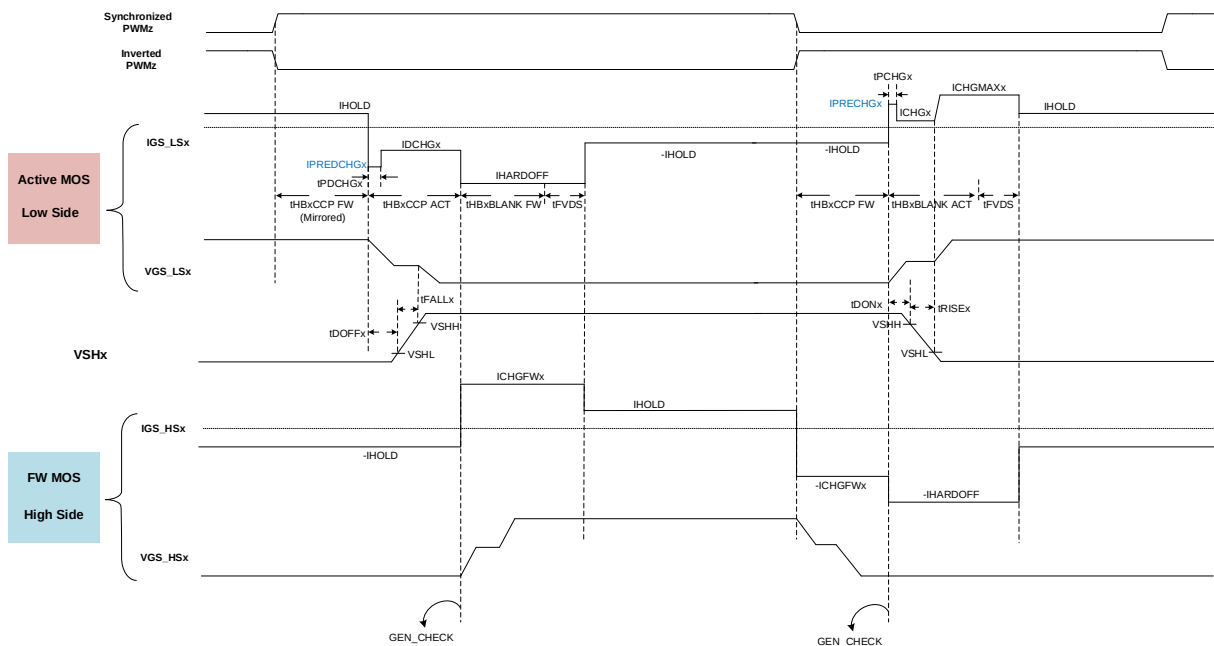


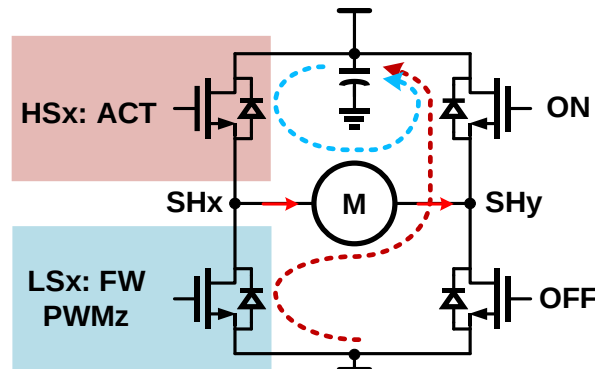
Figure 10-15 Adaptive turn-on and turn-off, high-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as generator.

#### 10.3.3.4 Low-side PWM with adaptive gate control, motor operating as generator

The control scheme during high-side PWM in generator mode is equivalent to low-side PWM in load mode with the complementary signal of the external PWM input. The turn-on, turn-off delay times and the rise and fall times are applied and measured for the active MOSFET.

----- Current Flow PWMz = High

----- Current Flow PWMz = Low



**Motor: Generator**

**Figure 10-16 PWM Channel z is mapped to low-side x, motor operating as generator.**

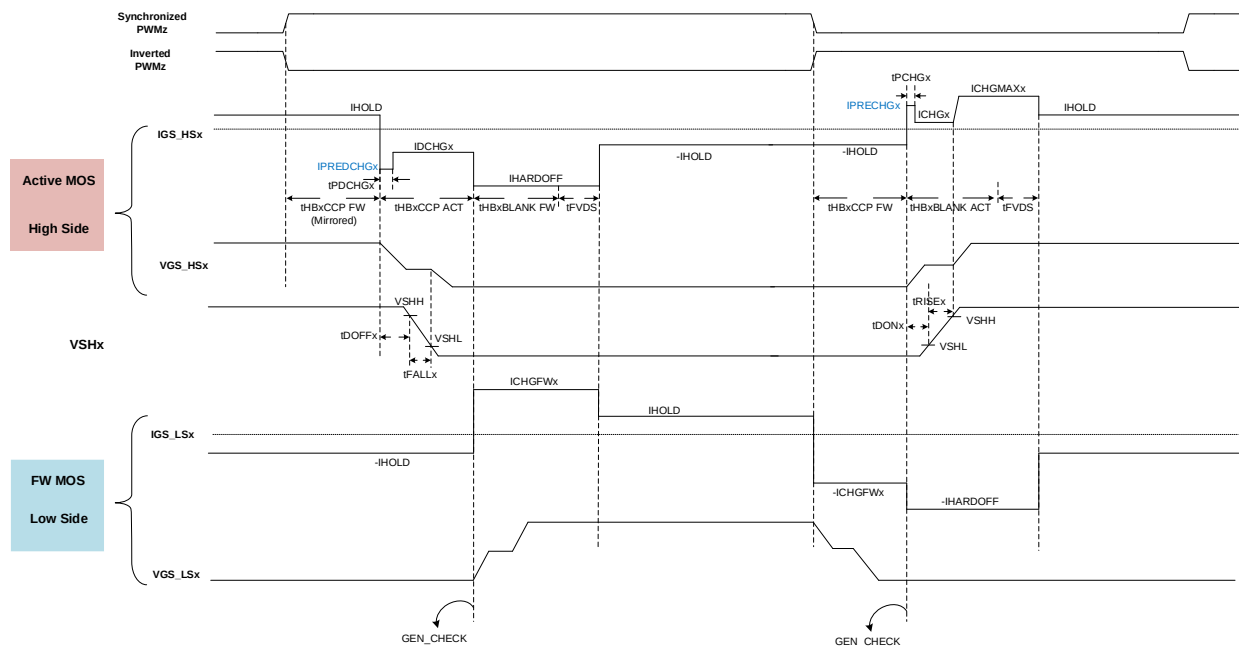


**Figure 10-17 Adaptive turn-on and turn-off, low-side PWM, AGC[1:0] = (1,0) or (1,1), motor operating as generator.**

### 10.3.3.5 Status bits for regulation of turn-on and turn-off delay times

The control bits TDREGx (**GENSTAT**) indicate if tDONx and tDOFFx of the PWM channel x using the adaptive gate control scheme (AGC[1:0] = 10B or 11B) is in regulation.

The PWM channel is considered in regulation if one of the following conditions are met:

- the effective turn-on and turn-off delays are equal to the configured delays for at least eight consecutive PWM cycles
- the error between the effective and configured delay changes its sign at least three times during the last 8 PWM cycles

**10.3.3.6 Precharge and predischARGE phases with EN\_DEEP\_AD = 1**

This section is valid if **EN\_DEEP\_AD** = 1. Enabling this feature leads to a lower granularity of the resulting precharge and predischARGE currents.

If **EN\_DEEP\_AD** = 1:

- The precharge phase can be divided in two parts, during which different precharge current steps are applied
- The predischARGE phase can be divided in two parts, during which different predischARGE current steps are applied

The device exits the “deep adaptation mode” if  $t_{DON}$ , respectively  $t_{DOFF}$ , cannot be regulated and the resolution of the precharge time cannot be further divided. Then, one single current step is applied during the precharge time.

**10.3.4 PWM operation without adaptive gate control**

The adaptive gate control is disabled if **AGC[1:0]** is set to (0,0) or (0,1). The effective turn-on and turn -off delays of the PWM MOSFETs are not regulated. Two modes can be selected.

The target turn-on and turn-off delay times of PWM MOSFETs (configured in **TDON\_OFF1**, **TDON\_OFF2**, **TDON\_OFF3**) are no longer regulated. Nevertheless the status registers **EFF\_TDON\_OFF1**, **EFF\_TDON\_OFF2**, **EFF\_TDON\_OFF3** still report the effective turn-on and turn-off times of the PWM MOSFET.

**10.3.4.1 PWM operation without adaptive gate control, AGC[1:0] = (0,0)**

When **AGC[1:0]** = (0,0) (see **GENCTRL2**), the control of the gate drivers in PWM mode differs from the description of **Chapter 10.3.3, PWM operation with adaptive gate control**, only by the suppression of the pre-charge and pre-discharge phases.

**10.3.4.2 PWM operation without adaptive gate control, AGC[1:0] = (0,1)**

When **AGC[1:0]** = (0,1) (see **GENCTRL2**), the control of the gate drivers in PWM mode differs from the description of **Chapter 10.3.4.1, PWM operation without adaptive gate control, AGC[1:0] = (0,0)**, only by the addition of a pre-discharge phase. During **tPDCHGz**, the gate of the PWM MOSFET mapped to the PWM channel z is discharged with the current **-IPDCHGINITz** (Refer to **PWM\_PDCHG\_INIT**).

**10.3.5 Gate driver current**

Each gate driver is able to source and sink currents from 1.0 mA to 100 mA with 32 steps.

The charge and discharge currents of the active and the FW MOSFETs are configured separately by:

- The **REG\_BANK** bit (**GENCTRL1**)
- The control registers **PWM\_ICHG\_ACT**, **PWM\_IDCHG\_ACT**, **PWM\_ICHG\_FW**

The charge current of the active MOSFETs are configured by **PWM\_ICHG\_ACT** (**REG\_BANK** = 0)

The discharge current of the active MOSFETs are configured by **PWM\_IDCHG\_ACT** (**REG\_BANK** = 0)

The charge and discharge current of the FW MOSFET are configured by **PWM\_ICHG\_FW** (**REG\_BANK** = 1)

| ICHGx[4:0], ICHGxFW[4:0],<br>IPCHGINITx[4:0] | charge current (mA) | deviation to nominal<br>values (%) |
|----------------------------------------------|---------------------|------------------------------------|
| 00000b                                       | 1.0                 | ±60%                               |



|        |      |      |
|--------|------|------|
| 00001b | 1.5  | ±60% |
| 00010b | 2.0  | ±60% |
| 00011b | 3.2  | ±60% |
| 00100b | 4.5  | ±60% |
| 00101b | 6.3  | ±60% |
| 00110b | 8.0  | ±38% |
| 00111b | 10.3 | ±38% |
| 01000b | 12.5 | ±38% |
| 01001b | 15.1 | ±38% |
| 01010b | 17.8 | ±38% |
| 01011b | 20.8 | ±38% |
| 01100b | 23.9 | ±38% |
| 01101b | 27.0 | ±38% |
| 01110b | 30.0 | ±28% |
| 01111b | 33.5 | ±28% |
| 10000b | 37.1 | ±28% |
| 10001b | 40.7 | ±28% |
| 10010b | 44.3 | ±28% |
| 10011b | 48.3 | ±28% |
| 10100b | 52.3 | ±28% |
| 10101b | 56.2 | ±28% |
| 10110b | 60.1 | ±28% |
| 10111b | 64.2 | ±28% |
| 11000b | 68.3 | ±28% |
| 11001b | 72.5 | ±28% |
| 11010b | 76.8 | ±28% |
| 11011b | 81.4 | ±28% |



|        |       |      |
|--------|-------|------|
| 11100b | 86.0  | ±28% |
| 11101b | 91.0  | ±28% |
| 11110b | 96.0  | ±25% |
| 11111b | 100.0 | ±25% |

Table 10-6 Charge currents in PWM operation

| IDCHGx[4:0],<br>IDCHGxFW[4:0],<br>IPDCHGINITx[4:0] | discharge current<br>(mA) | deviation to nominal<br>values (%) |
|----------------------------------------------------|---------------------------|------------------------------------|
| 00000b                                             | 1.0                       | ±60%                               |
| 00001b                                             | 1.9                       | ±60%                               |
| 00010b                                             | 2.8                       | ±60%                               |
| 00011b                                             | 4.3                       | ±60%                               |
| 00100b                                             | 5.7                       | ±60%                               |
| 00101b                                             | 7.5                       | ±60%                               |
| 00110b                                             | 9.4                       | ±38%                               |
| 00111b                                             | 11.8                      | ±38%                               |
| 01000b                                             | 14.2                      | ±38%                               |
| 01001b                                             | 17.0                      | ±38%                               |
| 01010b                                             | 19.7                      | ±38%                               |
| 01011b                                             | 22.9                      | ±38%                               |
| 01100b                                             | 26.0                      | ±38%                               |
| 01101b                                             | 29.0                      | ±38%                               |
| 01110b                                             | 32.0                      | ±28%                               |
| 01111b                                             | 35.8                      | ±28%                               |
| 10000b                                             | 39.5                      | ±28%                               |
| 10001b                                             | 43.1                      | ±28%                               |
| 10010b                                             | 46.8                      | ±28%                               |
| 10011b                                             | 50.8                      | ±28%                               |



|        |       |      |
|--------|-------|------|
| 10100b | 54.7  | ±28% |
| 10101b | 58.6  | ±28% |
| 10110b | 62.5  | ±28% |
| 10111b | 66.6  | ±28% |
| 11000b | 70.6  | ±28% |
| 11001b | 74.6  | ±28% |
| 11010b | 78.5  | ±28% |
| 11011b | 82.8  | ±28% |
| 11100b | 87.0  | ±28% |
| 11101b | 91.0  | ±28% |
| 11110b | 95.0  | ±25% |
| 11111b | 100.0 | ±25% |

Table 10-7 Discharge currents in PWM operation

## 10.4 Passive discharge

Resistors ( $R_{GGND}$ ) between the gate of GHx and GND, and between GLx and GND, ensure that the external MOSFETs are turned off, when EN = Low or when  $V_{DD} < V_{DDPOFFR}$ .

During normal mode with **BD\_PASS** bit reset (**GENCTRL2**) without failure causing the deactivation of the gate drivers, these pull-down resistors are switched off. The MOSFET are actively kept off with the discharge current IHOLD.

During normal mode with failure leading to the deactivation of the gate drivers (charge pump undervoltage, VS undervoltage and overvoltage, thermal shutdown) or in fail safe mode,  $R_{GGND}$  are activated, independently from the setting of **BD\_PASS**.

### Gate driver power down

The gate driver is deactivated in normal mode with **BD\_PASS** set to 1 and all HBxMODE[1:0]=00 or 11. The current consumption of the VS input is reduced to  $I_{S\_BD\_PASS}$  and  $R_{GGND}$  are activated.

## 10.5 Bridge driver in passive mode

The low-side MOSFETs LS1, LS2, LS3 and LS4 can be controlled when the bridge driver in the passive mode. All the other MOSFETs kept off by the passive discharge.

The bridge driver is in passive mode:

- If **BD\_PASS** = 1 in normal mode and all HBxMODE[1:0]=00B or 11B.
- In sleep mode (EN = Low).



- If  $V_{DD} < V_{DD\ POFFR}$ .

When the bridge driver is in passive mode, then the state of the low-side MOSFETs LS1-LS4 is configured by **PASS\_MOD**.

- If **PASS\_MOD**[1:0] = 00b : LS1, LS2, LS3 and LS4 are off (passive discharge).
- If **PASS\_MOD**[1:0] = 01b : LS1, LS2, LS3 and LS4 are on (static brake).
- If **PASS\_MOD**[1:0] = 10b : LS1, LS2, LS3 and LS4 are turned on if  $V_S > V_{SOV\_PASS\ OFF}$  (overvoltage brake). The PWM3 pin is pulled down by an internal open drain (**R<sub>PWM3\_OD</sub>**).
- If **PASS\_MOD**[1:0] = 11b : LS1, LS2, LS3 and LS4 are turned on if PWM1 = High and  $V_S > V_{SOV\_PASS\ OFF}$  (overvoltage brake conditioned by PWM1). The PWM3 pin is pulled down by an internal open drain (**R<sub>PWM3\_OD</sub>**).
- If **DIS\_PASS\_VS\_OV** = 1 (refer to **HB\_EN\_CFG**), **PASS\_MOD**[1:0] = 10b & 11b no longer need the condition  $V_S > V_{SOV\_PASS\_OFF}$ .
- If **EN\_PASS\_LS5678** = 1 (refer to **HB\_EN\_CFG**), all low side drivers will turn on when brake conditions satisfied.

LS1, LS2, LS3 and LS4 MOSFETs with an input capacitor up to 10 nF are turned on within **t<sub>ON\_BD\_PASS</sub>**.

The setting of LS1-LS4 according to **PASS\_MOD** in sleep mode or if  $V_{DD} < V_{DD\ POFFR}$  is valid only if  $V_S$  stays above **V<sub>SLEEP\_SET</sub>**. If  $V_S$  drops below **V<sub>SLEEP\_SET</sub>**, then LS1-LS4 behave as if **PASS\_MOD** = 10B, the latter setting is kept even after a  $V_S$  recovery.



## 11 Protections and diagnostics

### 11.1 Reverse polarity protection

The output of the charge pump (CP pin) can be used to supply an external n-channel MOSFET, building an active reverse polarity protection.

### 11.2 Drain-source voltage monitoring with bridge driver in active mode

When EN = High and **BD\_PASS** = 0 (bridge driver in active mode), voltage comparators monitor the activated MOSFETs to protect the high-side MOSFETs and low-side MOSFETs against a short circuit respectively to ground and to the battery during ON-state.

If a Drain-Source overvoltage is detected, the corresponding half-bridge is latched off.

If HBxD = 0, x = 1...8 (see **VDS1** and **VDS2**): The half-bridge x is latched off if the voltage difference between DH and VSHx exceeds the threshold voltage configured by **VDS1**, and **VDS2** (see **Table 11-1**).

If HBxD = 1, x = 1...8 (see **VDS1** and **VDS2**): The half-bridge x is latched off if the voltage difference between CSIN1 and VSHx exceeds the threshold voltage configured by **VDS1**, and **VDS2** (see **Table 11-1**).

If HBxVDSTH\_LS = 1, x = 1...8 (see **VDSOV\_IDCHG\_DESCALE**): The low side Vds protection of the half-bridge x add 0.2V to the HBxVDSTH.

Short circuits of low-side MOSFETs to VS are detected by monitoring the voltage difference between VSHx and SL (see **Table 11-1**).

| HBxVDSTH[2:0] | Drain-Source overvoltage threshold for HSx and LSx (typical) |
|---------------|--------------------------------------------------------------|
| 000b          | 0.15V (default)                                              |
| 001b          | 0.20V                                                        |
| 010b          | 0.25V                                                        |
| 011b          | 0.30V                                                        |
| 100b          | 0.40V                                                        |
| 101b          | 0.50V                                                        |
| 110b          | 0.60V                                                        |
| 111b          | 2.00V                                                        |

Table 11-1 Drain-Source overvoltage threshold, EN = High, **BD\_PASS** = 0

**Attention:** HBxVDSTH[2:0] = 111B (2 V threshold) is dedicated for the diagnostic in off-state. It is highly recommended to select another drain-source overvoltage threshold once the routine of the diagnostic in off-state has been performed to avoid additional current consumption from VS and from the charge pump.

The device reports a Drain-Source overvoltage error if both conditions are met:

- After expiration of the blank time.
- If the Drain-Source voltage monitoring exceeds the configured threshold for a duration longer than the configured filter time



(see **GENCTRL2** TFVDS bits).

Note: Exception with **static activated** MOSFETs when the short circuit is applied **before the expiration of the blank time**: the MOSFETs are turned off after the **blank time + 2 x tFVDS**

| HBxVDSTH[2:0] | Drain-Source overvoltage filter time (typical) |
|---------------|------------------------------------------------|
| 00b           | 0.5us (default)                                |
| 01b           | 1us                                            |
| 10b           | 2us                                            |
| 11b           | 3us                                            |

Table 11-2 Drain-Source overvoltage filter time

If a short circuit is detected by the Drain-Source voltage monitoring:

- The impacted half-bridge is latched off.
  - The discharge current is according to the settings of **ST\_ICHG**, as if the MOSFET was previously statically activated.
- The corresponding bit in the status register **DSOV** is set.
- The VDSE in Global Status Register **Global status byte** is set.

If a Drain-Source overvoltage is detected for one of the MOSFETs, then the status register **DSOV** must be cleared in order to re-enable the faulty half-bridge.

### 11.3 Drain-source voltage monitoring with bridge driver in passive mode

LS1 to LS4 can be activated when the bridge driver is in passive mode (refer to **Chapter 10.5**).

A drain-source overvoltage monitoring of LS1, LS2, LS3 and LS4 MOSFETs is enabled if **PASS\_VDS** is set. The drain-source monitoring (VSHx - VSL, x = 1 to 4) is ignored for **tBLK\_BD\_PASS** (blank time) after beginning of the activation of LS1, LS2, LS3 and LS4 MOSFETs.

The drain-source monitoring filter time is **tDSMON\_FILT\_BD\_PASS** and the VDS threshold is **VVDSMON\_BD\_PASS** (370 mV typ).

If a drain-source overvoltage is detected, then:

- The LS1, LS2, LS3 and LS4 MOSFETs are turned off.
- **PASS\_VDSOV** and the corresponding status bit in **DSOV** are set.

LS1-4 can be reactivated by clearing **DSOV**. Clearing **DSOV** also clears **PASS\_VDSOV**.

### 11.4 Cross-current protection and drain-source overvoltage blank time

All gate drivers feature a cross-current protection time and a Drain-Source overvoltage blank times.

The cross-current protection avoids the simultaneous activation of the high-side and the low-side MOSFETs of the same half-bridge.

During the blank time, the drain-source overvoltage detection is disabled, to avoid a wrong fault detection during the activation



phase of a MOSFET.

#### Notes

1. The setting of the cross-current protection and of the blank times may be changed by the microcontroller only if all PWMx\_EN bits are reset, x = 1 ... 3.
2. Changing the Drain-Source overvoltage of a half-bridge x (HBx) in on-state (HBxMODE[1:0]=(0,1) or (1,0)) may result in a wrong VDS overvoltage detection on HBx. Therefore, it is highly recommended to change this threshold when HBxMODE[1:0]=(0,0) or (1,1).

#### 11.4.1 Cross-current protection

Four pairs of cross-current protection and blank times ((tCCPx, tBLANKx), x = 1...4) can be mapped to each half-bridge with the control register **CCP\_BLK1**.

The cross-current protection time of the active MOSFET of the FW MOSFETs are set independently.

- The cross-current protection times of the active MOSFETs are configured by the control bits TCCPx\_ACT (**CCP\_BLK2\_ACT**, **PWM\_ICHGMAX\_CCP\_BLK3\_ACT**) and **CCP\_BLK1**
- The cross-current protection times of the free-wheeling MOSFETs are configured by the control bits TCCPx\_FW (**CCP\_BLK2\_FW**, **PWM\_ICHGMAX\_CCP\_BLK3\_FW**) and **CCP\_BLK1**

| TCCPx_ACT[2:0],<br>TCCPx_FW[2:0], x = 1...4 | Cross-current protection time tCCPx_ACT/tCCPx_FW, x = 1...4 (typical) |
|---------------------------------------------|-----------------------------------------------------------------------|
| 000b                                        | 375ns                                                                 |
| 001b                                        | 625ns                                                                 |
| 010b                                        | 1us                                                                   |
| 011b                                        | 1.5us                                                                 |
| 100b                                        | 2us (default)                                                         |
| 101b                                        | 3us                                                                   |
| 110b                                        | 4us                                                                   |
| 111b                                        | 16us                                                                  |

- 1) When applying a cross-current protection time of 16 µs to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA to avoid an overheating of the gate driver.

Table 11-3 Cross-current protection time

#### 11.4.2 Drain-source overvoltage blank time in bridge driver active mode

A configurable blank time (refer to **Table 11-4**) for the Drain-Source monitoring is applied at the turn-on of the MOSFETs. During the blank time, a Drain-Source overvoltage error is masked.

The blank time of the active MOSFET of the FW MOSFETs are set independently:

- The blank times of the active MOSFETs are configured by the control bits TBLANKx\_ACT (**CCP\_BLK2\_ACT**, **PWM\_ICHGMAX\_CCP\_BLK3\_ACT**) and **CCP\_BLK1**
- The blank times of the free-wheeling MOSFETs are configured by the control bits TBLANKx\_FW (**CCP\_BLK2\_FW**,

**PWM\_ICHGMAX\_CCP\_BLK3\_FW) and CCP\_BLK1****Half-bridges in PWM mode**

If the detection of the generator mode is disabled (**EN\_GEN\_CHECK** = 0):

- The blank time of the PWM MOSFET starts at the expiration of the cross-current protection time of the FW MOSFET (tHBxCCP FW).
- The blank time of the FW MOSFET starts after expiration of the cross-current protection time at turn-off of the PWM MOSFET (tHBxCCP Active).

If the detection of the generator mode is enabled (**EN\_GEN\_CHECK** = 1):

- The blank time of the Active MOSFET starts at the expiration of the cross-current protection time of the FW MOSFET (tHBxCCP FW).
- The blank time of the FW MOSFET starts after expiration of the cross-current protection time at turn-off of the Active MOSFET (tHBxCCP Active).

For statically activated half-bridges, the blank time starts:

- Case 1: At expiration of the active cross-current protection, if the opposite MOSFET was previously activated.
- Case 2: Right after the decoding of the SPI command to turn on a MOSFET, if the half-bridge was in high impedance.

The blank times can be configured with the control registers **CCP\_BLK2\_ACT** and **PWM\_ICHGMAX\_CCP\_BLK3\_ACT** for the active MOSFETs and **CCP\_BLK2\_FW** and **PWM\_ICHGMAX\_CCP\_BLK3\_FW** for the freewheeling MOSFETs.

| TBLANKx[2:0], x = 1...4 | Drain-Source overvoltage blank time tBLANKx, x = 1...4 (typical) |
|-------------------------|------------------------------------------------------------------|
| 000b                    | 625ns                                                            |
| 001b                    | 1us                                                              |
| 010b                    | 1.25us                                                           |
| 011b                    | 1.5us                                                            |
| 100b                    | 2us (default)                                                    |
| 101b                    | 3us                                                              |
| 110b                    | 4us                                                              |
| 111b <sup>1)</sup>      | 16us                                                             |

- 1) When applying a cross-current protection time of 16  $\mu$ s to a half-bridge, the max. drive current used for this half-bridge must be set below 30 mA to avoid an overheating of the gate driver.

**Table 11-4 Drain-source overvoltage blank time**

**11.4.3 Mapping of cross-current protection and blank times**

One of the pairs of cross-current protection and blank times are mapped to each half-bridge according to **Table 11-5**, by configuring the control register **CCP\_BLK1**.

|                          |                                |
|--------------------------|--------------------------------|
| HBxCCPBLK[1:0], x = 1..8 | tCCP and tBLANK applied to HBx |
|--------------------------|--------------------------------|



|     |                                    |
|-----|------------------------------------|
| 00b | (tCCP1, tBLANK1) are mapped to HBx |
| 01b | (tCCP2, tBLANK2) are mapped to HBx |
| 10b | (tCCP3, tBLANK3) are mapped to HBx |
| 11b | (tCCP4, tBLANK4) are mapped to HBx |

Table 11-5 Mapping of tCCP and tBLANK to the half-bridges

## 11.5 OFF-state diagnostic

In order to support the off-state diagnostic, the gate driver of each MOSFET provides pull-up (330  $\mu$ A typ.) and a pull-down current (1500  $\mu$ A typ.) at the SHx pins when the driver is active (**BD\_PASS** = 0). Under these conditions, the pull-up current sources are active.

**Attention:** The off-state diagnostic is possible only when the bridge driver is active (**BD\_PASS**=0) and the corresponding half-bridge is off (**HBxMODE** = 00b or 11b).

The pull-down current of each gate driver is activated by the control bits HBxIDIAG (**HBIDIAG** register).

During the off-state diagnostic routine performed by the microcontroller, the drain-source overvoltage threshold of the relevant half-bridges must be set to 2 V nominal. Refer to **Table 11-1**. Once the routine is finished, it is highly recommended to decrease the drain-source overvoltage threshold to a lower value, avoiding additional current consumption from the VS input.

The following failures can be detected:

- MOSFET short circuit to GND.
- MOSFET short circuit the battery.
- Open load (disconnected motor).

The status of the output voltages VOUTx, with x = 1 ... 8, can be read back with status bit HBxVOUT (register **HBVOUT\_PWMERR**) when the corresponding half-bridge is in off-state (**HBxMODE**[1:0] = 00 or 11).

Note: HBxVOUT = 0 if the half-bridge x is not in off-state (**HBxMODE**[1:0] = (0,1) or (1,0)).

## 11.6 Temperature monitoring

Temperature sensors are integrated in the device. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds.

### Temperature warning

If the temperature sensor reaches  $T_{JW}$ , then **TW** is set (see **GENSTAT**). This bit is latched and reset by clearing **GENSTAT** if the thermal warning condition has disappeared. The outputs stages however remain activated.

### Temperature shutdown

If the temperature sensor reaches  $T_{JSD}$  **all gate drivers are latched off, the charge pump is deactivated**; the SUPE bit (Supply Error bit, see **Global status byte**), **TSD** (Thermal Shutdown bit) and **CPUV** (Charge Pump Undervoltage) are set (see **GENSTAT**). All outputs remain deactivated until the temperature shutdown condition has disappeared and **GENSTAT** is cleared.

The discharge current is according to the settings of **ST\_ICHG**, as if the MOSFET was previously statically activated.

To resume normal functionality of the gate drivers (in the event the overtemperature condition disappears, or to verify if the failure still exists) the microcontroller shall clear **GENSTAT**.



## 11.7 $V_S$ overvoltage and undervoltage shutdown

The power supply rails  $V_S$  and  $V_{DD}$  are monitored for supply fluctuations. The  $V_S$  supply is monitored for under- and over-voltage conditions whereas the  $V_{DD}$  supply is monitored for under-voltage conditions.

### 11.7.1 $V_S$ undervoltage

If  $V_S$  drops below  $V_{SUV\ OFF}$ , then all external MOSFETs are latched off, however, the logic information remains intact and uncorrupted provided that  $V_{DD} > V_{DD\ POR}$ .

SUPE (Supply Error bit, see **Global status byte**), **VSUV** and **CPUV** bits (see **GENSTAT**), are set and latched.

The **VSUV** bit is reset by clearing **GENSTAT** to re-enable the MOSFETs.

The **VSUV** bit is reset if the following conditions are fulfilled:

- $V_S > V_{SUV\ ON}$ .
- The SC77708 receives a clear command to **GENSTAT**.

### 11.7.2 $V_S$ overvoltage with bridge driver in active mode

If  $V_S$  rises above the switch-off voltage ( $V_{SOV\ OFF1}$  if  $V_{SOVTH} = 0$ ,  $V_{SOV\ OFF2}$  if  $V_{SOVTH} = 1$ ) all external MOSFETs are latched off, and the charge pump is deactivated. SUPE bit (see **Global status byte**), **VSOV** bit ( $V_S$  over-voltage bit, see **GENSTAT**), and **CPUV** bit are set and latched. If  $V_S$  decreases below  $V_{SOV\ ON}$ , then the charge pump is reactivated automatically. The **VSOV** bit must be reset to re-enable the MOSFETs.

The **VSOV** bit is reset if the following conditions are fulfilled:

- $V_S < V_{SOV\ ON}$ .
- The SC77708 receives a clear command to **GENSTAT**.

The discharge current is according to the settings of **ST\_ICHG**, as if the MOSFET was previously statically activated.

### 11.7.3 $V_S$ overvoltage with bridge driver in passive mode

When the bridge driver is in passive mode (refer to **Chapter 10.5**):

- If  $PASS\_MOD[1:0] = 10B$ : LS1, LS2, LS3 and LS4 are turned on if  $V_S > V_{SOV\ PASS\ OFF}$  (overvoltage brake). The PWM3 pin is pulled down by an internal open drain (**R<sub>PWM3\_OD</sub>**).
- If  $PASS\_MOD[1:0] = 11B$ : LS1, LS2, LS3 and LS4 are turned on if  $V_S > V_{SOV\ PASS\ OFF}$  and PWM1 = High (overvoltage brake conditioned upon PWM1). The PWM3 pin is pulled down by an internal open drain (**R<sub>PWM3\_OD</sub>**).

### 11.7.4 $V_{DD}$ undervoltage

If the  $V_{DD}$  logic supply decreases below the undervoltage threshold,  $V_{DD\ POR}$ , the SPI interface shall no longer be functional. The digital block will be reset and the gate drivers are switched off. The undervoltage reset is released once  $V_{DD}$  voltage is above the undervoltage threshold,  $V_{DD\_POR}$ .



### 11.7.5 Charge pump undervoltage

The voltage of the charge pump output ( $V_{CP}$ ) is monitored in order to ensure a correct control of the external MOSFETs.

If  $V_{CP}$  falls below the configured charge pump undervoltage threshold:

- The external MOSFETs are actively discharged for the duration  $t_{HBXCCP}$  with the current  $I_{CHGSTx}$ , then the gate drivers are turned off.
- **CPUV** (**GENSTAT**), **SUPE** bits (**Global status byte**) and the Global Error Flag are set and latched.

The **CPUV** and **SUPE** bits are reset and the normal operation is resumed if **GENSTAT** is cleared, and  $V_{CP} > V_{CPUV}$ .

#### Notes

1. A charge pump undervoltage event is reported after a power-on reset, when the charge time of the capacitor connected to  $V_{CP}$  exceeds  $t_{CPUV}$
2. The charge pump is deactivated after a  $V_S$  undervoltage, a  $V_S$  overvoltage and a thermal shutdown, causing a charge pump undervoltage condition. Consequently, **CPUV** and **SUPE** bits are set together with **VSOV**, **VSUV** or **TSD** bits (see **GENSTAT**).

### 11.8 Switching parameters of MOSFETs in PWM mode

The effective switching parameters of the active MOSFETs (**EN\_GEN\_CHECK** =1) or of the PWM MOSFET (**EN\_GEN\_CHECK** =0) can be read out with dedicated status registers:

- The turn-on and turn off delays, noted  $t_{DON}$  and  $t_{DOFF}$ , are reported by the status register **EFF\_TDON\_OFF1**, **EFF\_TDON\_OFF2**, **EFF\_TDON\_OFF3**.
- The rise and fall times, noted  $t_{RISE}$  and  $t_{FALL}$ , are reported by the status register **TRISE\_FALL1**, **TRISE\_FALL2**, **TRISE\_FALL3**.

Refer to **Chapter 10.3** for the definition of  $t_{DON}$ ,  $t_{DOFF}$ ,  $t_{RISE}$  and  $t_{FALL}$ .

If  $t_{HBXBLANK\_ACT}$  has elapsed in motor mode, before the measurement of the effective  $t_{DON}$ , the device reports an effective  $t_{DON}$  corresponding to  $t_{HBXBLANK\_ACT}$ .

If  $t_{HBXCCP\_ACT}$  has elapsed while **EN\_GEN\_CHECK** =0, before the measurement of the effective  $t_{DOFF}$ , the device reports an effective  $t_{DOFF}$  corresponding to  $t_{HBXCCP\_ACT}$ .

### 11.9 Timeout watchdog

An integrated timeout watchdog supervises the integrity of the communication with the microcontroller. The watchdog period is programmable by the **WDPER** bit (refer to **GENCTRL1**).

After a Power-On Reset, the watchdog timer starts and the microcontroller must invert the logic value of the **WDTRIG** bit of the control register **GENCTRL1**. The default value of **WDTRIG** is 0. A correct trigger of the watchdog immediately resets the watchdog counter and starts the next cycle.

A watchdog failure is reported by the device if:

- The watchdog trigger bit is not served within the watchdog period (watchdog timeout event).
- The microcontroller writes the **WDTRIG** bit with the same value. In other words, if the **WDTRIG** value is 0 and the microcontroller re-writes **WDTRIG** to 0, or the **WDTRIG** is 1, and the microcontroller re-writes **WDTRIG** to 1, then a watchdog error is reported.

If a watchdog failure is detected, then the **FS** bit (see Global Status Byte) is set and latched, and the control registers are frozen to their default values. Consequently, all external MOSFETs are actively turned off.

In order to resume normal operation, the microcontroller must: 1. clear **GENSTAT**. 2. Set **WDTRIG** to 1 within the watchdog period, 3. Set **WDTRIG** to 0 within the watchdog period.

The watchdog period is configurable by SPI to **TWDPER1** or **TWDPER2** (refer to **WDPER**).



### Monitoring the watchdog timer

The status bits **WDMON**[1:0] report the relative position of the watchdog timer to the watchdog period. Refer to **Table 11-6**. This allows the detection of a potential latent failure associated to the watchdog

timer: the microcontroller can indeed verify that the watchdog timer is running.

| WDMON[1:0] | Position of the watchdog timer                              |
|------------|-------------------------------------------------------------|
| 00b        | watchdog timer is between [0%, 25%)of the watchdog period   |
| 01b        | watchdog timer is between [25%, 50%)of the watchdog period  |
| 10b        | watchdog timer is between [50%, 75%)of the watchdog period  |
| 11b        | watchdog timer is between [75%, 100%)of the watchdog period |

**Table 11-6 Monitoring of the watchdog timer**

### Disabling the watchdog

The watchdog is enabled by default.

It is disabled only if the following SPI sequence is sent:

- First frame: Set **UNLOCK** bit to '1' (**GENCTRL1**). Note: UNLOCK is automatically reset to '0' at the end of the following frame.
- Following frame: Set **WDDIS** bit to '1' (**GENCTRL2**).

The watchdog is directly re-enabled by setting WDDIS to '0'.

## 11.10 Current sense amplifier

Two current sense amplifiers allow to monitor the motor currents. The differential input stage measures the voltage drop across an external shunt resistor.

The input common mode range allows current sensing in high-side, in low-side configuration or in the motor phase.

### 11.10.1 Unidirectional and bidirectional operation

The current sense amplifiers (CSA) can work either as unidirectional or bi-directional CSA. See **CSD1** and **CSD2**.

#### Unidirectional operation CSDx = 0

In unidirectional operation, the CSAx, x = 1 or 2, is optimized to measure the current flowing through the external shunt resistor when  $V_{CSIPx} \geq V_{CSINx}$ .

$V_{CSOx} = V_{REF\ Unidir} + (V_{CSIPx} - V_{CSINx} + V_{os}) \times G_{DIFF}$ , provided that  $V_{CSOx}$  is in the linear range.

#### Bidirectional operation CSDx = 1

In bidirectional operation, the CSAx, x = 1 or 2, measures the current flowing through the external shunt resistor in both directions:  $V_{CSIPx} \geq V_{CSINx}$  or  $V_{CSIPx} \leq V_{CSINx}$ .

The output CSOx works at half-scale range:  $V_{CSOx} = V_{REF\ Bidir} + (V_{CSIPx} - V_{CSINx} + V_{os}) \times G_{DIFF}$  provided that  $V_{CSOx}$  is in the linear



range.

When the current sense amplifiers are deactivated (VS undervoltage, VS overvoltage, CP undervoltage or Overtemperature, or CSAX\_OFF = 1), CSOx is pulled Low (between GND to 150mV)

### 11.10.2 Gain configuration

The gain of the current sense amplifier is configurable by the configuration bits CSAGx bits. Refer to **Table 11-7** and **GENCTRL1**.

| CSAGx[1:0] | Typical current sense amplifier gain $G_{DIFF}$ |
|------------|-------------------------------------------------|
| 00b        | 10V/V                                           |
| 01b        | 20V/V                                           |
| 10b        | 40V/V                                           |
| 11b        | 80V/V                                           |

**Table 11-7 Configuration of the current sense amplifier gain**

### 11.10.3 High-side and low-side setting

The CSA can be used either in high-side configuration or in low-side configuration within the specified common mode range.

The control bits CSA1L and CSA2L (**HBIDIAg**) optimize the VDD current consumption by informing the device about the common mode voltage of the CSA inputs:

- CSAXL must be set to 0 if the shunt is in low-side configuration (i.e. connected to GND or to an output with an activated low-side).
- CSAXL must be set to 1 if the shunt is in high-side configuration (i.e. connected to VS or to an output with an activated high-side).

### Notes

1. A proper information from the CSA output is not ensured if the external shunt resistor is in high-side configuration while its CSAXL bit is set to 0.
2. The external shunt resistor may be in low-side configuration while its CSAXL bit is set to 1. The current consumption from VDD is however higher than if CSAXL is set to 0.

### 11.10.4 Overcurrent detection

A comparator at CSOx detects overcurrent conditions. The overcurrent threshold is configurable with the OTHx bits. Refer to **Table 11-8** for unidirectional operation and **Table 11-9** for bidirectional operation.

CSx\_SD\_HBz (refer to OC\_SD\_HB) can config HBz shutdown or keep when OCx occur

| OTHx[1:0] | Typical Overcurrent Detection Threshold |
|-----------|-----------------------------------------|
| 00b       | $V_{CSOX} > V_{DD}/2$                   |
| 01b       | $V_{CSOX} > V_{DD}/2 + V_{DD}/10$       |



|     |                                            |
|-----|--------------------------------------------|
| 10b | $V_{CSOX} > V_{DD}/2 + 2 \times V_{DD}/10$ |
| 11b | $V_{CSOX} > V_{DD}/2 + 3 \times V_{DD}/10$ |

Table 11-8 Overcurrent detection thresholds in unidirectional operation (CSDx = 0)

| CSAGx[1:0] | Typical current sense amplifier gain $G_{DIFF}$                                          |
|------------|------------------------------------------------------------------------------------------|
| 00b        | $V_{CSOX} > V_{DD}/2 + 2 \times V_{DD}/20$ or $V_{CSOX} < V_{DD}/2 - 2 \times V_{DD}/20$ |
| 01b        | $V_{CSOX} > V_{DD}/2 + 4 \times V_{DD}/20$ or $V_{CSOX} < V_{DD}/2 - 4 \times V_{DD}/20$ |
| 10b        | $V_{CSOX} > V_{DD}/2 + 5 \times V_{DD}/20$ or $V_{CSOX} < V_{DD}/2 - 5 \times V_{DD}/20$ |
| 11b        | $V_{CSOX} > V_{DD}/2 + 6 \times V_{DD}/20$ or $V_{CSOX} < V_{DD}/2 - 6 \times V_{DD}/20$ |

Table 11-9 Overcurrent detection thresholds in bidirectional operation (CSDx = 1)

It is possible to program the device behavior when an overcurrent condition is detected:

- OCEN bit = 0 (see **GENCTRL1**): the device only reports the overcurrent event (OC, OC1 or OC2 in **GENSTAT** and Global Error Flag are set), without any change of the gate driver states
  - If the overcurrent condition is not present for more than  $t_{FOC}$ , then the overcurrent status bits are automatically cleared by the device.
- OCEN bit = 1 (see **GENCTRL1**): the device reports the overcurrent event (OC, OC1 or OC2 in **GENSTAT** and Global Error Flag are set) and turns off all MOSFETs with their static discharge current.
  - The MOSFETs can be reactivated by clearing **GENSTAT** or by resetting the OCEN bit.
  - The overcurrent status bits are reset only if the overcurrent condition is no longer present and the microcontroller clears **GENSTAT**.

The overcurrent filter time is configurable (refer to  $t_{FOC}$ ) by the control bits OCxFILT (refer to **HBIDIAG**).

$t_{FOC}$  refers to the output of the current sense amplifier. The CSO settling time ( $2 \mu s$  max,  $t_{SET}$ ) and the analog propagation delay ( $< 1 \mu s$ ) are not taken into account by the overcurrent filter time.

#### 11.10.5 CSO outputs capacitor

The capacitor directly connected to CSOx (CCSOx) must be between 10 pF and 400 pF.

The control bit **CCSO** (see **PWM\_IDCHG\_ACT**, **PWM\_PDCHG\_INIT**) optimizes the VDD current consumption for CCSOx  $< 100$  pF or CCSOx  $> 100$  pF.

#### 11.10.6 Chopping

SC77708 has two 7bits DACs for current sense amplifier chopping, VREF\_DACx (refer to **CHOPPING\_TOFF1** and **CHOPPING\_TOFF2**) is adjustable for chopping current, 更新双向的描述



$$I_{chopx} = \begin{cases} \frac{VREF\_DACx * 0.6VDD}{127 * CSAGx * R_{sense}} & CSDx = 0, \text{DAC full 7 bits data is valid} \\ \frac{VREF\_DACx * 0.3VDD}{63 * CSAGx * R_{sense}} & CSDx = 1, \text{DAC low 6 bits data is valid} \end{cases}$$

If EN\_CHOPx = 1 (refer to CHOPPING\_TOFF1 and CHOPPING\_TOFF2), enable chopping mode, when  $|I_{CSAx}| \geq I_{chopx}$ , shutdown corresponding HB; when  $|I_{CSAx}| < I_{chopx}$ , retry turn on HB after CSx\_TOFF time elapsed

## 12 Serial Peripheral Interface - SPI

The 24-bit Serial Peripheral Interface (SPI) enables the communication between the microcontroller and the SC77708. It allows to configure and control the device, and to read out the status registers for diagnostic purpose. The MOSFET driver IC acts as a SPI-slave while the microcontroller acts as a SPI-master.

The interface has a serial data input pin (SDI) to transfer data to the device, a serial data output pin (SDO) for reading data back from the device, and a serial clock pin (SCLK) for clocking data into and out of the device. A chip select pin (CSN) enables or disables the serial interface.

The SPI frame starts with the falling edge of CSN. During the falling edge of CSN, SCLK must be low (Clock Polarity CPOL = 0). Received data on SDI are shifted in on the falling edge of SCLK. Transmitted data by SDO are shifted out on the rising edge of SCLK (Clock Phase CPHA = 1). Refer to **Figure 12-2**.

The Most Significant Bit (MSB, bit 23) is shifted in/out first.

Write and clear commands are executed at the rising edge of CSN.

The SPI protocol supports both independent slave selection and daisy chain configurations.

### 12.1 SPI protocol with independent slave selection

With individual slave selection, the microcontroller controls the CSN pin of each SPI slave individually (**Figure 13-1**).

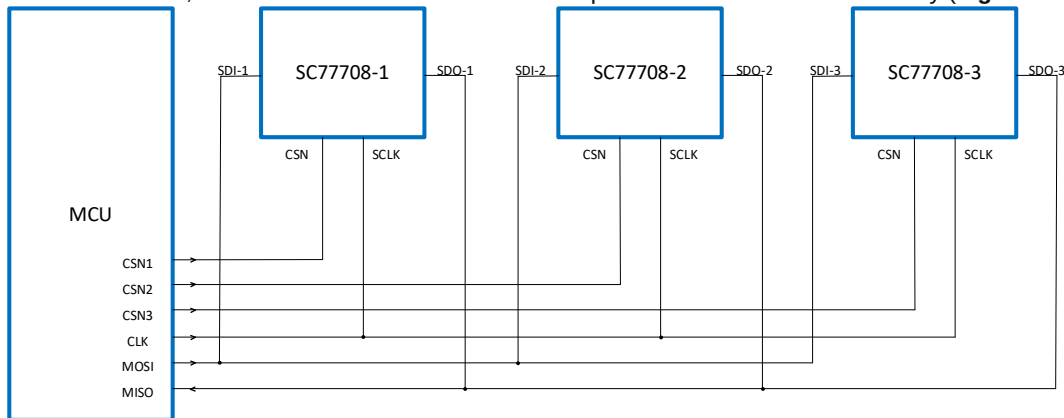
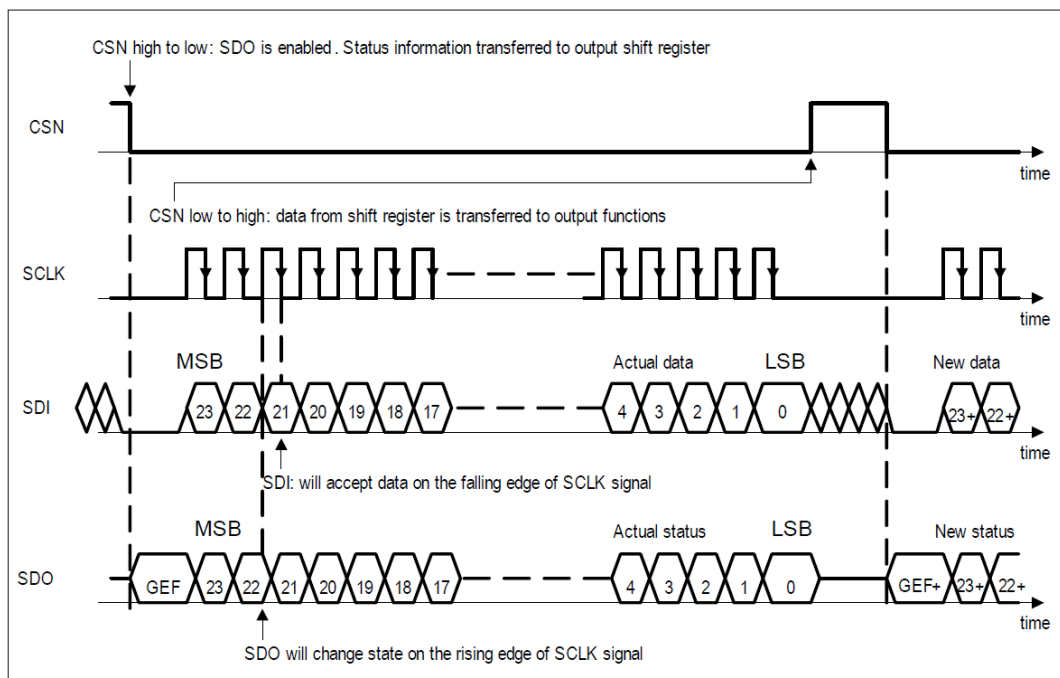


Figure 12-1 Individual slave selection with three slave devices

A SPI communication consists of 24-bit frame (**Figure 12-2**):

- SDI receives one address byte followed by two data bytes.
- SDO transmits the Global Error Flag and the Global Status Byte followed by two response bytes.


**Figure 12-2 SPI Data Transfer**

**The MSB of the address byte must be set to '1'.**

The address byte specifies (see **Figure 12-3**):

- the target register (A[4:0])
- the type of operation:
  - For control registers:
    - Read only: OP bit = '0'
    - Read and write: OP bit = '1'
  - For status registers:
    - Read only: OP bit = '0'
    - Read and clear: OP bit = '1'

**With individual slave selection, the Last Address Byte Token (LABT) must be set to '1'.**

#### **In-frame response**

The SPI protocol incorporates an in-frame response: The content of the addressed register is shifted out by SDO within the same SPI frame. This feature reduces the SPI bus load during the read out of the control or status registers.

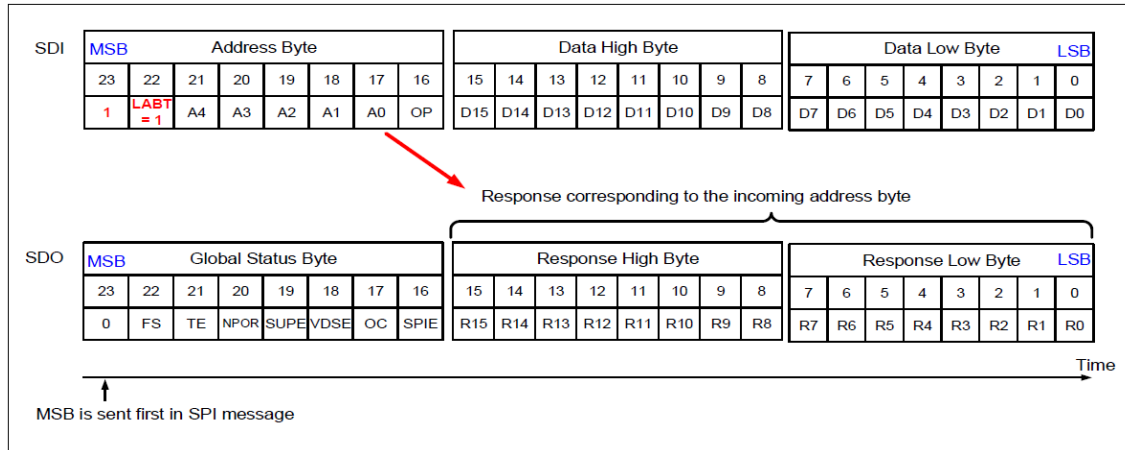


Figure 12-3 In-frame response with individual slave selection

## 12.2 Global Error Flag (GEF)

The Global Error Flag (GEF) is reported on SDO between the CSN falling edge and the first SCLK rising edge. GEF is set if a fault condition is detected or if the device comes from a Power On Reset (POR). It is therefore possible to have a quick device diagnostic without any SPI clock pulse (Figure 12-4).

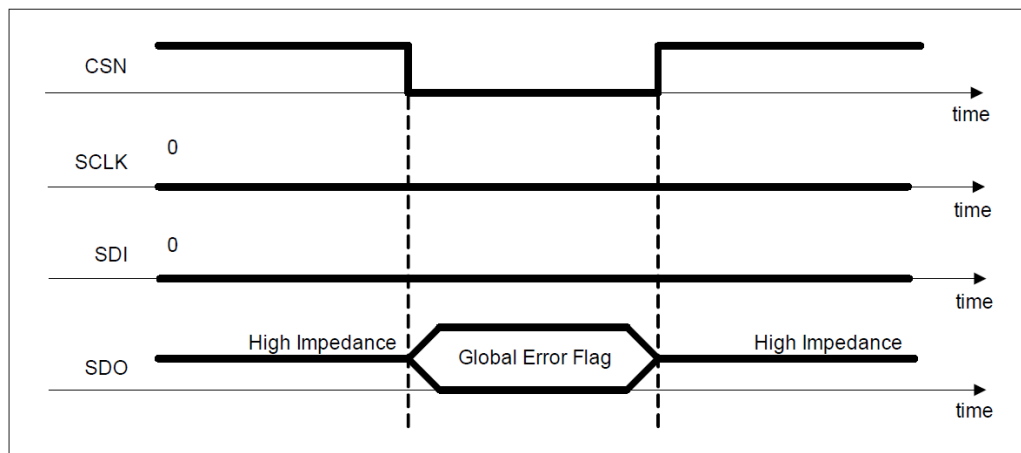


Figure 12-4 GEF - Diagnostic with 0-clock cycle

## 12.3 Global status byte

The SDO shifts out during the first eight SCLK cycles the Global Status Byte. This register provides an overview of the device status. The following error conditions are reported in this byte:

- Fail Safe (FS bit).
- Temperature error (TE bit): logical OR combination between Thermal Warning (**TW**) and Thermal shutdown (**TSD**).
- Negated Power ON Reset (NPOR bit, refer to **Chapter 10.3** for reset conditions).
- Supply Error (SUPE bit): logical OR combination between VS undervoltage shutdown (**VSUV**), VS overvoltage shutdown (**VSOV**) and charge pump undervoltage (**CPUV**).



- VDS monitoring Error (VDSE bit): logical OR combination between the bits of the **DSOV** register.
- Overcurrent (OC bit): logical OR combination between OC1 and OC2 status bits (**GENSTAT** register).
- SPI protocol Error (SPIE bit).

Note: The Global Error Flag is a logic OR combination of every bit of the Global Status Byte and of TDREGx:  $GEF = (FS) \text{ OR } (TE) \text{ OR } (NOT(NPOR)) \text{ OR } (SUPE) \text{ OR } (VDSE) \text{ OR } (OC) \text{ OR } (SPIE) \text{ OR } (NOT(TDREGx) \text{ AND } (PWMx\_EN = 1) \text{ AND } (NOT(MSKTDREG)))$ ,  $x = 1 \dots 3$ .

The following table shows how failures are reported in the Global Status Byte and the error Flag:

| Type of Error                   | Failure reported in the Global Status Byte                                                   | Global Error Flag                      |
|---------------------------------|----------------------------------------------------------------------------------------------|----------------------------------------|
| Fail safe                       | FS = 1                                                                                       | 1                                      |
| Thermal error                   | TE = 1                                                                                       | 1                                      |
| Power ON reset                  | NPOR = 0                                                                                     | 1                                      |
| Supply error                    | SUPE = 1                                                                                     | 1                                      |
| Drain source voltage monitoring | VDSE = 1                                                                                     | 1                                      |
| Overcurrent                     | OC = 1                                                                                       | 1                                      |
| SPI protocol error              | SPIE = 1                                                                                     | 1                                      |
| TDREGx, $x = 1 \dots 3$         | -                                                                                            | 1 if MSKTDREG = 0<br>0 if MSKTDREG = 1 |
| No error and no power ON reset  | SPIE = 0<br>OC = 0<br>VDSE = 0<br>SUPE = 0<br>NPOR = 1<br>TE = 0<br>FS = 0<br><br>TDREGx = 0 | 0                                      |

**Table 12-5 Failure reported in the global status byte and global error flag**

Note: The default value (after Power ON Reset) of NPOR is 0, therefore the default value of GEF is 1.

In fail safe mode, the control registers are frozen to their default value, with the exception of the WDTRIG bit. Any write access (except for WDTRIG bit) in fail safe mode will be discarded and the SPIE bit will set.

## 12.4 SPI error detection

The SPI incorporates an error flag in the Global Status Byte (SPIE) to supervise and preserve the data integrity.

If an SPI protocol error is detected during a given frame, the SPIE bit is set in the next SPI communication.

The SPIE bit is set in the following error conditions:

- The number of SCLK clock pulses received when CSN is Low is (protocol error):
  - not zero
  - or less than 24



- or more than 24 but not a multiple of 8
- The microcontroller sends an SPI command to an unused address (protocol error).
- A clock polarity error is detected: the incoming clock signal was High during CSN rising or falling edges (protocol error).
- No address byte or no last address byte are detected (protocol error).
- In daisy chain: the microcontroller does not send in sequence the first address byte until the last address byte (i.e. with gaps between two address bytes). In this case, the SDO signal is set to '0' during the remaining part of the SPI frame<sup>1</sup>), in order to prevent other devices from executing wrong commands (protocol error).
- A clear command to address 0x1F (Device ID register, Offset address = 0x1F).
- The same half-bridge is allocated to several activated PWM channels.
- Any write or clear command received in fail safe mode and not belonging to the exit sequence.

*Note: SPI commands to activate a half-bridge mapped to several PWM channels are ignored.*

In fail safe mode, the control registers may not be accessed, except for writing WDTRIG. An invalid write command in this mode sets the SPIE bit.

For a correct SPI communication:

- SCLK must be Low for a minimum  $t_{BEF}$  before CSN falling edge and  $t_{lead}$  after CSN falling edge.
- SCLK must be Low for a minimum  $t_{lag}$  before CSN rising edge and  $t_{BEH}$  after CSN rising edge.

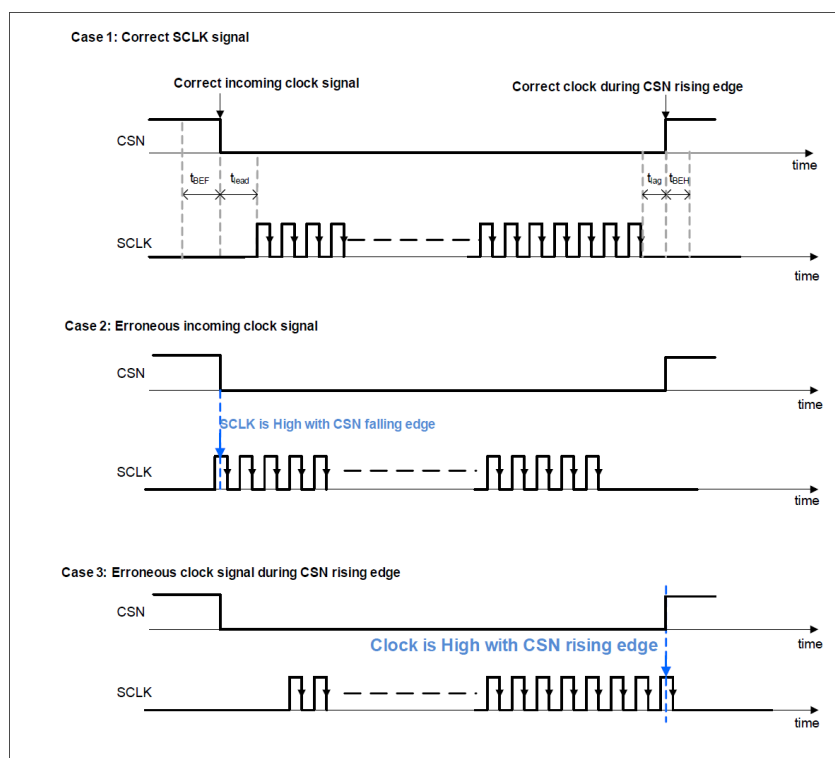


Figure 12-5 Clock polarity error



The reset condition of the SPIE bit depends on the cause of error:

- In normal mode:
  - The microcontroller must clear **HBVOUT\_PWMERR** if one half-bridge has been allocated to several PWM channels.
  - The microcontroller must send a correct SPI frame for the other errors reported by SPIE.
- If SPIE has been set in fail safe mode, the device must enter normal mode first.

## 12.5 Daisy chain

In daisy chain configuration the master output / slave input (noted MOSI) is connected to a slave SDI. The first slave SDO is connected to the next slave SDI in the chain. The SDO of the final in the chain is connected to the master input / slave output (noted MISO). In daisy chain configuration, the microcontroller MCSN is connected to all the slave CSN inputs (**Figure 13-6**).

To support daisy chain configurations, the SC77708 accepts SPI frames with more than 24 bits, provided that the number of bits is a multiple of 8, and the structure of the address byte is respected.

In daisy chain, the SC77708 works as follows:

1. The SC77708 operates as a 8-bit shift register until it receives the first address byte. This first received address byte is considered by the device as its own address byte.
2. The SC77708 copies directly SDI to SDO until the last address byte is detected.
3. The SC77708 shifts out the response high byte and low byte corresponding to the address byte.
4. After the last address byte, the SC77708 operates as a 16-bit shift register until the end of the SPI frame.

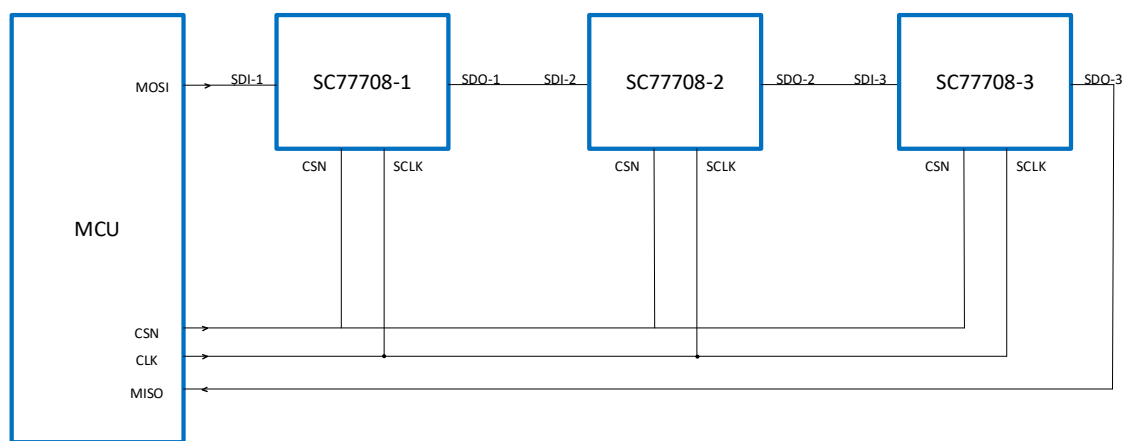


Figure 12-6 Daisy chain configuration with three SC77708 devices

In daisy chain configuration (**Figure 12-6**), the microcontroller must send the address and data bytes in the following order (**Figure 12-7**):

1. The address bytes altogether are sent first:
  - Address byte 1 (for SC77708-1) is sent first, followed by address byte 2 (for SC77708-2), followed by address byte 3 (for SC77708-3).
  - The LABT bit of the last address byte must be '1', while the LABT bit of all the other address bytes must be '0'.
2. The data bytes are sent altogether **in reverse order** once the address bytes are transmitted:
  - The data high byte for the SC77708-3 is sent first followed by the data low byte for the SC77708-3.



- Then the data high byte for the SC77708-2 is sent followed by the data low byte for the SC77708-2.
- Then the data high byte for the SC77708-1 is sent followed by the data low byte for the SC77708-1.

The Master Input / Slave Output (MISO), which is connected to SDO of the last device in the daisy chain receives:

1. A logic OR combination of all Global Error Flags (GEF) at the beginning of the SPI frame, between CSN falling edge and the first SCLK rising edge.
2. The Global Status Byte of each SC77708 in reverse order:
  - The Global Status Byte 3 (GSB3) corresponding to the SC77708-3 is received first, followed by GSB2 (corresponding to the SC77708-2), and finally the GSB1 (corresponding to the SC77708-1) is received.
3. The response of each SC77708 in reverse order:
  - The response high byte of the SC77708-3 is received first followed by the response low byte of the SC77708-3.
  - Then the response high byte of the SC77708-2 is received followed by the response low byte of the SC77708-2.
  - Then the response high byte of the SC77708-1 is received followed by the response low byte of the SC77708-1.

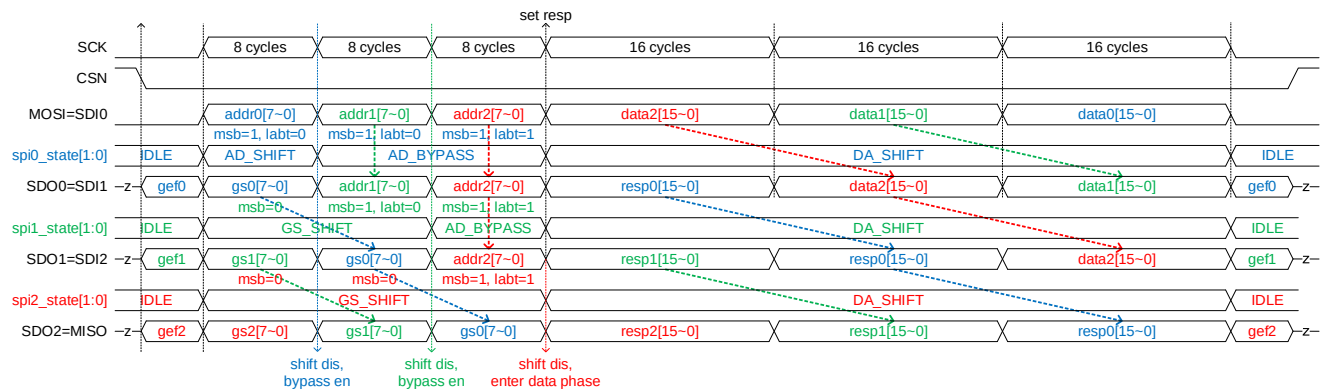


Figure 12-7 SPI Frame in daisy chain configuration with three SC77708 devices

## 12.6 Registers

### 12.6.1 Control registers

| Register Name | Register Description                       | Address                | Reset Value |
|---------------|--------------------------------------------|------------------------|-------------|
| GENCTRL1      | General control register 1                 | 0x00 &<br>REG_BANK = 0 | 0x0026      |
| GENCTRL2      | General control register 2                 | 0x01 &<br>REG_BANK = 0 | 0x4180      |
| HB_EN_CFG     | Half bridge control register               | 0x01 &<br>REG_BANK = 1 | 0x0000      |
| VDS1          | Drain-source overvoltage threshold HB1-4   | 0x02 &<br>REG_BANK = 0 | 0x0249      |
| PWM_HB        | Half bridge parallel mode with PWM setting | 0x02 &<br>REG_BANK = 1 | 0x0000      |



|                     |                                                                     |                        |        |
|---------------------|---------------------------------------------------------------------|------------------------|--------|
| VDS2                | Drain-source overvoltage threshold HB5-8                            | 0x03 &<br>REG_BANK = 0 | 0x0249 |
| HBDSOVMODE          | Drain-source overvoltage mode setting                               | 0x03 &<br>REG_BANK = 1 | 0x0000 |
| CCP_BLK1            | Cross current protection and blank times setting 1                  | 0x04 &<br>REG_BANK = 0 | 0x0000 |
| LIMP_HOME           | Half bridge state in limphone mode                                  | 0x04 &<br>REG_BANK = 1 | 0x0000 |
| CCP_BLK2_ACT        | Cross current protection and blank times setting for active MOSFETs | 0x05 &<br>REG_BANK = 0 | 0x4924 |
| CCP_BLK2_FW         | Cross current protection and blank times setting for fw MOSFETs     | 0x05 &<br>REG_BANK = 1 | 0x4924 |
| HBMODE              | Half-bridge mode                                                    | 0x06 &<br>REG_BANK = 0 | 0x0000 |
| VDSOV_IDCHG_DESCALE | Descal discharge current when Drain-source overvoltage occur        | 0x06 &<br>REG_BANK = 1 | 0x0000 |
| PWMSET              | Setting of PWM channels                                             | 0x07 &<br>REG_BANK = 0 | 0x6C60 |
| CHOPPING_TOFF1      | Chopping setting for CSA1                                           | 0x07 &<br>REG_BANK = 1 | 0x0000 |
| TPRECHG             | PWM precharge and predischage time                                  | 0x08 &<br>REG_BANK = 0 | 0x0000 |
| CHOPPING_TOFF2      | Chopping setting for CSA2                                           | 0x08 &<br>REG_BANK = 1 | 0x0000 |
| HBIDIAG             | Half-bridge diagnostic current control                              | 0x09 &<br>REG_BANK = 0 | 0xC000 |
| OC_SD_HB            | Half bridge state setting when overcurrent occur                    | 0x09 &<br>REG_BANK = 1 | 0xFFFF |
| ST_ICHG             | Charge current for static half bridges                              | 0x0A &<br>REG_BANK = 0 | 0x0044 |
| PWM_PCHG_INIT       | Precharge current initialization                                    | 0x0A &<br>REG_BANK = 1 | 0x18C6 |
| PWM_ICHG_ACT        | Charge current for half-bridges in PWM (active MOSFETs)             | 0x0B &<br>REG_BANK = 0 | 0x18C6 |
| PWM_ICHG_FW         | Charge current for half-bridges in PWM (fw MOSFETs)                 | 0x0B &<br>REG_BANK = 1 | 0x18C6 |



|                          |                                                                                                            |                          |        |
|--------------------------|------------------------------------------------------------------------------------------------------------|--------------------------|--------|
| PWM_IDCHG_ACT            | Discharge current of active MOSFETs in PWM operation                                                       | 0x0C &<br>REG_BANK = 0   | 0x1CE7 |
| PWM_PDCHG_INIT           | Predischarge current initialization                                                                        | 0x0C &<br>REG_BANK = 1   | 0x318C |
| PWM_ICHGMAX_CCP_BLK3_ACT | Max. pre-charge / predischage currents for half-bridges in PWM, tCCP and tBLANK setting for active MOSFETS | 0x0D &<br>REG_BANK = 0   | 0x4900 |
| PWM_ICHGMAX_CCP_BLK3_FW  | Max. pre-charge / predischage currents for half-bridges in PWM, tCCP and tBLANK setting for fw MOSFETS     | 0x0D &<br>REG_BANK = 1   | 0x4900 |
| TDON_OFF1                | Turn-on and turn-off delays for PWM channel 1                                                              | 0x0E &<br>REG_BANK = 0/1 | 0x0A0A |
| TDON_OFF2                | Turn-on and turn-off delays for PWM channel 2                                                              | 0x0F &<br>REG_BANK = 0/1 | 0x0A0A |
| TDON_OFF3                | Turn-on and turn-off delays for PWM channel 3                                                              | 0x10 &<br>REG_BANK = 0/1 | 0x0A0A |

Table 12-6 Control Register Overview

**12.6.1.1 GENCTRL1**

Address: 0x00 REG\_BANK=0 Reset Value: 0x0026

| Field | Bits  | Type | Description                                                                                                                            |
|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------|
| CSD2  | 15    | rw   | Direction of the current sense amplifier2<br>0b The current sense is unidirectional (default)<br>1b The current sense is bidirectional |
| CSAG2 | 14:13 | rw   | Gain of the current sense amplifier2<br>00b 10 V/V (default)<br>01b 20 V/V<br>10b 40 V/V<br>11b 80 V/V                                 |
| CSD1  | 12    | rw   | Direction of the current sense amplifier1<br>0b The current sense is unidirectional (default)<br>1b The current sense is bidirectional |
| CSAG1 | 11:10 | rw   | Gain of the current sense amplifier1<br>00b 10 V/V (default)<br>01b 20 V/V<br>10b 40 V/V<br>11b 80 V/V                                 |



|          |   |    |                                                                                                                                         |
|----------|---|----|-----------------------------------------------------------------------------------------------------------------------------------------|
| REG_BANK | 9 | rw | Register banking                                                                                                                        |
| VSOVTH   | 8 | rw | VS Overvoltage threshold<br>0b VSOV_OFF = VSOV_OFF1 (19 V, default)<br>1b VSOV_OFF = VSOV_OFF2 (29V)                                    |
| UNLOCK   | 7 | rw | Unlock bit to disable the watchdog<br>0b WDDIS cannot be reset (default)<br>1b WDDIS (GENCTRL2) can be reset in the following SPI frame |
| Reserved | 6 | r  | Reserved. Always read as 0                                                                                                              |
| FMODE    | 5 | rw | Frequency modulation<br>0b No modulation<br>1b Modulation frequency 15.6 kHz (default)                                                  |
| Reserved | 4 | r  | Reserved. Always read as 0                                                                                                              |
| IPCHGADT | 3 | rw | Adaptation of the pre-charge and pre-discharge current<br>0b 1 current step (default)<br>1b 2 current steps                             |
| OCEN     | 2 | rw | Overcurrent shutdown Enable<br>0b Disabled<br>1b Enabled (default)                                                                      |
| WDPER    | 1 | rw | Watchdog period<br>0b 50 ms<br>1b 200 ms (default)                                                                                      |
| WDTRIG   | 0 | rw | Watchdog trigger bit<br><br>This bit must be inverted within a watchdog period. After power on reset, the default value is 0.           |

Attention: Any write access to this register must invert the WDTRIG bit. Otherwise, the device enters fail safe mode.

#### 12.6.1.2 GENCTRL2

Address: 0x01 REG\_BANK=0 Reset Value: 0x4180

| Field    | Bits | Type | Description                                                                                                                         |
|----------|------|------|-------------------------------------------------------------------------------------------------------------------------------------|
| POCHGDIS | 15   | rw   | Postcharge disable bit<br>0b The postcharge phase is enabled during PWM (default)<br>1b The postcharge phase is disabled during PWM |
| BD_PASS  | 14   | rw   | Bridge driver passive mode                                                                                                          |



|          |       |    |                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----------|-------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |       |    | 0b Bridge driver is in active mode<br>1b Bridge driver is in passive mode (Default)                                                                                                                                                                                                                                                                                                                                   |
| AGCFILT  | 13    | rw | Filter for adaptive gate control<br>0b No filter applied (default)<br>1b Filter applied                                                                                                                                                                                                                                                                                                                               |
| AGC      | 12:11 | rw | Adaptive gate control<br>00b Adaptive gate control disabled, pre-charge and predischage disabled (default)<br>01b Adaptive gate control disabled, precharge is disabled, predischage is enabled with IPREDCHG = IPDCHGINIT (Refer to PWM_PCHG_INIT)<br>10b Adaptive gate control enabled, IPRECHG and IPREDCHG are self-adapted<br>11b Reserved. Adaptive gate control enabled, IPRECHG and IPREDCHG are self-adapted |
| IHOLD    | 10    | rw | Gate driver hold current IHOLD<br>0b Charge: $I_{CHG8}$ (12.5 mA typ.), discharge $I_{DCHG8}$ (14.2 mA typ.) (default)<br>1B Charge: $I_{CHG12}$ (23.9 mA typ.), discharge: $I_{DCHG12}$ (26.0 mA typ.)                                                                                                                                                                                                               |
| WDDIS    | 9     | rw | Watchdog disable bit<br>0b the watchdog is enabled (default)<br>1b the watchdog is disabled if the previous SPI frame has set UNLOCK bit (GENCTRL1)<br>Once the watchdog is disabled, it is directly re-enabled by resetting WDDIS                                                                                                                                                                                    |
| MSKTDREG | 8     | rw | Masking of the turn-on/off delay error in the Global Error Flag<br>0b Turn-on/off delay error is reported in the GEF<br>1b Turn-on/off delay error is masked in the GEF (default)                                                                                                                                                                                                                                     |
| CPUVTH   | 7     | rw | Charge pump undervoltage detection threshold<br>0b VCPUV (referred to VS) = 6.0V typ.<br>1b VCPUV (referred to VS)= 7.0 V typ. (default)                                                                                                                                                                                                                                                                              |
| CPSTGA   | 6     | rw | Automatic switch-over between dual and single charge pump stage<br>0b Automatic switch over deactivated (default)<br>1b Automatic switch over activated                                                                                                                                                                                                                                                               |
| TFVDS    | 5:4   | rw | Filter time of drain-source voltage monitoring<br>00b 0.5 $\mu$ s (default)<br>01b 1 $\mu$ s                                                                                                                                                                                                                                                                                                                          |



|       |     |    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|-----|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |     |    | 10b 2 $\mu$ s<br>11b 3 $\mu$ s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| OCTH2 | 3:2 | rw | Overcurrent detection threshold of CSO2 with CSD2 = 0<br>00b $V_{CSO2} > V_{DD}/2$ (default)<br>01b $V_{CSO2} > V_{DD}/2 + V_{DD}/10$<br>10b $V_{CSO2} > V_{DD}/2 + 2 \times V_{DD}/10$<br>11b $V_{CSO2} > V_{DD}/2 + 3 \times V_{DD}/10$<br>Overcurrent detection threshold of CSO2 with CSD2 = 1<br>00b $V_{CSO2} > V_{DD}/2 + 2 \times V_{DD}/20$ or $V_{CSO2} < V_{DD}/2 - 2 \times V_{DD}/20$ (default)<br>01b $V_{CSO2} > V_{DD}/2 + 4 \times V_{DD}/20$ or $V_{CSO2} < V_{DD}/2 - 4 \times V_{DD}/20$<br>10b $V_{CSO2} > V_{DD}/2 + 5 \times V_{DD}/20$ or $V_{CSO2} < V_{DD}/2 - 5 \times V_{DD}/20$<br>11b $V_{CSO2} > V_{DD}/2 + 6 \times V_{DD}/20$ or $V_{CSO2} < V_{DD}/2 - 6 \times V_{DD}/20$ |
| OCTH1 | 1:0 | rw | Overcurrent detection threshold of CSO1 with CSD1 = 0<br>00b $V_{CSO1} > V_{DD}/2$ (default)<br>01b $V_{CSO1} > V_{DD}/2 + V_{DD}/10$<br>10b $V_{CSO1} > V_{DD}/2 + 2 \times V_{DD}/10$<br>11b $V_{CSO1} > V_{DD}/2 + 3 \times V_{DD}/10$<br>Overcurrent detection threshold of CSO1 with CSD1 = 1<br>00b $V_{CSO1} > V_{DD}/2 + 2 \times V_{DD}/20$ or $V_{CSO1} < V_{DD}/2 - 2 \times V_{DD}/20$ (default)<br>01b $V_{CSO1} > V_{DD}/2 + 4 \times V_{DD}/20$ or $V_{CSO1} < V_{DD}/2 - 4 \times V_{DD}/20$<br>10b $V_{CSO1} > V_{DD}/2 + 5 \times V_{DD}/20$ or $V_{CSO1} < V_{DD}/2 - 5 \times V_{DD}/20$<br>11b $V_{CSO1} > V_{DD}/2 + 6 \times V_{DD}/20$ or $V_{CSO1} < V_{DD}/2 - 6 \times V_{DD}/20$ |

### 12.6.1.3 HB\_EN\_CFG

Address: 0x01 REG\_BANK=1 Reset Value: 0x0000

| Field          | Bits | Type | Description                                                                                                                                                                                                                  |
|----------------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EN_PASS_LS5678 | 15   | rw   | Enable LS5/6/7/8 in passive mode, remain value in passive mode:<br>0b: disable (default)<br>1b: enable                                                                                                                       |
| PASS_VS_OV     | 14   | rw   | Disable $V_S > V_{SOV PASS OFF}$ effect in passive mode when PASS_MOD[1:0] = 10b or 11b, but OV event happen, will pull down PWM3:<br>0b: enable (default)<br>1b: disable : PASS_MOD[1:0] = 10b equal to PASS_MOD[1:0] = 01b |



|               |     |    |                                                                                                                                                                                                                                                                                                                |
|---------------|-----|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved      | 13  | r  | Reserved. Always read as 0                                                                                                                                                                                                                                                                                     |
| DIS_DRV       | 12  | rw | Disable all half bridge driver:<br>0b enable (default)<br>1b disable                                                                                                                                                                                                                                           |
| DIS_FW3       | 11  | rw | Disable PWM3 freewheeling MOS switching<br>0b enable PWM3 FW MOSFET turn on (default)<br>1b disable PWM3 FW MOSFET turn on                                                                                                                                                                                     |
| DIS_FW2       | 10  | rw | Disable PWM2 freewheeling MOS switching<br>0b enable PWM2 FW MOSFET turn on (default)<br>1b disable PWM2 FW MOSFET turn on                                                                                                                                                                                     |
| DIS_FW1       | 9   | rw | Disable PWM1 freewheeling MOS switching<br>0b enable PWM1 FW MOSFET turn on (default)<br>1b disable PWM1 FW MOSFET turn on                                                                                                                                                                                     |
| Reserved      | 8:1 | r  | Reserved. Always read as 0                                                                                                                                                                                                                                                                                     |
| EN_PWM_HB_IND | 0   | rw | Enable PWM mapping to HB independently<br>0b: disable one PWM mapping to HBs, using PWMSET register for PWM mapping<br>1b: enable one PWM mapping to HBs, using PWM_HB register for PWM mapping, if PWM map to multiple HBs output, please set these HBs with the same HBDSOVMODE, and OC_SD_HB configurations |

**12.6.1.4 VDS1**

Address: 0x02 REG\_BANK=0 Reset Value: 0x0249

| Field | Bits | Type | Description                                                                                                                |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------|
| HB4D  | 15   | rw   | HS4 Drain-source monitoring<br>0b Drain-source monitoring: DH - VSH4 (default)<br>1b Drain-source monitoring: CSIN1 - VSH4 |
| HB3D  | 14   | rw   | HS3 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH3 (default)<br>1b Drain-source monitoring: CSIN1 – VSH3 |
| HB2D  | 13   | rw   | HS2 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH2 (default)<br>1b Drain-source monitoring: CSIN1 – VSH2 |



|          |      |    |                                                                                                                                                                          |
|----------|------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB1D     | 12   | rw | HS1 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH1 (default)<br>1b Drain-source monitoring: CSIN1 – VSH1                                               |
| HB4VDSTH | 11:9 | rw | HB4 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V |
| HB3VDSTH | 8:6  | rw | HB3 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V |
| HB2VDSTH | 5:3  | rw | HB2 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V |
| HB1VDSTH | 2:0  | rw | HB1 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V                                              |



|  |  |  |             |
|--|--|--|-------------|
|  |  |  | 101b 0.50 V |
|  |  |  | 110b 0.60 V |
|  |  |  | 111b 2.00 V |

**12.6.1.5 PWM\_HB**

Address: 0x02 REG\_BANK=1 Reset Value: 0x0000

| Field   | Bits  | Type | Description                                                                                                                                    |
|---------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------|
| PWM_HB8 | 15:14 | rw   | PWMx mapping to HB8 independently<br>00b disconnect (default)<br>01b HB8 mapping to PWM1<br>10b HB8 mapping to PWM2<br>11b HB8 mapping to PWM3 |
| PWM_HB7 | 13:12 | rw   | PWMx mapping to HB7 independently<br>00b disconnect (default)<br>01b HB7 mapping to PWM1<br>10b HB7 mapping to PWM2<br>11b HB7 mapping to PWM3 |
| PWM_HB6 | 11:10 | rw   | PWMx mapping to HB6 independently<br>00b disconnect (default)<br>01b HB6 mapping to PWM1<br>10b HB6 mapping to PWM2<br>11b HB6 mapping to PWM3 |
| PWM_HB5 | 9:8   | rw   | PWMx mapping to HB5 independently<br>00b disconnect (default)<br>01b HB5 mapping to PWM1<br>10b HB5 mapping to PWM2<br>11b HB5 mapping to PWM3 |
| PWM_HB4 | 7:6   | rw   | PWMx mapping to HB4 independently<br>00b disconnect (default)<br>01b HB4 mapping to PWM1<br>10b HB4 mapping to PWM2<br>11b HB4 mapping to PWM3 |
| PWM_HB3 | 5:4   | rw   | PWMx mapping to HB3 independently<br>00b disconnect (default)                                                                                  |



|         |     |    |                                                                                                                                                |
|---------|-----|----|------------------------------------------------------------------------------------------------------------------------------------------------|
|         |     |    | 01b HB3 mapping to PWM1<br>10b HB3 mapping to PWM2<br>11b HB3 mapping to PWM3                                                                  |
| PWM_HB2 | 3:2 | rw | PWMx mapping to HB2 independently<br>00b disconnect (default)<br>01b HB2 mapping to PWM1<br>10b HB2 mapping to PWM2<br>11b HB2 mapping to PWM3 |
| PWM_HB1 | 1:0 | rw | PWMx mapping to HB1 independently<br>00b disconnect (default)<br>01b HB1 mapping to PWM1<br>10b HB1 mapping to PWM2<br>11b HB1 mapping to PWM3 |

**12.6.1.6 VDS2**

Address: 0x03 REG\_BANK=0 Reset Value: 0x0249

| Field    | Bits | Type | Description                                                                                                                |
|----------|------|------|----------------------------------------------------------------------------------------------------------------------------|
| HB8D     | 15   | rw   | HS8 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH8 (default)<br>1b Drain-source monitoring: CSIN1 – VSH8 |
| HB7D     | 14   | rw   | HS7 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH7 (default)<br>1b Drain-source monitoring: CSIN1 – VSH7 |
| HB6D     | 13   | rw   | HS6 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH6 (default)<br>1b Drain-source monitoring: CSIN1 – VSH6 |
| HB5D     | 12   | rw   | HS5 Drain-source monitoring<br>0b Drain-source monitoring: DH – VSH5 (default)<br>1b Drain-source monitoring: CSIN1 – VSH5 |
| HB8VDSTH | 11:9 | rw   | HB8 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V               |



|          |     |    |                                                                                                                                                                          |
|----------|-----|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |     |    | 100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V                                                                                                                 |
| HB7VDSTH | 8:6 | rw | HB7 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V |
| HB6VDSTH | 5:3 | rw | HB6 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V |
| HB5VDSTH | 2:0 | rw | HB5 drain-source overvoltage threshold<br>000b 0.15 V<br>001b 0.20 V (default)<br>010b 0.25 V<br>011b 0.30 V<br>100b 0.40 V<br>101b 0.50 V<br>110b 0.60 V<br>111b 2.00 V |

**12.6.1.7 HBDSOVMODE**

Address: 0x03 REG\_BANK=1 Reset Value: 0x0000

| Field | Bits | Type | Description |
|-------|------|------|-------------|
|-------|------|------|-------------|



|          |       |    |                                                                                                                                                                  |
|----------|-------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB8DSOVM | 15:14 | rw | HB8 action when $V_{DSOV}$ occur :<br>00b turnoff HB8 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
| HB7DSOVM | 13:12 | rw | HB7 action when $V_{DSOV}$ occur :<br>00b turnoff HB7 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
| HB6DSOVM | 11:10 | rw | HB6 action when $V_{DSOV}$ occur :<br>00b turnoff HB6 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
| HB5DSOVM | 9:8   | rw | HB5 action when $V_{DSOV}$ occur :<br>00b turnoff HB5 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
| HB4DSOVM | 7:6   | rw | HB4 action when $V_{DSOV}$ occur :<br>00b turnoff HB4 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
| HB3DSOVM | 5:4   | rw | HB3 action when $V_{DSOV}$ occur :<br>00b turnoff HB3 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
| HB2DSOVM | 3:2   | rw | HB2 action when $V_{DSOV}$ occur :<br>00b turnoff HB2 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |



|          |     |    |                                                                                                                                                                  |
|----------|-----|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB1DSOVM | 1:0 | rw | HB1 action when $V_{DSOV}$ occur :<br>00b turnoff HB1 driver (default)<br>01b cycle by cycle retry<br>10b warning report only, DSOV, VDSE set 1<br>11b no action |
|----------|-----|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**12.6.1.8 CCP\_BLK1**

Address: 0x04 REG\_BANK=0 Reset Value: 0x0000

| Field     | Bits  | Type | Description                                                                                                                                                                                                                                                   |
|-----------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB8CCPBLK | 15:14 | rw   | Cross-current protection and blank times applied to HB8<br>00b (tHB8CCP, tHB8BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB8CCP, tHB8BLANK) = (tCCP2, tBLANK2)<br>10b (tHB8CCP, tHB8BLANK) = (tCCP3, tBLANK3)<br>11b (tHB8CCP, tHB8BLANK) = (tCCP4, tBLANK4) |
| HB7CCPBLK | 13:12 | rw   | Cross-current protection and blank times applied to HB7<br>00b (tHB7CCP, tHB7BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB7CCP, tHB7BLANK) = (tCCP2, tBLANK2)<br>10b (tHB7CCP, tHB7BLANK) = (tCCP3, tBLANK3)<br>11b (tHB7CCP, tHB7BLANK) = (tCCP4, tBLANK4) |
| HB6CCPBLK | 11:10 | rw   | Cross-current protection and blank times applied to HB6<br>00b (tHB6CCP, tHB6BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB6CCP, tHB6BLANK) = (tCCP2, tBLANK2)<br>10b (tHB6CCP, tHB6BLANK) = (tCCP3, tBLANK3)<br>11b (tHB6CCP, tHB6BLANK) = (tCCP4, tBLANK4) |
| HB5CCPBLK | 9:8   | rw   | Cross-current protection and blank times applied to HB5<br>00b (tHB5CCP, tHB5BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB5CCP, tHB5BLANK) = (tCCP2, tBLANK2)<br>10b (tHB5CCP, tHB5BLANK) = (tCCP3, tBLANK3)<br>11b (tHB5CCP, tHB5BLANK) = (tCCP4, tBLANK4) |
| HB4CCPBLK | 7:6   | rw   | Cross-current protection and blank times applied to HB4<br>00b (tHB4CCP, tHB4BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB4CCP, tHB4BLANK) = (tCCP2, tBLANK2)<br>10b (tHB4CCP, tHB4BLANK) = (tCCP3, tBLANK3)<br>11b (tHB4CCP, tHB4BLANK) = (tCCP4, tBLANK4) |



|           |     |    |                                                                                                                                                                                                                                                               |
|-----------|-----|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB3CCPBLK | 5:4 | rw | Cross-current protection and blank times applied to HB3<br>00b (tHB3CCP, tHB3BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB3CCP, tHB3BLANK) = (tCCP2, tBLANK2)<br>10b (tHB3CCP, tHB3BLANK) = (tCCP3, tBLANK3)<br>11b (tHB3CCP, tHB3BLANK) = (tCCP4, tBLANK4) |
| HB2CCPBLK | 3:2 | rw | Cross-current protection and blank times applied to HB2<br>00b (tHB2CCP, tHB2BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB2CCP, tHB2BLANK) = (tCCP2, tBLANK2)<br>10b (tHB2CCP, tHB2BLANK) = (tCCP3, tBLANK3)<br>11b (tHB2CCP, tHB2BLANK) = (tCCP4, tBLANK4) |
| HB1CCPBLK | 1:0 | rw | Cross-current protection and blank times applied to HB1<br>00b (tHB1CCP, tHB1BLANK) = (tCCP1, tBLANK1) (default)<br>01b (tHB1CCP, tHB1BLANK) = (tCCP2, tBLANK2)<br>10b (tHB1CCP, tHB1BLANK) = (tCCP3, tBLANK3)<br>11b (tHB1CCP, tHB1BLANK) = (tCCP4, tBLANK4) |

**12.6.1.9 LIMP\_HOME**

Address: 0x04 REG\_BANK=1 Reset Value: 0x0000

| Field    | Bits  | Type | Description                                                                                      |
|----------|-------|------|--------------------------------------------------------------------------------------------------|
| Reserved | 15:12 | r    | Reserved. Always read as 0                                                                       |
| LIMP_HB8 | 11    | rw   | Output of HB8 in limp home mode<br>0b turn off HB8 output (default)<br>1b keep static HB8 status |
| LIMP_HB7 | 10    | rw   | Output of HB7 in limp home mode<br>0b turn off HB7 output (default)<br>1b keep static HB7 status |
| LIMP_HB6 | 9     | rw   | Output of HB6 in limp home mode<br>0b turn off HB6 output (default)<br>1b keep static HB6 status |
| LIMP_HB5 | 8     | rw   | Output of HB5 in limp home mode<br>0b turn off HB5 output (default)<br>1b keep static HB5 status |
| LIMP_HB4 | 7     | rw   | Output of HB4 in limp home mode                                                                  |



|              |   |    |                                                                                                                                                       |
|--------------|---|----|-------------------------------------------------------------------------------------------------------------------------------------------------------|
|              |   |    | 0b turn off HB4 output (default)<br>1b keep static HB4 status                                                                                         |
| LIMP_HB3     | 6 | rw | Output of HB3 in limp home mode<br>0b turn off HB3 output (default)<br>1b keep static HB3 status                                                      |
| LIMP_HB2     | 5 | rw | Output of HB2 in limp home mode<br>0b turn off HB2 output (default)<br>1b keep static HB2 status                                                      |
| LIMP_HB1     | 4 | rw | Output of HB1 in limp home mode<br>0b turn off HB1 output (default)<br>1b keep static HB1 status                                                      |
| LIMP_PWM3    | 3 | rw | PWM3 mapping in limp home mode<br>0b disconnect PWM3 mapping to all HBs, HBs output depend on static setting (default)<br>1b keep PWM3 mapping to HBs |
| LIMP_PWM2    | 2 | rw | PWM2 mapping in limp home mode<br>0b disconnect PWM2 mapping to all HBs, HBs output depend on static setting (default)<br>1b keep PWM2 mapping to HBs |
| LIMP_PWM1    | 1 | rw | PWM1 mapping in limp home mode<br>0b disconnect PWM1 mapping to all HBs, HBs output depend on static setting (default)<br>1b keep PWM1 mapping to HBs |
| EN_LIMP_HOME | 0 | rw | Enable limp home mode<br>0b disable (default)<br>1b enable                                                                                            |

**12.6.1.10 CCP\_BLK2\_ACT**

Address: 0x05 REG\_BANK=0 Reset Value: 0x4924

| Field     | Bits  | Type | Description                                                                                   |
|-----------|-------|------|-----------------------------------------------------------------------------------------------|
| Reserved  | 15    | rw   | Reserved. Always read as 0                                                                    |
| TCCP3_ACT | 14:12 | rw   | Cross-current protection - tCCP3 Active<br>Refer to Table 11-3<br>Default: 100b: typ. 2000 ns |



|             |      |    |                                                                                               |
|-------------|------|----|-----------------------------------------------------------------------------------------------|
| TBLANK2_ACT | 11:9 | rw | Blank time - tBLANK2 Active<br>Refer to Table 11-4<br>Default: 100b: typ. 2000 ns             |
| TCCP2_ACT   | 8:6  | rw | Cross-current protection – tCCP2 Active<br>Refer to Table 11-3<br>Default: 100b: typ. 2000 ns |
| TBLANK1_ACT | 5:3  | rw | Blank time – tBLANK1 Active<br>Refer to Table 11-4<br>Default: 100b: typ. 2000 ns             |
| TCCP1_ACT   | 2:0  | rw | Cross-current protection – tCCP1 Active<br>Refer to Table 11-3<br>Default: 100b: typ. 2000 ns |

**12.6.1.11 CCP\_BLK2\_FW**

Address: 0x05 REG\_BANK=1 Reset Value: 0x4924

| Field      | Bits  | Type | Description                                                                                         |
|------------|-------|------|-----------------------------------------------------------------------------------------------------|
| Reserved   | 15    | rw   | Reserved. Always read as 0                                                                          |
| TCCP3_FW   | 14:12 | rw   | Cross-current protection - tCCP3 Freewheeling<br>Refer to Table 11-3<br>Default: 100b: typ. 2000 ns |
| TBLANK2_FW | 11:9  | rw   | Blank time - tBLANK2 Freewheeling<br>Refer to Table 11-4<br>Default: 100b: typ. 2000 ns             |
| TCCP2_FW   | 8:6   | rw   | Cross-current protection – tCCP2 Freewheeling<br>Refer to Table 11-3<br>Default: 100b: typ. 2000 ns |
| TBLANK1_FW | 5:3   | rw   | Blank time – tBLANK1 Freewheeling<br>Refer to Table 11-4<br>Default: 100b: typ. 2000 ns             |
| TCCP1_FW   | 2:0   | rw   | Cross-current protection – tCCP1 Freewheeling<br>Refer to Table 11-3<br>Default: 100b: typ. 2000 ns |

**12.6.1.12 HBMODE**

Address: 0x06 REG\_BANK=0 Reset Value: 0x0000

| Field   | Bits  | Type | Description                                                                                                                                                |
|---------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB8MODE | 15:14 | rw   | Half-bridge output 8 mode selection<br>00b HB8 is in high impedance (default)<br>01b LS8 is ON<br>10b HS8 is ON<br>11b Reserved - HB8 is in high impedance |
| HB7MODE | 13:12 | rw   | Half-bridge output 7 mode selection<br>00b HB7 is in high impedance (default)<br>01b LS7 is ON<br>10b HS7 is ON<br>11b Reserved – HB7 is in high impedance |
| HB6MODE | 11:10 | rw   | Half-bridge output 6 mode selection<br>00b HB6 is in high impedance (default)<br>01b LS6 is ON<br>10b HS6 is ON<br>11b Reserved – HB6 is in high impedance |
| HB5MODE | 9:8   | rw   | Half-bridge output 5 mode selection<br>00b HB5 is in high impedance (default)<br>01b LS5 is ON<br>10b HS5 is ON<br>11b Reserved – HB5 is in high impedance |
| HB4MODE | 7:6   | rw   | Half-bridge output 4 mode selection<br>00b HB4 is in high impedance (default)<br>01b LS4 is ON<br>10b HS4 is ON<br>11b Reserved – HB4 is in high impedance |
| HB3MODE | 5:4   | rw   | Half-bridge output 3 mode selection<br>00b HB3 is in high impedance (default)<br>01b LS3 is ON<br>10b HS3 is ON<br>11b Reserved – HB3 is in high impedance |
| HB2MODE | 3:2   | rw   | Half-bridge output 2 mode selection                                                                                                                        |



|         |     |    |                                                                                                                                                            |
|---------|-----|----|------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         |     |    | 00b HB2 is in high impedance (default)<br>01b LS2 is ON<br>10b HS2 is ON<br>11b Reserved – HB2 is in high impedance                                        |
| HB1MODE | 1:0 | rw | Half-bridge output 1 mode selection<br>00b HB1 is in high impedance (default)<br>01b LS1 is ON<br>10b HS1 is ON<br>11b Reserved – HB1 is in high impedance |

**12.6.1.13 VDSOV\_IDCHG\_DESCALE**

Address: 0x06 REG\_BANK=1 Reset Value: 0x0000

| Field       | Bits | Type | Description                                                                                                                                                                              |
|-------------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB8VDSTH_LS | 15   | rw   | Increase HB8 low side VDS protection threshold<br>0b HB8 low side VDS protection threshold same as high side (default)<br>1b HB8 low side VDS protection threshold higher than high side |
| HB7VDSTH_LS | 14   | rw   | Increase HB7 low side VDS protection threshold<br>0b HB7 low side VDS protection threshold same as high side (default)<br>1b HB7 low side VDS protection threshold higher than high side |
| HB6VDSTH_LS | 13   | rw   | Increase HB6 low side VDS protection threshold<br>0b HB6 low side VDS protection threshold same as high side (default)<br>1b HB6 low side VDS protection threshold higher than high side |
| HB5VDSTH_LS | 12   | rw   | Increase HB5 low side VDS protection threshold<br>0b HB5 low side VDS protection threshold same as high side (default)<br>1b HB5 low side VDS protection threshold higher than high side |
| HB4VDSTH_LS | 11   | rw   | Increase HB4 low side VDS protection threshold<br>0b HB4 low side VDS protection threshold same as high side (default)<br>1b HB4 low side VDS protection threshold higher than high side |
| HB3VDSTH_LS | 10   | rw   | Increase HB3 low side VDS protection threshold<br>0b HB3 low side VDS protection threshold same as high side (default)                                                                   |



|             |     |    |                                                                                                                                                                                                                                                                                                                                                 |
|-------------|-----|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|             |     |    | 1b HB3 low side VDS protection threshold higher than high side                                                                                                                                                                                                                                                                                  |
| HB2VDSTH_LS | 9   | rw | Increase HB2 low side VDS protection threshold<br>0b HB2 low side VDS protection threshold same as high side (default)<br>1b HB2 low side VDS protection threshold higher than high side                                                                                                                                                        |
| HB1VDSTH_LS | 8   | rw | Increase HB1 low side VDS protection threshold<br>0b HB1 low side VDS protection threshold same as high side (default)<br>1b HB1 low side VDS protection threshold higher than high side                                                                                                                                                        |
| Reserved    | 7:3 | r  | Reserved. Always read as 0                                                                                                                                                                                                                                                                                                                      |
| DESCALE     | 2:0 | rw | Descal discharge current when VDSOV happened, ST_IDCHG right shift DESCAL<br>000b ST_IDCHG right shift 0 bit (default)<br>001b ST_IDCHG right shift 1 bit<br>010b ST_IDCHG right shift 2 bit<br>011b ST_IDCHG right shift 3 bit<br>100b ST_IDCHG right shift 4 bit<br>101b ST_IDCHG right shift 5 bit<br>110b same as 101b<br>111b same as 101b |

**12.6.1.14 PWMSET**

Address: 0x07 REG\_BANK=0 Reset Value: 0x6c60

| Field    | Bits  | Type | Description                                                                                                                                                                                                                                                                                                         |
|----------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved | 15    | rw   | Reserved. Always read as 0                                                                                                                                                                                                                                                                                          |
| PASS_VDS | 14    | rw   | Drain-Source monitoring in bridge passive mode<br>0b DS monitoring in bridge passive mode disabled<br>1b DS monitoring in bridge passive mode enabled (Default)                                                                                                                                                     |
| PASS_MOD | 13:12 | rw   | Settings for bridge driver passive mode<br>00b LS1-4 are always off<br>01b LS1-4 are always on (static brake)<br>10b LS1-4 are activated if passive VS OV is detected (overvoltage brake) (Default)<br>11b LS1-4 are activated if passive VS OV is detected and PWM1 = High (overvoltage brake conditioned by PWM1) |



|         |      |    |                                                                                                                                           |
|---------|------|----|-------------------------------------------------------------------------------------------------------------------------------------------|
| PWM3_HB | 11:9 | rw | Allocation of the PWM channel 3<br>000b HB1<br>001b HB2<br>010b HB3<br>011b HB4<br>100b HB5<br>101b HB6<br>110b HB7 (default)<br>111b HB8 |
| PWM3_EN | 8    | rw | PWM channel 3 enable<br>0b PWM3 is disabled (default)<br>1b PWM3 is enabled                                                               |
| PWM2_HB | 7:5  | rw | Allocation of the PWM channel 2<br>000b HB1<br>001b HB2<br>010b HB3<br>011b HB4 (default)<br>100b HB5<br>101b HB6<br>110b HB7<br>111b HB8 |
| PWM2_EN | 8    | rw | PWM channel 2 enable<br>0b PWM2 is disabled (default)<br>1b PWM2 is enabled                                                               |
| PWM1_HB | 11:9 | rw | Allocation of the PWM channel 1<br>000b HB1 (default)<br>001b HB2<br>010b HB3<br>011b HB4<br>100b HB5<br>101b HB6<br>110b HB7<br>111b HB8 |
| PWM1_EN | 8    | rw | PWM channel 1 enable<br>0b PWM1 is disabled (default)                                                                                     |



|  |  |  |                    |
|--|--|--|--------------------|
|  |  |  | 1b PWM1 is enabled |
|--|--|--|--------------------|

**12.6.1.15 CHOPPING\_TOFF1**

Address: 0x07 REG\_BANK=1 Reset Value: 0x0000

| Field            | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------------------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved         | 15:14 | r    | Reserved. Always read as 0                                                                                                                                                                                                                                                                                                                                                                         |
| EN_CSO_CFG       | 13    | rw   | Enable CSO alternate function configuration<br>0b CSO1 pin output current sense amplifier1 output, CSO2 pin output current sense amplifier2 output (default)<br>1b enable CSO1/2 pin alternate function configuration                                                                                                                                                                              |
| CSO2_DRVOFF_NFLT | 12    | rw   | CSO2 pin alternate function configuration<br>0b input pin, input high to turn off driver (default)<br>1b open drain output pin, when SC77708 has fault, output low                                                                                                                                                                                                                                 |
| CSO1_CFG         | 11:10 | rw   | CSO1 pin alternate function configuration<br>00b current sense amplifier1 output (default)<br>01b current sense amplifier2 output<br>10b high impedance<br>11b reserved                                                                                                                                                                                                                            |
| CS1_TOFF         | 9:8   | rw   | Current sense amplifier1 constant $T_{off}$ time in chopping mode<br>00b 25us (default)<br>01b 50us<br>10b 100us<br>11b 200us                                                                                                                                                                                                                                                                      |
| EN_CHOP1         | 7     | rw   | Enable chopping mode on current sense amplifier1<br>0b disable chopping mode (default)<br>1b: enable chopping mode, when $I_{CSA1} \geq I_{chop1}$ , shutdown HB;<br>when $I_{CSA1} < I_{chop1}$ , retry HB after CS1_TOFF time elapsed                                                                                                                                                            |
| VREF_DAC1        | 6:0   | rw   | VREF_DAC1 is the DAC value of VREF, VREF is adjustable for chopping current, the compared result of VREF and CSO1 could shutdown HB output<br><br>if CSD1=0, $I_{chop1} = VREF\_DAC1 * 0.6V_{DD} / (127 * CSAG1 * R_{sense})$ , full 7 bits data is valid;<br><br>if CSD1=1, $I_{chop1} = VREF\_DAC1 * 0.3V_{DD} / (63 * CSAG1 * R_{sense})$ , low 6 bits data is valid.<br><br>0000000b (default) |

**12.6.1.16 TPRECHG**

Address: 0x08 REG\_BANK=0 Reset Value: 0x0000

| Field        | Bits  | Type | Description                                                                                                                |
|--------------|-------|------|----------------------------------------------------------------------------------------------------------------------------|
| Reserved     | 15    | rw   | Reserved. Always read as 0                                                                                                 |
| EN_DEEP_AD   | 14    | rw   | Deep adaptation enabled<br>0b Deep adaptation disabled (default)<br>1b Deep adaptation enabled. Refer to Chapter 10.3.3.6. |
| Reserved     | 13    | rw   | Reserved. Always read as 0                                                                                                 |
| EN_GEN_CHECK | 12    | rw   | Enable generator check<br>0b Detection of generator mode disabled (default)<br>1b Detection of generator mode enabled      |
| TPDCHG3      | 11:10 | rw   | Pre-discharge time of PWM channel 3<br>00b 125 ns (default)<br>01b 250 ns<br>10b 500 ns<br>11b 1000 ns                     |
| TPCHG3       | 9:8   | rw   | Pre-charge time of PWM channel 3<br>00b 125 ns (default)<br>01b 250 ns<br>10b 500 ns<br>11b 1000 ns                        |
| TPDCHG2      | 7:6   | rw   | Pre-discharge time of PWM channel 2<br>00b 125 ns (default)<br>01b 250 ns<br>10b 500 ns<br>11b 1000 ns                     |
| TPCHG2       | 5:4   | rw   | Pre-charge time of PWM channel 2<br>00b 125 ns (default)<br>01b 250 ns<br>10b 500 ns<br>11b 1000 ns                        |
| TPDCHG1      | 3:2   | rw   | Pre-discharge time of PWM channel 1<br>00b 125 ns (default)<br>01b 250 ns                                                  |



|        |     |    |                                                                                                     |
|--------|-----|----|-----------------------------------------------------------------------------------------------------|
|        |     |    | 10b 500 ns<br>11b 1000 ns                                                                           |
| TPCHG1 | 1:0 | rw | Pre-charge time of PWM channel 1<br>00b 125 ns (default)<br>01b 250 ns<br>10b 500 ns<br>11b 1000 ns |

**12.6.1.17 CHOPPING\_TOFF2**

Address: 0x08 REG\_BANK=1 Reset Value: 0x0000

| Field     | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved  | 15:10 | r    | Reserved. Always read as 0                                                                                                                                                                                                                                                                                                                                                                         |
| CS2_TOFF  | 9:8   | rw   | Current sense amplifier2 constant $T_{off}$ time in chopping mode<br>00b 25us (default)<br>01b 50us<br>10b 100us<br>11b 200us                                                                                                                                                                                                                                                                      |
| EN_CHOP2  | 7     | rw   | Enable chopping mode on current sense amplifier2<br>0b disable chopping mode (default)<br>1b: enable chopping mode, when $I_{CSA2} \geq I_{chop2}$ , shutdown HB;<br>when $I_{CSA2} < I_{chop2}$ , retry HB after CS2_TOFF time elapsed                                                                                                                                                            |
| VREF_DAC2 | 6:0   | rw   | VREF_DAC2 is the DAC value of VREF, VREF is adjustable for chopping current, the compared result of VREF and CSO2 could shutdown HB output<br><br>if CSD2=0, $I_{chop2} = VREF\_DAC2 * 0.6V_{DD} / (127 * CSAG2 * R_{sense})$ , full 7 bits data is valid;<br><br>if CSD1=2, $I_{chop2} = VREF\_DAC2 * 0.3V_{DD} / (63 * CSAG2 * R_{sense})$ , low 6 bits data is valid.<br><br>0000000b (default) |

**12.6.1.18 HBIDIAG**

Address: 0x09 REG\_BANK=0 Reset Value: 0xC000

| Field | Bits | Type | Description                                        |
|-------|------|------|----------------------------------------------------|
| CSA2L | 15   | rw   | Level of CSA2<br>0b CSA2 is configured as low-side |



|          |       |    |                                                                                                                          |
|----------|-------|----|--------------------------------------------------------------------------------------------------------------------------|
|          |       |    | 1b CSA2 is configured as high-side (default)                                                                             |
| CSA1L    | 14    | rw | Level of CSA1<br>0b CSA1 is configured as low-side<br>1b CSA1 is configured as high-side (default)                       |
| OC2FILT  | 13:12 | rw | Overcurrent filter time for CSO2<br>00b 6 $\mu$ s (default)<br>01b 10 $\mu$ s<br>10b 50 $\mu$ s<br>11b 100 $\mu$ s       |
| OC1FILT  | 11:10 | rw | Overcurrent filter time for CSO1<br>00b 6 $\mu$ s (default)<br>01b 10 $\mu$ s<br>10b 50 $\mu$ s<br>11b 100 $\mu$ s       |
| CSA2_OFF | 9     | rw | Disable of CSA2<br>0b CSA2 enabled(default)<br>1b CSA2 disabled                                                          |
| CSA1_OFF | 8     | rw | Disable of CSA1<br>0b CSA1 enabled(default)<br>1b CSA1 disabled                                                          |
| HB8IDIAG | 7     | rw | Control of HB8 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |
| HB7IDIAG | 6     | rw | Control of HB7 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |
| HB6IDIAG | 5     | rw | Control of HB6 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |
| HB5IDIAG | 4     | rw | Control of HB5 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |
| HB4IDIAG | 3     | rw | Control of HB4 off-state current source and current sink<br>0b Pull-down deactivated (default)                           |



|          |   |    |                                                                                                                          |
|----------|---|----|--------------------------------------------------------------------------------------------------------------------------|
|          |   |    | 1b Pull-down activated                                                                                                   |
| HB3IDIAG | 2 | rw | Control of HB3 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |
| HB2IDIAG | 1 | rw | Control of HB2 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |
| HB1IDIAG | 0 | rw | Control of HB1 off-state current source and current sink<br>0b Pull-down deactivated (default)<br>1b Pull-down activated |

**12.6.1.19 OC\_SD\_HB**

Address: 0x09 REG\_BANK=1 Reset Value: 0xFFFF

| Field      | Bits | Type | Description                                                                                  |
|------------|------|------|----------------------------------------------------------------------------------------------|
| CS2_SD_HB8 | 15   | rw   | HB8 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS2_SD_HB7 | 14   | rw   | HB7 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS2_SD_HB6 | 13   | rw   | HB6 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS2_SD_HB5 | 12   | rw   | HB5 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS2_SD_HB4 | 11   | rw   | HB4 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS2_SD_HB3 | 10   | rw   | HB3 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS2_SD_HB2 | 9    | rw   | HB2 action when current sense amplifier2 occur OC                                            |



|            |   |    |                                                                                              |
|------------|---|----|----------------------------------------------------------------------------------------------|
|            |   |    | 0b no action<br>1b: turn off (default).                                                      |
| CS2_SD_HB1 | 8 | rw | HB1 action when current sense amplifier2 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB8 | 7 | rw | HB8 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB7 | 6 | rw | HB7 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB6 | 5 | rw | HB6 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB5 | 4 | rw | HB5 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB4 | 3 | rw | HB4 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB3 | 2 | rw | HB3 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB2 | 1 | rw | HB2 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |
| CS1_SD_HB1 | 0 | rw | HB1 action when current sense amplifier1 occur OC<br>0b no action<br>1b: turn off (default). |

**12.6.1.20 ST\_I CHG**

Address: 0x0A REG\_BANK=0 Reset Value: 0x0044

| Field | Bits | Type | Description |
|-------|------|------|-------------|
|-------|------|------|-------------|



|           |    |    |                                                                                                                                                                                                                                   |
|-----------|----|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB8ICHGST | 15 | rw | <p>HB8 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 8 (default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 8.</p> |
| HB7ICHGST | 14 | rw | <p>HB7 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 7(default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 7.</p>  |
| HB6ICHGST | 13 | rw | <p>HB6 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 6 (default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 6.</p> |
| HB5ICHGST | 12 | rw | <p>HB5 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 5(default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 5.</p>  |
| HB4ICHGST | 11 | rw | <p>HB4 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 4 (default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 4.</p> |
| HB3ICHGST | 10 | rw | <p>HB3 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 3(default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 3.</p>  |
| HB2ICHGST | 9  | rw | <p>HB2 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 2 (default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 2.</p> |
| HB1ICHGST | 8  | rw | <p>HB1 Selection of charge and discharge currents</p> <p>0b The static charge/discharge current 1 is applied to the half bridge 1(default).</p> <p>1b The static charge/discharge current 2 is applied to the half bridge 1.</p>  |



|         |     |    |                                                                                                                                            |
|---------|-----|----|--------------------------------------------------------------------------------------------------------------------------------------------|
| ICHGST2 | 7:4 | rw | Static gate driver charge and discharge currents 2<br>Refer to Table 10-3<br>0100b - Charge 12.5 mA typ., discharge 14.2 mA typ (default). |
| ICHGST1 | 3:0 | rw | Static gate driver charge and discharge currents 1<br>Refer to Table 10-3<br>0100b - Charge 12.5 mA typ., discharge 14.2 mA typ (default). |

**12.6.1.21 PWM\_PCHG\_INIT**

Address: 0x0A REG\_BANK=1 Reset Value: 0x18C6

| Field     | Bits  | Type | Description                                                                                         |
|-----------|-------|------|-----------------------------------------------------------------------------------------------------|
| Reserved  | 15    | r    | Reserved. Always read as 0                                                                          |
| PCHGINIT3 | 14:10 | rw   | Initial precharge current of PWM Channel 3<br>Refer to Table 10-6<br>00110b: typ. 8.0 mA (default). |
| PCHGINIT2 | 9:5   | rw   | Initial precharge current of PWM Channel 2<br>Refer to Table 10-6<br>00110b: typ. 8.0 mA (default). |
| PCHGINIT1 | 4:0   | rw   | Initial precharge current of PWM Channel 1<br>Refer to Table 10-6<br>00110b: typ. 8.0 mA (default). |

**12.6.1.22 PWM\_ICHG\_ACT**

Address: 0x0B REG\_BANK=0 Reset Value: 0x18C6

| Field    | Bits  | Type | Description                                                                                                          |
|----------|-------|------|----------------------------------------------------------------------------------------------------------------------|
| Reserved | 15    | r    | Reserved. Always read as 0                                                                                           |
| ICHG3    | 14:10 | rw   | Gate driver charge current of PWM Channel 3 (Active MOSFET)<br>Refer to Table 10-6<br>00110b: typ. 8.0 mA (default). |
| ICHG2    | 9:5   | rw   | Gate driver charge current of PWM Channel 2 (Active MOSFET)<br>Refer to Table 10-6<br>00110b: typ. 8.0 mA (default). |
| ICHG1    | 4:0   | rw   | Gate driver charge current of PWM Channel 1 (Active MOSFET)                                                          |



|  |  |  |                                                       |
|--|--|--|-------------------------------------------------------|
|  |  |  | Refer to Table 10-6<br>00110b: typ. 8.0 mA (default). |
|--|--|--|-------------------------------------------------------|

**12.6.1.23 PWM\_ICHG\_FW**

Address: 0x0B REG\_BANK=1 Reset Value: 0x18C6

| Field    | Bits  | Type | Description                                                                                                                                                               |
|----------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved | 15    | r    | Reserved. Always read as 0                                                                                                                                                |
| ICHG3_FW | 14:10 | rw   | Gate driver charge and discharge current of PWM Channel 3 (FW MOSFET)<br>Refer to Table 10-6, Table 10-7<br>00110b. Typ. charge 8.0 mA, typ. discharge: 9.4 mA (default). |
| ICHG2_FW | 9:5   | rw   | Gate driver charge and discharge current of PWM Channel 2 (FW MOSFET)<br>Refer to Table 10-6, Table 10-7<br>00110b. Typ. charge 8.0 mA, typ. discharge: 9.4 mA (default). |
| ICHG1_FW | 4:0   | rw   | Gate driver charge and discharge current of PWM Channel 1 (FW MOSFET)<br>Refer to Table 10-6, Table 10-7<br>00110b. Typ. charge 8.0 mA, typ. discharge: 9.4 mA (default). |

**12.6.1.24 PWM\_IDCHG\_ACT**

Address: 0x0C REG\_BANK=0 Reset Value: 0x1CE7

| Field  | Bits  | Type | Description                                                                                                                                              |
|--------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| CCSO   | 15    | rw   | Capacitor connected to the current sense amplifier outputs<br>0b Capacitor connected to CSO < 100 pF (default)<br>1b Capacitor connected to CSO < 400 pF |
| IDCHG3 | 14:10 | rw   | Discharge current for PWM Channel 3 (Active MOSFET)<br>Refer to Table 10-7<br>00111b: typ. 11.8 mA (default).                                            |
| IDCHG2 | 9:5   | rw   | Discharge current for PWM Channel 2 (Active MOSFET)<br>Refer to Table 10-7<br>00111b: typ. 11.8 mA (default).                                            |
| IDCHG1 | 4:0   | rw   | Discharge current for PWM Channel 1 (Active MOSFET)                                                                                                      |



|  |  |  |                                                        |
|--|--|--|--------------------------------------------------------|
|  |  |  | Refer to Table 10-7<br>00111b: typ. 11.8 mA (default). |
|--|--|--|--------------------------------------------------------|

**12.6.1.25 PWM\_PDCHG\_INIT**

Address: 0x0C REG\_BANK=1 Reset Value: 0x318C

| Field      | Bits  | Type | Description                                                                                                                                              |
|------------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| CCSO       | 15    | rw   | Capacitor connected to the current sense amplifier outputs<br>0b Capacitor connected to CSO < 100 pF (default)<br>1b Capacitor connected to CSO < 400 pF |
| PDCHGINIT3 | 14:10 | rw   | Initial predischage current of PWM Channel 3<br>Refer to Table 10-7<br>01100b: typ. 26.0 mA (default).                                                   |
| PDCHGINIT2 | 9:5   | rw   | Initial predischage current of PWM Channel 2<br>Refer to Table 10-7<br>01100b: typ. 26.0 mA (default).                                                   |
| PDCHGINIT1 | 4:0   | rw   | Initial predischage current of PWM Channel 1<br>Refer to Table 10-7<br>01100b: typ. 26.0 mA (default).                                                   |

**12.6.1.26 PWM\_ICHGMAX\_CCP\_BLK3\_ACT**

Address: 0x0D REG\_BANK=0 Reset Value: 0x4900

| Field       | Bits  | Type | Description                                                                          |
|-------------|-------|------|--------------------------------------------------------------------------------------|
| Reserved    | 15    | r    | Reserved. Always read as 0                                                           |
| TBLANK4_ACT | 14:12 | rw   | Blank time - tBLANK4 Active<br>Refer to Table 11-4<br>100b: typ. 2000 ns (default).  |
| TCCP4_ACT   | 11:9  | rw   | Cross-current protection - tCCP4 Active<br>Refer to Table 11-3<br>100b: typ. 2000 ns |
| TBLANK3_ACT | 8:6   | rw   | Blank time – tBLANK3 Active<br>Refer to Table 11-4<br>100b: typ. 2000 ns (default).  |



|          |     |    |                                                                                                                                                                                                                                                                                                                                        |
|----------|-----|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ICHGMAX3 | 5:4 | rw | Maximum drive current of half-bridge mapped to PWM channel 3 during the pre-charge phase and pre-discharge phases2)<br>00b charge: typ. 18.8 mA, discharge: typ. 19.7 mA (default)<br>01b charge: typ. 41mA, discharge: typ. 43 mA<br>10b charge: typ. 77 mA, discharge: typ. 79 mA<br>11b charge: typ. 100 mA, discharge: typ. 100 mA |
| ICHGMAX2 | 3:2 | rw | Maximum drive current of half-bridge mapped to PWM channel 2 during the pre-charge phase and pre-discharge phases2)<br>00b charge: typ. 18.8 mA, discharge: typ. 19.7 mA (default)<br>01b charge: typ. 41mA, discharge: typ. 43 mA<br>10b charge: typ. 77 mA, discharge: typ. 79 mA<br>11b charge: typ. 100 mA, discharge: typ. 100 mA |
| ICHGMAX1 | 1:0 | rw | Maximum drive current of half-bridge mapped to PWM channel 1 during the pre-charge phase and pre-discharge phases2)<br>00b charge: typ. 18.8 mA, discharge: typ. 19.7 mA (default)<br>01b charge: typ. 41mA, discharge: typ. 43 mA<br>10b charge: typ. 77 mA, discharge: typ. 79 mA<br>11b charge: typ. 100 mA, discharge: typ. 100 mA |

**12.6.1.27 PWM\_ICHGMAX\_CCP\_BLK3\_FW**

Address: 0x0D REG\_BANK=1 Reset Value: 0x4900

| Field      | Bits  | Type | Description                                                                                                                                                                        |
|------------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved   | 15    | r    | Reserved. Always read as 0                                                                                                                                                         |
| TBLANK4_FW | 14:12 | rw   | Blank time - tBLANK4 Freewheeling<br>Refer to Table 11-4<br>100b: typ. 2000 ns (default).                                                                                          |
| TCCP4_FW   | 11:9  | rw   | Cross-current protection - tCCP4 Freewheeling<br>Refer to Table 11-3<br>100b: typ. 2000 ns                                                                                         |
| TBLANK3_FW | 8:6   | rw   | Blank time – tBLANK3 Freewheeling<br>Refer to Table 11-4<br>100b: typ. 2000 ns (default).                                                                                          |
| ICHGMAX3   | 5:4   | rw   | Maximum drive current of half-bridge mapped to PWM channel 3 during the pre-charge phase and pre-discharge phases2)<br>00b charge: typ. 18.8 mA, discharge: typ. 19.7 mA (default) |



|          |     |    |                                                                                                                                                                                                                                                                                                                                        |
|----------|-----|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          |     |    | 01b charge: typ. 41mA, discharge: typ. 43 mA<br>10b charge: typ. 77 mA, discharge: typ. 79 mA<br>11b charge: typ. 100 mA, discharge: typ. 100 mA                                                                                                                                                                                       |
| ICHGMAX2 | 3:2 | rw | Maximum drive current of half-bridge mapped to PWM channel 2 during the pre-charge phase and pre-discharge phases2)<br>00b charge: typ. 18.8 mA, discharge: typ. 19.7 mA (default)<br>01b charge: typ. 41mA, discharge: typ. 43 mA<br>10b charge: typ. 77 mA, discharge: typ. 79 mA<br>11b charge: typ. 100 mA, discharge: typ. 100 mA |
| ICHGMAX1 | 1:0 | rw | Maximum drive current of half-bridge mapped to PWM channel 1 during the pre-charge phase and pre-discharge phases2)<br>00b charge: typ. 18.8 mA, discharge: typ. 19.7 mA (default)<br>01b charge: typ. 41mA, discharge: typ. 43 mA<br>10b charge: typ. 77 mA, discharge: typ. 79 mA<br>11b charge: typ. 100 mA, discharge: typ. 100 mA |

**12.6.1.28 TDON\_OFF1**

Address: 0x0E REG\_BANK=0/1 Reset Value: 0x0A0A

| Field  | Bits | Type | Description                                                                                                                        |
|--------|------|------|------------------------------------------------------------------------------------------------------------------------------------|
| TDOFF1 | 15:8 | rw   | Turn-off delay time of PWM Channel 1.<br>Typical TDOFF1 = 62.5 x TDOFF1[7:0] <sub>D</sub> ns<br>0000 1010B: 625 ns typ. (default). |
| TDON1  | 15:8 | rw   | Turn-on delay time of PWM Channel 1.<br>Typical TDOFF1 = 62.5 x TDOFF1[7:0] <sub>D</sub> ns<br>0000 1010B: 625 ns typ. (default).  |

**12.6.1.29 TDON\_OFF2**

Address: 0x0F REG\_BANK=0/1 Reset Value: 0x0A0A

| Field  | Bits | Type | Description                                                                                                                        |
|--------|------|------|------------------------------------------------------------------------------------------------------------------------------------|
| TDOFF2 | 15:8 | rw   | Turn-off delay time of PWM Channel 2.<br>Typical TDOFF1 = 62.5 x TDOFF1[7:0] <sub>D</sub> ns<br>0000 1010B: 625 ns typ. (default). |
| TDON2  | 15:8 | rw   | Turn-on delay time of PWM Channel 2.<br>Typical TDOFF1 = 62.5 x TDOFF1[7:0] <sub>D</sub> ns                                        |



|  |  |  |                                    |
|--|--|--|------------------------------------|
|  |  |  | 0000 1010B: 625 ns typ. (default). |
|--|--|--|------------------------------------|

**12.6.1.30 TDON\_OFF3**

Address: 0x10 REG\_BANK=0/1 Reset Value: 0x0A0A

| Field  | Bits | Type | Description                                                                                                                        |
|--------|------|------|------------------------------------------------------------------------------------------------------------------------------------|
| TDOFF3 | 15:8 | rw   | Turn-off delay time of PWM Channel 3.<br>Typical TDOFF1 = 62.5 x TDOFF1[7:0] <sub>D</sub> ns<br>0000 1010B: 625 ns typ. (default). |
| TDON3  | 15:8 | rw   | Turn-on delay time of PWM Channel 3.<br>Typical TDOFF1 = 62.5 x TDOFF1[7:0] <sub>D</sub> ns<br>0000 1010B: 625 ns typ. (default).  |

**12.6.2 Status register**

| Register Name | Register Description                                           | Address | Reset Value |
|---------------|----------------------------------------------------------------|---------|-------------|
| GENSTAT       | General status register                                        | 0x11    | 0x0000      |
| DSOV          | Drain-source overvoltage                                       | 0x12    | 0x0000      |
| HBVOUT_PWMERR | Half-Bridge output voltage                                     | 0x13    | 0x0000      |
| EFF_TDON_OFF1 | Effective MOSFET turn-on and turn-off delays for PWM Channel 1 | 0x14    | 0x0000      |
| EFF_TDON_OFF2 | Effective MOSFET turn-on and turn-off delays for PWM Channel 2 | 0x15    | 0x0000      |
| EFF_TDON_OFF3 | Effective MOSFET turn-on and turn-off delays for PWM Channel 3 | 0x16    | 0x0000      |
| TRISE_FALL1   | Effective MOSFET rise and fall times for PWM Channel 1         | 0x17    | 0x0000      |
| TRISE_FALL2   | Effective MOSFET rise and fall times for PWM Channel 2         | 0x18    | 0x0000      |
| TRISE_FALL3   | Effective MOSFET rise and fall times for PWM Channel 3         | 0x19    | 0x0000      |
| LIMPSTAT      | Limphome mode state                                            | 0x1D    | 0x0000      |
| DEVID         | Device identifier                                              | 0x1F    | 0x0001      |

Table 12-7 Status Register Overview



## 12.6.2.1 GENSTAT

| Field      | Bits  | Type | Description                                                                                                                                                                                                                                            |
|------------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PASS_VDSOV | 15    | r    | DS overvoltage while the bridge driver is in passive mode<br>0b No overvoltage on drain-source of any low-sides (default)<br>1b Overvoltage on drain-source of one of the low-side is detected.                                                        |
| WDMON      | 14:13 | rw   | Watchdog Monitoring<br>00b WD Timer is between [0%;25%[ of the WD period (default)<br>01b WD Timer is between [25%;50%[ of the WD period<br>10b WD Timer is between [50%;75%[ of the WD period<br>11b WD Timer is between [75%;100 %[ of the WD period |
| PWM3STAT   | 12    | r    | Status of PWM3 input<br>0b PWM3 is low (default)<br>1b PWM3 is high                                                                                                                                                                                    |
| PWM2STAT   | 11    | r    | Status of PWM2 input<br>0b PWM2 is low (default)<br>1b PWM2 is high                                                                                                                                                                                    |
| PWM1STAT   | 10    | r    | Status of PWM1 input<br>0b PWM1 is low (default)<br>1b PWM1 is high                                                                                                                                                                                    |
| TDREG3     | 9     | rc   | PWM channel 3 - Regulation of turn-on and turn-off delays<br>0b the turn-on delay or the turn-off delay are not in regulation (default)<br>1b the turn-on and turn-off delays are in regulation                                                        |
| TDREG2     | 8     | rc   | PWM channel 2 - Regulation of turn-on and turn-off delays<br>0b the turn-on delay or the turn-off delay are not in regulation (default)<br>1b the turn-on and turn-off delays are in regulation                                                        |
| TDREG1     | 7     | rc   | PWM channel 1 - Regulation of turn-on and turn-off delays<br>0b the turn-on delay or the turn-off delay are not in regulation (default)<br>1b the turn-on and turn-off delays are in regulation                                                        |
| TSD        | 6     | rc   | Thermal Shutdown<br>0b No thermal shutdown is detected (default)<br>1b A thermal shutdown is detected                                                                                                                                                  |



|      |   |    |                                                                                                                   |
|------|---|----|-------------------------------------------------------------------------------------------------------------------|
| TW   | 5 | rc | Thermal Warning<br>0b No thermal warning is detected (default)<br>1b A thermal warning is detected                |
| OC2  | 4 | rc | Overcurrent detection of CSO2<br>0b No overcurrent detection on CSO2 (default)<br>1b Overcurrent detected on CSO2 |
| OC1  | 3 | rc | Overcurrent detection of CSO1<br>0b No overcurrent detection on CSO1 (default)<br>1b Overcurrent detected on CSO1 |
| VSOV | 2 | rc | VS Overvoltage<br>0b No overvoltage on VS detected (default)<br>1b Overvoltage on VS detected                     |
| VSUV | 1 | rc | VS Undervoltage<br>0b No undervoltage on VS detected (default)<br>1b undervoltage on VS detected                  |
| CPUV | 0 | rc | Charge Pump Undervoltage<br>0b No charge pump undervoltage (default)<br>1b A charge pump undervoltage is detected |

**12.6.2.2 DSOV**

| Field   | Bits | Type | Description                                                                                                                                                      |
|---------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LS8DSOV | 15   | rc   | Drain-Source overvoltage on low-side 8<br>0b No overvoltage on drain-source of low-side 8 (default)<br>1b Overvoltage on drain-source of low-side 8 detected.    |
| HS8DSOV | 14   | rc   | Drain-Source overvoltage on high-side 8<br>0b No overvoltage on drain-source of high-side 8 (default)<br>1b Overvoltage on drain-source of high-side 8 detected. |
| LS7DSOV | 13   | rc   | Drain-Source overvoltage on low-side 7<br>0b No overvoltage on drain-source of low-side 7 (default)<br>1b Overvoltage on drain-source of low-side 7 detected.    |
| HS7DSOV | 12   | rc   | Drain-Source overvoltage on high-side 7<br>0b No overvoltage on drain-source of high-side 7 (default)<br>1b Overvoltage on drain-source of high-side 7 detected. |



|         |    |    |                                                                                                                                                                  |
|---------|----|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LS6DSOV | 11 | rc | Drain-Source overvoltage on low-side 6<br>0b No overvoltage on drain-source of low-side 6 (default)<br>1b Overvoltage on drain-source of low-side 6 detected.    |
| HS6DSOV | 10 | rc | Drain-Source overvoltage on high-side 6<br>0b No overvoltage on drain-source of high-side 6 (default)<br>1b Overvoltage on drain-source of high-side 6 detected. |
| LS5DSOV | 9  | rc | Drain-Source overvoltage on low-side 5<br>0b No overvoltage on drain-source of low-side 5 (default)<br>1b Overvoltage on drain-source of low-side 5 detected.    |
| HS5DSOV | 8  | rc | Drain-Source overvoltage on high-side 5<br>0b No overvoltage on drain-source of high-side 5 (default)<br>1b Overvoltage on drain-source of high-side 5 detected. |
| LS4DSOV | 7  | rc | Drain-Source overvoltage on low-side 4<br>0b No overvoltage on drain-source of low-side 4 (default)<br>1b Overvoltage on drain-source of low-side 4 detected.    |
| HS4DSOV | 6  | rc | Drain-Source overvoltage on high-side 4<br>0b No overvoltage on drain-source of high-side 4 (default)<br>1b Overvoltage on drain-source of high-side 4 detected. |
| LS3DSOV | 5  | rc | Drain-Source overvoltage on low-side 3<br>0b No overvoltage on drain-source of low-side 3 (default)<br>1b Overvoltage on drain-source of low-side 3 detected.    |
| HS3DSOV | 4  | rc | Drain-Source overvoltage on high-side 3<br>0b No overvoltage on drain-source of high-side 3 (default)<br>1b Overvoltage on drain-source of high-side 3 detected. |
| LS2DSOV | 3  | rc | Drain-Source overvoltage on low-side 2<br>0b No overvoltage on drain-source of low-side 2 (default)<br>1b Overvoltage on drain-source of low-side 2 detected.    |
| HS2DSOV | 2  | rc | Drain-Source overvoltage on high-side 1<br>0b No overvoltage on drain-source of high-side 1 (default)<br>1b Overvoltage on drain-source of high-side 1 detected. |
| LS1DSOV | 1  | rc | Drain-Source overvoltage on low-side 0<br>0b No overvoltage on drain-source of low-side 0 (default)<br>1b Overvoltage on drain-source of low-side 0 detected.    |



|         |   |    |                                                                                                                                                                  |
|---------|---|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HS1DSOV | 0 | rc | Drain-Source overvoltage on high-side 0<br>0b No overvoltage on drain-source of high-side 0 (default)<br>1b Overvoltage on drain-source of high-side 0 detected. |
|---------|---|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## 12.6.2.3 HBVOUTPWMERR

| Field   | Bits | Type | Description                                                                                                                                                     |
|---------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HB8PWME | 15   | rc   | PWM Error on HB8<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB8                                                       |
| HB7PWME | 14   | rc   | PWM Error on HB7<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB7                                                       |
| HB6PWME | 13   | rc   | PWM Error on HB6<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB6                                                       |
| HB5PWME | 12   | rc   | PWM Error on HB5<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB5                                                       |
| HB4PWME | 11   | rc   | PWM Error on HB4<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB4                                                       |
| HB3PWME | 10   | rc   | PWM Error on HB3<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB3                                                       |
| HB2PWME | 9    | rc   | PWM Error on HB2<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB2                                                       |
| HB1PWME | 8    | rc   | PWM Error on HB1<br>0b No PWM error (default)<br>1b More than one activated PWM channels is mapped to HB1                                                       |
| HB8VOUT | 7    | rc   | Voltage level at SH8 when HB8MODE[1:0] = (0,0) or (1,1):<br>0b Low: $ VDH - VSH8  > V_{VDSMONTHX}$ if HB8D = 0<br>$ VCSIN1 - VSH8  > V_{VDSMONTHX}$ if HB8D = 1 |



|         |   |    |                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------|---|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         |   |    | <p>1b High: <math> VDH - VSH8  &lt; V_{VDSMONTHx}</math> if HB8D = 0;<br/> <math> VCSIN1 - VSH8  &lt; V_{VDSMONTHx}</math> if HB8D = 1</p> <p><i>Note: HB8VOUT = 0 if HB8MODE[1:0] = (0,1) or (1,0)</i></p>                                                                                                                                                                                                          |
| HB7VOUT | 6 | rc | <p>Voltage level at SH7 when HB7MODE[1:0] = (0,0) or (1,1):</p> <p>0b Low: <math> VDH - VSH7  &gt; V_{VDSMONTHx}</math> if HB7D = 0<br/> <math> VCSIN1 - VSH7  &gt; V_{VDSMONTHx}</math> if HB7D = 1</p> <p>1b High: <math> VDH - VSH7  &lt; V_{VDSMONTHx}</math> if HB7D = 0;<br/> <math> VCSIN1 - VSH7  &lt; V_{VDSMONTHx}</math> if HB7D = 1</p> <p><i>Note: HB7VOUT = 0 if HB7MODE[1:0] = (0,1) or (1,0)</i></p> |
| HB6VOUT | 5 | rc | <p>Voltage level at SH6 when HB6MODE[1:0] = (0,0) or (1,1):</p> <p>0b Low: <math> VDH - VSH6  &gt; V_{VDSMONTHx}</math> if HB6D = 0<br/> <math> VCSIN1 - VSH6  &gt; V_{VDSMONTHx}</math> if HB6D = 1</p> <p>1b High: <math> VDH - VSH6  &lt; V_{VDSMONTHx}</math> if HB6D = 0;<br/> <math> VCSIN1 - VSH6  &lt; V_{VDSMONTHx}</math> if HB6D = 1</p> <p><i>Note: HB6VOUT = 0 if HB6MODE[1:0] = (0,1) or (1,0)</i></p> |
| HB5VOUT | 4 | rc | <p>Voltage level at SH5 when HB5MODE[1:0] = (0,0) or (1,1):</p> <p>0b Low: <math> VDH - VSH5  &gt; V_{VDSMONTHx}</math> if HB5D = 0<br/> <math> VCSIN1 - VSH5  &gt; V_{VDSMONTHx}</math> if HB5D = 1</p> <p>1b High: <math> VDH - VSH5  &lt; V_{VDSMONTHx}</math> if HB5D = 0;<br/> <math> VCSIN1 - VSH5  &lt; V_{VDSMONTHx}</math> if HB5D = 1</p> <p><i>Note: HB5VOUT = 0 if HB5MODE[1:0] = (0,1) or (1,0)</i></p> |
| HB4VOUT | 3 | rc | <p>Voltage level at SH4 when HB4MODE[1:0] = (0,0) or (1,1):</p> <p>0b Low: <math> VDH - VSH4  &gt; V_{VDSMONTHx}</math> if HB4D = 0<br/> <math> VCSIN1 - VSH4  &gt; V_{VDSMONTHx}</math> if HB4D = 1</p> <p>1b High: <math> VDH - VSH4  &lt; V_{VDSMONTHx}</math> if HB4D = 0;<br/> <math> VCSIN1 - VSH4  &lt; V_{VDSMONTHx}</math> if HB4D = 1</p> <p><i>Note: HB4VOUT = 0 if HB4MODE[1:0] = (0,1) or (1,0)</i></p> |
| HB3VOUT | 2 | rc | <p>Voltage level at SH3 when HB3MODE[1:0] = (0,0) or (1,1):</p> <p>0b Low: <math> VDH - VSH3  &gt; V_{VDSMONTHx}</math> if HB3D = 0<br/> <math> VCSIN1 - VSH3  &gt; V_{VDSMONTHx}</math> if HB3D = 1</p> <p>1b High: <math> VDH - VSH3  &lt; V_{VDSMONTHx}</math> if HB3D = 0;</p>                                                                                                                                   |



|         |   |    |                                                                                                                                                                                                                                                                                                                                               |
|---------|---|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|         |   |    | $ VCSIN1 - VSH3  < V_{VDSMONTHx}$ if HB3D = 1<br><br><i>Note: HB3VOUT = 0 if HB3MODE[1:0] = (0,1) or (1,0)</i>                                                                                                                                                                                                                                |
| HB2VOUT | 1 | rc | Voltage level at SH2 when HB2MODE[1:0] = (0,0) or (1,1):<br><br>0b Low: $ VDH - VSH2  > V_{VDSMONTHx}$ if HB2D = 0<br>$ VCSIN1 - VSH2  > V_{VDSMONTHx}$ if HB2D = 1<br>1b High: $ VDH - VSH2  < V_{VDSMONTHx}$ if HB2D = 0;<br>$ VCSIN1 - VSH2  < V_{VDSMONTHx}$ if HB2D = 1<br><br><i>Note: HB2VOUT = 0 if HB2MODE[1:0] = (0,1) or (1,0)</i> |
| HB1VOUT | 0 | rc | Voltage level at SH1 when HB1MODE[1:0] = (0,0) or (1,1):<br><br>0b Low: $ VDH - VSH1  > V_{VDSMONTHx}$ if HB1D = 0<br>$ VCSIN1 - VSH1  > V_{VDSMONTHx}$ if HB1D = 1<br>1b High: $ VDH - VSH1  < V_{VDSMONTHx}$ if HB1D = 0;<br>$ VCSIN1 - VSH1  < V_{VDSMONTHx}$ if HB1D = 1<br><br><i>Note: HB1VOUT = 0 if HB1MODE[1:0] = (0,1) or (1,0)</i> |

## 12.6.2.4 EFF\_TDON\_OFF1

| Field     | Bits | Type | Description                                                                                                                      |
|-----------|------|------|----------------------------------------------------------------------------------------------------------------------------------|
| TDOFF1EFF | 15:8 | r    | Effective MOSFET turn-off delay of PWM Channel 1<br>Effective turn-off delay = $62.5 \times TDOFF1EFF[7:0]_D$ ns<br>0b (default) |
| TDON1EFF  | 7:0  | r    | Effective MOSFET turn-on delay of PWM Channel 1<br>Effective turn-on delay = $62.5 \times TDON1EFF[7:0]_D$ ns<br>Default: 0b     |

## 12.6.2.5 EFF\_TDON\_OFF2

| Field     | Bits | Type | Description                                                                                                                      |
|-----------|------|------|----------------------------------------------------------------------------------------------------------------------------------|
| TDOFF2EFF | 15:8 | r    | Effective MOSFET turn-off delay of PWM Channel 2<br>Effective turn-off delay = $62.5 \times TDOFF1EFF[7:0]_D$ ns<br>0b (default) |
| TDON2EFF  | 7:0  | r    | Effective MOSFET turn-on delay of PWM Channel 2                                                                                  |



|  |  |  |                                                                                           |
|--|--|--|-------------------------------------------------------------------------------------------|
|  |  |  | Effective turn-on delay = $62.5 \times \text{TDON1EFF}[7:0]_{\text{D}}$ ns<br>Default: 0b |
|--|--|--|-------------------------------------------------------------------------------------------|

**12.6.2.6 EFF\_TDON\_OFF3**

| Field     | Bits | Type | Description                                                                                                                                      |
|-----------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| TDOFF2EFF | 15:8 | r    | Effective MOSFET turn-off delay of PWM Channel 3<br>Effective turn-off delay = $62.5 \times \text{TDOFF1EFF}[7:0]_{\text{D}}$ ns<br>0b (default) |
| TDON2EFF  | 7:0  | r    | Effective MOSFET turn-on delay of PWM Channel 3<br>Effective turn-on delay = $62.5 \times \text{TDON1EFF}[7:0]_{\text{D}}$ ns<br>0b (default)    |

**12.6.2.7 TRISE\_FALL1**

| Field  | Bits | Type | Description                                                                                                            |
|--------|------|------|------------------------------------------------------------------------------------------------------------------------|
| TFALL1 | 15:8 | r    | MOSFET fall time of PWM Channel 1<br>MOSFET fall time = $62.5 \times \text{TFALL1}[7:0]_{\text{D}}$ ns<br>0b (default) |
| TRISE1 | 7:0  | r    | MOSFET rise time of PWM Channel 1<br>MOSFET rise time = $62.5 \times \text{TRISE}[7:0]_{\text{D}}$ ns<br>0b (default)  |

**12.6.2.8 TRISE\_FALL2**

| Field  | Bits | Type | Description                                                                                                            |
|--------|------|------|------------------------------------------------------------------------------------------------------------------------|
| TFALL2 | 15:8 | r    | MOSFET fall time of PWM Channel 2<br>MOSFET fall time = $62.5 \times \text{TFALL1}[7:0]_{\text{D}}$ ns<br>0b (default) |
| TRISE2 | 7:0  | r    | MOSFET rise time of PWM Channel 2<br>MOSFET rise time = $62.5 \times \text{TRISE}[7:0]_{\text{D}}$ ns<br>0b (default)  |

**12.6.2.9 TRISE\_FALL3**

| Field | Bits | Type | Description |
|-------|------|------|-------------|
|-------|------|------|-------------|



|        |      |   |                                                                                                            |
|--------|------|---|------------------------------------------------------------------------------------------------------------|
| TFALL3 | 15:8 | r | MOSFET fall time of PWM Channel 3<br>MOSFET fall time = 62.5 x TFALL1[7:0] <sub>D</sub> ns<br>0b (default) |
| TRISE3 | 7:0  | r | MOSFET rise time of PWM Channel 3<br>MOSFET rise time = 62.5 x TRISE[7:0] <sub>D</sub> ns<br>0b (default)  |

**12.6.2.10 LIMPSTAT**

| Field      | Bits | Type | Description                                                                             |
|------------|------|------|-----------------------------------------------------------------------------------------|
| Reserved   | 15:1 | r    | Reserved. Always read as 0                                                              |
| LIMP_STATE | 0    | r    | Limphone mode state<br>0b Not in limphone mode(default)<br>1b In limphone mode(default) |

**12.6.2.11 DEVID**

| Field      | Bits  | Type | Description                                                                                                                                                        |
|------------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved   | 15:11 | r    | Reserved. Always read as 0                                                                                                                                         |
| VERSION_ID | 10:8  | r    | SC77708 version<br>0 1p0<br>1 1p1                                                                                                                                  |
| Reserved   | 7:3   | r    | Reserved. Always read as 0                                                                                                                                         |
| DEV_ID     | 2:0   | r    | Device derivative identifier<br>000b SC77708<br>001b SC77704<br>010b Reserved<br>011b Reserved<br>100b Reserved<br>101b Reserved<br>110b Reserved<br>111b Reserved |



## 13 Application Information

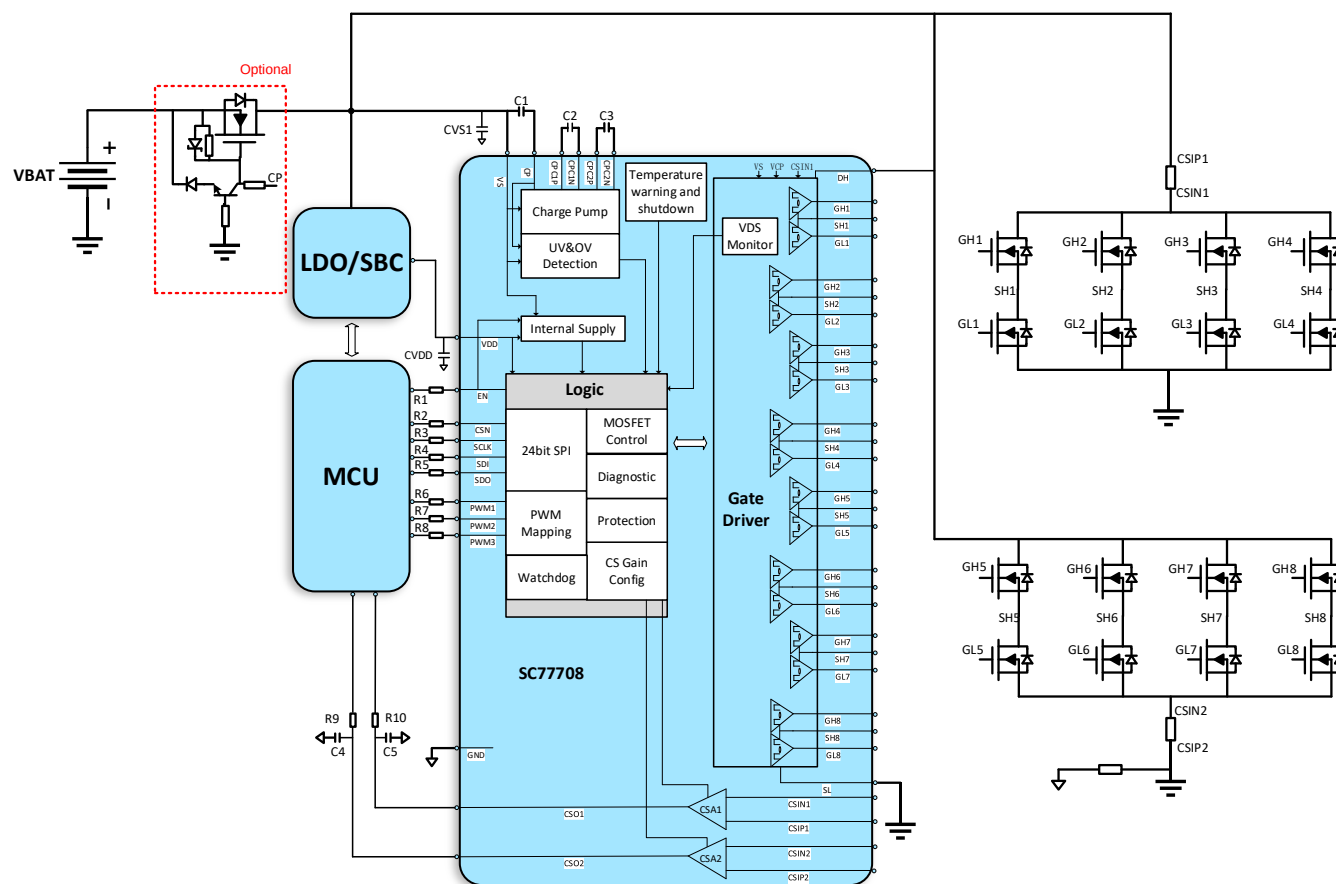


Figure 13-1 Application diagram SC77708

Note: This is a simplified example of an application circuit. The function must be verified in the real application.



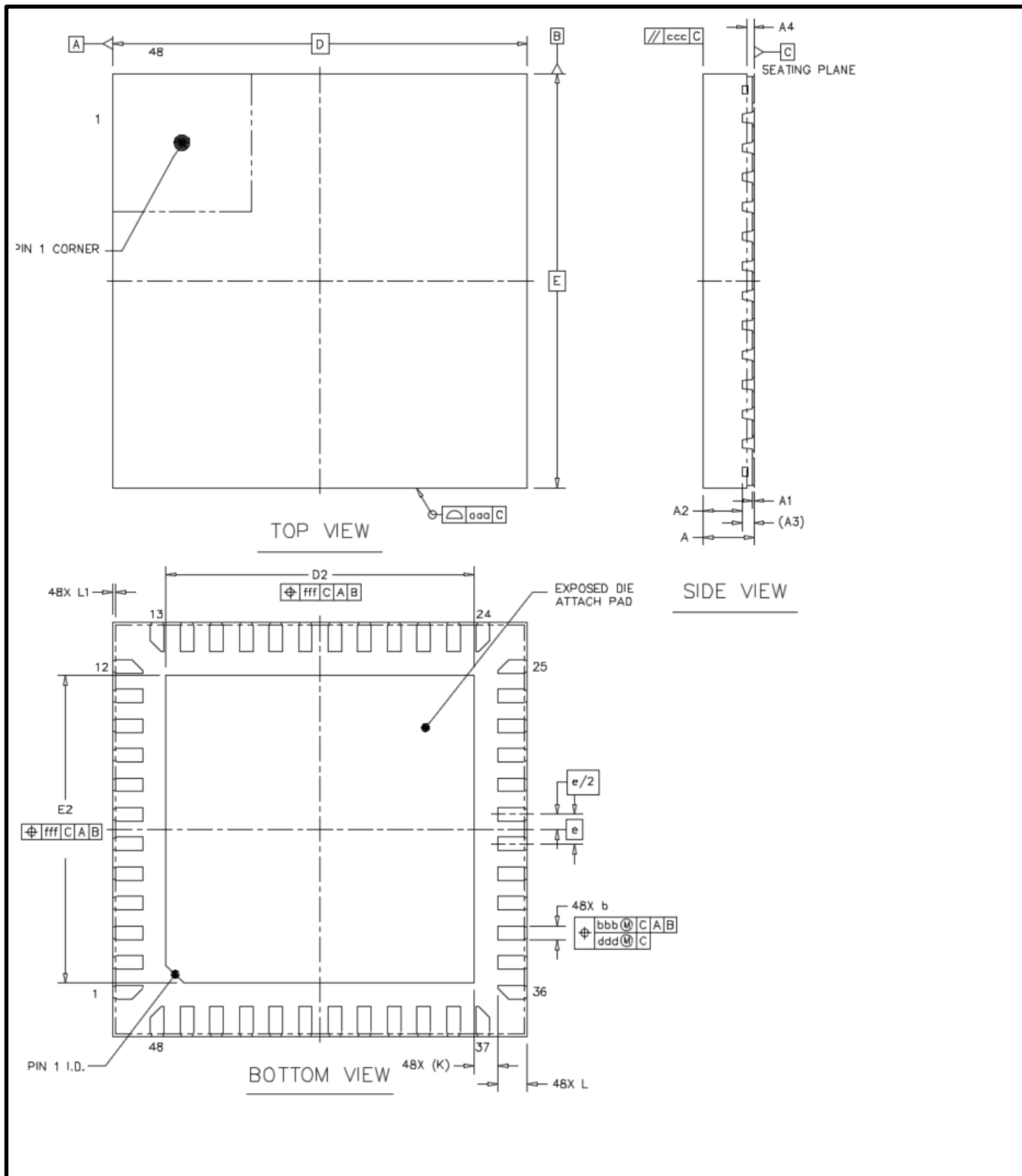
## **14 Layout Guide**

TBD



## MECHANICAL DATA

QFN48





|                              |   | SYMBOL | MIN       | NOM  | MAX  |
|------------------------------|---|--------|-----------|------|------|
| TOTAL THICKNESS              |   | A      | 0.8       | 0.85 | 0.9  |
| STAND OFF                    |   | A1     | 0         | 0.02 | 0.05 |
| MOLD THICKNESS               |   | A2     | ---       | 0.65 | ---  |
| L/F THICKNESS                |   | A3     | 0.203 REF |      |      |
| SIDE WETTABLE DEPTH          |   | A4     | 0.075     | ---  | 0.18 |
| LEAD WIDTH                   |   | b      | 0.18      | 0.23 | 0.28 |
| BODY SIZE                    | X | D      | 7 BSC     |      |      |
|                              | Y | E      | 7 BSC     |      |      |
| LEAD PITCH                   |   | e      | 0.5 BSC   |      |      |
| EP SIZE                      | X | D2     | 5.1       | 5.2  | 5.3  |
|                              | Y | E2     | 5.1       | 5.2  | 5.3  |
| LEAD LENGTH                  |   | L      | 0.4       | 0.5  | 0.6  |
| SIDE WETTABLE WIDTH          |   | L1     | 0.01      | ---  | 0.09 |
| LEAD TIP TO EXPOSED PAD EDGE |   | K      | 0.4 REF   |      |      |
| PACKAGE EDGE TOLERANCE       |   | aaa    | 0.1       |      |      |
| MOLD FLATNESS                |   | ccc    | 0.1       |      |      |
| LEAD OFFSET                  |   | bbb    | 0.1       |      |      |
|                              |   | ddd    | 0.05      |      |      |
| EXPOSED PAD OFFSET           |   | fff    | 0.1       |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |
|                              |   |        |           |      |      |



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**RECOMMENDED FOOTPRINT**

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## TAPE AND REEL INFORMATION

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