

SC77108AQ Single Channel 8-mΩ Smart High Side Driver with Advanced Protections and Diagnostics

1 Descriptions

The SC77108AQ is a fully-protected single channel smart high side driver qualified in automotive grade. Full diagnostics and high accuracy current sense enable intelligent control of the load even in harsh conditions. It integrates an 8mΩ MOSFET in a compact package size with advanced protections of overload protection, dynamic thermal swing shutdown, absolute thermal shutdown. Auto-restart or fault latch-off mode in over temperature events can be configured by an external /FaultRST pin. A multiplexed pin delivers proportional current sense and fault indications in both Normal Operation Mode and OFF-State diagnostics.

2 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C4B
- Single Channel 8mΩ Smart High-Side Switch with Full Diagnostics
 - 16-pins, Auto-restart or Fault Latch-off Mode, Channel Fault Diagnosis, Proportional Load Current.
- Operating Junction Temperature: -40 to 150°C
- Wide Operating Voltage from 4 to 28V with Load Dump Withstand Voltage up to 40V
- Ultra Low Standby Current < 500 nA
- Input Control, 3.3 V and 5 V Logic Compatible
- High Accuracy Current Sense:
 - ±4.5% @ 6A
 - ±5% @ 1A
 - ±13% @ 0.1A
 - ±20% @ 0.05A
 - ±50% @ 0.02A
- Electrical Transient Disturbance Immunity Certification of ISO7637-2 and ISO16750-2

- Advanced Protections:
 - Short to GND Protection by Internal Current Limit
 - Dynamic Thermal Swing Shutdown and Absolute Thermal Shutdown with Auto-restart
 - Configurable Fault Latch-off Mode for Both Thermal Swing Shutdown and Absolute Thermal Shutdown Events
 - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
 - Loss of GND and Loss of Battery Protection
 - Under Voltage Lockout (UVLO) Protection
- Diagnostics:
 - Overload and Short to Ground Detection in Normal Operation Mode
 - Open Load and Short to Battery Detection in OFF-State

3 Applications

- High Side Power Driver for Sub-module
- Power Switch for Automotive Lamp
- High Side Relays and Solenoids
- General Resistive, Inductive and Capacitive Loads

4 Device Information

ORDER NUMBER	DESCRIPTION	PACKAGE	BODY SIZE
SC77108AQSHER	<ul style="list-style-type: none"> Auto-restart or Fault Latch-off Mode Channel Fault Diagnosis Output Proportional Load Current Sense Output 	eSSOP-16	5.2mm x 3.9 mm x 1.4mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
1.0	2024.12.19		
1.0.1	2025.6.4	5~7	<p>8.5 Electrical Characteristics</p> <ul style="list-style-type: none"> (1) Add superscripts “ (1) ” to some parameters, including “I_{LIML}”, “$I_{OUT,REV}$”, “$I_{OUT,INV}$”, “T_{SD}”, “T_R”, “T_{SW}”, “T_{HYS}”, “I_{sense_sat}”. (2) Delete footnotes: <ul style="list-style-type: none"> 1. “The current includes... ” 2. “The accuracy of external... ” 3. “The external current limit ...” (3) Add new footnotes: “Parameter guaranteed by design ...” (4) “Turn-off Delay Time” Updated (Min./Typ.:30us/60us → Min./Typ.:20us/50us) (5) “Pulse Skew $t_{Pd_rise-tPd_fall}$” Updated (Min.: -50us → Min.: -65us)
1.0.2	2025.9.4	5~7	<p>8.5 Electrical Characteristics</p> <ul style="list-style-type: none"> (1) “Drain to source internal clamp voltage@-40℃” Updated (Min.:38V → Min.:36V) (2) “Drain to source internal clamp voltage@25~150℃” Updated (Min./Typ./Max.:42V/48V/52V → Min./Typ./Max.: 38V/43V/48V) (3) “Deglitch Time for Reset Fault” Updated (Min./Typ./Max.:3us/10us/20us → Min./Typ./Max.: 60us/80us/90us) (4) “Current SENSE Settling Time from SEN Falling Edge” Updated (Max.:15us → Max.: 20us) (5) “Turn-off Delay Time” Updated (Min./Typ.:30us/60us → Min./Typ.: 25us/50us) (6) “Pulse Skew $t_{Pd_rise-tPd_fall}$” Updated (Min.: -50us → Min.: -65us)
1.0.3	2026.03	2-22	Update the parameters name, function description in the datasheet

6 Typical Application Circuit

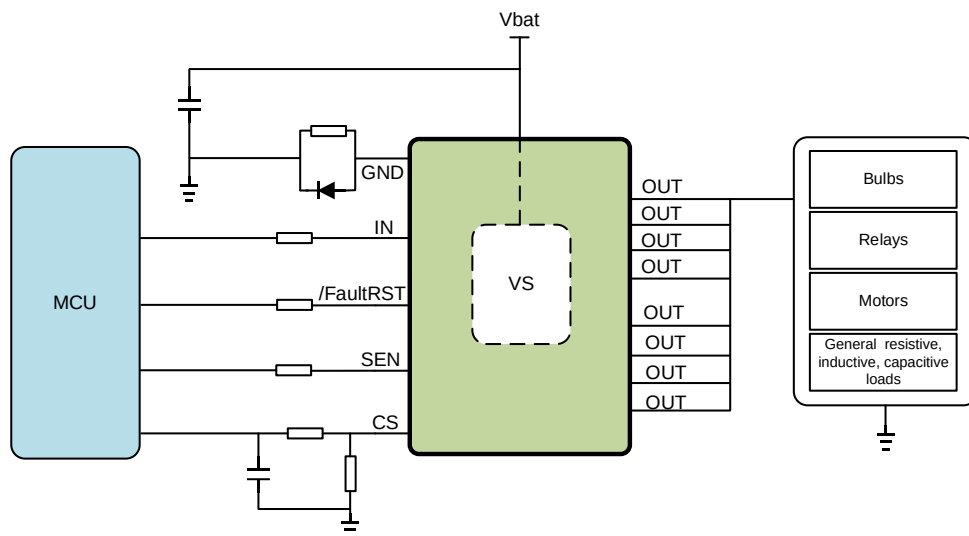
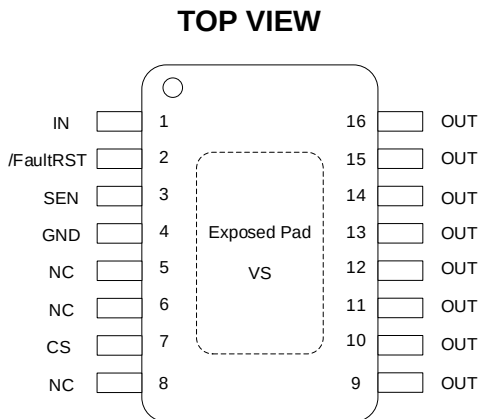


Figure 6-1. Typical Application Circuit

7 Terminal Configuration and Functions



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	IN	I	Input pin. Active high to turn on Channel.
2	/FaultRST	I	Latch fault if it's set high; clear fault or keep auto-restart if it's set low.
3	SEN	I	Diagnosis enable pin. Active high.
4	GND	-	Ground connection.
5	NC	-	Not connected.
6	NC	-	Not connected.
7	CS	O	Multiplexed sense output. It delivers proportional current sense and fault indications in both Normal Operation Mode and Standby Mode.
8	NC	-	Not connected.

9	OUT	O	Output of Channel.
10	OUT	O	Output of Channel.
11	OUT	O	Output of Channel.
12	OUT	O	Output of Channel.
13	OUT	O	Output of Channel.
14	OUT	O	Output of Channel.
15	OUT	O	Output of Channel.
16	OUT	O	Output of Channel.
Exposed Pad	VS	I	Power supply connection.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	UNIT
Voltage range at terminals ⁽²⁾	Supply Voltage ⁽³⁾	-0.3	40	V
	Reverse Polarity Voltage with External Blocking Diode ⁽⁴⁾	-18		V
	Supply Voltage for Short Circuit Protection		18	V
	Voltage on IN, SEN, /FaultRST Pins	-0.3	7	V
	Voltage on CS Pin	-2.7	7	V
Current range at terminals ⁽²⁾	DC Current on OUT Pins ⁽⁵⁾		Internally limited	A
	Current on GND Pin	-50 -250 ⁽⁵⁾	50	mA
	Current on IN, SEN, /FaultRST Pins	-20	20	mA
	Current on CS Pin	-25	30	mA
f _{IN,MAX}	PWM Frequency on IN Pin		2	kHz
E _{AS}	Inductive Load Switch-off Energy Dissipation, Single Pulse ⁽⁶⁾		45	mJ
T _A	Operating Ambient Temperature Range	-40	125	°C
T _J	Operating Junction Temperature Range	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Supply voltage to withstand load dump test for 400ms, according to ISO 16750-2:2010 load dump Test B.
- (4) Reverse polarity condition: t < 60 s, reverse current < I_{OUT,REV}, GND pin 4.7-kΩ resistor in parallel with diode.
- (5) For limited time range: t < 120s
- (6) Test condition: V_S = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-μm Cu, 2- × 35-μm Cu. 600-mm² thermal pad copper area.

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human Body Model (HBM) ESD Stress Voltage ⁽²⁾	All Pins	-4	4	kV
	Charged Device Model (CDM) ESD Stress Voltage ⁽³⁾	All Pins	-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per AEC-Q100-002. The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
- (3) Level listed above is the passing level per AEC-Q100-011.

8.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V _S	Voltage on VS pin	5		28	V
V _{IH}	Input Logic High on IN, SEN, /FaultRST Pins	2		5.5	V
V _{IL}	Input Logic Low on IN, SEN, /FaultRST Pins	0		0.8	V
I _{OUT,NOM}	Nominal DC load current		10		A
T _A	Operating ambient temperature	-40		125	°C
T _J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		eSSOP-16	UNIT
R _{ΘJA}	Junction to ambient thermal resistance ⁽²⁾	32.2	°C/W
R _{ΘJC(top)}	Junction to case(top) thermal resistance	21.9	°C/W
R _{ΘJC(bottom)}	Junction to case(bottom) thermal resistance	1.5	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	8.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	3.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	8.4	°C/W

- (1) Measured on JESD51-7, 4-layer PCB.
- (2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

8.5 Electrical Characteristics

-40°C < T_J < 150°C and 5V < V_S < 28V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{S,NOM}	Nominal Operating Voltage		5	13.5	28	V
V _{S,EXT}	Extended Operating Voltage	R _{on} and switching characteristics may increase compared to those in V _{S,NOM} , but protection functions are still operative.	4		5	V
V _{S,UVR}	Undervoltage Restart	Rising threshold to exit UVLO	3.5	3.7	4	V
V _{S,UVF}	Undervoltage Shutdown	Falling threshold to enter UVLO	3	3.2	3.5	V
V _{S,UVhys}	Undervoltage Shutdown Hysteresis			0.5		V
OPERATING CURRENT						
I _{S_ON}	Supply Current for No Load, No Diagnosis	V _s =13.5V, V _{IN} =5V, V _{FR} =V _{SEN} =0V; I _{OUT} = 0 A		1.8	3	mA
I _{GND_ON}	Iq in ON-state with All Channels Active	V _s =13.5V, V _{IN} =V _{SEN} =5V, V _{FR} =0V; I _{OUT} = 5A			3	mA
I _{S_STBY}	Supply Current in Standby Mode	V _s =13.5V; V _{IN} =V _{SEN} =V _{FR} =V _{OUT} =0V, T _J = 25°C			0.5	uA
		V _s =13.5V; V _{IN} = V _{SEN} =V _{FR} =V _{OUT} =0 V, T _J = 125°C			3	uA
I _{L,OFF}	Output Leakage Current in OFF-state	V _s =13.5V; V _{IN} =V _{SEN} =V _{FR} = V _{OUT} = 0 V; T _J = 25°C		0.01	0.5	uA
		V _s =13.5V; V _{IN} =V _{SEN} =V _{FR} = V _{OUT} = 0 V; T _J =125°C			3	uA
t _{D_STBY}	Blanking Time into Standby Mode	V _s =13.5V, V _{SEN} =5V to 0V, V _{IN} = V _{OUT} = V _{FR} = 0 V		12		ms
POWER STAGE						
R _{ON}	ON-state Resistance	V _s =13.5V, I _{OUT} = 5A, T _J = 25°C		8		mΩ
		V _s =13.5V, I _{OUT} = 5A, T _J = 150°C			17	mΩ
I _{LIMH}	Current Limit	V _s = 5~18 V	45	70	95	A
I _{LIML} ⁽¹⁾	Current Limit during Thermal Cycling	V _s = 13 V; T _R < T _J < T _{SD}		23		A
V _{DS,CLP}	Drain to source internal clamp voltage	I _{OUT} = 2 A, L=6mH, T _J = -40°C	36			V
		I _{OUT} = 2 A, L=6mH, T _J = 25~150°C	38	43	48	V
OUTPUT DIODE CHARACTERISTICS						
V _{OUT,F}	Drain to Source Diode Voltage	V _{IN} =0, I _{OUT} =-3A		0.7		V
I _{OUT,REV} ⁽¹⁾	Continuous Reverse Current when Reverse Polarity	t < 60 s, V _s = 13.5 V, GND pin 1kΩ resistor in parallel with diode. T _J = 25°C		5		A

$I_{OUT,INV}^{(1)}$	Continuous Inverse Current When $V_{OUT} > V_S + V_{diode}$	$t < 60\text{ s}$, $V_S = 13.5\text{ V}$, $T_J = 25^\circ\text{C}$	5	A
LOGIC INPUT (IN, SEN, /FaultRST)				
V_{IH}	Input Logic High		2	V
V_{IL}	Input Logic Low		0.8	V
$V_{L,HYS}$	Input Logic Hysteresis		150	mV
I_{IH}	High Level Pull-down Current	$V_{IH} = 2\text{V}$	10	μA
I_{IL}	Low Level Pull-down Current	$V_{IL} = 0.8\text{V}$	1 10	μA
DIAGNOSTICS				
$I_{loss,GND}$	Output Leakage Current when Loss of Ground		100	μA
$V_{OL,OFF}$	Open Load Detection Threshold in OFF-state ($V_{OUT}-GND$)	$V_{SEN}=5\text{V}$, $V_{IN}=0\text{V}$	2 3 4	V
$I_{OL,OFF}$	OFF-state Output Sink Current with Open Load	$V_S=13.5\text{ V}$, $V_{SEN}=5\text{V}$, $V_{IN}=0\text{ V}$, $V_{OUT}=4\text{V}$	-40	μA
$t_{D_OL_IN}$	OFF-state Diagnostic Delay Time from Falling Edge of Input	$V_S=V_{OUT}=13.5\text{V}$, $V_{SEN}=5\text{V}$, $V_{IN}=5\text{V}$ to 0V	260 500 700	μs
$t_{D_OL_VO}$	OFF-state Diagnostic Delay Time from Rising Edge of V_{OUT}	$V_S=13.5\text{V}$, $V_{SEN}=5\text{V}$, $V_{IN}=0\text{ V}$, $V_{OUT}=0\text{V}$ to 4V	150 220	μs
$t_{D_OL_SEN}$	OFF-state Diagnostic Delay Time from Rising Edge of SEN	$V_S=13.5\text{V}$, $V_{IN}=0\text{ V}$, $V_{OUT}=4\text{V}$, $V_{SEN}=0\text{V}$ to 5V	150 220	μs
$T_{SD}^{(1)}$	Thermal Shutdown Temperature		170	$^\circ\text{C}$
$T_R^{(1)}$	Thermal Shutdown Flag Reset Temperature		140	$^\circ\text{C}$
$T_{SW}^{(1)}$	Thermal Swing Shutdown Threshold	$T_J = -40\text{ }^\circ\text{C}$, $V_S=13.5\text{V}$	45	$^\circ\text{C}$
$T_{HYS}^{(1)}$	Hysteresis for Resetting the Thermal Shutdown and Swing		20	$^\circ\text{C}$
t_{LATCH_RST}	Deglitch Time for Reset Fault	$V_{SEN}=5\text{V}$, $V_{IN}=5\text{V}$, Latched fault triggered, then $V_{FR}=5\text{V}$ to 0V	60 80 90	μs
Multiple SENSE Functions				
K_{SNS}	Ratio of Current Sense		6000	
dK_{SNS}/K_{SNS}	Accuracy of Current Sense ($I_{CS} \times K_{SNS} - I_{OUT}$) / $I_{OUT} \times 100$	$I_{OUT} = 0.02\text{A}$	-50 50	%
		$I_{OUT} = 0.05\text{A}$	-20 20	
		$I_{OUT} = 0.1\text{A}$	-13 13	
		$I_{OUT} = 1\text{A}$	-5 5	
		$I_{OUT} = 6\text{A}$	-4.5 4.5	
V_{SENSE_SAT}	SENSE Saturation Voltage	$V_S=7\text{V}$; $R_{SENSE}=2.5\text{k}\Omega$; $V_{SEN}=V_{IN}=5\text{V}$;	4.8	V
I_{SENSE_SAT}	SENSE Saturation Current	$V_S=7\text{V}$; $V_{SENSE} = 4\text{V}$; $V_{IN}=V_{SEN} = 5\text{V}$;	4	mA
$V_{CS,H}$	Fault High Voltage of SENSE	$V_S \geq 7\text{V}$	5 5.5 6	V

		5V≤V _S <7V	4.3	6	V	
I _{CS,H}	Fault Current of SENSE	V _S ≥ 7V, V _{SENSE} = 4.3V	10		mA	
I _{SNS,LEAK1}	Leakage Current of SENSE in Diagnostic Disable State	V _{SEN} =0V, V _{IN} =5V, I _{OUT} =5A, V _{SENSE} =0V, T _J =125°C		0.5	uA	
I _{SNS,LEAK2}	Leakage Current of SENSE in Diagnostic Enable State	V _{SEN} =V _{IN} =5V, I _{OUT} =0A, V _{SENSE} =0V, T _J =125°C		2	uA	
t _{SNS,ON1}	Current SENSE Settling Time from SEN Rising Edge	V _{IN} = 5 V, I _{OUT} ≥ 1A. V _{SEN} from 0 to 5 V. V _{SENSE} to 90% of sense value, R _{SENSE} = 1kΩ		30	us	
t _{SNS,OFF1}	Current SENSE Settling Time from SEN Falling Edge	V _{IN} = 5 V, I _{OUT} ≥ 1A. V _{SEN} from 5 to 0 V. V _{SENSE} to 10% of sense value, R _{SENSE} = 1kΩ		20	us	
t _{SNS,ON2}	Current SENSE Settling Time from IN Current Rising Edge	V _{SEN} =5V, I _{OUT} ≥ 1A. V _{IN} from 0 to 5 V. V _{SENSE} to 90% of sense value, R _{SENSE} = 1kΩ		150	us	
t _{SNS,OFF2}	Current SENSE Settling Time from IN Falling Edge	V _{SEN} = 5 V, I _{OUT} ≥ 1A. V _{IN} from 5 to 0 V. V _{SENSE} to 10% of sense value, R _{SENSE} = 1kΩ		10	us	
Switching Characteristics						
t _{D,ON}	Turn-on Delay Time	V _{IN} rising edge to V _{OUT} =20%*V _s , V _s =13.5V, R _L =2.6Ω, T _J = 25°C	30	55	100	us
t _{D,OFF}	Turn-off Delay Time	V _{IN} falling edge to V _{OUT} =80%*V _s , V _s =13.5V, R _L =2.6Ω, T _J = 25°C	25	50	120	us
dV/dt _{ON}	Turn-on Slew Rate	V _{OUT} from 20% to 80%, T _J = 25°C	0.3	0.45	0.6	V/us
dV/dt _{OFF}	Turn-off Slew Rate	V _{OUT} from 80% to 20%, T _J = 25°C	0.3	0.5	0.75	V/us
t _{skew}	Pulse Skew t _{Pd_rise} -t _{Pd_fall}	V _s =13.5V, R _L =2.6Ω, T _J = 25°C t _{Pd_rise} : V _{IN} rising edge to V _{OUT} = 80%*V _s t _{Pd_fall} : V _{IN} falling edge to V _{OUT} = 20%*V _s	-65		65	us

(1) Parameter guaranteed by design and characterization; not subject to production test.

8.6 Typical Characteristics

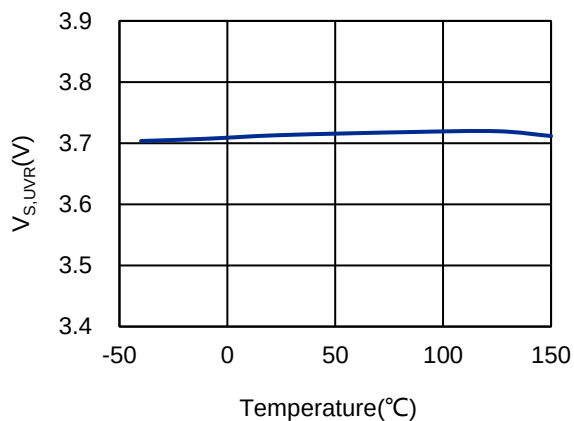


Figure 8-1. V_{S,UVR} vs T_A

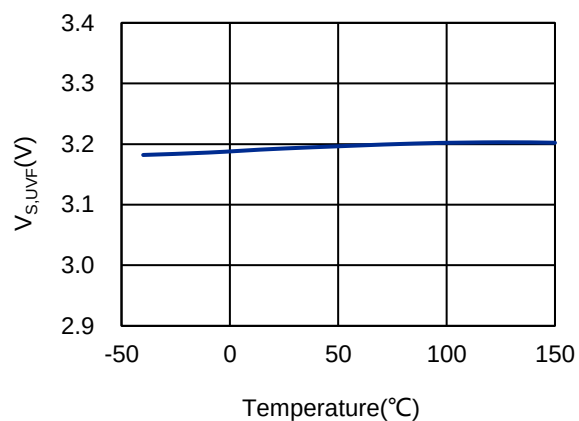


Figure 8-2. V_{S,UVF} vs T_A

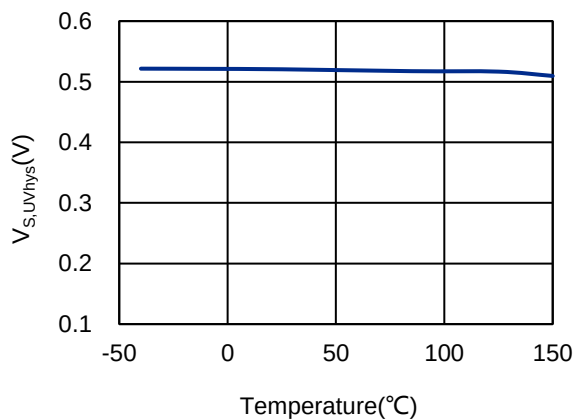


Figure 8-3. V_{S,UVhys} vs T_A

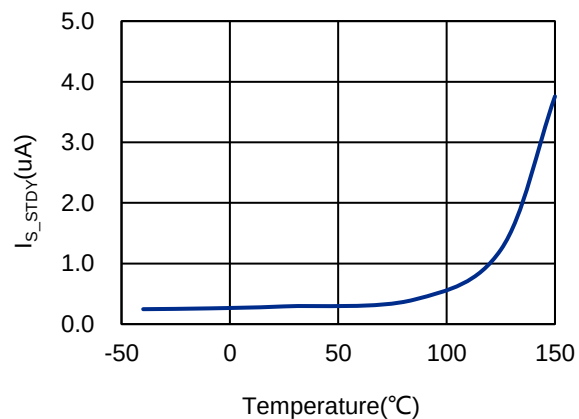


Figure 8-4. I_{S,STBY} vs T_A

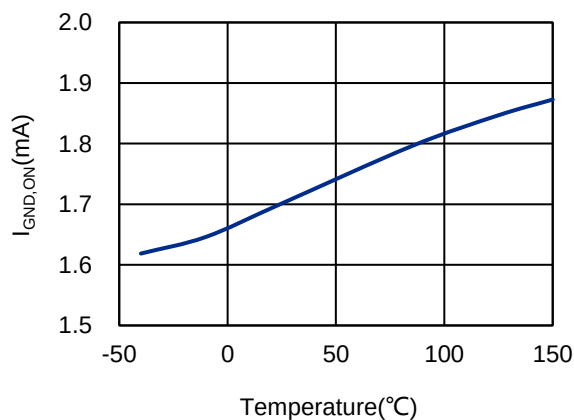


Figure 8-5. I_{GND,ON} vs T_A

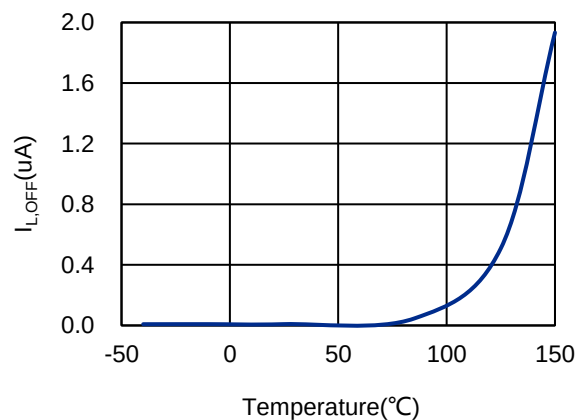


Figure 8-6. I_{L,OFF} vs T_A

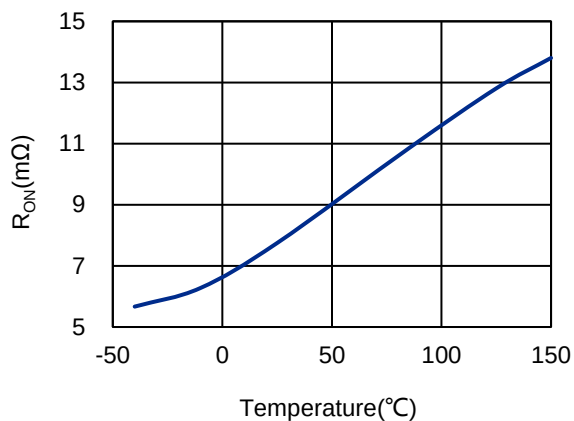


Figure 8-7. R_{ON} vs T_A

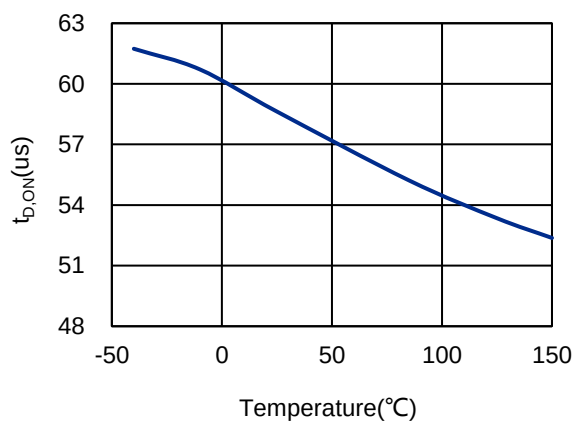


Figure 8-8. t_{D,ON} vs T_A

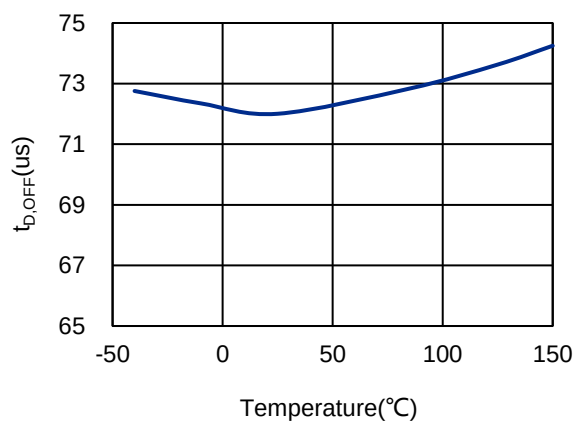


Figure 8-9. t_{D,OFF} vs T_A

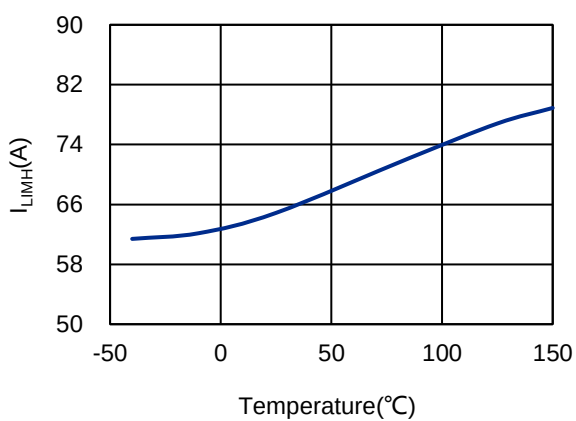


Figure 8-10. I_{LIMH} vs T_A

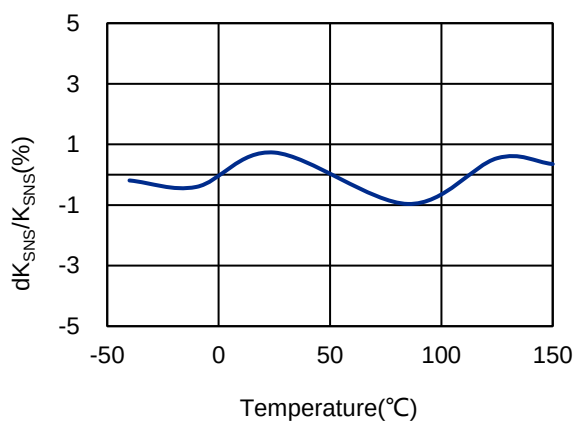


Figure 8-11. dK_{SNS} / K_{SNS} vs T_A (I_{OUT} = 0.1A)

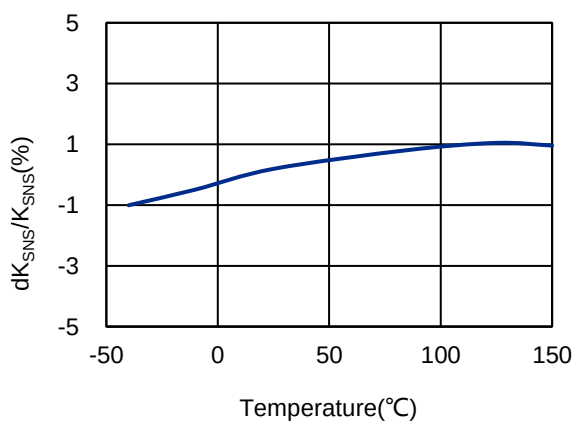


Figure 8-12. dK_{SNS} / K_{SNS} vs T_A (I_{OUT} = 6A)

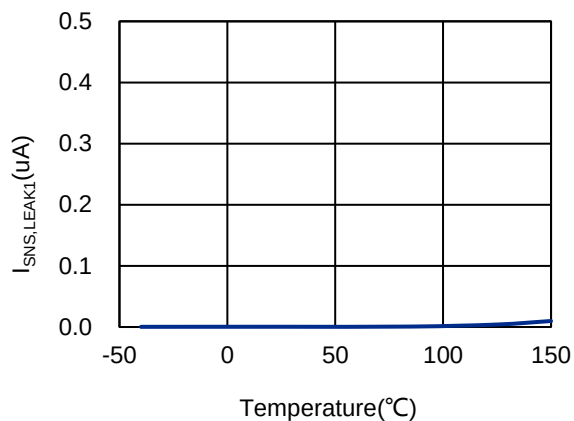


Figure 8-13. $I_{SNS,LEAK1}$ VS T_A

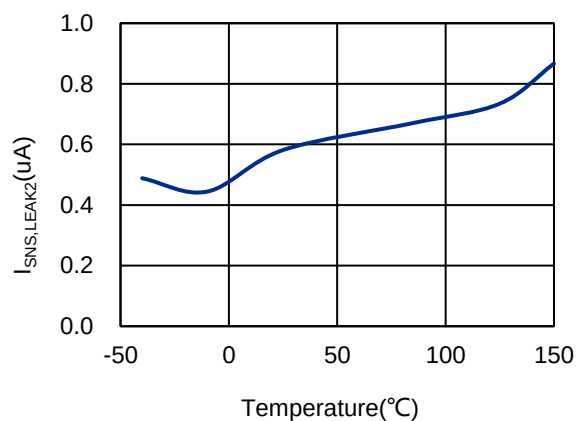


Figure 8-14. $I_{SNS,LEAK2}$ VS T_A

9 Functional Block Diagram

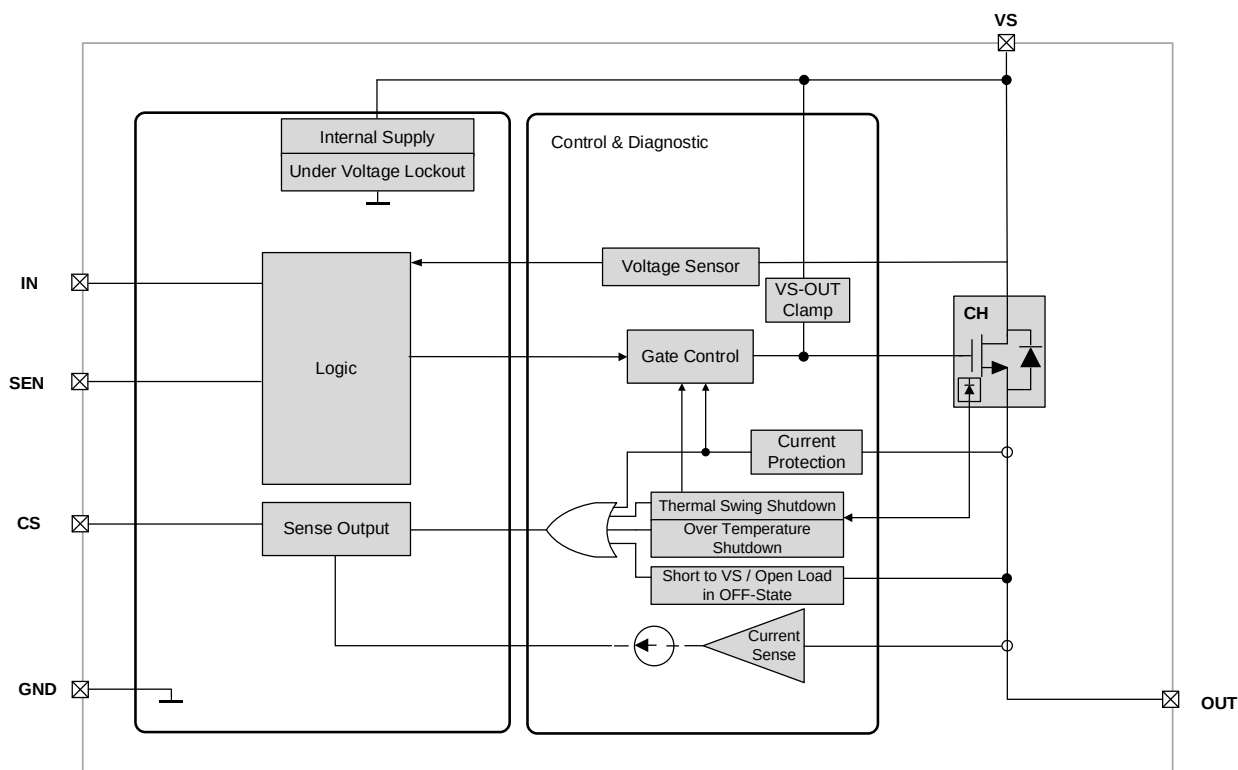
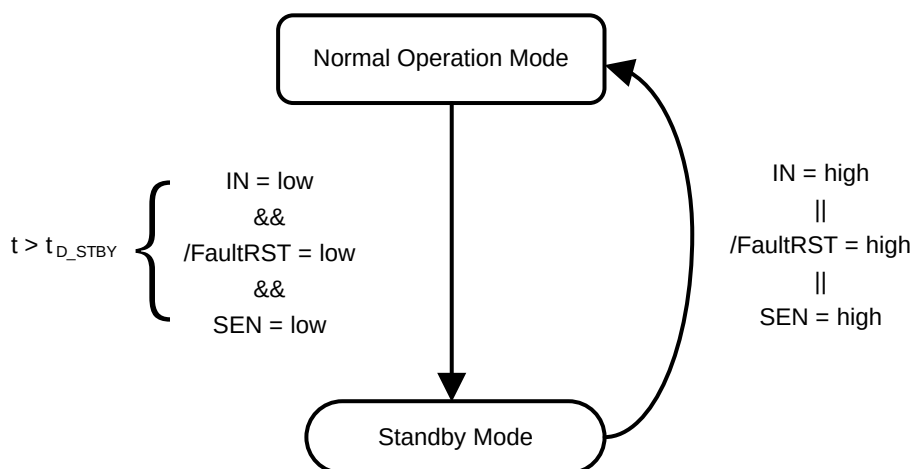


Figure 9-1. Functional Block Diagram

10 Feature Description

10.1 Operating States Diagram

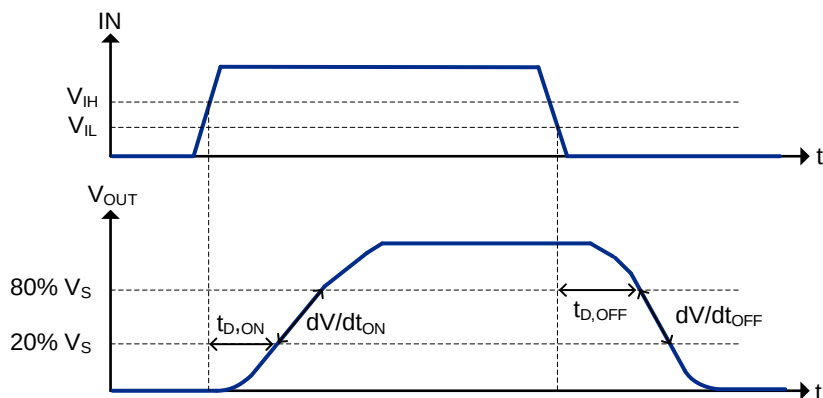
The chip has two operating states called 'Normal Operation Mode' and 'Standby Mode', which are decided by input logic signal status and deglitch time, shown as below:


Figure 10-1. Operating States Diagram

10.2 Power Stages

10.2.1 Switching Resistive Loads

When switching resistive loads, the switching time and slew rates are shown in Figure 10-2.


Figure 10-2. Operating States Diagram

10.2.2 Switching Inductive Loads

When turning OFF inductive loads with high-side driver, the output voltage V_{OUT} drops to a negative potential, because the inductance tends to maintain the current flow. To prevent the device from damage due to overvoltage, a voltage clamp mechanism is implemented. The clamping mechanism limits the negative output voltage to a safe value. Figure 10-3 shows a concept drawing of implementation.

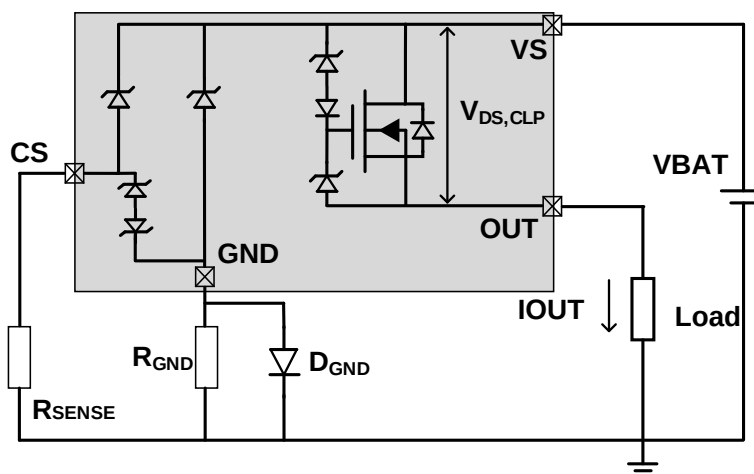


Figure 10-3. Output Clamp Diagram

10.3 CS timings

CS timings of Current sense mode are shown in Figure 10-4.

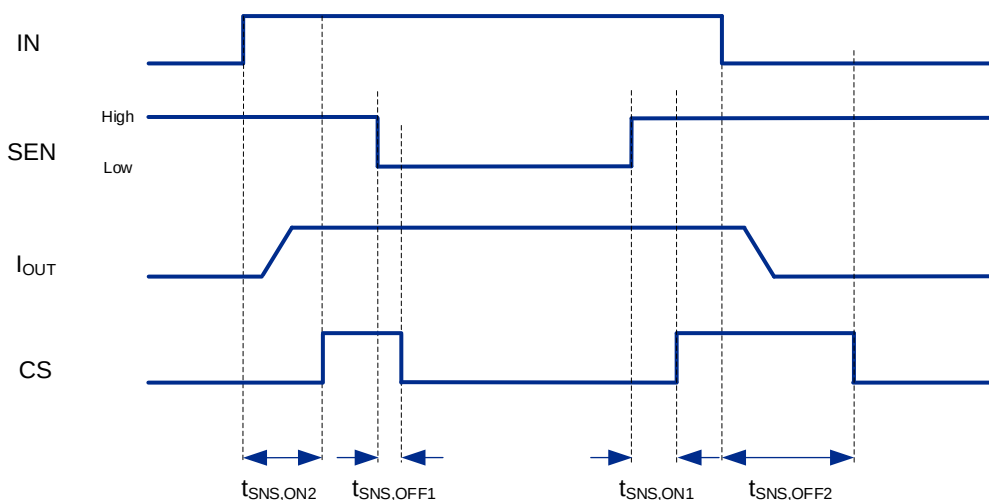


Figure 10-4. Current Sense timings

10.4 Protections

10.4.1 Overload Protection

The device features protection against overload and short circuit to ground. Its overload threshold decreases as junction temperature rises: at high temperatures, the overload threshold is reduced to prevent device damage. When the supply voltage V_S exceeds 16.5V-19.5V, the overload detection current decrease to I_{LIML} as shown in Figure 10-5.

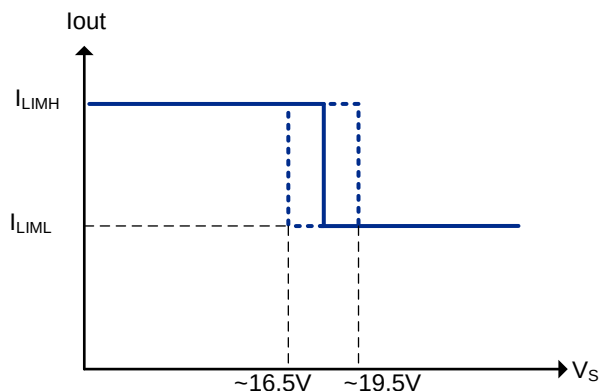


Figure 10-5. The overload detection current decrease to I_{LIML}

Once the load current meets or exceeds the applicable overload threshold, the output channel is switched off. The channel is allowed to restart, according to the Auto-restart strategy is shown in Figure 10-6.

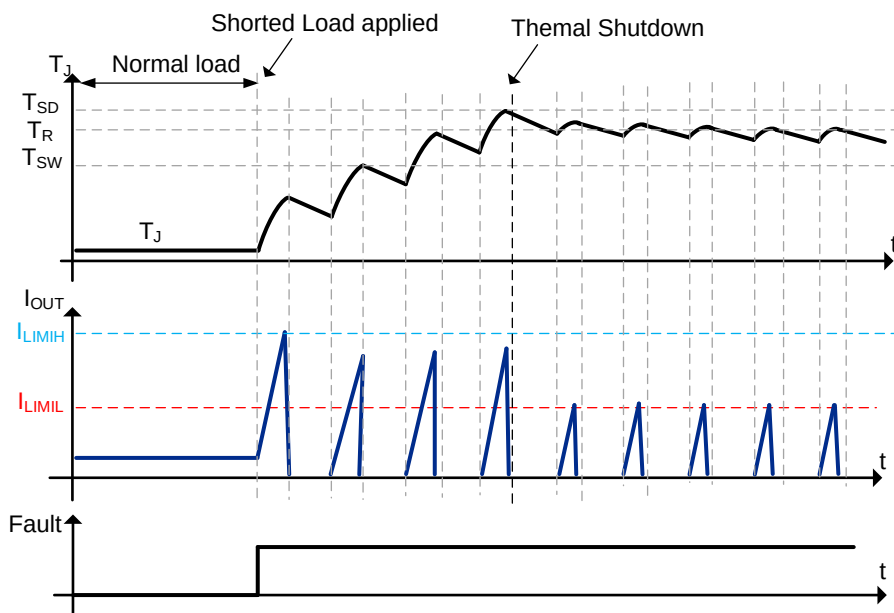


Figure 10-6. Auto-restart strategy

10.4.2 Undervoltage Protection

Undervoltage protection monitors the supply voltage (V_s). If V_s drops below the minimum undervoltage threshold ($V_{s,UVF}$), the output is turned off regardless of the input status. As soon as V_s is above the operative threshold ($V_{s,UVR}$), the channel is switched ON again as shown in Figure 10-7.

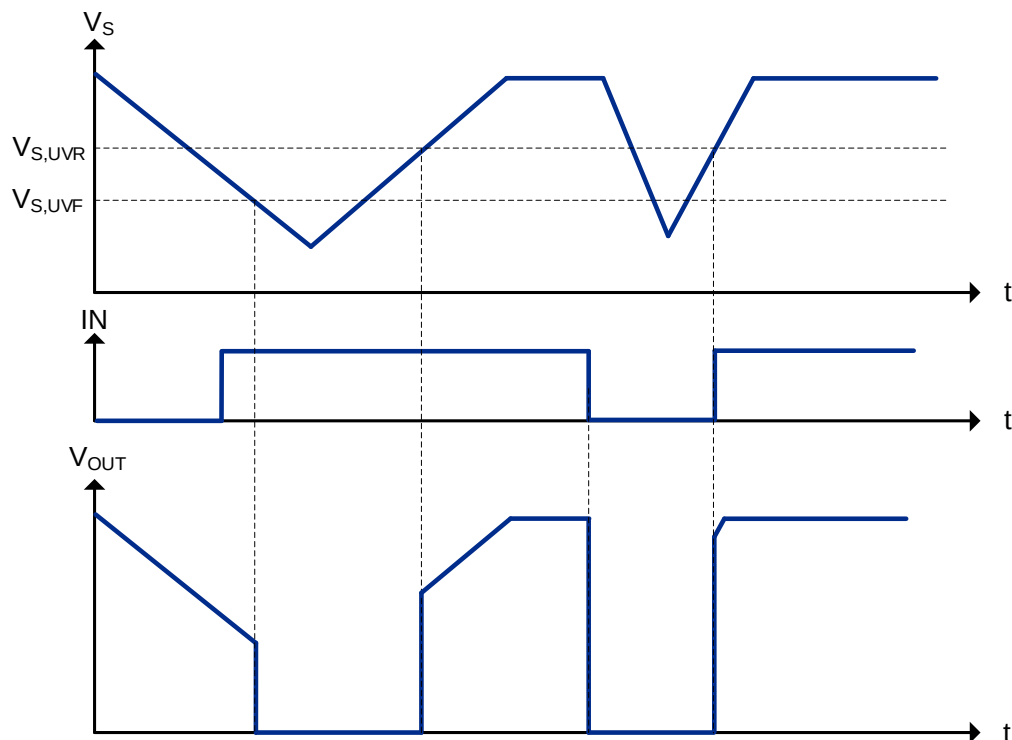


Figure 10-7. Vs Undervoltage Protection

10.4.3 Loss of Ground Protection

In the event of Loss of Ground, the device automatically switches off the power MOSFET, ensuring no current flows into the load. It is recommended to connect a resistor between any logic pins and the microcontroller to ensure the channel switch OFF.

Note: In case any logic pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.

10.4.4 Thermal Swing Shutdown

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing T_{SW} through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level. According to the voltage level on the /FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (/FaultRST = Low) or remains off (/FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

10.4.5 Thermal Shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 170°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the /FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (/FaultRST = Low) or remains off (/FaultRST = High).

10.5 Multiplexed Output of CS Pin

- a) Normal output: current sense of channel.
- b) Fault indication: over load, short to ground, TSW/TSD, open load or short to Vs in OFF-state

Table 10-1. Multiplexed Output

SEN	MUX channel	CS Output			
		Normal Mode	Over Load	Off-State Diagnostic	Negative Output
L		Hi-Z			
H	Output diagnostic	$I_{CS} = I_{out} / K$	$V_{CS,H}$	$V_{CS,H}$	Hi-Z

10.6 Truth Table of Protections and Diagnostics

Table 10-2. Truth Table of Protections and Diagnostics.

Mode	Conditions	IN	/FaultRST	SEN	OUT	CurrentSense	Comments
Standby	All logic inputs low	L	L	L	L	Hi-Z	Low I_{S_STBY} consumption
Normal	Nominal load connected: $T_J < 150\text{ }^{\circ}\text{C}$	L	X	L	L	Referring to Table 10-1	/
		H	L	H	H		Configured in auto-restart mode
		H	H	H	H		Configured in latch-off mode
Over Load	Over load current: $T_J > T_{SD}$ or $\Delta T_J > T_{SW}$	L	X	L	L	Referring to Table 10-1	
		H	L	H	L		Output restarts with temperature protection hysteresis
		H	H	L	L		Output latches-off
Undervoltage	$V_S < V_{S_UVF}$	X	X	X	L	Hi-Z	Restart when $V_S > V_{S_UVR}$
Off-state Diagnostic	Short to V_S	L	X	H	H	Referring to Table 10-1	/
	Open Load	L	X	H	H		External pull-up required
Negative Output Voltage	Inductive loads turn off	L	X	$< 0\text{ V}$	$< 0\text{ V}$	Referring to Table 10-1	/

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. This is a very simplified example of an application circuit. The function must be verified in the real application.

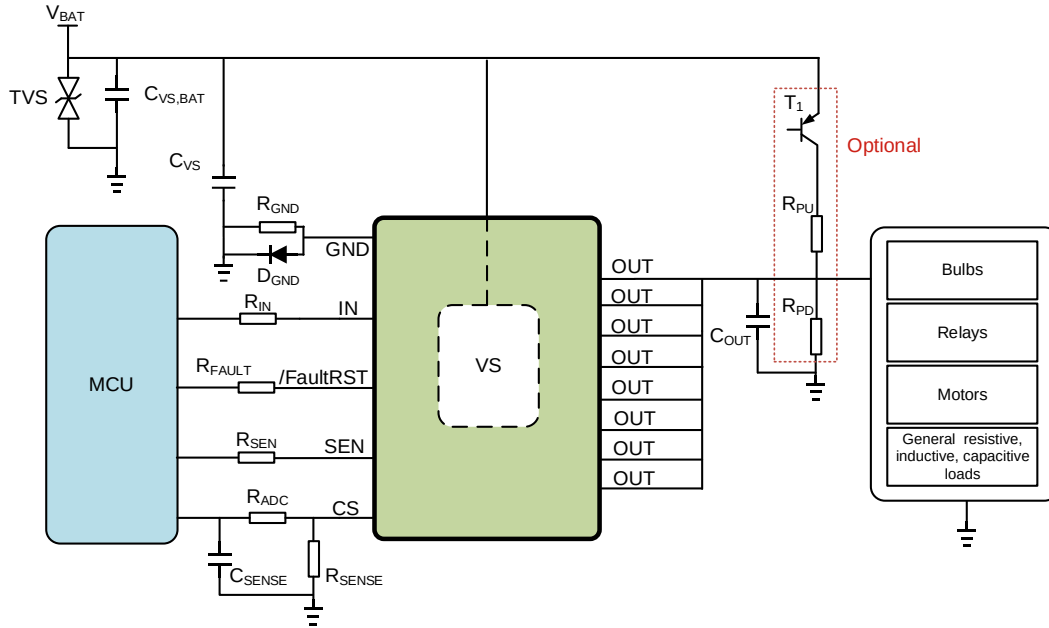


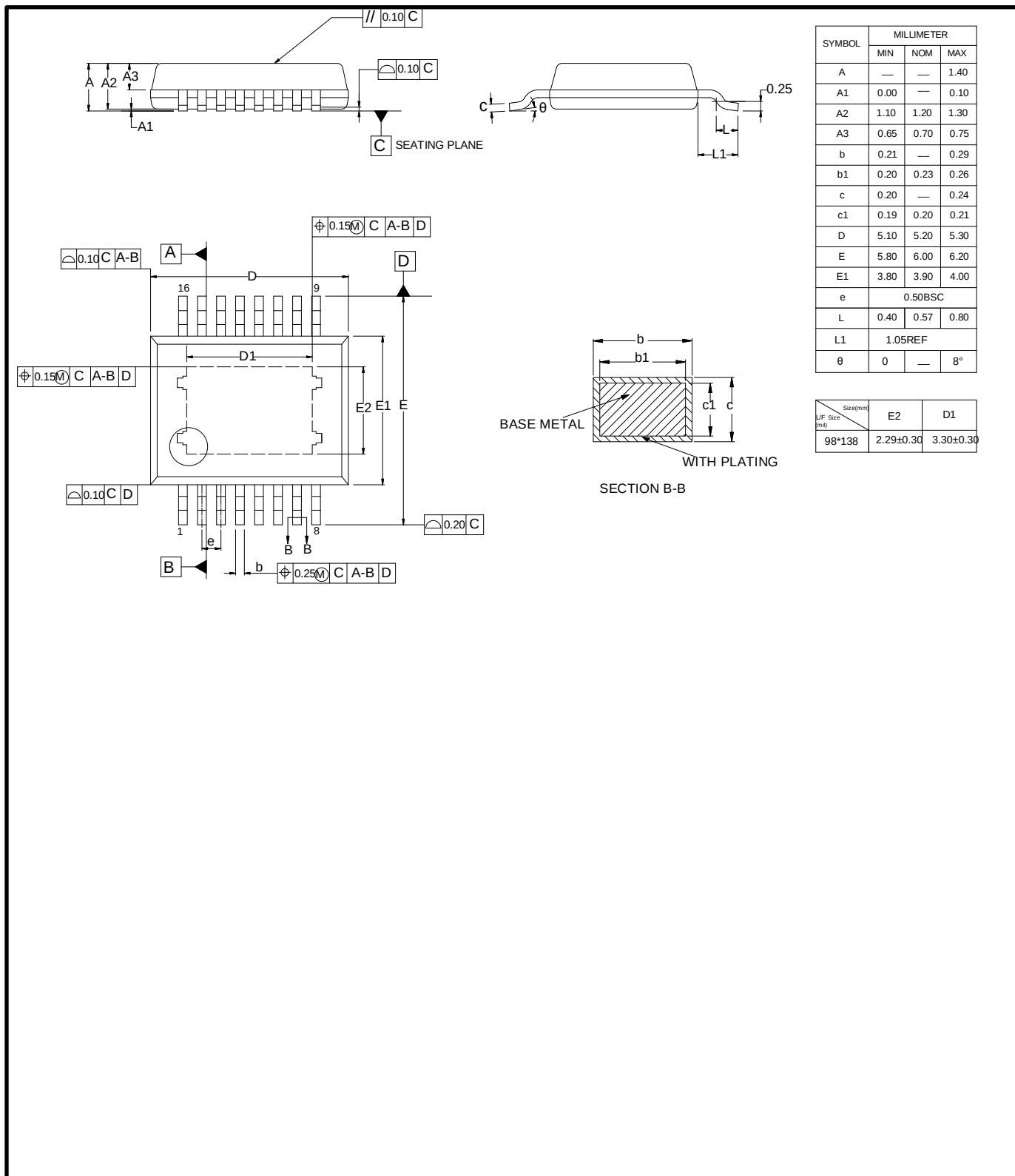
Figure 11-1. Application Diagram

Table 11-1. Suggested Component Values

Reference	Value	Purpose
R _{IN}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{FAULT}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{SEN}	4.7kΩ	Protection of the microcontroller during Overvoltage and Reverse Battery
R _{PD}	47kΩ	Output pull-down Ensure polarization of the device outputs to distinguish between Open Load and Short to VS in OFF-State
R _{PU}	1.5kΩ	Output pull-up Ensure polarization of the device output during Open Load in OFF-State
C _{OUT}	10nF	Protection of the device output during ESD events
T ₁	-	Switch the battery voltage for Open Load in OFF-State
C _{VS}	100nF	Filtering of voltage spikes on the battery line
TVS	33V	Diode transient voltage suppressor diode
C _{VS,BAT}	-	Filtering / buffer capacitor located at V _{BAT} connector
R _{SENSE}	1.2kΩ	Sense resistor
R _{ADC}	4.7kΩ	Protection of microcontroller ADC input during Overvoltage, Reverse Battery, Loss of Ground
C _{SENSE}	220pF	Sense signal filtering
D _{GND}	-	Reverse polarity protection Schottky diode.
R _{GND}	4.7kΩ	Protection in case of Loss of Battery while driving inductive loads

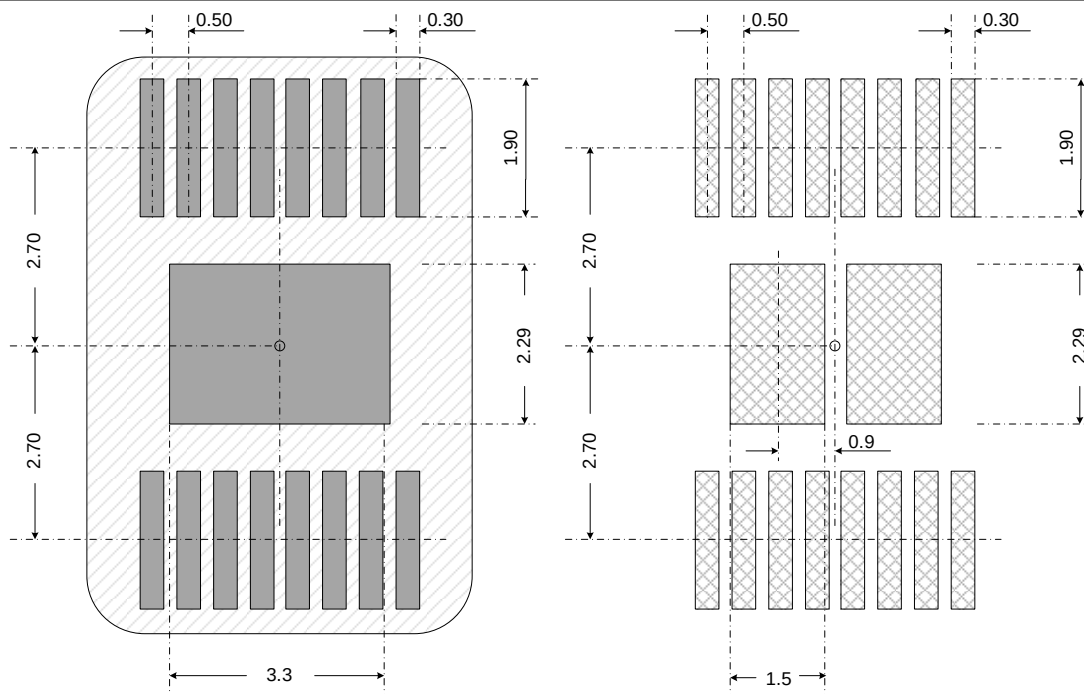
MECHANICAL DATA

eSSOP-16



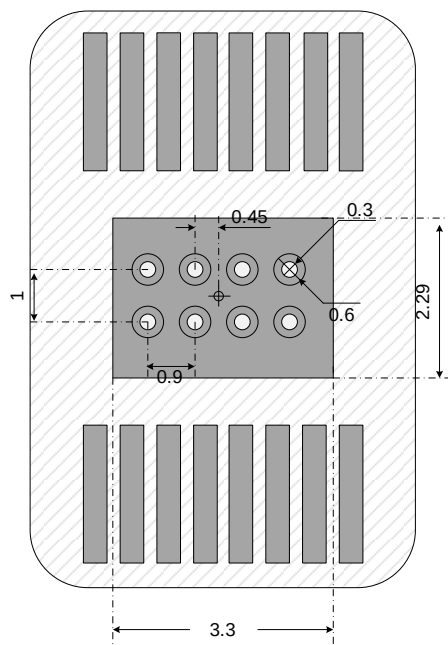
RECOMMENDED FOOTPRINT

eSSOP-16



ALL DIMENSIONS ARE IN UNITS MM

Copper Solder mask Stencil apertures



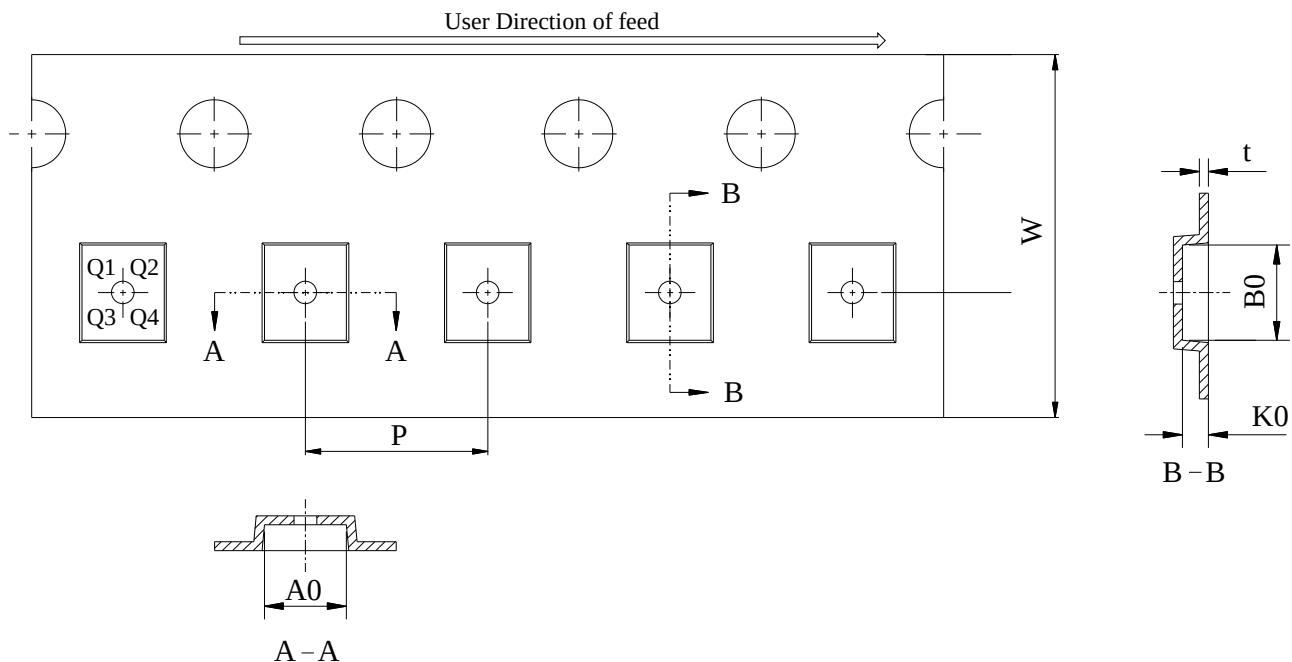
ALL DIMENSIONS ARE IN UNITS MM

Copper Solder mask

NOTE: Via diameters and positions shall be set according to the actual PCB situation

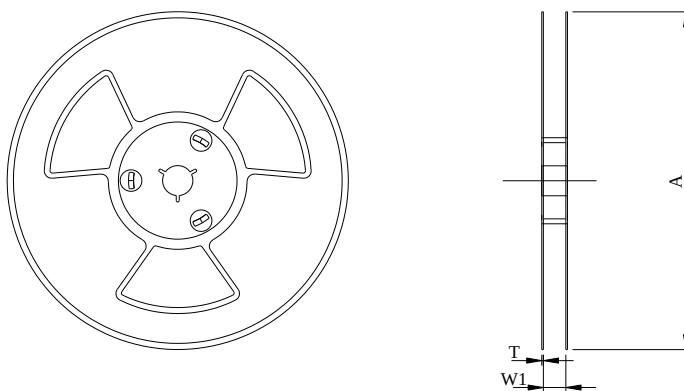
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00+0.30/-0.1	8.00±0.10	6.50±0.10	5.50±0.10	1.75±0.10	0.30±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	12.4 +1/-0	2.1±0.3

Asfdgy

IMPORTANT NOTICE AND DISCLAIMER

Southchip Semiconductor Technology (Shanghai) Co., Ltd. and its subsidiaries (“**SOUTHCHIP**”) provides technical and reliability data (including datasheets), design resources (including reference designs, software), application or other design advice and other resources (“**Resources**”) “**AS IS**” **AND WITH ALL FAULTS**.

The Resources are intended for skilled developers designing with SOUTHCHIP’s products. SOUTHCHIP may provide but **DISCLAIMS WARRANTY FOR** SOUTHCHIP’s technical support or design services for the customers. Customers are solely responsible for (1) selecting and using the appropriate SOUTHCHIP’s products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. SOUTHCHIP **DISCLAIMS RESPONSIBILITY FOR** any claims, damages, costs, losses, liabilities arising out of Customers’ use of the Resources.

SOUTHCHIP’s sample products are provided “**AS IS**” and only for purposes of designing, validating and testing. SOUTHCHIP reserves the right to make changes, corrections, enhancements, modifications and improvements to SOUTHCHIP’s products and/or to the Resources at any time without notice. Customers shall, prior to, mass producing, using or distributing any products of their own that incorporate SOUTHCHIP’s products, obtain the latest relevant information on SOUTHCHIP’s products and thoroughly test such products for purposes of mass production, quality and safety. Use of SOUTHCHIP’s products without a safety design is fully at the risk of Customers, subject only to applicable laws and regulations governing limitations on product liability.