SC6206Q High-Performance ASIL-B Rated PMIC with Buck Converters and LDO for Automotive Camera Module

1 Descriptions

The SC6206Q is a high-performance Power Management IC (PMIC) for automotive camera modules. It integrates a high-voltage buck converter for a primary regulator, dual low-voltage buck converters and a low noise LDO for secondary regulators.

The devices feature a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient performance. The high-frequency operation allows for the use of all ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low-RDS(ON) switches improve efficiency at heavy loads and make layout simpler than discrete solutions.

I2C digital interface allows for application flexibility. Output voltage, power sequence, and protection thresholds can all be adjusted through the interface. Fault status can also be monitored. Protection features include undervoltage lockout (UVLO), over current protection (OCP), over voltage protection (OVP), under voltage protection (UVP) and thermal shutdown (TSD).

The SC6206Q supports applications with a high automotive safety integrity level up to ASIL-B. Functional safety features such as an analog built-in self-testing (ABIST), diagnostics, a nRESET and a nINT output pin are all included. It is developed under Functional Safety Product Development process, which has been independently certified to meet ISO26262 guidelines.

The SC6206Q is available in 22-pin 3mm X 3.5mm Wettable-Flank MIS package.

2 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range: -40°C to 125 °C
- Integrated 3-Buck converters:
  - Buck1 V_{IN} range from 4V to 19V
  - Buck1 V_{OUT} range from 2.5V to 4V
  - Buck1 output current up to 2A
  - Buck2/Buck3 V_{IN} range from 2.7V to 5.5V
  - Buck2/Buck3 V_{OUT} range from 0.8V to 1.9V
  - Buck2/Buck3 output current up to 2A
  - Spread spectrum for better EMI performance
  - Fixed 2.2MHz frequency PWM operation
- Integrated high-PSRR low dropout (LDO) regulator:
  - V_{IN} range from 2.7V to 5.5V
  - V_{OUT} range from 1.8V to 3.3V
  - High PSRR 60dB @ 100kHz
  - Adjustable output voltage through I2C
  - Up to 300mA current capability (Transient to 400mA)
- High precision:
  - +/- 1.5% output voltage accuracy
  - +/- 1.0% OV/UV monitoring accuracy
- Functional Safety:
  - Hardware capable to ASIL-B
  - Integrated ABIST and reference monitor
  - Documents available to support ISO26262 design
  - Failure modes effects and diagnostic analysis
  - Safety manual
- Over current protection and power good output

3 Applications

- Automotive Camera Module
- Automotive Sensor Applications

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4 Device Information

ORDER NUMBER	HVBUCK1 OUTPUT(*)	LDO OUTPUT (*)	LVBUCK2 OUTPUT(*)	LV BUCK3 OUTPUT (*)	SEQUENCY (*)	BODY SIZE (*)
SC6206QA1MDKR	3.8V	3.3V	1.8V	1.1V	B1>LDO>B2>B3	3mm x 3.5mm x 1.0mm
SC6206QA2MDKR	3.3V	2.9V	1.8V	1.1V	B1>LDO>B2>B3	3mm x 3.5mm x 1.0mm
SC6206QA3MDKR	3.8V	3.3V	1.8V	1.1V	B1>B2>B3>LDO	3mm x 3.5mm x 1.0mm
SC6206QA4MDKR	3.3V	2.8V	1.8V	1.15V	B1>LDO>B2>B3	3mm x 3.5mm x 1.0mm
SC6206QA5MDKR	3.3V	2.8V	1.8V	1.075V	B1>B3>B2>LDO	3mm x 3.5mm x 1.0mm
SC6206QA6MDKR	3.3V	2.8V	1.8V	1.05V	B1>B3>B2>LDO	3mm x 3.5mm x 1.0mm
SC6206QA7MDKR	3.8V	3.3V	1.8V	1.1V	B1>LDO>B3>B2	3mm x 3.5mm x 1.0mm
SC6206QA8MDKR	3.6V	2.8V	1.8V	1.2V	B1>LDO>B2>B3	3mm x 3.5mm x 1.0mm
SC6206QA9MDKR	3.3V	2.8V	1.8V	1.2V	B1>LDO>B2>B3	3mm x 3.5mm x 1.0mm
SC6206QAAMDKR	3.3V	2.8V	1.8V	1.2V	B1>B2>B3>LDO	3mm x 3.5mm x 1.0mm
SC6206QADMDKR	3.6V	3.3V	1.8V	1.3V	B1>B3>LDO>B2	3mm x 3.5mm x 1.0mm
SC6206QAEMDKR	3.8V	3.3V	1.8V	1.1V	B1>LDO>B2>B3	3mm x 3.5mm x 1.0mm
SC6206QAFMDKR	3.3V	2.8V	1.8V	1.15V	B1>B2>B3>LDO	3mm x 3.5mm x 1.0mm
SC6206QAHMDKR	3.3V	2.8V	1.8V	0.9V	B1>B2>B3>LDO	3mm x 3.5mm x 1.0mm
SC6206QAJMDKR	3.3V	2.8V	1.8V	1.1V	B1>B2>B3>LDO	3mm x 3.5mm x 1.0mm

For other output voltage, sequence or package option, please contact Southchip

5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.0.1	2025/6	Page2	1. Add Device information
V1.0.0	2025/3	/	2. Initial version

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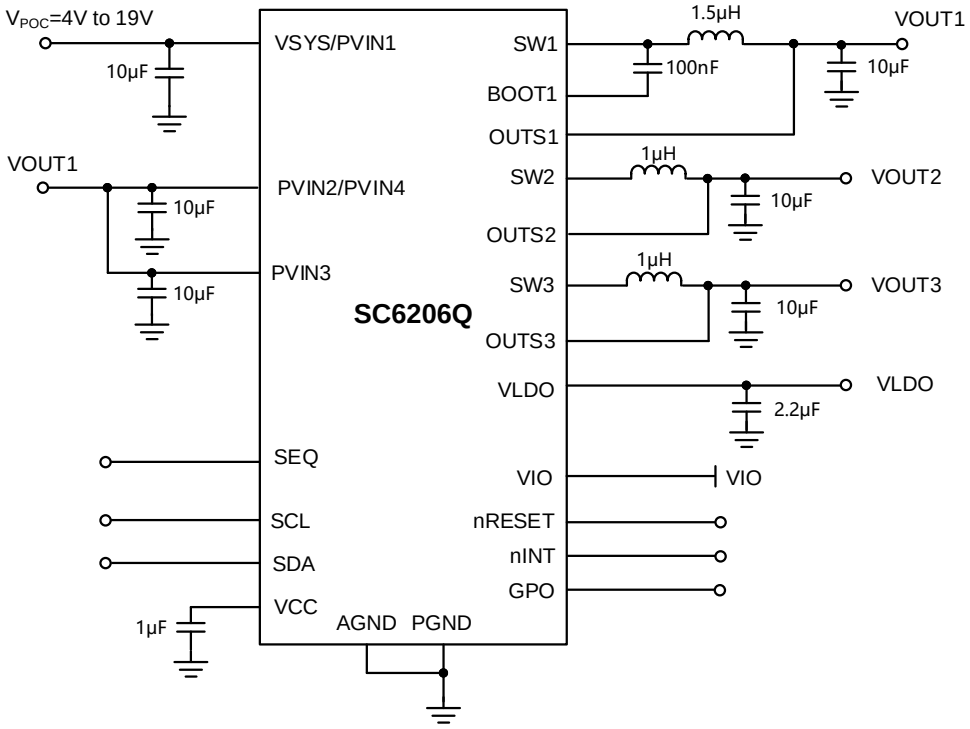
6 Typical Application Circuit



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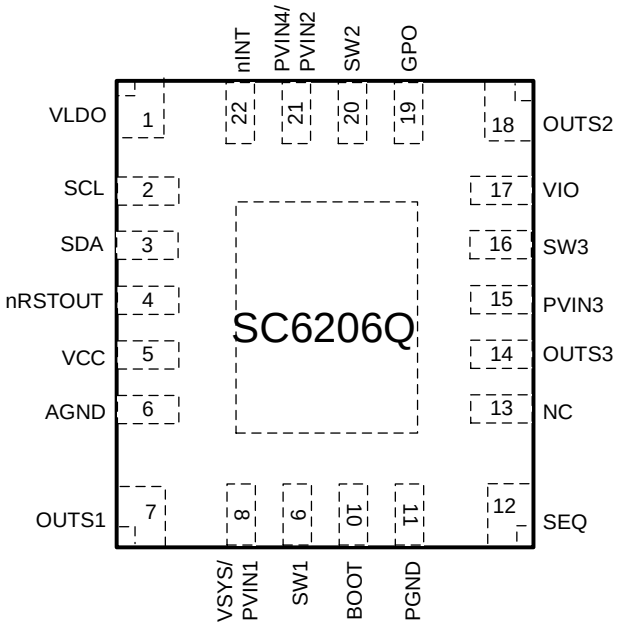
7 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	VLDO	O	LDO output voltage
2	SCL	I	Clock of I2C Interface
3	SDA	I/O	Data of I2C Interface
4	nRSTOUT	O	Push-Pull or Open-Drain RESET Output
5	VCC	O	Internal LDO regulator output. Decouple with a 2.2μF/0603 capacitor between this pin and the AGND pin
6	AGND	GND	Signal ground of the IC.
7	OUTS1	I	Buck1 output voltage-sense input
8	VSYS/PVIN1	PWR	Device Input Power
9	SW1	O	Switching node pin of the Buck1. Connected to inductor.
10	BOOT	O	Power Supply for high-side MOSFET gate driver. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW1 pin.
11	PGND	GND	Power ground of the IC.
12	SEQ	I	Sequence Control Pin

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13	NC	/	Not connected
14	OUTS3	I	BUCK3 Output Voltage-Sense Input
15	PVIN3	PWR	Input voltage for Buck3.
16	SW3	O	Switching node pin of the buck3. Connected to inductor
17	VIO	I	IO supply voltage pin
18	OUTS2	I	BUCK2 Output Voltage-Sense Input
19	GPO	O	General Purpose Output
20	SW2	O	Switching node pin of the buck2. Connected to inductor
21	PVIN2/PVIN4	PWR	Power supply for Buck2 and LDO
22	nINT	O	Interrupt Request Output
	EP	/	Connect to a large ground plane to maximize thermal performance. Internally connect the PGND

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8 Specifications

8.1 Absolute Maximum Ratings

Over the recommend operating junction temperature range of - 40°C to + 150°C (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals (2)	VSYS, VSYS_S, PVIN1, SEQ	-0.3	25	V
	BOOT1 to SW1	-0.3	6	V
	SW2, SW3	-0.3	6.5	V
	All other pins	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) ESD stress voltage (2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage (3), all pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range for primary high-voltage buck	4		19	V
V_{OUT1}	Input voltage range for secondary low-voltage buck and LDO	2.7		5.5	V
L_{HV}	Inductor for primary high-voltage buck	1	1.5	2.2	μH
L_{LV}	Inductor for secondary low-voltage buck	0.68	1	1.2	μH
C_{INH}	Input capacitor for primary high-voltage buck	4.7	10		μF
C_{OUTH}	Output capacitor for primary high-voltage buck	4.7	10	50	μF
C_{INL}	Input capacitor for secondary low-voltage buck	7	10	50	μF
C_{OUTL}	Output capacitor for secondary low-voltage buck	7	10	30	μF
C_{INLDO}	Input capacitor for secondary LDO	1.5	2.2	50	μF

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C_{OUTLDO}	Output capacitor for secondary LDO	1	2.2	20	μF
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE (1)		MIS-22 (3mm x 3.5mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	47.9	°C/W
Θ_{JC}	Junction to case thermal resistance	30.4	°C/W
Θ_{JB}	Junction to board thermal resistance	7.2	°C/W

(1) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application.

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 12V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATE CONDITION						
V_{SYS_UVLO}	Input under voltage lockout threshold	Rising edge	3.6	3.8	4.0	V
		Falling edge	3.1	3.3	3.5	V
V_{SYS_OVP}	Input over voltage protection threshold for primary Buck1	Rising edge	20	21	22	V
		Hysteresis		1	1.6	V
T_{TW}	Thermal warning temperature			125		°C
	Thermal warning hysteresis			20		°C
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			20		°C
VCC REGULATOR						
V_{CC}	Internal VCC output voltage		4.4	4.6	4.8	V
V_{CC_UV}	VCC under-voltage detection threshold	Falling threshold	2.85	3	3.15	V
$V_{CC_UV_HYS}$	VCC under-voltage detection threshold hysteresis			0.1		V
V_{CC_OVP}	VCC over-voltage protection detection threshold	Rising threshold	5.0	5.5	6.0	V
$V_{CC_OVP_HYS}$	VCC over-voltage protection detection threshold hysteresis			0.2		V
SWITCHING CHARACTERISTICS						
F_{SW}	Switching frequency		2.0	2.2	2.4	MHz
F_{SS}	Spread spectrum range			6		%
BUCK1 CONVERTER						

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V_{BUCK1_UVLO}	BUCK1 V_{IN} under voltage lockout threshold	Rising edge	4.4	4.6	4.8	V
		Falling edge	3.7	3.9	4.1	V
V_{OUT1_RANGE}	V_{OUT1} output voltage range	Normal buck mode	2.5		4.0	V
	V_{OUT1} voltage accuracy	VIN=12V, I_{OUT}=2A, V_{OUT1}=2.5V ~ 4V	-1.5		1.5	%
I_{PCL_HVB1}	Inductor peak current limit		2.4	3	3.6	A
I_{VCL_HVB1}	Inductor valley current limit		2.2	2.7	3.5	A
I_{NCL_HVB1}	Negative inductor peak current limit			-2.2		A
$R_{ON_HVB1_H}$	High-side MOSFET on resistance			200	330	mΩ
$R_{ON_HVB1_L}$	Low-side MOSFET on resistance			110	200	mΩ
R_{VO1}	Fast discharge resistance			250		Ω
T_{SS_VO1}	Soft start-up time	From 0 to 90% of V_{O1}, no load	0.4	0.8	1.5	ms
$T_{MIN_ON_HVB1}$	HVBUCK1 minimum on time				70	ns
$T_{MIN_OFF_HVB1}$	HVBUCK1 minimum off time			55	110	ns
BUCK2/3 CONVERTER						
$V_{OUT2/3_RANGE}$	V_{O2} output voltage range	Normal buck mode	0.8		2.5	V
	V_{O2} voltage accuracy	V_{IN2}=3.6V, I_{OUT}=I_{OUT_MAX}, V_{OUT2}=0.9V ~ 1.9V	-1.5		1.5	%
$I_{PCL_LVB2/3}$	Inductor peak current limit		2.4	3.0	3.6	A
$I_{NCL_LVB2/3}$	Negative inductor peak current limit			-1.7		A
$R_{ON_LVB2/3_H}$	High-side PMOS on resistance			100	180	mΩ
$R_{ON_LVB2/3_L}$	Low-side NMOS on resistance			50	100	mΩ
$R_{VO2/3}$	Fast discharge resistance	V_{O2}=0.3V		100		Ω
$T_{SS_VO2/3}$	Soft start-up time	From 0 to 90% of V_{O2}, no load	0.2	0.5	0.8	ms
$T_{MIN_ON_LVB2/3}$	LVBUCK2 minimum on time				70	ns
$T_{MIN_OFF_LVB2/3}$	LVBUCK2 minimum off time				60	ns
LOW NOISE LDO						
V_{OUT4_RANGE}	LDO output range		1.8		3.5	V
	V_{O4} voltage accuracy	V_{IN4}=3.6V	-1.5		1.5	%
I_{OUT4_MAX}	Maximum output current capability	Continuous			300	mA
		Transient			400	mA
I_{CL_LDO}	LDO current limit		400	470	540	mA
V_{DROP_LDO}	LDO dropout voltage	I_{OUT4}=150mA			150	mV
		I_{OUT4}=300mA			300	mV
R_{VO4}	Fast discharge resistance			60		Ω
T_{SS_VO4}	Soft start-up time	From 0 to 90% of V_{O4}, no load	0.3	0.7	1.5	ms
eN_{VO4}	Output noise voltage	Peak to peak in one switching cycle		60		μV
PSRR	Power supply rejection ratio	f=100KHz, IO4=100mA		60		dB
		f=1MHz, IO4=100mA		40		dB

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LOGIC AND INTERFACE						
V_{IN_VIO}	VIO input voltage range		1.8		5	V
V_{SEQ_IL}	Low-level input voltage	$V_{BIAS}=V_{IO}$	0.54			V
V_{SEQ_IH}	High-level input voltage	$V_{BIAS}=V_{IO}$			1.26	V
V_{OL_OD}	nINT and nRESET low level output voltage(open-drain)	V_{IO}=1.8V, I_{OL}=2mA			0.1	V
R_{PU_OD}	Internal pull-up resistor			10		kΩ
V_{OL_PP}	nINT and nRESET low level output voltage(push-pull)	V_{IO}=1.8V, I_{OL}=2mA			0.1	V
V_{OH_PP}	nINT and nRESET high level output voltage(push-pull)	V_{IO}=1.8V, I_{OL}=2mA	0.7 *VIO			V
V_{IH}	Input logic high for I2C and GPO				1.3	V
V_{IL}	Input logic low for I2C and GPO		0.4			V
I_{nRESET_LKG}	nRESET pin leakage				1	μA
T_{d_PG}	nRESET pin output delay time			10		ms
MONITOR REFERENCE						
$V_{OUT1/2/3/4_OV}$	PG Over Voltage Threshold. Rising	Register Programmable	103	104	105	%
			105	106	107	%
$V_{OUT1/2/3/4_OV_HYS}$	PG Over Voltage Threshold, Hysteresis			1		%
$V_{OUT1/2/3/4_OVP}$	Over voltage protection detection threshold		112	115	118	%
$V_{OUT1/2/3/4_OVP_HYS}$	Over voltage protection detection threshold hysteresis			5		%
$V_{OUT1/2/3/4_UV}$	PG under voltage threshold rising	Register Programmable	95	96	97	%
			93	94	95	%
$V_{OUT1/2/3/4_UV_HYS}$	PG under voltage threshold, hysteresis			1		%
$V_{OUT1/2/3/4_SCG}$	Short-circuit detection threshold		250	300	350	mV
V_{SCG_HYS}	Short-circuit detection threshold hysteresis			100		mV
TIMING CHARACTERISTICS						
t_{DEG_SEQ}	Deglitch time on both rising and falling edge			10		μs
$t_{OUT_VMON_DEQ}$	Output voltage fault detection deglitch time			22		μs
t_{DEG_LOG}	Loss of ground detection deglitch time			10		μs

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8.6 Typical Characteristics

V_{INH}=8V, V_{O1}=V_{INL}=V_{LDOIN}=3.6V, V_{O2}=1.1V, V_{O3}=1.8V, V_{O4}=3.3V, unless otherwise noted.

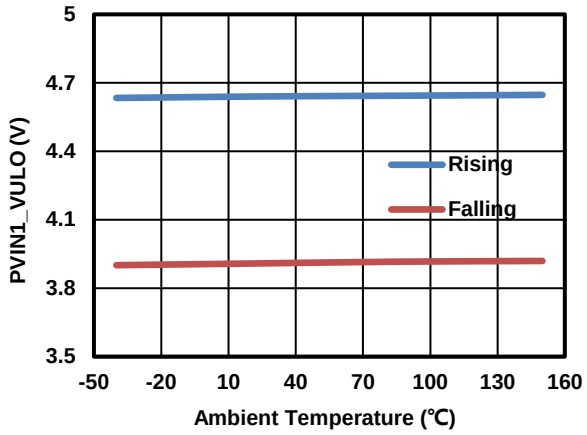

Figure 8-1, PVIN1_VULO vs Temperature

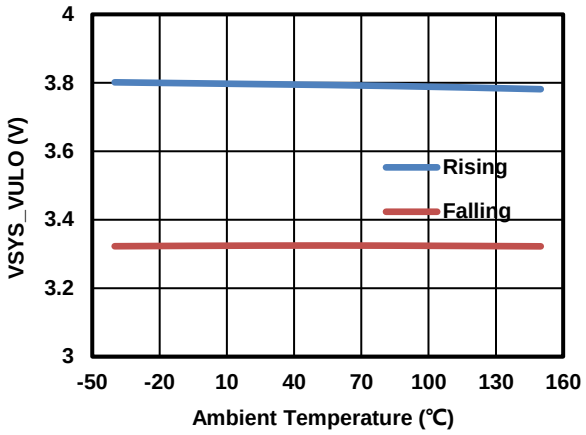

Figure 8-2, VSYS_VULO vs Temperature

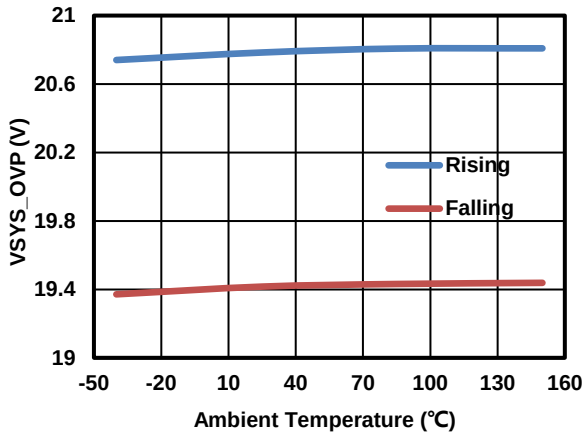

Figure 8-3, VSYS_OVP vs Temperature

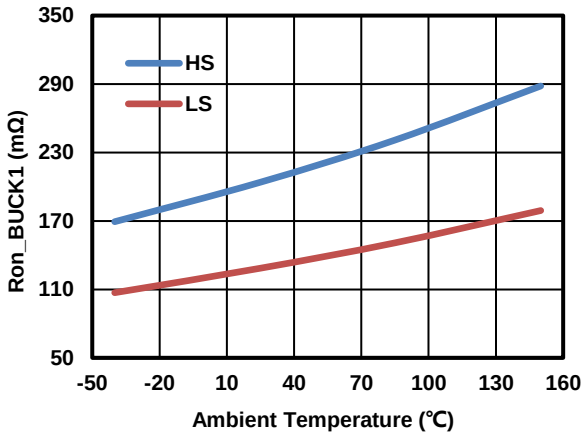

Figure 8-4, Ron_BUCK1 vs Temperature

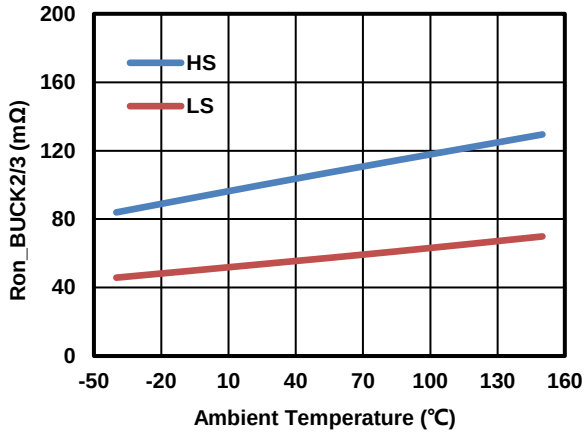

Figure 8-5, Ron_BUCK2/3 vs Temperature

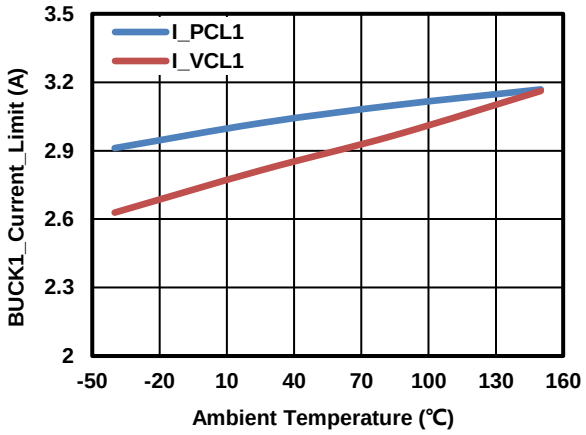

Figure 8-6, BUCK1_Current_Limit vs Temperature

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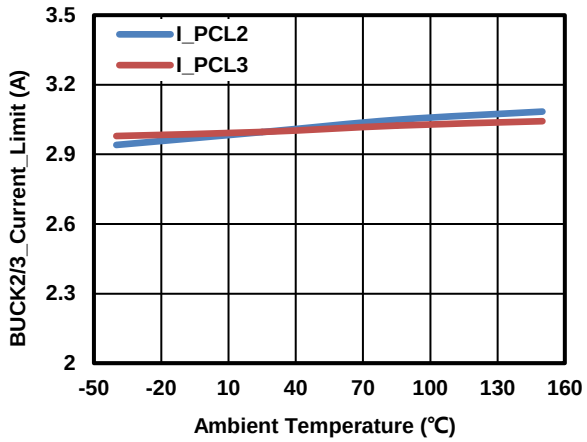

Figure 8-7, BUCK2/3_Current_Limit vs Temperature

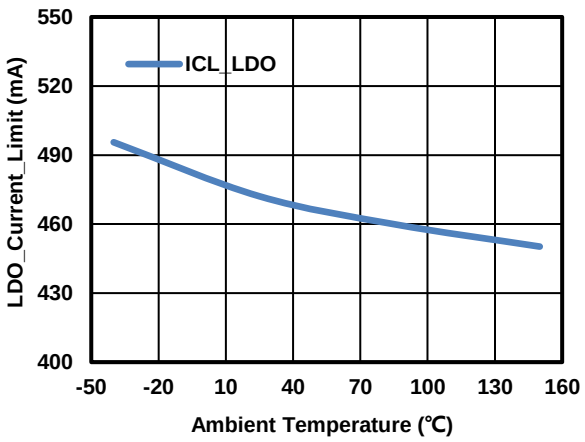

Figure 8-8, LDO_Current_Limit vs Temperature

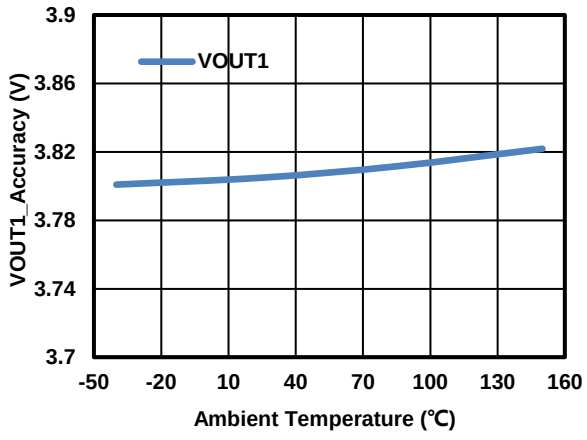

Figure 8-9, VOUT1_Accuracy vs Temperature

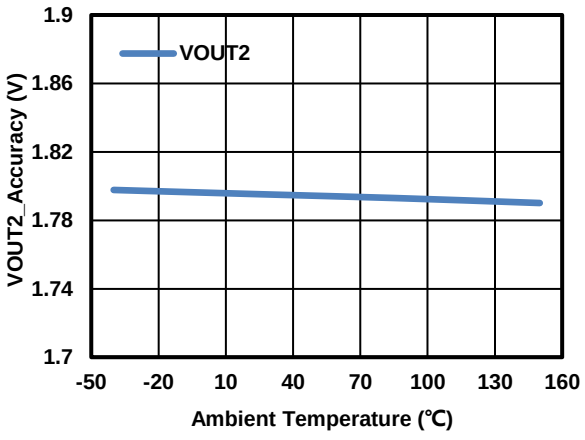

Figure 8-10, VOUT2_Accuracy vs Temperature

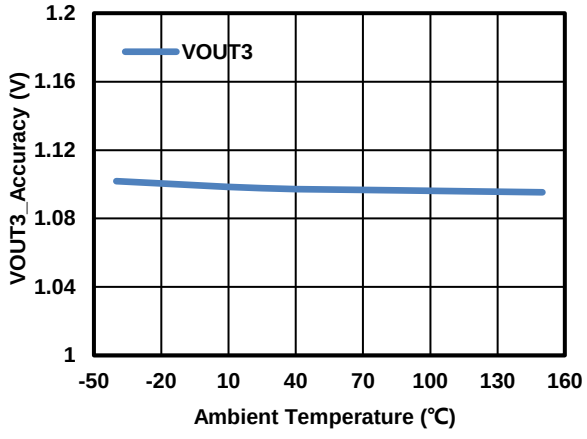

Figure 8-11, VOUT3_Accuracy vs Temperature

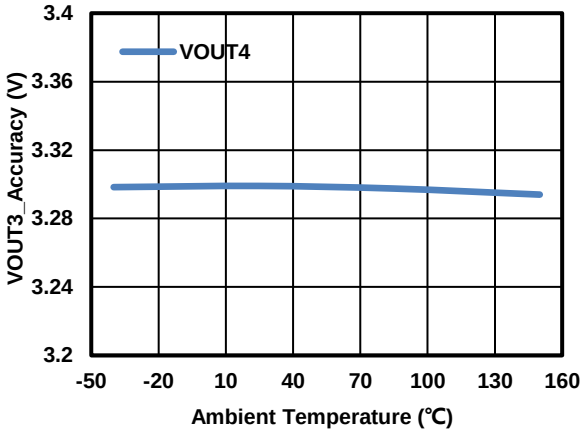

Figure 8-12, VOUT4_Accuracy vs Temperature

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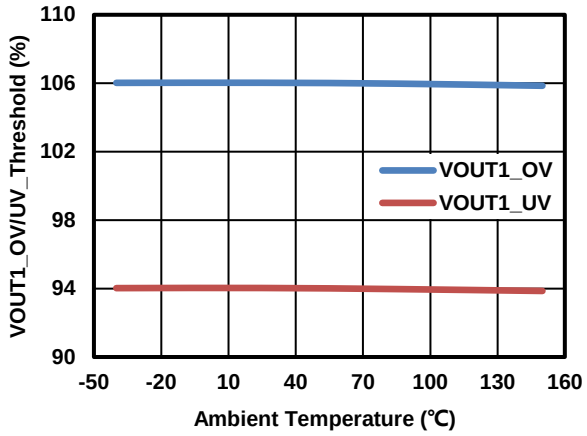

Figure 8-13, VOUT1_OV/UV_Threshold vs Temperature

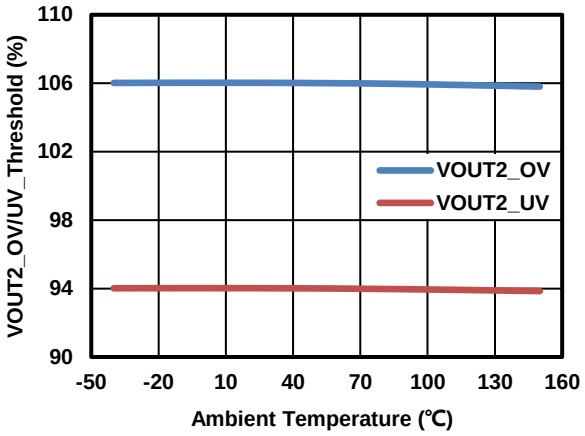

Figure 8-14, VOUT2_OV/UV_Threshold vs Temperature

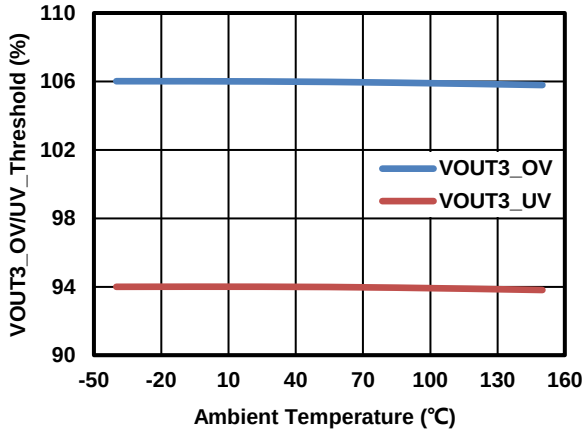

Figure 8-15, VOUT3_OV/UV_Threshold vs Temperature

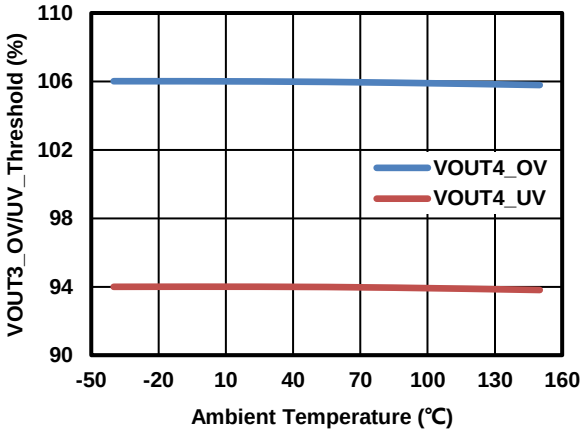

Figure 8-16, VOUT4_OV/UV_Threshold vs Temperature

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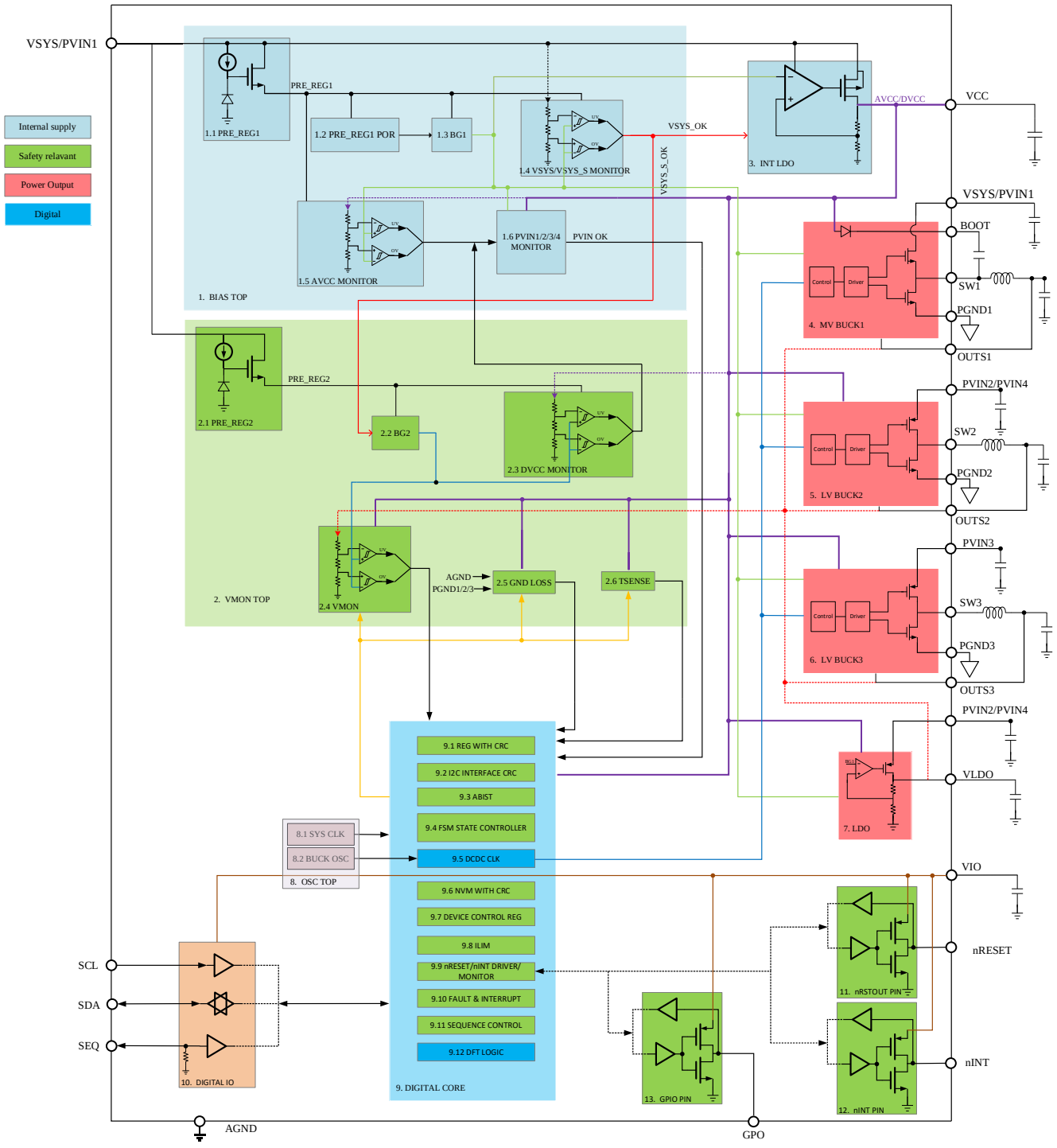
9 Functional Block Diagram



10 Feature Description

The SC6206Q is designed for automotive surround view camera sensors, but not limited to. It provides a high voltage buck converter as a primary regulator, dual low-voltage buck converters and one low dropout regulator for secondary regulators. It allows voltage settings and sequence control with I2C interface.

In order to meet the ASIL-B functional safety level, it Integrates analog build in self-test function, output voltage monitoring, overvoltage protection, undervoltage protection, overload protection, overcurrent protection, thermal monitoring and support fault detection functions, built-in registers can record fault events. The nINT and nRESET pins level indicate the state machine status for reporting the interrupt to the upper level system in real time.

10.1 BUCK Converters

The three buck converters use a peak current mode control scheme and operate at forced-PWM mode with a fixed frequency of 2.2MHz. The topology benefits lower output voltage ripple, fast load and line transient with a compact solution size.

The three buck converters have an independent internal soft start circuit. The soft-start circuit monotonically increases the output voltage and reaches the nominal output voltage at the specified ramp time. This feature creates a smooth output voltage slope, avoiding output voltage overshoot and excessive surge current

Meanwhile, the device adopts a spread-spectrum function with phase-shifted to optimize EMI performance. The spread spectrum range is ±6% of the switching frequency. With this feature, the switching frequency of the device varies from 2MHz to 2.4MHz (Max.) and does not drop into the 1.8MHz AM band limit. The phase shift scheme among the three buck converters avoids the simultaneous switching energy radiation.

All the buck converters integrate power switches. The high voltage buck converter (HVBuck1) integrates an NMOS for the high-side power switch, while the low-voltage buck converters (LVBuck1&2) adopt PMOS for its high-side power switch. A 100nF bootstrap capacitor is needed between the BT and SW pin to drive the high-side NMOS of HVBuck1. All the low-side power switches adopt NMOS and are driven by the internal VCC.

The HVBuck1 acts as a primary regulator and provides its output voltage VO1 as the input power source of secondary LVBuck and LDO.

The output voltage of the three-buck converters can be configured by writing to internal registers via the I2C interface.

All the buck converters have a separate output discharge path to the ground, and the discharge patch activates automatically when the corresponding converter is disabled.

10.2 LDO Regulator

The LDO regulator is designed to meet the requirements of sensitive analog circuits, it can provide a low noise output with drive capacity up to 400 ma, and high PSRR performance can suppress the input ripple from VO1 effectively. To decrease the impact of switching noise from the buck converters, the LDO regulator has a dedicated input voltage pin that can be tied to the output of the HVBuck1 independently.

The LDO regulator has an independent internal soft-start circuit. The soft-start circuit monotonically increases the output voltage and reaches the nominal output voltage at the specified ramp time. This feature creates a smooth output voltage slope, avoiding output voltage overshoot and excessive surge current.

The output voltage of LDO regulator can be adjusted by configuring internal register via I2C interface. The LDO regulator can be configured in "bypass mode" to operate as a load switch.

The LDO regulator has a separate output discharge resistor to the ground, and the discharge resistor activates automatically when the regulator is disabled

10.3 Power ON/OFF Sequence Control

The SC6206Q features a one-time programmable power-on sequence. The delayed start times for the BUCK2, BUCK3, and LDO converters are determined based on BUCK1 reaching 90% of its target output voltage. Additionally, the shutdown sequence will close all four output at the same time. The commonly optional power-on sequences are as follows (*For more power-on sequences, please contact South Chip sales)

Option1:
BUCK1-> LDO (1.8ms typ.)-> BUCK2(2.8ms typ.)-> BUCK3(4.8ms typ.)-> GPO (20.8ms typ.)

Option2:
BUCK1-> BUCK3(1.8ms typ.)-> LDO (2.8ms typ.)-> Buck2(3.8ms typ.)-> GPO (4.8ms typ.)

10.4 SEQ pin

The SEQ pin serves as a control interface for initiating the power-on or power-off sequence. Setting this pin to a high

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logic level triggers the power-on sequence, while pulling it low disables all outputs.

The SEQ pin can be directly connected to the input voltage to enable the device. Additionally, the device offers a factory-programmable option that latches the state of the SEQ pin. When this feature is enabled, the internal SEQ signal is automatically set to a high logic level upon application of power to the VSYS pin, thereby initiating the power-on sequence.

10.5 nRSTOUT pin

The nRSTOUT pin can be used to reset the rear stage system until the desired voltage rail is activated. The nRSTOUT pin state is part of the power on sequence and is pulled up at a fixed time after buck1 PG (90% output voltage of the BUCK1).

nRSTOUT pin can be configured as a push-pull or open drain through register. As an open drain output, the pull-up resistor (10kΩ typ.) is integrated as part of the device, and the pull-up voltage comes from the VIO pin

10.6 nINT pin

The nINT output is used as an interrupt signal indicating when the fault occurred. The I2C bus can be used to query the device to determine the exact type of fault.

nINT pin can be configured as a push-pull or open drain through register. As an open drain output, the pull-up resistor (10kΩ typ.) is integrated as part of the device, and the pull-up voltage comes from the VIO pin

10.7 General Purpose Output (GPO) pin

The GPO output status is part of the power-on sequence and can be used to enable an external power rail or keep it floating. This pin is an open drain output, the pull-up resistor (10kΩ type) is integrated as part of the device, and the pull-up voltage comes from the VIO pin.

10.8 VIO Pin

VIO pin provides pull-up level for nRSTOUT, nINT, and GPO pins. Typically, the VIO input power is provided by one of the four power rails. For external power supply, VIO needs to be powered up before the nRSTOUT pull up.

10.9 Safety Description

10.9.1 Overview

The SC6206Q meets the requirements of the ASIL-B functional safety class and is suitable for automotive applications with functional safety requirements. The following list of functions is implemented.

- Voltage monitoring on all regulator outputs
- Regulator current limit
- Loss-of-ground monitoring
- Temperature monitoring
- Analog built-in self-tests
- Output error monitor on nRSTOUT pin and nINT pin
- Cyclic Redundancy Check (CRC) on Device Efuse value
- Cyclic Redundancy Check (CRC) on Device Configuration Registers
- CRC on I2C Interface

10.9.2 Device State Controller

The SC6206Q has five built-in state machines to control device transitions from different states.

The SC6206Q nRSTOUT and nINT pins output levels can be used to indicate state machine status. The current state machine can also be read via register DEV_STATE (0x2A [1:0])

	ACTIVE STATE	SAFE STATE	RESET STATE	OFF STATE	WT_PWR_RST STATE
nRST OUT	H	H	L	L	L
nINT	H	L	H	H	H
DEV_ STATE	1	3	2	0	0

ACTIVE STATE

- All enabled voltage regulator outputs are powered on in sequence
- nRESET pin pull high
- nINT pin pull high
- DEV_STATE (0x2A [1:0]) = 1

ACTIVE STATE Entry:

All faults are cleared

ACTIVE STATE Exit:

Any fault is triggered

SAFE STATE

- All enabled voltage regulator outputs remain on
- nRESET pin pull high

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• nINT pin pull low

• DEV_STATE (0x2A [1:0]) = 3

SAFE STATE Entry:

Triger priority 3 fault (The corresponding fault types of MASK register configuration of 0 or the corresponding fault types of RST_EN registers configuration is 0)

SAFE STATE Exit:

Priority 3 faults status are cleared, the device transitions to the ACTIVE State

RESET STATE

• All regulator outputs are off

• nRESET pin pull low

• nINT pin pull high

• DEV_STATE (0x2A [1:0]) = 2

• Reset priority 3 fault ACK register status to 0

RESET STATE Entry:

Triger priority 2 fault and STAT_TRANSITION (0x06 [6]) = 0

RESET STATE Exit:

The device transitions from the RESET State to the ACTIVE State.

•Tj < WARM threshold (WARM_THR_STARTUP_CTRL bit =0) or Tj < HOT threshold (WARM_THR_STARTUP_CTRL bit = 1)

• PVIN1 > PVIN1_UVLO rising threshold

• VO1 > 90% Vref1

• nRSTOUT_ERR = 0

OFF STATE

• All regulator outputs are off

• nRESET pin pull low

• nINT pin pull high

• DEV_STATE (0x2A [1:0]) = 0

OFF STATE Entry:

Triger priority 1 fault

OFF STATE Exit:

The device transitions from the OFF State to the RESET State if VSYS and VSYS_S exceed the VSYSUVLO_R threshold.

WT_PWR_RST STATE

• All regulator outputs are off

• nRESET pin pull low

• nINT pin pull high

• DEV_STATE (0x2A [1:0]) = 2

WT_PWR_RST STATE Entry:

Triger priority 2 fault and STAT_TRANSITION (0x06 [6]) = 1

WT_PWR_RST STATE Exit:

VSYS and VSYS_S voltage must be reduced below UVLO threshold to enter the OFF STATE

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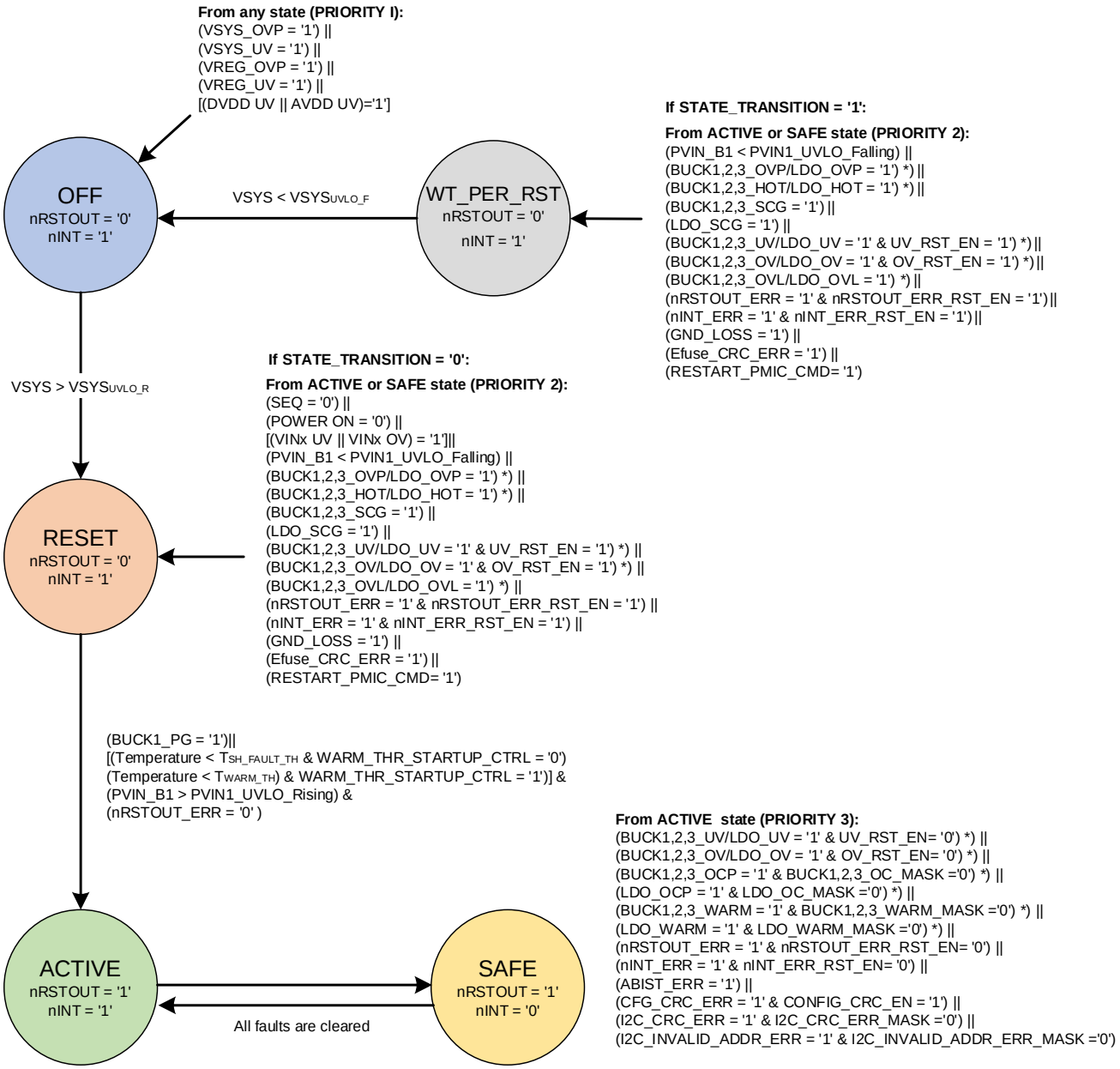

Note:

(1) applicable to enabled rails only

(2) the state of the nINT pin and nRSTOUT pin is also dependent on fault-conditions and VIO-supply

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10.9.3 Voltage Monitoring (VMON)

The SC6206Q contains two separate references inside, one for regulating the circuit and the other for monitoring the circuit to ensure that the voltage monitor is not affected by the voltage regulator. All internal voltage regulators and reference regulation and monitoring circuits are powered by VSYS pins and VSYS_S pins, respectively.

The SC6206Q monitors input supply voltage undervoltage and overvoltage events. If VSYS and VSYS_S or PVIN2/3/4 overvoltage or undervoltage is detected, the device turns off all voltage regulators and enters the RESET STATE.

All three switching regulators and linear regulator outputs have undervoltage (UV), overvoltage (OV) and overvoltage protection (OVP) monitoring.

If the output voltage exceeds the OV threshold (register configurable) of the output voltage, the device enters SAFE STATE, or RESET STAT, or WT_PWR_RST STATE (depending on OV_RST_EN and STATE_TRANSITION setting). For example, If the output voltage exceeds the configurable OV threshold relative to the configured output voltage and OV_RST_EN='0', the device enters the SAFE state and forces the nINT pin to pull down and corresponding _OV_ACK set '1', the MCU must clear this bit by writing '1' to the corresponding _OV_ACK error bit.

The output undervoltage monitoring function is similar to that of overvoltage. If the output voltage is lower than the UV threshold (register configurable) of the output voltage, the device enters either SAFE STATE, RESET STAT, or WT_PWR_RST STATE (depending on OV_RST_EN and STATE_TRANSITION setting).

The output overvoltage protection monitoring threshold is fixed at 115%*Vref. When any output rail exceeds the OVP threshold, the device enters the RESET STAT or WT_PWR_RST (depending on STATE_TRANSITION setting), and the corresponding _OVP_STATUS register is set to 1, he MCU must clear this bit by writing '1' to the corresponding _OVP_STATUS error bit.

10.9.4 Regulator current limit

All regulators include a current limiting circuit to protect the internal power MOSFETs.

When an overcurrent event occurs, each current limiting circuit limits the output current of its own regulator and sets the corresponding status bit (BUCKx_OCP_ACK or LDO_OCP_ACK). If the corresponding _OCP_MASK bit is set to '0', the device switches to the SAFE state and pulls down nINT pin. The MCU must clear this bit by writing '1' to the corresponding _OCP_ACK bit.

10.9.5 Short Circuit to Ground (SCG) detection

All regulators include ground short circuit detection.

If the output voltage is lower than the threshold voltage defined by VBUCKx_SCG or LDO_SCG, then the corresponding status bit (BUCKx_SCG_STATUS or LDO_SCG_STATUS) is set. The device transitions to the REST state or WT_PWR_RST state (depending on the STATE_TRANSITION bit setting) and the nRSTOUT pull down. If the fault no longer exists, the MCU can clear the bit by writing '1' to the corresponding error bit.

10.9.6 Overload Fault Detection

All regulators include overload detection.

The overload state is defined as a combination of overcurrent and undervoltage. If an overload occurs, the device sets the appropriate state bit (BUCKx_OVL_STATUS or LDO_OVL_STATUS) and transitions to the REST state or WT_PWR_RST state (depending on the STATE_TRANSITION bit setting). Then pull down the nRSTOUT pin. If the fault no longer exists, the MCU can clear that bit by writing '1' to the corresponding error bit.

10.9.7 Ground Loss monitoring

All regulators include ground loss detection.

The ground loss detection circuit monitors the voltage difference between analog ground and digital ground. If the difference exceeds the defined voltage threshold, then the device shuts down all regulators and enters the REST state or WT_PWR_REC state (depending on the STATE_TRANSITION bit setting), and pull down nRSTOUT pin. If the fault no longer exists, the MCU can clear this bit by writing '1' to the GND_LOSS_ERR_STATUS bit.

10.9.8 Temperature Monitoring

All regulators include a temperature monitor.

Each monitor has a warning threshold and a hot threshold and contains separate register status bits. When the temperature rises above the defined level, the device will set the corresponding _WARM_ACK status bit to '1', and pull down nINT pin to alert the external MCU and transition to the SAFE state. The MCU must clear this bit by writing '1' to the corresponding _WARM_ACK bit.

If the temperature continues to rise beyond the temperature defined by HOT, the device shuts down all regulators and transitions to the REST state or WT_PWR_RST state (depending on the STATE_TRANSITION bit setting), and sets the corresponding _HOT_STATUS bit. Then pull down nRSTOUT pin. If the fault no longer exists, the MCU can

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clear this bit by writing ‘1’ to the corresponding _HOT_STATUS bit.

10.9.9 Output Error Monitor on nINT and nRSTOUT pin

Both nINT and nRSTOUT pins have error detection capabilities. If the device detects that the nINT or nRSTOUT output level is inconsistent with the expected output level, an error is triggered. The state machine then enters either SAFE STATE or RESET STATE or WT_PWR_RST STATE (depending on the configuration of _ERR_RST_EN and STATE_TRANSITION bits).

10.9.10 Restart PMIC Command

The device provides a software-controlled reset path. Users can restart the device by writing ‘1’ to the RESTART_CMD register through the IIC interface. After the reset, the RESTART_CMD_STATUS bit is set, indicating that the previous restart was due to the MCU restart command. The MCU can clear this bit by writing '1' to the RESTART_CMD_STATUS bit.

10.9.11 Device Control Registers

The device’s control registers contain a write access restriction function. Users need to unlock write access restrictions by writing '0xDD' to the CONTROL_ACCESS_CMD register before change control register values. Control registers access will be reset when the RESET state is entered.

10.9.12 Device Configuration Register Access Control

The device’s configuration registers contain a write access restriction function. Users need to unlock write access restrictions by writing '0xAA' to the CONFIG_ACCESS_CMD register before change configuration register values. Configuration registers access will be reset when the RESET state is entered.

10.9.13 CRC on Device Configuration Registers

The device configuration registers are protected by CRC. The CRC controller calculates the checksum value of the actual configuration register values. The CRC controller then compares this checksum value to what the MCU writes to the DEV_CFG_CRC register. If the CRC controller detects a checksum error, it will set the CFG_REG_CRC_ERR_ACK bit and enter the SAFE state. To exit the SAFE state, the MCU must writing ‘1’ to the CFG_REG_CRC_ERR_ACK bit.

Configuration registers overwrite flow summary

(1) Read the initial value of the configuration registers

(2) Disable the configuration registers CRC check (0x04[2] = 0)

(3) Overwrite the configuration registers value

(4) Calculate the checksum value of all configuration registers and write to DEV_CFG_CRC register (0x29)

(5) Enable the configuration registers CRC check (0x04[2] = 1)

The CRC controller adopts CRC-8 polynomial to calculate checksum-value, which is X8 + X2 + X1 + 1, and initial value is 0xFF.

The configuration registers (CRC protection registers) are as follows:

#	Register	Address
1	LDO_SYS_CFG	0x06
2	BUCK1_VOUT	0x07
3	RESERVED	0x08
4	BUCK2_VOUT	0x09
5	BUCK3_VOUT	0x0A
6	LDO_VOUT	0x0B
7	RESERVED	0x0C
8	RESERVED	0x0D
9	RESERVED	0x0E
10	RESERVED	0x0F
11	RESERVED	0x10
12	RESERVED	0x11
13	RESERVED	0x12
14	BUCK1_DLY	0x13
15	BUCK2_DLY	0x14
16	BUCK3_DLY	0x15
17	LDO_DLY	0x16
18	nRESET_DLY	0x17
19	GPO_DLY	0x18
20	INT_MASK_BUCKx_LDO	0x1E
21	VMON_BUCK1_CFG	0x23
22	VMON_BUCK2_CFG	0x24
23	VMON_BUCK3_CFG	0x25
24	VMON_LDO_CFG	0x26
25	ERR_BUCKx_LDO_CFG	0x27
26	INT MASK SAFETY	0x2F
27	PIN_MON_ERR_CFG	0x30

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10.9.14 I2C Serial Interface

The device integrates a standard I2C interface, allowing users to access and overwrite internal registers through the 7-bit device address 1100000b.

If users attempt to access a register address does not exist, the device will detect it and enter SAFE state, pull down nINT pin and set the I2C_INVALID_ADDR_ACK bit (I2C_INVALID_ADDR_MASK=0). The users can clear this bit by writing '1' to the I2C_INVALID_ADDR_ACK bit.

10.9.15 I2C CRC Calculations

The device I2C interface supports read and write protocols with embedded CRC data fields. Both master and slave devices use CRC-8 polynomials to calculate checksum values: X8 + X2 + X + 1, and initial value is 0xFF.

During the write protocol, the device uses this polynomial to calculate the checksum value for each bit except the ACK and NACK bits received from the MCU. The device compares the calculated checksum with the MCRC checksum value received by the device from the MCU. If the two CRC checksum value do not match, the device will enter SAFE state, pull down nINT pin and set the I2C_CRC_ERR_ACK bit (I2C_CRC_ERR _MASK=0). The MCU can clear this bit by writing '1' to the I2C_CRC_ERR_ACK bit.

During the read protocol, the device also uses this polynomial to compute the SCRC checksum value based on each bit except the ACK and NACK bits, which the device transmits to the MCU. The MCU must use the same polynomial to calculate the checksum value based on the bits the MCU receives from the device. The MCU must compare the calculated checksum with the SCRC checksum value received from the device.

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11 Application Curves

PVIN1=9V, V_{O1}=3.8V, V_{O2}=1.8V, V_{O3}=1.1V, V_{O4}=3.3V, unless otherwise noted

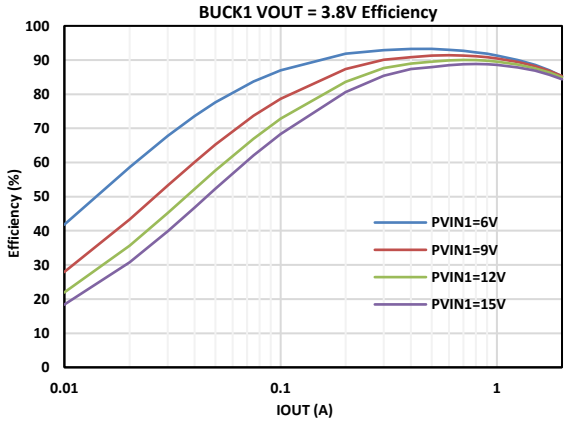

Figure 11-1, BUCK1 Efficiency

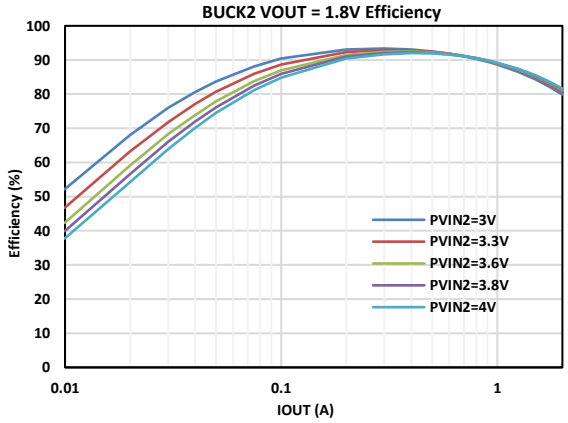

Figure 11-2, BUCK2 Efficiency

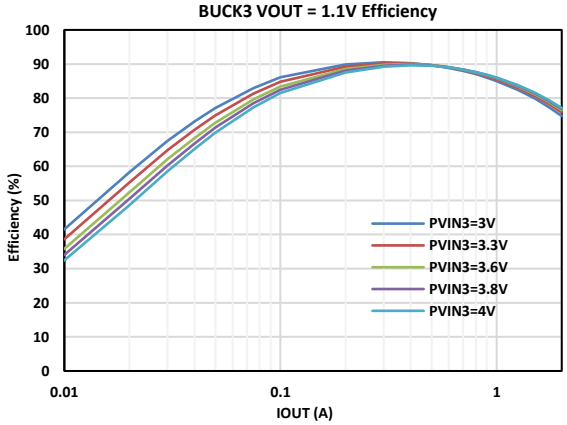

Figure 11-3, BUCK3 Efficiency

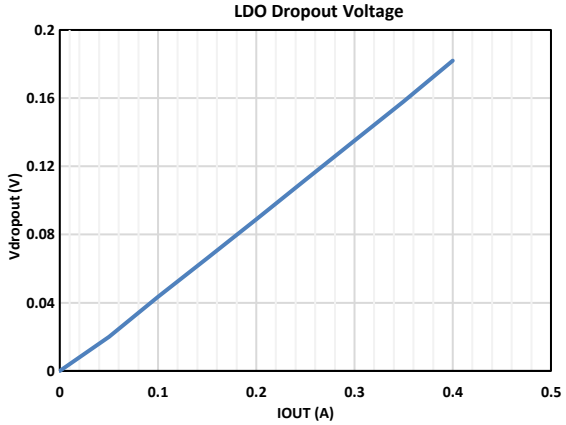

Figure 11-4, LDO Dropout Voltage

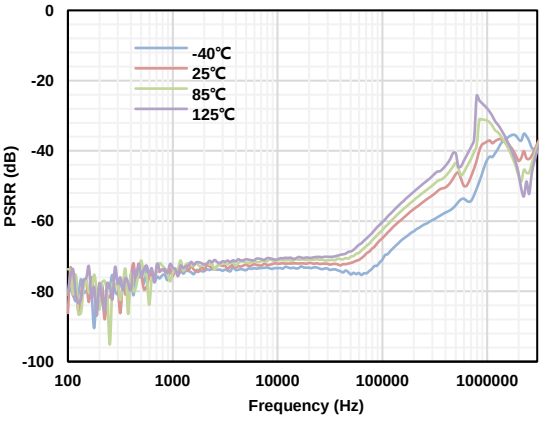

Figure 11-5, LDO PSRR, LDOIN=3.8V, LDO=3.3V, IO4=300mA

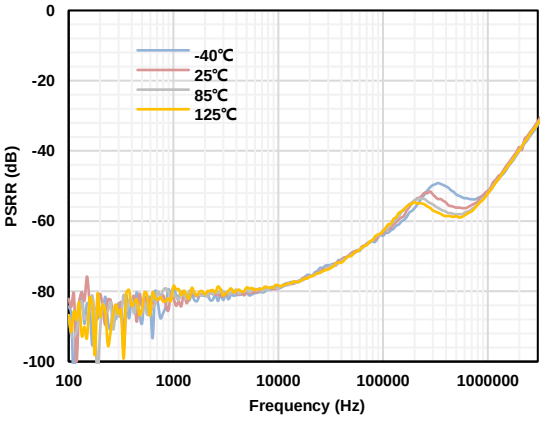

Figure 11-6, LDO PSRR, LDOIN=3.8V, LDO=3.3V, IO4=1mA

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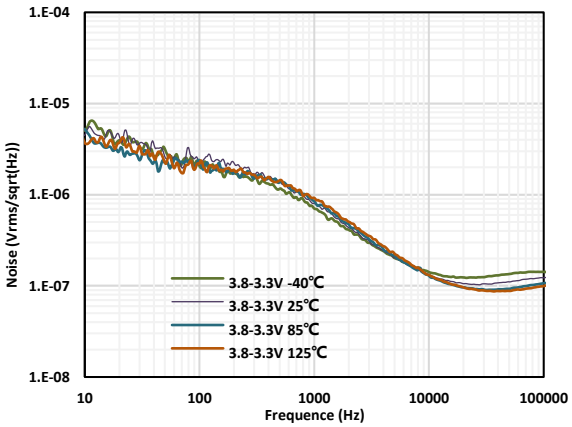

Figure11-7, LDO Output Noise, IO4=300mA

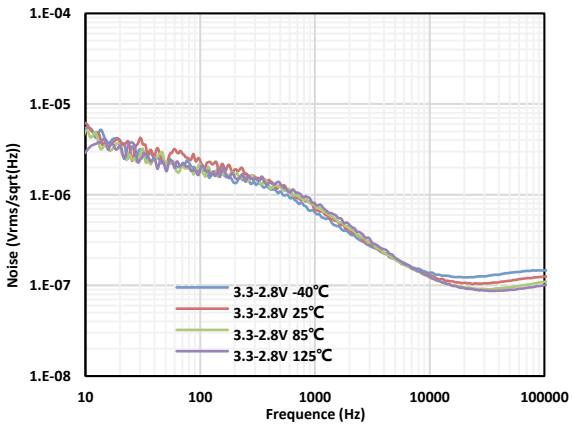

Figure11-8, LDO Output Noise, IO4=300mA

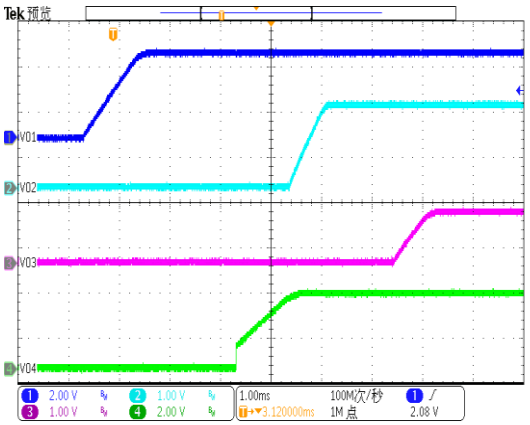

Figure 11-9, Option1 Power ON Sequence

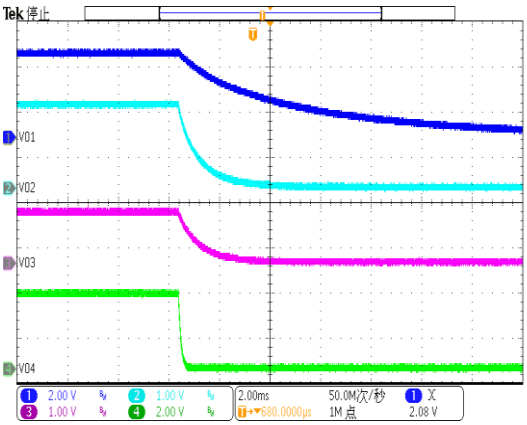

Figure 11-10, Option1 Power OFF Sequence

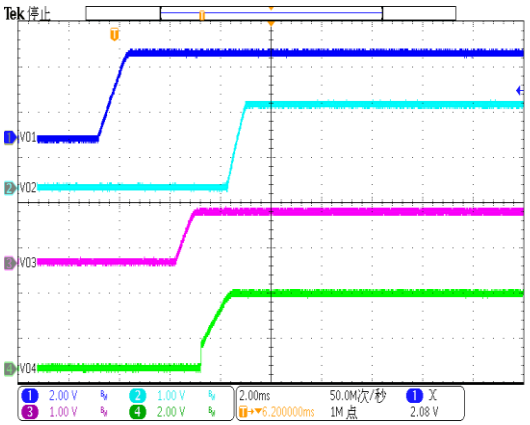

Figure 11-11, Option2 Power ON Sequence

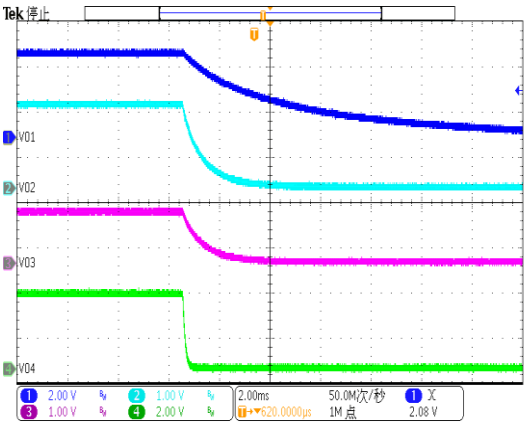

Figure 11-12, Option2 Power OFF Sequence

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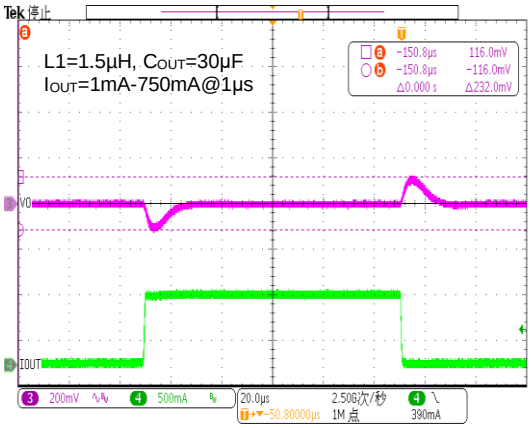

Figure 11-13, BUCK1 Load Transient

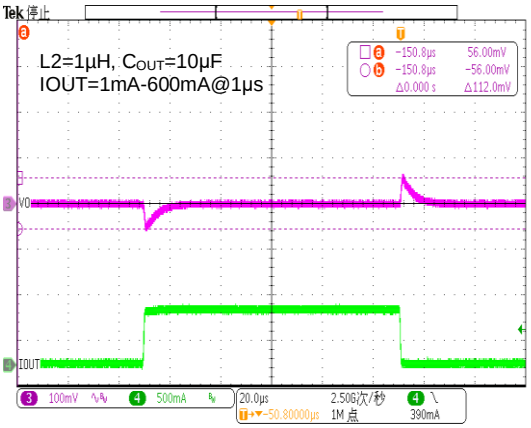

Figure 11-14, BUCK2 Load Transient

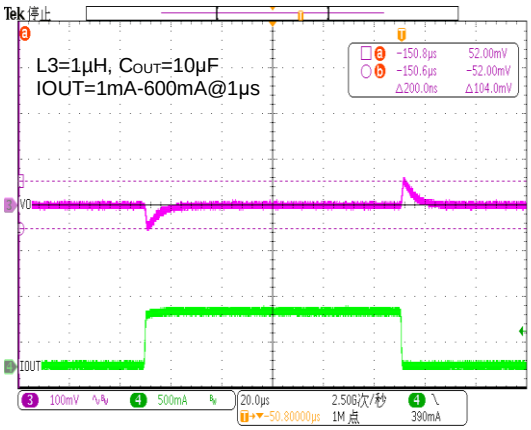

Figure 11-15, BUCK3 Load Transient

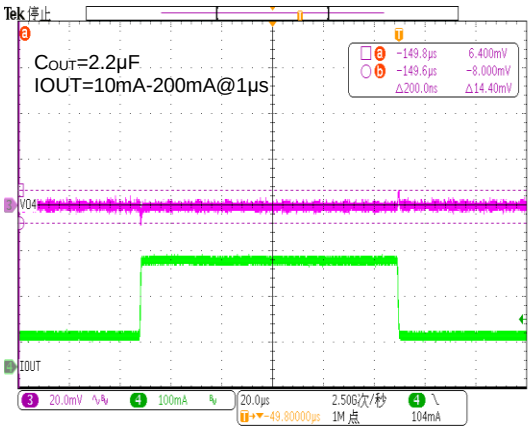

Figure 11-16, LDO Load Transient

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12 Layout Guide

12.1 PCB Layout Guide

The PCB layout should be carefully designed for best performance to avoid instability, switching noise interference, and EMI issues. Minimizing the area of alternating current and voltage loops in the layout helps reduce EMI.

Here are some guidelines for reference:

1) The PVIN1, PVIN2, PVIN3 and PVIN4 pins must each be bypassed to the PGND with a low-ESR ceramic bypass capacitor. Use the typical bypass capacitance of 10μF for the DC-DC converters and 2.2μF for the LDO with an X7R dielectric. The optimum capacitor placement is closest to the PVINx pins of the device. Minimize the loop area formed by the bypass capacitor connection from the PVINx and the thermal pad of the device. Minimize the loop area formed by the bypass capacitor connection from the PVIN4 and the AGND pin of the device.

2) The FB pin feedback traces must be routed away from any potential noise source to avoid coupling.

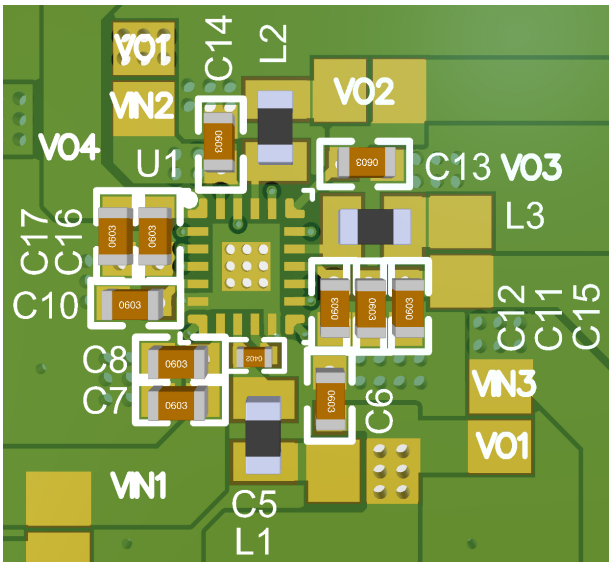
3) The optimum placement of the VCC and LDOOUT output capacitors is directly at their respective pins. Excessive input and output capacitor distances for regulator pins may cause poor converter performance.

4) Minimize the loop area of the bootstrap capacitor from the LX1 to the BT pin.

5) Connect the AGND and PGND to a strong ground plane for better noise and thermal performance.

6) The thermal pad must be tied to the PCB ground plane with multiple vias.

12.2 Layout Example



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13 Register Maps

The 7-bit I2C address of the chip is 0x60H.

ADD (HEX)	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	CONTROL LOCK	CONTROL_ACCESS_CMD							
0x03	BUCK_LDO_CTRL	RESERVED			SPREAD SPECTRUM	ENABLE_BUCK3	ENABLE_BUCK2	ENABLE_BUCK1	ENABLE_LDO
0x04	SYS_CTRL	RESERVED				WARM_THR_STARTUP_CTRL	CONFIG_CRC_EN	PWR_ON	RESERVED
0x05	CONFIG_LOCK	CONFIG_ACCESS_CMD							
0x06	LDO_SYS_CFG	RESERVED	STATE_TRANSITION	RESERVED	nRESET_PIN_CONFIG	nINT_PIN_CONFIG	RESERVED	LDO_BYP_EN	RESERVED
0x07	BUCK1_VOUT	RESERVED			BUCK1_VOUT				
0x09	BUCK2_VOUT	RESERVED			BUCK2_VOUT				
0x0A	BUCK3_VOUT	RESERVED			BUCK3_VOUT				
0x0B	LDO_VOUT	RESERVED			LDO_VOUT				
0x13	BUCK1_DLY_ON	RESERVED				BUCK1_DLY_ON			
0x14	BUCK2_DLY_ON	RESERVED				BUCK2_DLY_ON			
0x15	BUCK3_DLY_ON	RESERVED				BUCK3_DLY_ON			
0x16	LDO_DLY_ON	RESERVED				LDO_DLY_ON			
0x17	nRESET_DLY	RESERVED				nRESET_DLY			
0x18	GPO_DLY	RESERVED				GPO_DLY			
0x19	INT_ACK	RESERVED				BUCK3_ACK	BUCK2_ACK	BUCK1_ACK	LDO_ACK
0x1A	INT_ACK_BUCK1	RESERVED				BUCK1_OV_ACK	BUCK1_UV_ACK	BUCK1_OCP_ACK	BUCK1_WARM_ACK
0x1B	INT_ACK_BUCK2	RESERVED				BUCK2_OV_ACK	BUCK2_UV_ACK	BUCK2_OCP_ACK	BUCK2_WARM_ACK
0x1C	INT_ACK_BUCK3	RESERVED				BUCK3_OV_ACK	BUCK3_UV_ACK	BUCK3_OCP_ACK	BUCK3_WARM_ACK

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ADD (HEX)	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1D	INT_ACK_LDO	RESERVED				LDO_OV_ACK	LDO_UV_ACK	LDO_OCP_ACK	LDO_WARM_ACK
0x1E	INT_MASK	BUCK3_OCP_MASK	BUCK3_WARM_MASK	BUCK2_OCP_MASK	BUCK2_WARM_MASK	BUCK1_OCP_MASK	BUCK1_WARM_MASK	LDO_OCP_MASK	LDO_WARM_MASK
0x1F	FAULT_STATUS_BUCK1	RESERVED	PVIN1_UVLO_STATUS	BUCK1_OV_STATUS	BUCK1_HOT_STATUS	BUCK1_OVP_STATUS	BUCK1_SCG_STATUS	BUCK1_OVL_STATUS	BUCK1_UV_STATUS
0x20	FAULT_STATUS_BUCK2	RESERVED	PVIN2_UVLO_STATUS	BUCK2_OV_STATUS	BUCK2_HOT_STATUS	BUCK2_OVP_STATUS	BUCK2_SCG_STATUS	BUCK2_OVL_STATUS	BUCK2_UV_STATUS
0x21	FAULT_STATUS_BUCK3	RESERVED	PVIN3_UVLO_STATUS	BUCK3_OV_STATUS	BUCK3_HOT_STATUS	BUCK3_OVP_STATUS	BUCK3_SCG_STATUS	BUCK3_OVL_STATUS	BUCK3_UV_STATUS
0x22	FAULT_STATUS_LDO	RESERVED	PVIN4_UVLO_STATUS	LDO_OV_STATUS	LDO_HOT_STATUS	LDO_OVP_STATUS	LDO_SCG_STATUS	LDO_OVL_STATUS	LDO_UV_STATUS
0x23	VMON_BUCK1_CFG	RESERVED				BUCK1_OV_SET		BUCK1_UV_SET	
0x24	VMON_BUCK2_CFG	RESERVED				BUCK2_OV_SET		BUCK2_UV_SET	
0x25	VMON_BUCK3_CFG	RESERVED				BUCK3_OV_SET		BUCK3_UV_SET	
0x26	VMON_LDO_CFG	RESERVED				LDO_OV_SET		LDO_UV_SET	
0x27	ERR_BUCKx_LDO_CFG	BUCK3_OV_RST_EN	BUCK3_UV_RST_EN	BUCK2_OV_RST_EN	BUCK2_UV_RST_EN	BUCK1_OV_RST_EN	BUCK1_UV_RST_EN	LDO_OV_RST_EN	LDO_UV_RST_EN
0x28	RESTART_CMD	PMIC_RESTART_CMD							
0x29	CFG_REG_CRC	DEV_CFG_CRC							
0x2A	DEV_STAT	RESERVED				CTRL_LOCK	CFG_LOCK	DEV_STATE	
0x2B	DEV_ERR_ACK_1	RESERVED			SYSTEM_ERR_ACK	ABIST_LDO_ACK	ABIST_BUCK3_ACK	ABIST_BUCK2_ACK	ABIST_BUCK1_ACK
0x2C	DEV_ERR_ACK_2	RESERVED			CFG_REG_CRC_ERR_ACK	nINT_ERR_ACK	nRESET_ERR_ACK	I2C_INVALID_ADDR_ERR_ACK	I2C_CRC_ERR_ACK
0x2D	DEV_FAULT STATUS_1	RESERVED			SYS_HOT_STATUS	SYS_WARM_STATUS	RESTART_CMD_STATUS	RESERVED	
0x2E	DEV_FAULT STATUS_2	RESERVED		GPO_ERR_STATUS	nINT_ERR_STATUS	nRESET_ERR_STATUS	EFUSE_CRC_ERR_STATUS	RESERVED	GND_LOSS_ERR_STATUS
0x2F	INT MASK SAFETY	RESERVED						I2C_INVALID_ADDR_MASK	I2C_CRC_ERR_MASK
0x30	PIN_MON_ERR_CFG	RESERVED						nINT_ERR_RST_EN	nRESET_ERR_RST_EN

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ADD (HEX)	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x31	ABIST_GROUP_DONE	RESERVED			ABIST_SYS	ABIST_LDO	ABIST_BUCK3	ABIST_BUCK2	ABIST_BUCK1
0x32	ABIST_BUCK1 BUCK2 ACK	ABIST_BUCK2_HOT_ACK	ABIST_BUCK2_OVP_ACK	ABIST_BUCK2_OV_ACK	ABIST_BUCK2_UV_ACK	ABIST_BUCK1_HOT_ACK	ABIST_BUCK1_OVP_ACK	ABIST_BUCK1_OV_ACK	ABIST_BUCK1_UV_ACK
0x33	ABIST_LDO BUCK3 ACK	ABIST_LDO_HOT_ACK	ABIST_LDO_OVP_ACK	ABIST_LDO_OV_ACK	ABIST_LDO_UV_ACK	ABIST_BUCK3_HOT_ACK	ABIST_BUCK3_OVP_ACK	ABIST_BUCK3_OV_ACK	ABIST_BUCK3_UV_ACK
0x34	ABIST_SYSTEM_ACK	RESERVED	ABIST_LDO_WARM_ACK	ABIST_BUCK3_WARM_ACK	ABIST_BUCK2_WARM_ACK	ABIST_BUCK1_WARM_ACK	ABIST_SYSTEM_TSD_ACK	RESERVED	ABIST_GNDLOSS_ERR_ACK
0x36	POWER_GOOD_STATUS	nINT_STATUS	nRESET_STATUS	GPO_STATUS	SEQ_STATUS	LDO_PG_STATUS	BUCK3_PG_STATUS	BUCK2_PG_STATUS	BUCK1_PG_STATUS
0x37	BUCKX_SSEND	RESERVED	LDO_VIN_OVP	BUCK3_VIN_OVP	BUCK2_VIN_OVP	VSYS_OVP	BUCK1_SSEND	BUCK2_SSEND	BUCK3_SSEND

Note: All *registers are OTP programmable

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Address 0x02H: CONTROL LOCK

Bit	Type	Bit Name	Default	Description
7:0	R/W	CONTROL_ACCESS_CMD	0h	Write to this to either lock or unlock the control registers. A readback of this result in '0x00'. 0h = Locks the control registers DDh = Unlocks the control registers

Address 0x03H: BUCK_LDO_CTRL

Bit	Type	Bit Name	Default	Description
7:5	R	RESERVED	0h	RESERVED
4	R/W	SPREAD_SPECTRUM	1h	Spread Spectrum Enable 0h = Disabled 1h = Enabled
3	R/W	ENABLE_BUCK3	1h	BUCK3 enable bit 0h = Disabled 1h = Enabled
2	R/W	ENABLE_BUCK2	1h	BUCK2 enable bit 0h = Disabled 1h = Enabled.
1	R/W	ENABLE_BUCK1	1h	BUCK1 enable bit 0h = Disabled 1h = Enabled
0	R/W	ENABLE_LDO	1h	LDO1 enable bit 0h = Disabled 1h = Enabled

Address 0x04H: SYS_CTRL

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3	R/W	WARM_THR_STARTUP _CTRL	1h	WARM_THR_STARTUP_CTRL 0h = Device powers up if temperature is above the warm threshold setting but below the over temperature setting 1h = Device does not power up until the temperature is below the warm threshold setting
2	R/W	CONFIG_CRC_EN	1h	Config CRC Enable 0h = Disabled 1h = Enabled
1	R/W	PWR_ON	1h	Power up/down control 0h = Device powers off 1h = Device powers on
0	R	RESERVED	0h	RESERVED

Address 0x05H: CONFIG_LOCK

Bit	Type	Bit Name	Default	Description
7:0	R/W	CONFIG_ACCESS_CMD	0h	Write to this register to either lock or unlock the configuration registers. A readback of this register results in '0x00'. 0h = Locks the Configuration Registers AAh = Unlocks the Configuration Registers

Address 0x06H: LDO_SYS_CFG

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	R/W	STATE_TRANSITION	0h	State Transition for Priority 2 Faults 0h = Priority 2 faults transition to the RESET state 1h = Priority 2 faults transition to the WAIT_PWR_CYCLE state

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5	R	RESERVED	0h	RESERVED
4	R/W	nRESET_PIN_CONFIG	0h	nRESET PIN Configuration 0h = Open-drain 1h = Push-pull
3	R/W	nINT_PIN_CONFIG	0h	nINT PIN Configuration 0h = Open-drain 1h = Push-pull
2	R	RESERVED	0h	RESERVED
1	R/W	LDO_BYP_EN	0h	LDO bypass enable bit: 0h = LDO operation (default) 1h = Bypass mode operation (Load switch operation)
0	R	RESERVED	0h	RESERVED

Address 0x07H: BUCK1_VOUT

Bit	Type	Bit Name	Default	Description
7:5	R	RESERVED	0h	RESERVED
4:0	R/W	BUCK1_VOUT	Depends on part number	The output voltage range is from 2.5V to 4.0V in increments of 50mV: 0h = 2.50V 1h = 2.55V 2h = 2.60V 3h = 2.65V 4h = 2.70V 5h = 2.75V 6h = 2.80V 7h = 2.85V 8h = 2.90V 9h = 2.95V Ah = 3.00V Bh = 3.05V Ch = 3.10V Dh = 3.15V Eh = 3.20V Fh = 3.25V 10h = 3.30V 11h = 3.35V 12h = 3.40V 13h = 3.45V 14h = 3.50V 15h = 3.55V 16h = 3.60V 17h = 3.65V 18h = 3.70V 19h = 3.75V 1Ah = 3.80V 1Bh = 3.85V 1Ch = 3.90V 1Dh = 3.95V 1Eh = 4.00V 1Fh = 4.00V

Address 0x09H: BUCK2_VOUT

Bit	Type	Bit Name	Default	Description
7:5	R	RESERVED	0h	RESERVED
4:0	R/W	BUCK2_VOUT	Depends on part number	The output voltage range is from 0.8V to 1.9V: 0h = 0.8V 1h = 0.85V 2h = 1.000V 3h = 1.025V 4h = 1.050V

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				5h = 1.075V 6h = 1.100V 7h = 1.125V 8h = 1.150V 9h = 1.175V Ah = 1.200V Bh = 1.225V Ch = 1.250V Dh = 1.275V Eh = 1.300V Fh = 2.500V 10h = 1.350V 11h = 1.375V 12h = 1.400V 13h = 1.425V 14h = 1.450V 15h = 1.475V 16h = 1.500V 17h = 1.525V 18h = 1.550V 19h = 1.575V 1Ah = 1.600V 1Bh = 1.700V 1Ch = 1.750V 1Dh = 1.800V 1Eh = 1.850V 1Fh = 1.900V

Address 0x0AH: BUCK3_VOUT

Bit	Type	Bit Name	Default	Description
7:5	R	RESERVED	0h	RESERVED
4:0	R/W	BUCK3_VOUT	Depends on part number	The output voltage range is from 0.9V to 1.9V: 0h = 0.9V 1h = 0.95V 2h = 1.000V 3h = 1.025V 4h = 1.050V 5h = 1.075V 6h = 1.100V 7h = 1.125V 8h = 1.150V 9h = 1.175V Ah = 1.200V Bh = 1.225V Ch = 1.250V Dh = 1.275V Eh = 1.300V Fh = 1.325V 10h = 2.500V 11h = 1.375V 12h = 1.400V 13h = 1.425V 14h = 1.450V 15h = 1.475V 16h = 1.500V 17h = 1.525V 18h = 1.550V

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				19h = 1.575V 1Ah = 1.600V 1Bh = 1.700V 1Ch = 1.750V 1Dh = 1.800V 1Eh = 1.850V 1Fh = 1.900V

Address 0x0BH: BUCK3_VOUT

Bit	Type	Bit Name	Default	Description
7:5	R	RESERVED	0h	RESERVED
4:0	R/W	LDO_VOUT	Depends on part number	The output voltage range is from 1.8V to 3.3V: 0h = 1.800V 1h = 1.825V 2h = 2.500V 3h = 2.525V 4h = 2.550V 5h = 2.575V 6h = 2.600V 7h = 2.625V 8h = 2.650V 9h = 2.675V Ah = 2.700V Bh = 2.725V Ch = 2.750V Dh = 2.775V Eh = 2.800V Fh = 2.825V 10h = 2.850V 11h = 2.875V 12h = 2.900V 13h = 2.925V 14h = 2.950V 15h = 2.975V 16h = 3.000V 17h = 3.025V 18h = 3.050V 19h = 3.075V 1Ah = 3.100V 1Bh = 3.125V 1Ch = 3.150V 1Dh = 3.175V 1Eh = 3.200V 1Fh = 3.300V

Address 0x13H: BUCK1_DLY_ON

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:0	R/W	BUCK1_DLY_ON	Depends on part number	BUCK1 sequence delay from trigger point: 0h = 0ms; 1h = 0.5ms; 2h = 1ms; 3h = 2ms; 4h = 3ms; 5h = 4ms; 6h = 5ms; 7h = 6ms; 8h = 7ms;

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				9h = 8ms; Ah = 9ms; Bh = 10ms; Ch = 12ms; Dh = 14ms; Eh = 16ms; Fh = 20ms

Address 0x14H: BUCK2_DLY_ON

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:0	R/W	BUCK2_DLY_ON	Depends on part number	BUCK2 sequence delay from BUCK1 PG: 0h = 0ms; 1h = 0.5ms; 2h = 1ms; 3h = 2ms; 4h = 3ms; 5h = 4ms; 6h = 5ms; 7h = 6ms; 8h = 7ms; 9h = 8ms; Ah = 9ms; Bh = 10ms; Ch = 12ms; Dh = 14ms; Eh = 16ms; Fh = 20ms

Address 0x15H: BUCK3_DLY_ON

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:0	R/W	BUCK3_DLY_ON	Depends on part number	BUCK3 sequence delay from BUCK1 PG: 0h = 0ms; 1h = 0.5ms; 2h = 1ms; 3h = 2ms; 4h = 3ms; 5h = 4ms; 6h = 5ms; 7h = 6ms; 8h = 7ms; 9h = 8ms; Ah = 9ms; Bh = 10ms; Ch = 12ms; Dh = 14ms; Eh = 16ms; Fh = 20ms

Address 0x16H: LDO_DLY_ON

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:0	R/W	LDO_DLY_ON	Depends on part number	LDO sequence delay from BUCK1 PG: 0h = 0ms; 1h = 0.5ms; 2h = 1ms; 3h = 2ms; 4h = 3ms; 5h = 4ms; 6h = 5ms; 7h = 6ms;

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				8h = 7ms; 9h = 8ms; Ah = 9ms; Bh = 10ms; Ch = 12ms; Dh = 14ms; Eh = 16ms; Fh = 20ms

Address 0x17H: nRESET_DLY

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:0	R/W	nRESET_DLY	Depends on part number	nRESET sequence delay from BUCK1 PG: 0h = 0ms; 1h = 0.5ms; 2h = 1ms; 3h = 2ms; 4h = 3ms; 5h = 4ms; 6h = 5ms, 7h = 6ms; 8h = 7ms; 9h = 8ms; Ah = 9ms; Bh = 10ms; Ch = 12ms; Dh = 14ms; Eh = 16ms; Fh = 20ms

Address 0x18H: GPO_DLY

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:0	R/W	GPO_DLY	Depends on part number	GPO sequence delay from BUCK1 PG: 0h = 0ms; 1h = 0.5ms; 2h = 1ms; 3h = 2ms; 4h = 3ms; 5h = 4ms; 6h = 5ms; 7h = 6ms; 8h = 7ms; 9h = 8ms; Ah = 9ms; Bh = 10ms; Ch = 12ms; Dh = 14ms; Eh = 16ms; Fh = 20ms

Address 0x19H: INT_ACK

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3	RW1C	BUCK3_ACK	0h	Interrupt acknowledge BUCK3 0h = No interrupt 1h = Interrupt set
2	RW1C	BUCK2_ACK	0h	Interrupt acknowledge BUCK2 0h = No interrupt 1h = Interrupt set
1	RW1C	BUCK1_ACK	0h	Interrupt acknowledge BUCK1 0h = No interrupt 1h = Interrupt set

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0	RW1C	LDO_ACK	0h	Interrupt acknowledge LDO 0h = No interrupt 1h = Interrupt set

Address 0x1AH: INT_ACK_BUCK1

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3	RW1C	BUCK1_OV_ACK	0h	BUCK1 overvoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
2	RW1C	BUCK1_UV_ACK	0h	BUCK1 undervoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
1	RW1C	BUCK1_OCP_ACK	0h	BUCK1 overcurrent protection interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
0	RW1C	BUCK1_WARM_ACK	0h	BUCK1 over temperature warning interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set

Address 0x1BH: INT_ACK_BUCK2

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3	RW1C	BUCK2_OV_ACK	0h	BUCK2 overvoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
2	RW1C	BUCK2_UV_ACK	0h	BUCK2 undervoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
1	RW1C	BUCK2_OCP_ACK	0h	BUCK2 overcurrent protection interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
0	RW1C	BUCK2_WARM_ACK	0h	BUCK2 over temperature warning interrupt acknowledge(Write 1 to clear) 0h = No interrupt 1h = Interrupt set

Address 0x1CH: INT_ACK_BUCK3

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3	RW1C	BUCK3_OV_ACK	0h	BUCK3 overvoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
2	RW1C	BUCK3_UV_ACK	0h	BUCK3 undervoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
1	RW1C	BUCK3_OCP_ACK	0h	BUCK3 overcurrent protection interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
0	RW1C	BUCK3_WARM_ACK	0h	BUCK3 over temperature warning interrupt acknowledge (Write 1 to clear)

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				0h = No interrupt 1h = Interrupt set

Address 0x1DH: INT_ACK_LDO

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3	RW1C	LDO_OV_ACK	0h	LDO overvoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
2	RW1C	LDO_UV_ACK	0h	LDO undervoltage interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
1	RW1C	LDO_OCP_ACK	0h	LDO overcurrent protection interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set
0	RW1C	LDO_WARM_ACK	0h	LDO over temperature warning interrupt acknowledge (Write 1 to clear) 0h = No interrupt 1h = Interrupt set

Address 0x1EH: INT_MASK_BUCKx_LDO

Bit	Type	Bit Name	Default	Description
7	RW	BUCK3_OCP_MASK	0h	BUCK3 overcurrent protection interrupt mask 0h = Not masked 1h = Masked
6	RW	BUCK3_WARM_MASK	0h	BUCK3 over temperature warning interrupt mask 0h = Not Masked 1h = Masked
5	RW	BUCK2_OCP_MASK	0h	BUCK2 overcurrent protection interrupt mask 0h = Not Masked 1h = Masked
4	RW	BUCK2_WARM_MASK	0h	BUCK2 over temperature warning interrupt mask 0h = Not Masked 1h = Masked
3	RW	BUCK1_OCP_MASK	0h	BUCK1 overcurrent protection interrupt mask 0h = Not Masked 1h = Masked
2	RW	BUCK1_WARM_MASK	0h	BUCK1 over temperature warning interrupt mask 0h = Not Masked 1h = Masked
1	RW	LDO_OCP_MASK	0h	LDO overcurrent protection interrupt mask 0h = Not Masked 1h = Masked
0	RW	LDO_WARM_MASK	0h	LDO over temperature warning interrupt mask 0h = Not Masked 1h = Masked

Address 0x1FH: FAULT_STATUS_BUCK1

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	R	PVIN1_UVLO_STATUS	0h	BUCK1 PVIN1 under voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
5	RW1C	BUCK1_OV_STATUS	0h	BUCK1 over voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected

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4	RW1C	BUCK1_HOT_STATUS	0h	BUCK1 over temperature shutdown status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
3	RW1C	BUCK1_OVP_STATUS	0h	BUCK1 overvoltage protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
2	RW1C	BUCK1_SCG_STATUS	0h	BUCK1 short circuit to ground status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
1	RW1C	BUCK1_OVL_STATUS	0h	BUCK1 over-load protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
0	RW1C	BUCK1_UV_STATUS	0h	BUCK1 undervoltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected

Address 0x20H: FAULT_STATUS_BUCK2

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	R	PVIN2_UVLO_STATUS	0h	BUCK2 PVIN2 under voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
5	RW1C	BUCK2_OV_STATUS	0h	BUCK2 over voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
4	RW1C	BUCK2_HOT_STATUS	0h	BUCK2 over temperature shutdown status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
3	RW1C	BUCK2_OVP_STATUS	0h	BUCK2 overvoltage protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
2	RW1C	BUCK2_SCG_STATUS	0h	BUCK2 short circuit to ground status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
1	RW1C	BUCK2_OVL_STATUS	0h	BUCK2 over-load protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
0	RW1C	BUCK2_UV_STATUS	0h	BUCK2 undervoltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected

Address 0x21H: FAULT_STATUS_BUCK3

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	R	PVIN3_UVLO_STATUS	0h	BUCK3 PVIN3 under voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
5	RW1C	BUCK3_OV_STATUS	0h	BUCK3 over voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
4	RW1C	BUCK3_HOT_STATUS	0h	BUCK3 over temperature shutdown status (Write 1 to clear) 0h = No fault detected 1h = Fault detected

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3	RW1C	BUCK3_OVP_STATUS	0h	BUCK3 overvoltage protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
2	RW1C	BUCK3_SCG_STATUS	0h	BUCK3 short circuit to ground status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
1	RW1C	BUCK3_OVL_STATUS	0h	BUCK3 over-load protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
0	RW1C	BUCK3_UV_STATUS	0h	BUCK3 undervoltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected

Address 0x22H: FAULT_STATUS_LDO

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	R	PVIN4_UVLO_STATUS	0h	LDO PVIN3 under voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
5	RW1C	LDO_OV_STATUS	0h	LDO over voltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
4	RW1C	LDO_HOT_STATUS	0h	LDO over temperature shutdown status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
3	RW1C	LDO_OVP_STATUS	0h	LDO overvoltage protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
2	RW1C	LDO_SCG_STATUS	0h	LDO short circuit to ground status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
1	RW1C	LDO_OVL_STATUS	0h	LDO over-load protection status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
0	RW1C	LDO_UV_STATUS	0h	LDO undervoltage status (Write 1 to clear) 0h = No fault detected 1h = Fault detected

Address 0x23H: VMON_BUCK1_CFG

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:2	RW	BUCK1_OV_SET	3h	BUCK1 OV detection threshold with respect to target voltage setting: 0h = 104%; 1h = 104% 2h = 106%; 3h = 106%
1:0	RW	BUCK1_UV_SET	3h	BUCK1 UV detection threshold with respect to target voltage setting: 0h = 96%; 1h = 96% 2h = 94%; 3h = 94%

Address 0x24H: VMON_BUCK2_CFG

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED

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3:2	RW	BUCK2_OV_SET	3h	BUCK2 OV detection threshold with respect to target voltage setting: 0h = 104%; 1h = 104% 2h = 106%; 3h = 106%
1:0	RW	BUCK2_UV_SET	3h	BUCK2 UV detection threshold with respect to target voltage setting: 0h = 96%; 1h = 96% 2h = 94%; 3h = 94%

Address 0x25H: VMON_BUCK3_CFG

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:2	RW	BUCK3_OV_SET	3h	BUCK3 OV detection threshold with respect to target voltage setting: 0h = 104%; 1h = 104% 2h = 106%; 3h = 106%
1:0	RW	BUCK3_UV_SET	3h	BUCK3 UV detection threshold with respect to target voltage setting: 0h = 96%; 1h = 96% 2h = 94%; 3h = 94%

Address 0x26H: VMON_LDO_CFG

Bit	Type	Bit Name	Default	Description
7:4	R	RESERVED	0h	RESERVED
3:2	RW	LDO_OV_SET	3h	LDO OV detection threshold with respect to target voltage setting: 0h = 104%; 1h = 104% 2h = 106%; 3h = 106%
1:0	RW	LDO_UV_SET	3h	LDO UV detection threshold with respect to target voltage setting: 0h = 96%; 1h = 96% 2h = 94%; 3h = 94%

Address 0x27H: ERR_BUCKx_LDO_CFG

Bit	Type	Bit Name	Default	Description
7	RW	BUCK3_OV_RST_EN	0h	BUCK3 over voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the state transition bit
6	RW	BUCK3_UV_RST_EN	0h	BUCK3 under voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the state transition bit
5	RW	BUCK2_OV_RST_EN	0h	BUCK2 over voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC State depending on the state transition bit
4	RW	BUCK2_UV_RST_EN	0h	BUCK2 under voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state

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				1h = Fault causes a transition to the RESET State or the WT_PWR_REC state depending on the state transition bit
3	RW	BUCK1_OV_RST_EN	0h	BUCK1 over voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET state or the WT_PWR_REC state depending on the state transition bit
2	RW	BUCK1_UV_RST_EN	0h	BUCK1 under voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC state depending on the state transition bit
1	RW	LDO_OV_RST_EN	0h	LDO over voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC state depending on the state transition bit
0	RW	LDO_UV_RST_EN	0h	LDO under voltage fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET State or the WT_PWR_REC state depending on the state transition bit

Address 0x28H: RESTART_CMD

Bit	Type	Bit Name	Default	Description
7:0	RW	PMIC_RESTART_CMD	0h	Write to this to re-start the device. A readback of this results in '0x00'. DDh = Re-start the device

Address 0x29H: CFG_REG_CRC

Bit	Type	Bit Name	Default	Description
7	RW	DEV_CFG_CRC	0h	Expected CRC8 value for device configuration registers

Address 0x2AH: DEV_STATE

Bit	Type	Bit Name	Default	Description
7~4	R	RESERVED	0h	RESERVED
3	R	CTRL_LOCK	1h	Control Lock Status 0h = Write access allowed based on CONTROL_LOCK 1h = Write access not allowed based on CONTROL_LOCK
2	R	CFG_LOCK	1h	Configuration Lock Status 0h = Write access allowed based on CONFIG_LOCK 1h = Write access not allowed based on CONFIG_LOCK
1~0	R	DEV_STATE	1h	Device State 0h = Any State other than the ACTIVE, RESET or SAFE State 1h = ACTIVE State 2h = RESET State 3h = SAFE/ALERT State

Address 0x2BH: DEV_ERR_ACK_1

Bit	Type	Bit Name	Default	Description
7~5	R	RESERVED	0h	RESERVED
4	R	SYSTEM_ERR_ACK	0h	System error acknowledge 0h = Not detected 1h = Detected
3	R	ABIST_LDO_ACK	0h	ABIST LDO error acknowledge 0h = Not detected 1h = Detected

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2	R	ABIST_BUCK3_ACK	0h	ABIST BUCK3 error acknowledge 0h = Not detected 1h = Detected
1	R	ABIST_BUCK2_ACK	0h	ABIST BUCK2 error acknowledge 0h = Not detected 1h = Detected
0	R	ABIST_BUCK1_ACK	0h	ABIST BUCK1 error acknowledge 0h = Not detected 1h = Detected

Address 0x2CH: DEV_ERR_ACK_2

Bit	Type	Bit Name	Default	Description
7~5	R	RESERVED	0h	RESERVED
4	RW1C	CFG_CRC_ERR_ACK	0h	CFG CRC error acknowledge 0h = No error detected 1h = Error detected
3	RW1C	nINT_ERR_ACK	0h	nINT error acknowledge 0h = No error detected 1h = Error detected
2	RW1C	nRESET_ERR_ACK	0h	nRESET error acknowledge 0h = No error detected 1h = Error detected
1	RW1C	I2C_INVALID_ ADDR_ERR_ACK	0h	I2C invalid address error acknowledge 0h = No error detected 1h = Error detected
0	RW1C	I2C_CRC_ERR_ACK	0h	I2C CRC error acknowledge 0h = No error detected 1h = Error detected

Address 0x2DH: DEV_FAULT_STATUS_1

Bit	Type	Bit Name	Default	Description
7~5	R	RESERVED	0h	RESERVED
4	RW1C	SYS_HOT_STATUS	0h	System over temperature shutdown status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
3	RW1C	SYS_WARM_STATUS	0h	System warm temperature status (Write 1 to clear) 0h = No fault detected 1h = Fault detected
2	RW1C	RESTART_CMD_STATUS	0h	The previous shutdown was due to a Restart Command from the MCU 0h = Not detected 1h = Detected
1:0	R	RESERVED	0h	RESERVED

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Address 0x2EH: DEV_FAULT_STATUS_2

Bit	Type	Bit Name	Default	Description
7~6	R	RESERVED	0h	RESERVED
5	RW1C	GPO_ERR_STATUS	0h	GPO pin monitor detection error status 0h = Not detected 1h = Detected
4	RW1C	nINT_ERR_STATUS	0h	nINT pin monitor detection error status 0h = Not detected 1h = Detected
3	RW1C	nRESET_ERR_STATUS	0h	nRESET pin monitor detection error status 0h = Not detected 1h = Detected
2	RW1C	EFUSE_CRC_ERR_STATUS	0h	EFUSE CRC detection error status 0h = Not detected 1h = Detected
1	R	RESERVED	0h	RESERVED
0	RW1C	GND_LOSS_ERR_STATUS	0h	Ground loss detection error status 0h = Not detected 1h = Detected

Address 0x2FH: INT_MASK_SAFETY

Bit	Type	Bit Name	Default	Description
7~2	R	RESERVED	0h	RESERVED
1	RW	I2C_INVALID_ADDR_MASK	0h	I2C invalid address interrupt mask 0h = Not masked 1h = Masked
0	RW	I2C_CRC_ERR_MASK	0h	I2C CRC error interrupt mask 0h = Not masked 1h = Masked

Address 0x30H: PIN_MON_ERR_CFG

Bit	Type	Bit Name	Default	Description
7~2	R	RESERVED	0h	RESERVED
1	RW	nINT_ERR_RST_EN	0h	nINT_ERR pin monitor fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET state
0	RW	nRESET_ERR_RST_EN	0h	nRESET_ERR pin monitor fault configuration 0h = Fault generates an interrupt and transitions to the SAFE state 1h = Fault causes a transition to the RESET state

Address 0x31H: ABIST_GROUP_DONE

Bit	Type	Bit Name	Default	Description
7~5	R	RESERVED	0h	RESERVED
4	R	ABIST_SYS	0h	ABIST System is done. 0h = Not done 1h = Done
3	R	ABIST_LDO	0h	ABIST LDO is done. 0h = Not done 1h = Done
2	R	ABIST_BUCK3	0h	ABIST BUCK3 is done. 0h = Not done 1h = Done

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1	R	ABIST_BUCK2	0h	ABIST BUCK2 is done. 0h = Not done 1h = Done
0	R	ABIST_BUCK1	0h	ABIST BUCK1 is done. 0h = Not done 1h = Done

Address 0x32H: ABIST_BUCK1/2_ACK

Bit	Type	Bit Name	Default	Description
7	RW1C	ABIST_BUCK2_HOT_ACK	0h	ABIST BUCK2 thermal shutdown error acknowledge 0h = Not detected 1h = Detected
6	RW1C	ABIST_BUCK2_OVP_ACK	0h	ABIST BUCK2 over voltage protection error acknowledge 0h = Not detected 1h = Detected
5	RW1C	ABIST_BUCK2_OV_ACK	0h	ABIST BUCK2 over voltage error acknowledge 0h = Not detected 1h = Detected
4	RW1C	ABIST_BUCK2_UV_ACK	0h	ABIST BUCK2 under voltage error acknowledge 0h = Not detected 1h = Detected
3	RW1C	ABIST_BUCK1_HOT_ACK	0h	ABIST BUCK1 thermal shutdown error acknowledge 0h = Not detected 1h = Detected
2	RW1C	ABIST_BUCK1_OVP_ACK	0h	ABIST BUCK1 over voltage protection error acknowledge 0h = Not detected 1h = Detected
1	RW1C	ABIST_BUCK1_OV_ACK	0h	ABIST BUCK1 over voltage error acknowledge 0h = Not detected 1h = Detected
0	RW1C	ABIST_BUCK1_UV_ACK	0h	ABIST BUCK1 under voltage error acknowledge 0h = Not detected 1h = Detected

Address 0x33H: ABIST_LDO_BUCK3_ACK

Bit	Type	Bit Name	Default	Description
7	RW1C	ABIST_LDO_HOT_ACK	0h	ABIST LDO thermal shutdown error acknowledge 0h = Not detected 1h = Detected
6	RW1C	ABIST_LDO_OVP_ACK	0h	ABIST LDO over voltage protection error acknowledge 0h = Not detected 1h = Detected
5	RW1C	ABIST_LDO_OV_ACK	0h	ABIST LDO over voltage error acknowledge 0h = Not detected 1h = Detected
4	RW1C	ABIST_LDO_UV_ACK	0h	ABIST LDO under voltage error acknowledge 0h = Not detected 1h = Detected
3	RW1C	ABIST_BUCK3_HOT_ACK	0h	ABIST BUCK3 thermal shutdown error acknowledge 0h = Not detected 1h = Detected
2	RW1C	ABIST_BUCK3_OVP_ACK	0h	ABIST BUCK3 over voltage protection error acknowledge 0h = Not detected 1h = Detected

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1	RW1C	ABIST_BUCK3_OV_ACK	0h	ABIST BUCK3 Over Voltage Error Acknowledge 0h = Not detected 1h = Detected
0	RW1C	ABIST_BUCK3_UV_ACK	0h	ABIST BUCK3 Under Voltage Error Acknowledge 0h = Not detected 1h = Detected

Address 0x34H: ABIST_WARM_SYSTEM_OK

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	RW1C	ABIST_LDO_ WARM_ACK	0h	ABIST LDO warm error acknowledge 0h = Not detected 1h = Detected
5	RW1C	ABIST_BUCK3_ WARM_ACK	0h	ABIST BUCK3 warm error acknowledge 0h = Not detected 1h = Detected
4	RW1C	ABIST_BUCK2_ WARM_ACK	0h	ABIST BUCK2 warm error acknowledge 0h = Not detected 1h = Detected
3	RW1C	ABIST_BUCK1_ WARM_ACK	0h	ABIST BUCK1 warm error acknowledge 0h = Not detected 1h = Detected
2	RW1C	ABIST_SYSTEM_ TSHUT_ACK	0h	ABIST thermal shutdown error acknowledge 0h = Not detected 1h = Detected
1	R	RESERVED	0h	RESERVED
0	RW1C	ABIST_GNDLOSS _ERR_ACK	0h	ABIST ground loss error acknowledge 0h = Not detected 1h = Detected

Address 0x36H: POWER_GOOD_STATUS

Bit	Type	Bit Name	Default	Description
7	R	nINT_STATUS	0h	nINT Pin Logic Level Status 0h = nINT pin is at a low level 1h = nINT pin is at a high level
6	R	nRESET_STATUS	0h	nRESET Pin Logic Level Status 0h = nRESET pin is at a low level 1h = nRESET pin is at a high level
5	R	GPO_STATUS	0h	GPO Pin Logic Level Status 0h = GPO pin is at a low level 1h = GPO pin is at a high level
4	R	SEQ_STATUS	0h	SEQ Pin Logic Level Status 0h = SEQ pin is at a low level 1h = SEQ pin is at a high level
3	R	LDO_PG_STATUS	0h	LDO Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits
2	R	BUCK3_PG_STATUS	0h	BUCK3 Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits
1	R	BUCK2_PG_STATUS	0h	BUCK2 Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits
0	R	BUCK1_PG_STATUS	0h	BUCK1 Power Good Status 0h = Voltage rail is not within regulation limits 1h = Voltage rail is within regulation limits

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Address 0x37H: BUCKx_SSEND

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0h	RESERVED
6	R	LDO_VIN_OVP	0h	LDO_VIN_OVP status 0h = Not detected 1h = Detected
5	R	BUCK3_VIN_OVP	0h	BUCK3_VIN_OVP status 0h = Not detected 1h = Detected
4	R	BUCK2_VIN_OVP	0h	BUCK2_VIN_OVP status 0h = Not detected 1h = Detected
3	R	VSYS_OVP	0h	VSYS_OVP status 0h = Not detected 1h = Detected
2	R	BUCK1_SSEND	0h	BUCK1 soft-start end status 0h = Soft-start do not end 1h = Soft-start end
1	R	BUCK2_SSEND	0h	BUCK2 soft-start end status 0h = Soft-start do not end 1h = Soft-start end
0	R	BUCK3_SSEND	0h	BUCK3 soft-start end status 0h = Soft-start do not end 1h = Soft-start end

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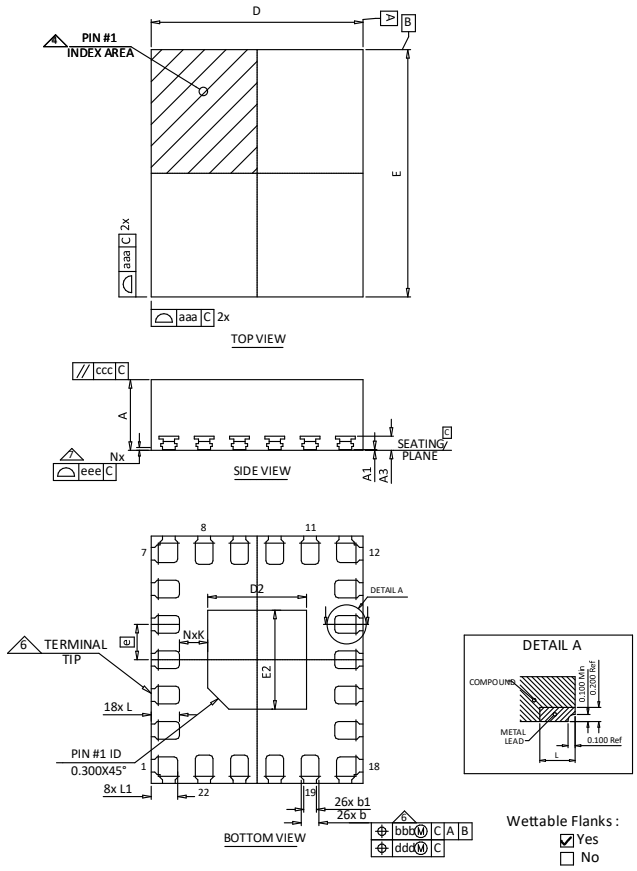
MECHANICAL DATA

MIS-22-3mm*3.5mm Wettable Flank



Thickness / Symbol	Dimension Table		
	1.00		
	MINIMUM	NOMINAL	MAXIMUM
A	0.90	1.00	1.10
A1	-0.01	---	0.05
A3	---	0.200 Ref.	---
b	0.20	0.25	0.30
b1	0.13	0.18	0.23
D		3.00 BSC	
E		3.50 BSC	
e		0.50 BSC	
D2	1.30	1.40	1.50
E2	1.30	1.40	1.50
K	0.20	---	---
L	0.30	0.40	0.50
L1	0.275	0.375	0.475
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

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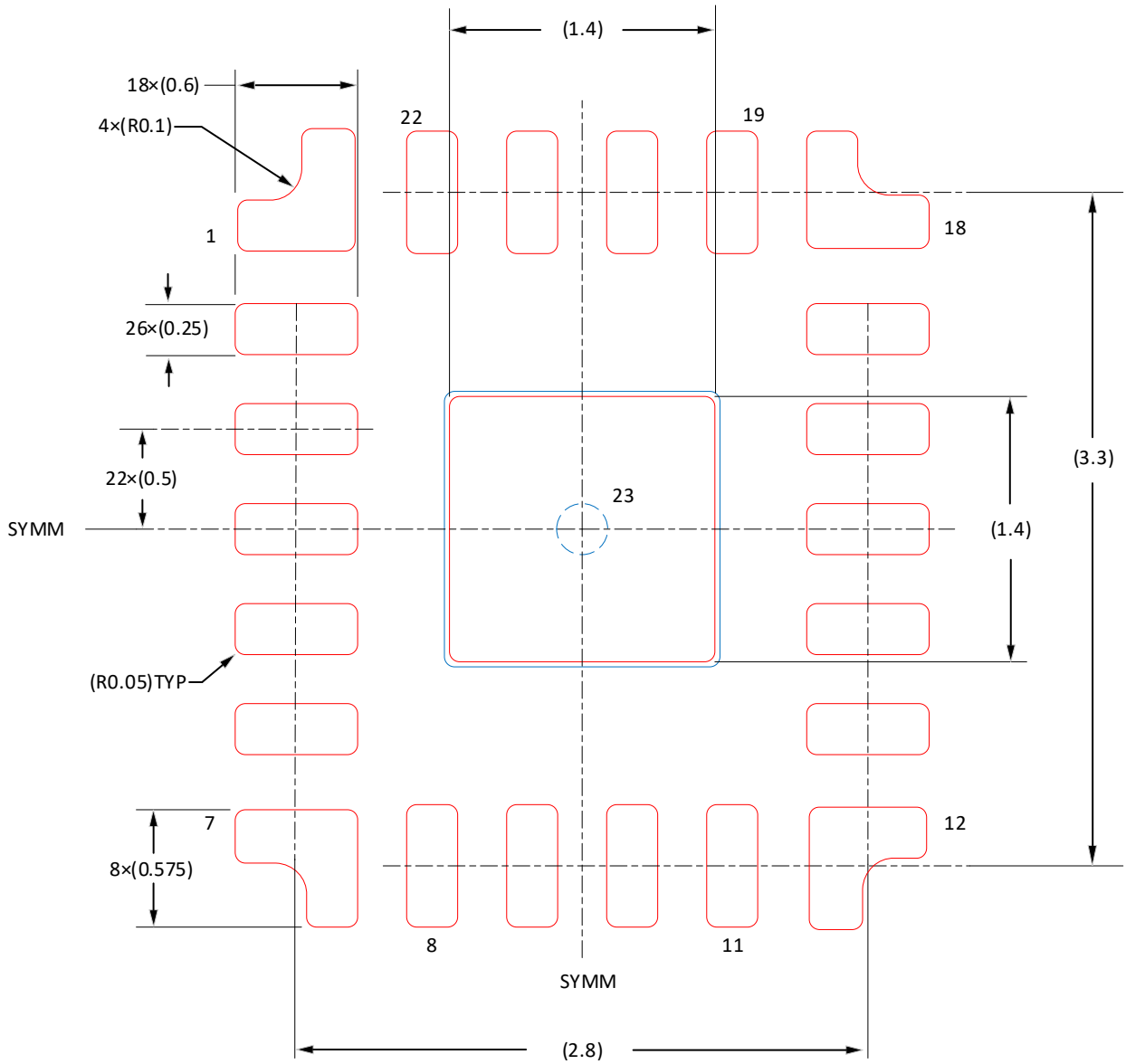
Example Board Layout



SOLDER PASTE EXAMPLE

BASED ON 0.125 MM THICK STENCIL

SCALE:20X

EXPOSED PAD 19

86%PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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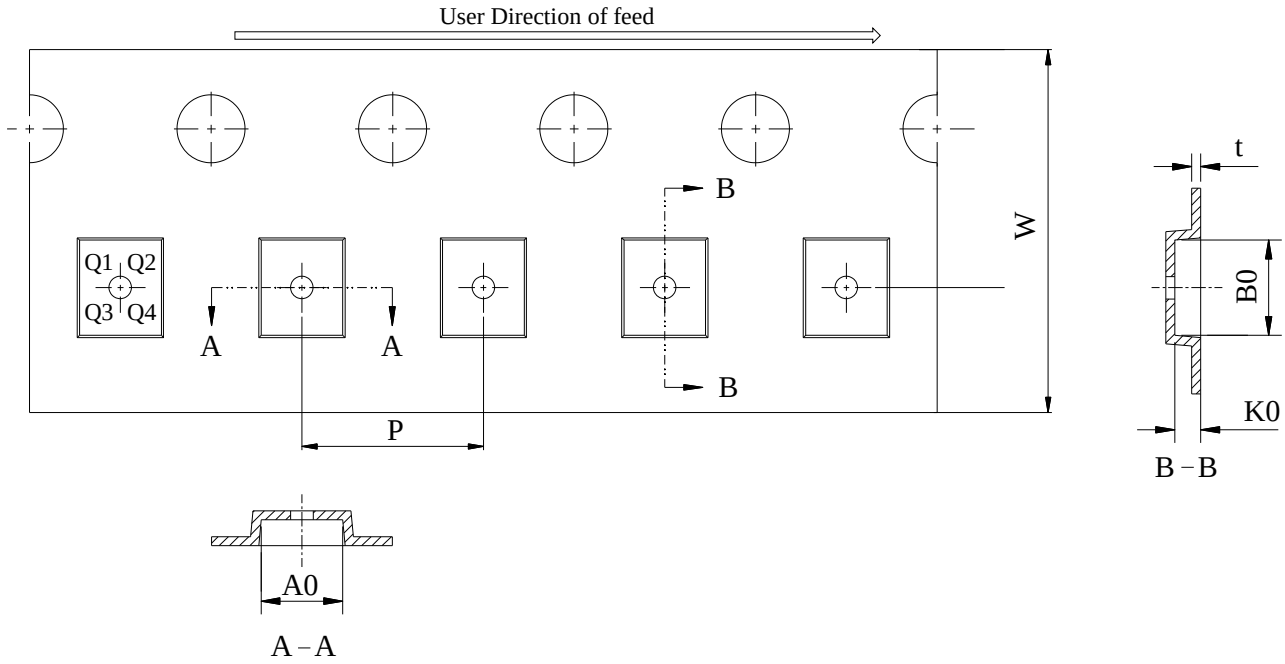
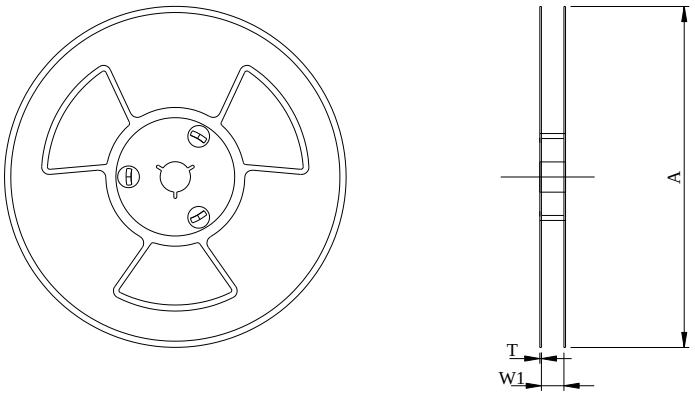
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 ±0.10	8.00±0.10	3.20±0.05	3.75±0.05	1.20±0.05	0.30±0.03	Q1

REEL



Item	A	W1	T
Size (mm)	330±2	12.4 +2/-0	2.1±0.15

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