High Efficiency, Synchronous 4-Switch Bidirectional Buck-Boost Charge & Discharge Controller

1 Descriptions

The SC8802 is a synchronous 4-switch bidirectional buck-boost charge and discharge controller. It supports battery charging regardless of whether the input voltage is lower than, equal to, or higher than the battery voltage. When the system needs to supply power from the battery, the SC8802 reverses power flow to output adjustable voltage which can be lower than, equal to, or higher than the battery voltage.

SC8802 has an ultra-wide input and output voltage range of 2.7 V to 30 V, covering 1S to 6S lithium battery applications. It adopts industry-leading 10 V gate drive voltage to maximize conversion efficiency with external power MOSFETs.

The device adopts current-mode control for buck, boost and buck-boost operation. External resistors can adjust switching frequency, battery voltage threshold and input/output current limit, simplifying design while meeting diverse application requirements.

Bidirectional power flow is controlled via the DIR pin. A full set of protection functions are integrated, including input current limit, output current limit, dynamic input power regulation, cycle-by-cycle inductor current limit, output overvoltage protection, bidirectional short-circuit protection and thermal shutdown to handle all abnormal operating conditions.

SC8802 is packaged in a 32-pin 4 mm × 4 mm QFN package with exposed thermal pad.

2 Features

- Bidirectional buck-boost charging for 1~6 series lithium-ion batteries
- Reverse buck-boost discharge power output from battery
- Dynamically adjustable output voltage under discharge mode
- Ultra-wide input voltage range: 2.7 V ~ 30 V
- Ultra-wide reverse output voltage range: 2 V ~ 30 V
- Integrated 10 V, 2 A high-current gate drivers
- High efficiency across full load range for buck-boost operation
- Adjustable switching frequency: 200 kHz ~ 600 kHz
- Built-in cycle-by-cycle inductor peak current limit
- Programmable input & output current limits, bidirectional short-circuit protection
- Charge/discharge status monitoring, under-voltage & overvoltage protection
- 32-pin 4 mm × 4 mm QFN package with exposed thermal pad

3 Applications

- Power Banks
- Smart USB Sockets
- USB PD Adapters
- USB Hubs
- Vehicle On-Board Chargers
- Energy Recovery Equipment
- Industrial Instruments & Meters

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC8802QDER	32 pin QFN	4mm x 4mm x 0.75mm

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5 Device Selection Table

ORDER NUMBER	SC8801	SC8802	SC8803	SC8804
Max Operating Voltage	30V	30V	36V	36V
Topology	Buck-Boost Charger	Buck-Boost Charger	Buck Charger	Boost Charger
IPWM function	No	Yes	Yes	Yes
DPDM function	Yes	No	No	No

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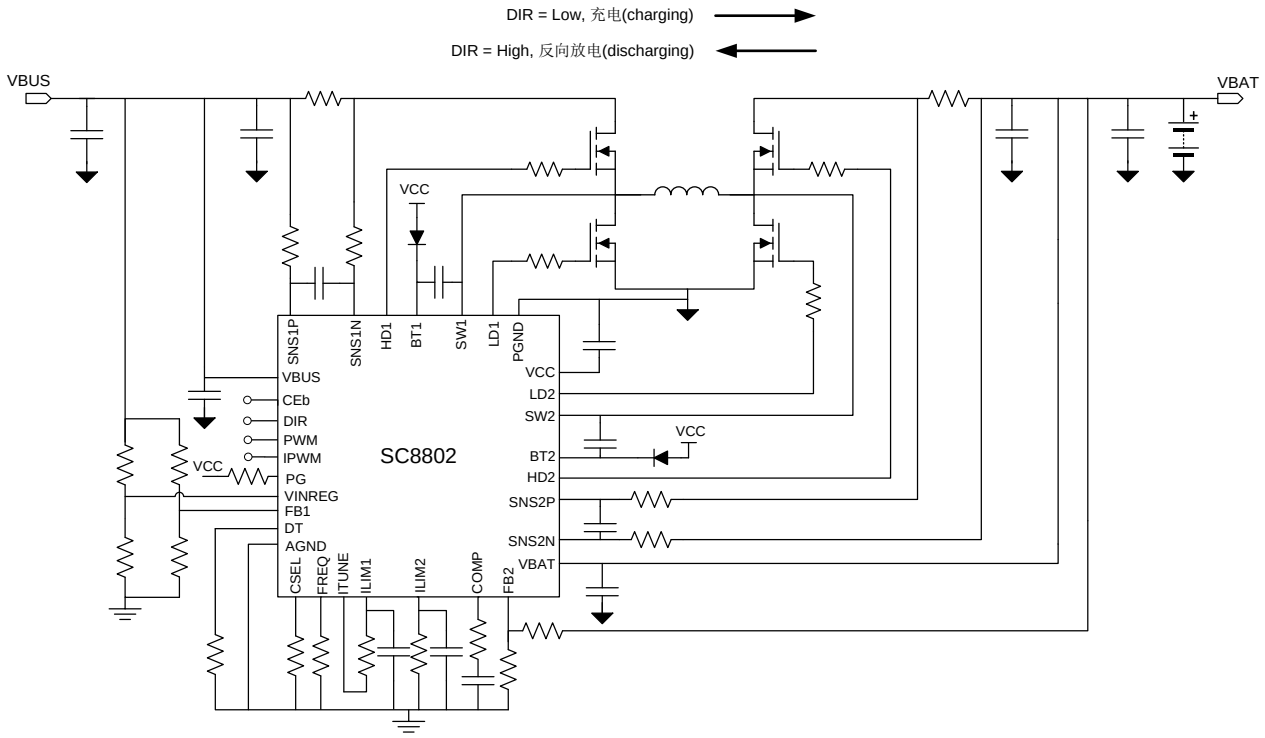
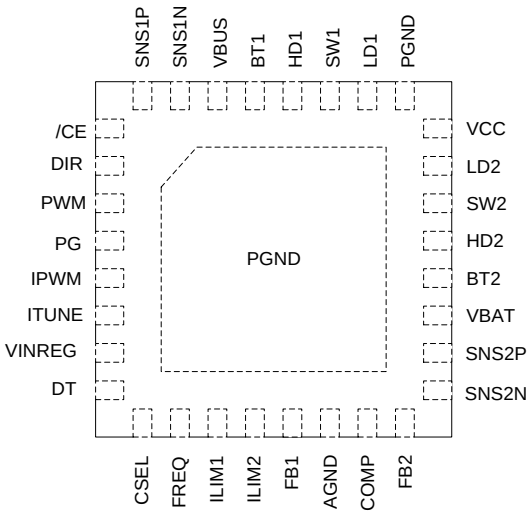
6 Typical Application Circuit



7 Terminal Configuration and Functions

TOP VIEW



SC8802

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	/CE	I	Chip enable, active low. Pull high (>1.3 V) to disable the device.
2	DIR	I	Operation mode selector. DIR = Low: Charge mode, VBUS charges VBAT battery pack. DIR = High (>1.3 V): Discharge mode, VBAT supplies regulated voltage to VBUS port.
3	PWM	I	Dynamic VBUS output voltage adjustment (Discharge mode only). VBUS formula: $VBUS = VBUS_SET \times (\frac{1}{6} + \frac{5}{6} \times D)$ D = PWM duty cycle (0% ~ 100%). PWM input frequency range: 20 kHz ~ 100 kHz. 100% duty cycle outputs full set voltage; 0% duty cycle outputs 1/6 of set voltage.
4	PG	O	Requires external pull-up resistor to logic supply rail. Charge mode (DIR=Low): PG low = charging in progress; PG high = charge termination completed. Discharge mode (DIR=High): PG high when VBUS output voltage is within 90%~110% of target value; PG low otherwise.
5	IPWM	I	A PWM signal with a frequency ranging from 20 kHz to 100 kHz can be input through the IPWM pin to realize dynamic adjustment of the input or output current, with the adjustment range being 0% to 100% of the set value. This function is valid in both charging and discharging modes, but needs to be used in conjunction with ITUNE.
6	ITUNE	I/O	Use the ITUNE pin to select the current limit target for IPWM adjustment. Connect ITUNE to the negative terminal of the ILIM1 resistor to adjust the current limit value of the VBUS terminal. To dynamically adjust the current limit value of the VBAT

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			terminal, connect ITUNE to the negative terminal of the ILIM2 resistor. If this function is not required, leave the ITUNE pin floating.
7	VINREG	I	Charge mode only. Set minimum VBUS operating voltage via external resistor divider. $$VBUS_min = VREF \times \left(1 + \frac{RUP}{RDOWN}\right)$$ The IC starts charging only when VBUS exceeds \(VBUS_{MIN}\). If VBUS drops below threshold, input current will be reduced to stabilize voltage; charging stops if regulation fails. Tie VINREG to VCC to disable this function.
8	DT	I	Dead time setting, 4 options: ● DT shorted to GND = 20 ns; ● 68 kΩ resistor to GND = 40 ns; ● 270 kΩ resistor to GND = 60 ns; ● DT open = 80 ns
9	CSEL	I	Battery charge termination voltage setting (Charge mode only): ● CSEL shorted to GND: Termination voltage defined by FB2 resistor divider ● 68 kΩ to GND: 4.2 V (1S lithium battery) ● 270 kΩ to GND: 8.4 V (2S lithium battery) ● CSEL open: 12.6 V (3S lithium battery)
10	FREQ	I	Switching frequency setting, 3 options: ● FREQ pin shorted to GND: 200 kHz ● FREQ pin connect 68 kΩ resistor to GND: 400 kHz ● FREQ pin is open: 600 kHz
11	ILIM1	I	VBUS port current limit programming. Charge mode = input current limit; Discharge mode = output current limit: $$IBUS_LIM = \frac{VREF}{RILIM1} \times \frac{RSS1}{RSNS1}$$ VREF: Internal reference value 1.21V RSNS1: VBUS current sense resistor (typical 10 mΩ); RSS1: 1 kΩ differential series resistor; Connect a 10 nF capacitor from ILIM1 to GND. Short ILIM1 to GND to disable VBUS current limit function.
12	ILIM2	I	VBAT battery port current limit programming. Charge mode = battery charging current limit; Discharge mode = battery output current limit: $$IBAT_LIM = \frac{VREF}{RILIM2} \times \frac{RSS2}{RSNS2}$$ VREF: Internal reference value 1.21V RSNS2: VBAT current sense resistor (typical 10 mΩ); RSS2: 1 kΩ differential series resistor; Connect a 10 nF capacitor from ILIM1 to GND. Do NOT short ILIM2 directly to GND.
13	FB1	I	Discharge mode VBUS output voltage feedback divider. 1. Without PWM dynamic adjustment, the Basic formula: $$VBUS = VREF \times \left(1 + \frac{RUP}{RDOWN}\right)$$ VREF is the internal voltage reference of 1.21 V, and

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			RUP and RDOWN are the external voltage divider resistors connected to FB1 respectively 2. With PWM dynamic adjustment: $VBUS = VREF \times \left(1+\frac{RUP}{RDOWN}\right) \times (\frac{1}{6}+\frac{5}{6} \times D)$ where D stands for the duty cycle of the PWM signal.
14	AGND	I/O	Analog signal ground
15	COMP	O	Internal control loop compensation pin. Connect RC network to stabilize regulation loop.
16	FB2	I	Charge mode battery termination voltage feedback divider (Only valid when CSEL is shorted to GND). $VBAT = VREF \times \left(1+\frac{RUP}{RDOWN}\right)$ If CSEL configures fixed 1S/2S/3S voltage, float or ground FB2 pin.
17	SNS2N	I	Negative input of current sense amplifier. Connect an external current sense resistor between SNS2P and SNS2N.
18	SNS2P	I	Positive input of current sense amplifier. Connect an external current sense resistor between SNS2P and SNS2N.
19	VBAT	I	Output node of the converter when DIR = Low, and input node of the converter when DIR = High. Connect to battery cells.
20	BT2	PWR	Connect a capacitor between BT2 pin and SW2 pin to bootstrap a voltage to provide the bias voltage for high side MOSFET gate driver
21	HD2	PWR	High side MOSFET gate driver 2 output
22	SW2	PWR	Switching Node 2
23	LD2	PWR	Low side MOSFET gate driver 2 output
24	VCC	O	Output of internal regulator to provide max. 10V voltage for the bias voltage of internal gate drivers. Connect a 1 μF ceramic capacitor from VCC to PGND pin.
25	PGND	PWR	Power Ground.
26	LD1	PWR	Low side MOSFET gate driver 1 output
27	SW1	PWR	Switching Node 1
28	HD1	PWR	High side MOSFET gate driver 1 output
29	BT1	PWR	Connect a capacitor between BT1 pin and SW1 pin to bootstrap a voltage to provide the bias voltage for high side MOSFET gate driver
30	VBUS	I	Input node of the converter when DIR = Low, and output node of the converter when DIR = High. Connect to adapter input port or USB port.
31	SNS1N	I	Negative input of current sense amplifier. Connect an external current sense resistor between SNS1P and SNS1N.
32	SNS1P	I	Positive input of current sense amplifier. Connect an external current sense resistor between SNS1P and SNS1N.
	Thermal Pad	-	For thermal dissipation. Connect to AGND and PGND.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VBUS, VBAT, SNS1P, SNS1N, SNS2P, SNS2N, /CE	-0.3	42	V
	SW1, SW2	-1	42	V
	VCC, PG, DIR, PWM, VINREG, IPWM	-0.3	20	V
	FREQ, ITUNE, ILIM1, ILIM2, COMP, CSEL, DT, FB1, FB2	-0.3	5.5	V
	LD1, LD2	-0.3	12	V
	BT1, HD1 to SW1	-0.3	12	V
	BT2, HD2 to SW2	-0.3	12	V
	BT1, BT2	-0.3	50	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	All pins	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{BUS}	VBUS voltage range	2.7		30	V
V_{BAT}	VBAT voltage range	2		30	V
C_{BUS}	VBUS Bulk Capacitance	30			µF
C_{BAT}	VBAT Bulk Capacitance	30			µF
L	Power Inductor L	2.2		6.8	µH
$R_{SNS1/2}$	Current Sensing Resistor	5	10	20	mΩ

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f_{SW}	Switching Frequency	200		600	kHz
f_{PWM}	PWM Signal Frequency Range	20		100	kHz
D_{PWM} ,D_{IPWM}	PWM, IPWM Signal Duty Cycle Range	0		100	%
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

8.4 Thermal Information

THERMAL RESISTANCE(1)		**QFN-32 (4mm x 4mm)**	**UNIT**
θ_{JA}	Junction to ambient thermal resistance	35	°C/W
θ_{JC}	Junction to case thermal resistance	7	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

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8.5 Electrical Characteristics

T_J= -40°C to 125°C, V_{BUS} = 5V and V_{BAT} = 3.6V, typical values are tested at T_J= 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VBUS, VBAT)						
V_{BUS}	Operating voltage	DIR = Low, as input voltage	2.7		30	V
		DIR = High, as output voltage	2		30	V
V_{BAT}	Operating voltage	DIR = Low, as output voltage	1.5		30	V
		DIR = High, as input voltage	2.7		30	V
V_{UVLO_VBUS}	VBUS under-voltage lockout threshold	DIR = Low, rising edge		2.6	2.7	V
		DIR = Low, hysteresis		160		mV
V_{UVLO_VBAT}	VBAT under-voltage lockout threshold	DIR = High, rising edge		2.6	2.7	V
		DIR = High, hysteresis		160		mV
I_Q	Standby current into VBUS or VBAT pin (whichever is higher)	/CE = low, controller non-switching		0.7	2	mA
I_{Q_VBAT}	Standby current into VBAT pin under EOC status	/CE = low, VBUS removed			15	μA
I_{SD}	Shutdown current into VBUS or VBAT pin (which is higher)	/CE = high		6	10	μA
	Shutdown current into VBUS or VBAT pin (which is lower)	/CE = high			2	μA
VCC AND DRIVER						
V_{CC}	VCC clamp voltage		9.4	10	10.6	V
I_{VCC_LIM}	VCC current limit	V_{CC} = 2V ~10V	50	75	100	mA
R_{HV_pu}	High side driver pull up resistor			1.5		Ω
R_{HV_pd}	High side driver pull down resistor			1		Ω
R_{LV_pu}	Low side driver pull up resistor			1.5		Ω
R_{LV_pd}	Low side driver pull down resistor			1		Ω
ERROR AMPLIFIER						
V_{FB2_REF}	FB2 reference voltage		1.214	1.22	1.226	V
V_{INREG_REF}	VINREG reference voltage		1.196	1.226	1.244	V
V_{ILIMx_REF}	ILIMx reference voltage		1.196	1.212	1.228	V
V_{FB1_REF}	FB1 reference voltage		1.196	1.212	1.228	V
Gm_{EA}	Error amplifier gm			0.16		mS
R_{OUT}	Error amplifier output resistance(1)			20		MΩ
$I_{BIAS(FBx)}$	FBx pin input bias current	FBx in regulation			100	nA
OUTPUT TARGET AND THRESHOLD						
V_{BAT_TRGT}	Battery termination target	R_{CSEL} = 68 kΩ (±10%)	4.158	4.2	4.242	V
		R_{CSEL} = 270 kΩ (±10%)	8.316	8.4	8.484	V
		R_{CSEL} = open	12.474	12.6	12.726	V
V_{BAT_TERM}	Termination threshold over V_{BAT_TRGT}	DIR = Low, rising edge	96.5%	98%	99.5%	
V_{BAT_RECH}	Recharge threshold over V_{BAT_TRGT}	DIR = Low, falling edge		95.8%		
V_{TRK_CH}	Trickle charge threshold over V_{BAT_TRGT}	DIR = Low, rising edge	64%	70%	76%	
		DIR = Low, hysteresis		5%		
I_{BAT_TRK}	Battery trickle charge current, over ILIM2 set current	DIR = Low		10%		

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I_{BAT_TERM}	Battery current termination threshold, over ILIM2 set current	DIR = Low, falling edge		4%		
V_{OVP}	OVP threshold, over VBUS target	DIR = high	105%	110%	115%	
CURRENT LIMIT						
I_{LIMx}	ILIM1 current limit accuracy DIR = low	I_{BUS_LIM} R_{SNS1} ≥ 30 mV	-10%		10%	
	ILIM2 current limit accuracy DIR = low	I_{BAT_LIM} R_{SNS2} ≥ 30 mV	-5%		5%	
	ILIM1 current limit accuracy DIR = high	I_{BUS_LIM} R_{SNS1} ≥ 30 mV	-5%		5%	
	ILIM2 current limit accuracy DIR = high	I_{BAT_LIM} R_{SNS2} ≥ 30 mV	-10%		10%	
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	R_{FREQ} = 0Ω	180	210	240	kHz
		R_{FREQ} = 68kΩ (±10%)	360	410	460	kHz
		R_{FREQ} = 270kΩ (±10%)	540	600	660	kHz
INDICATION						
$t_{PG_deglitch}$	PG signal deglitch time	f_{sw} = 200kHz	27	38.5	50	ms
I_{SINK_PG}	PG sink current	V_{PG} = 0.4 V	3.6	4.1	4.6	mA
V_{BUS_PG}	VBUS power good threshold	DIR = High, high limit falling edge (PG from low to high)		110%		
		DIR = High, high limit hysteresis (PG from high to low)		5%		
		DIR = High, low limit rising edge (PG from low to high)		90%		
		DIR = High, low limit hysteresis (PG from high to low)		5%		
LOGIC CONTROL						
R_{PD}	/CE, DIR pin internal pull down resistor			1		MΩ
	PWM pin internal pull down resistor			0.5		MΩ
	IPWM pin internal pull down resistor			1		MΩ
V_{IL}	/CE, DIR, PWM, IPWM input low voltage				0.4	V
V_{IH}	/CE, DIR PWM, IPWM input high voltage		1.2			V
Soft Start						
t_{SS}	Internal soft-start time	From /CE low to 90% VBUS		8	15	ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature(1)			165		°C
	Thermal shutdown hysteresis(1)			15		°C

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8.6 Typical Characteristics

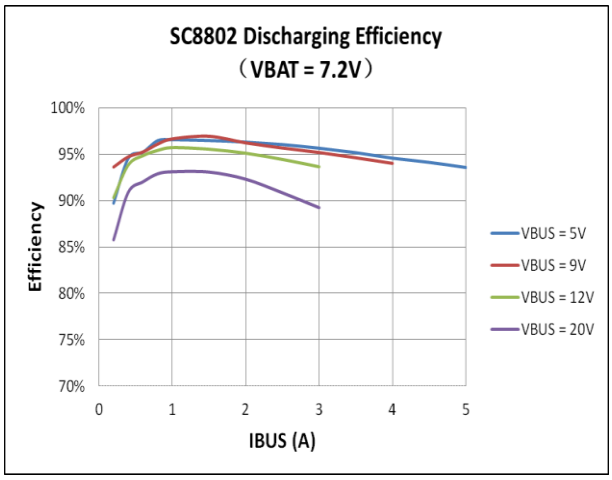

Figure 1. Fsw=400kHz, L=3.3μH, discharging efficiency

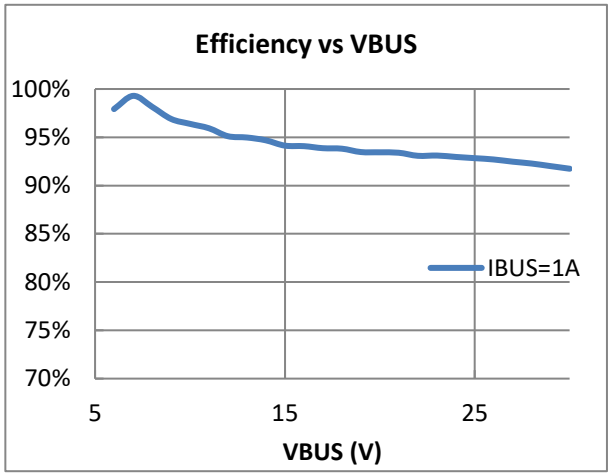

Figure 2. Fsw=400kHz, L=3.3μH, discharging efficiency

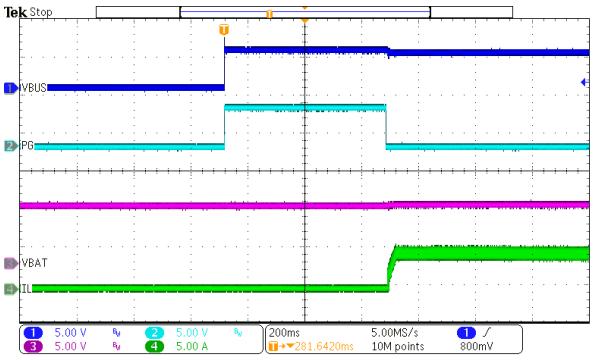

Figure 3. Start up in charging mode

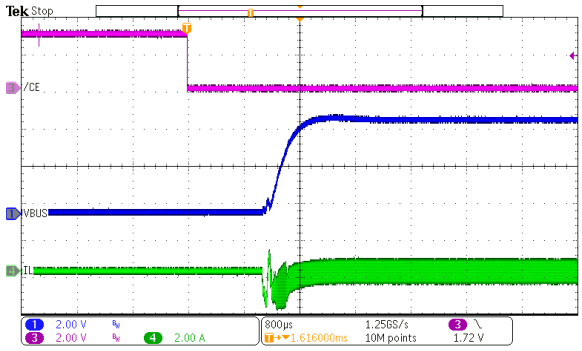

Figure 4. Startup with /CE pull low

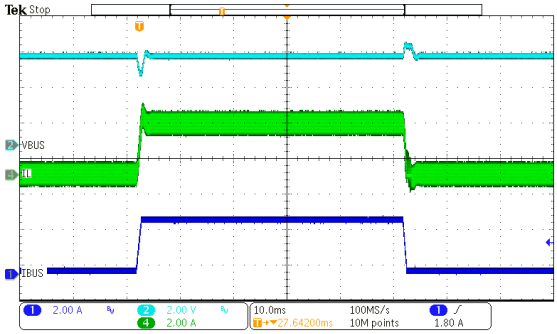

Figure 5. Load trans，VBUS = 5V, 0.5A<—>3A

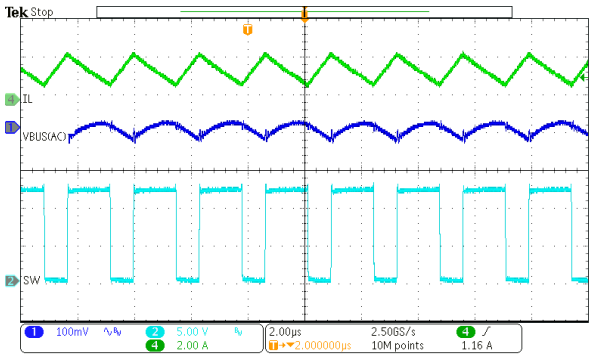

Figure 6. PWM operation(DIR=HIGH), VBUS=5V/1A

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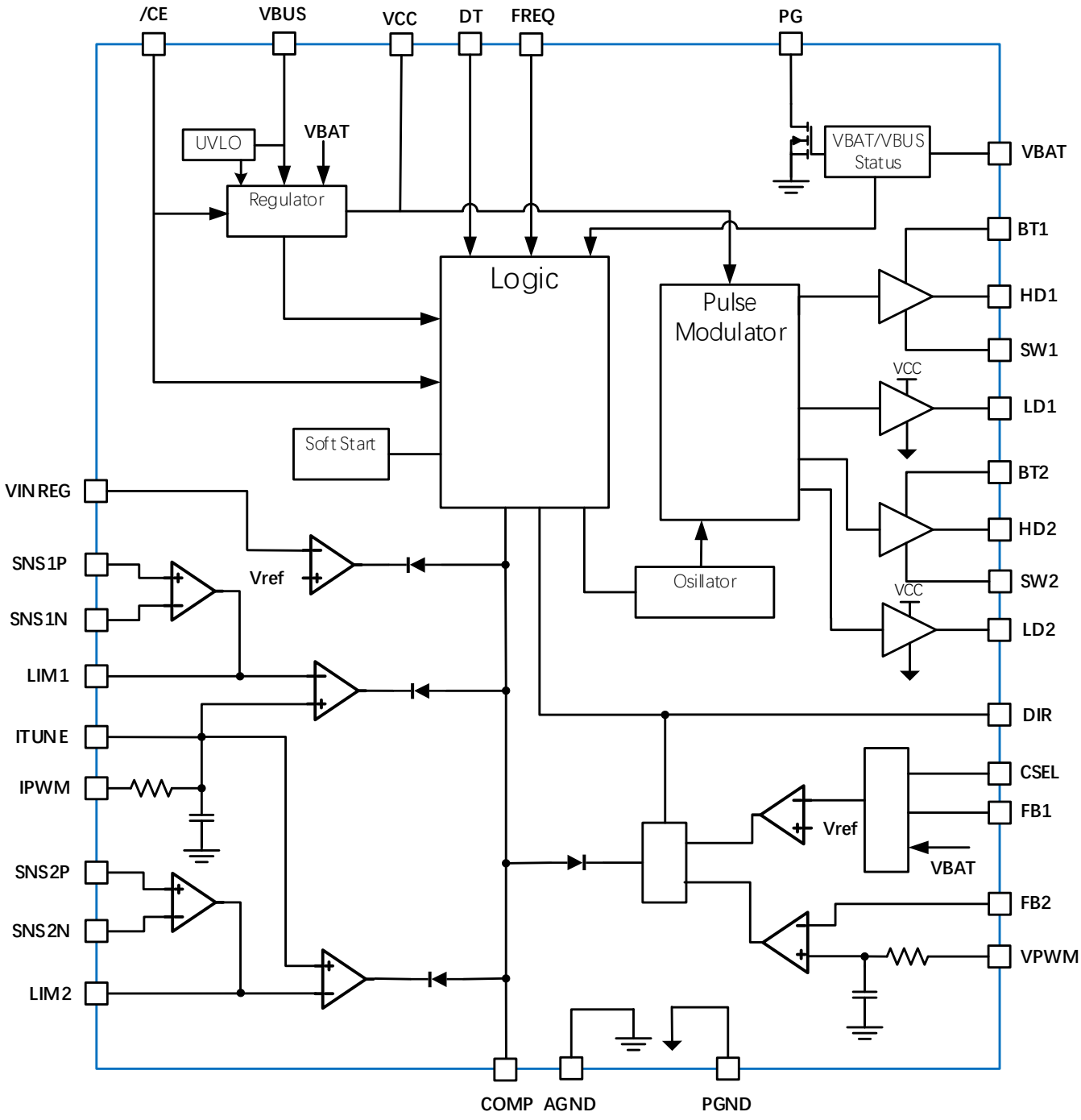
9 Functional Block Diagram



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10 Feature Description

The SC8802 is bi-directional synchronous Buck-boost charge controller for 1- to 6-cell battery with a wide input/output voltage range. The charging and discharging mode is selected by DIR pin.

The SC8802 operates as a charger when DIR pin is pulled logic low, and it is called charging mode. In this mode, SC8802 works in buck-boost switching mode to step up voltage and charges battery. The SC8802 features trickle charging, CC charging, CV charging and charging termination functions. The SC8802 supports self-adaptive feature for different adaptors and can limit the charging current automatically to avoid overloading adaptors.

When operating in discharge mode, the SC8802 adopts a 4-switch synchronous buck-boost architecture, enabling its output voltage to be higher than, lower than, or equal to the battery voltage. The SC8802 automatically switches between buck and boost modes with seamless transitions, and the maximum input and output current limits can be set via external resistors. When paired with fast charging or USB PD protocol ICs, a fast charging or USB PD solution can be easily implemented.

10.1 Charging Mode

The charge and discharge modes of SC8802 are controlled by the DIR signal.

When the DIR input level is low, SC8802 operates in charge mode. In this state, power flows from the adapter interface (VBUS pin) to charge the battery (VBAT pin), and the power path is shown in the figure below.

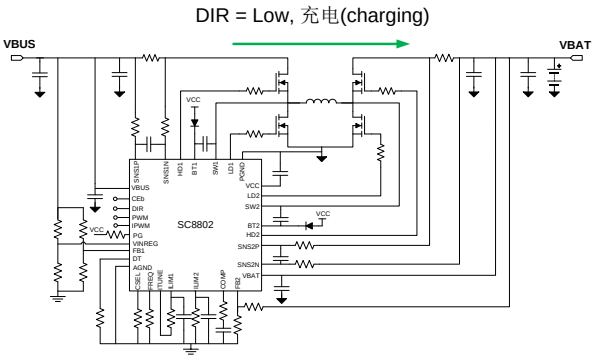

Figure 7. Charging mode when DIR=LOW

10.1.1 Charge Termination Voltage Setting (CSEL and FB2)

In charging mode, termination voltage is set by one of two cases.

Case 1: Set the termination voltage using CSEL pin. When the SC8802 is enabled, the IC checks the resistor value at CSEL pin and set the charge termination voltage internally.

Table 1 shows the resistor value for different charge termination voltage.

Table 1. CSEL resistor value vs Charge termination voltage

CSEL resistor value	Charge termination voltage
68kΩ	4.2V (1S battery)
270kΩ	8.4V (2S battery)
Open	12.6V (3S battery)
0Ω	Set by FB2 pin resistors

When setting the charge termination voltage by CSEL pin, the battery voltage is monitored by VBAT pin voltage directly. In this case, FB2 pin should be open or connected to GND.

The SC8802 checks the resistor value at CSEL pin only during the startup process. After SC8802 is enabled, termination voltage change by changing resistor value at CSEL pin will not be valid until system restarts (Off and on the VBUS voltage or cycling the /CE voltage)

Case 2: Set the termination voltage using resistor divider at FB2 pin. When CSEL pin is connected to GND, termination voltage is adjusted by external resistor divider at FB2 pin and is calculated as:

$$VBAT = V_{FB2_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

With V_{FB2_REF} voltage is 1.22V and R_{UP} and R_{DOWN} resistors are the resistor divider between VBAT to FB2 pins.

10.1.2 CC Charge current setting (ILIMx)

The SC8802 can adjust the current limit of both adaptor side (VBUS) and battery side (VBAT) by resistors at ILIM1 and ILIM2 pins.

Table 2 Charge current limit setting

Control Pins	Description
ILM1	Monitor R_{SNS1} to set the adaptor side (VBUS) charge current (IBUS_LIM)

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ILM2	**Monitor R_{SNS2} to set the battery side (VBAT) charge current (IBAT_LIM)**

The SC8802 senses the VBUS and VBAT current by monitoring R_{SNS1} and R_{SNS2} respectively as below figure shows.

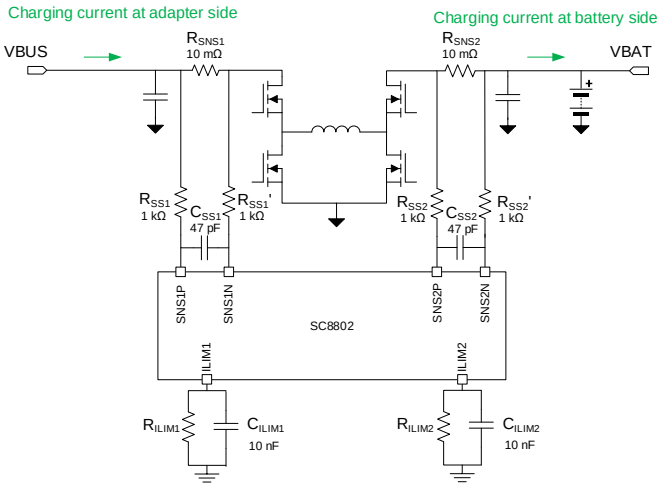


Figure 8 Charge current monitoring circuit

R_{SNSX} is the current sense resistor (x means 1 or 2) connected in series with the input supply or output of the charger. The SC8802 monitors the voltage across the sense resistors R_{SNSx} through R_{SSX} and $R_{SSX'}$ and calculate the input and output current. C_{SSX} is the filter capacitor.

The ILIMx pin is used to set the charge current limit. Connect the R_{ILIMX} resistor between $ILIM_X$ pin and GND with 10nF capacitor in parallel.

The current limit is calculated as:

$$I_{BUS_LIM} = \frac{V_{LIM_REF}}{R_{ILIM1}} \times \frac{R_{SS1}}{R_{SNS1}}$$

$$I_{BAT_LIM} = \frac{V_{LIM_REF}}{R_{ILIM2}} \times \frac{R_{SS2}}{R_{SNS2}}$$

Where:

V_{LIM_REF} = Internal reference voltage 1.21V;

R_{ILIMx} = Resistors at ILIMx pin;

R_{SNSx} = Current sense resistors;

R_{SSx} = Resistors between current sense resistor and the SC8802 pins (SNSxP, SNSxN).

To get accurate values, keep below two conditions;

1) R_{SNSx} should be placed between MOSFET and input/ output capacitor.

2) R_{SS1} and $R_{SS1'}$ should be same value; R_{SS2} and $R_{SS2'}$ should be also same value. Typically 1kΩ resistor is used.

If R_{SNSx} is changed, $R_{SSx}/R_{SSX'}$ values need to be adjusted accordingly with below calculation:

$$\frac{R_{SNSx}}{R_{SSx}} = \frac{10\ m\Omega}{1\ k\Omega}$$

For example, If R_{SNSX} is 20mΩ, then $R_{SSX}/R_{SSX'}$ should be 2kΩ; if R_{SNSX} is 5mΩ, then $R_{SSX}/R_{SSX'}$ should be 500Ω.

In charging mode, if both VBUS and VBAT current limits are programmed, the SC8802 controls the charge current as soon as one of VBUS and VBAT current reaches its current limit.

For example, if the adaptor side (VBUS) current reaches its current limit set value (ex. 3A) first, then adaptor side current is regulated to 3A; whereas if battery side (VBAT) current limit reaches its current limit set value (ex. 6A) first, then battery side current is regulated to 6A, and at this case, adaptor side current could be lower than VBUS current limit set value.

If VBUS current limit is not required, connect ILIM1 pin to GND. Then VBUS current is not regulated and the SC8802 regulates VBAT current limit for constant current charge.

In charging mode, VBAT current limit is necessary, otherwise, the SC8802 will misjudge the end of charge condition.

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

10.1.3 Current Limit Dynamic Adjustment (IPWM)

By configuring the IPWM and ITUNE pins, the SC8802 enables flexible adjustment of the charging current.

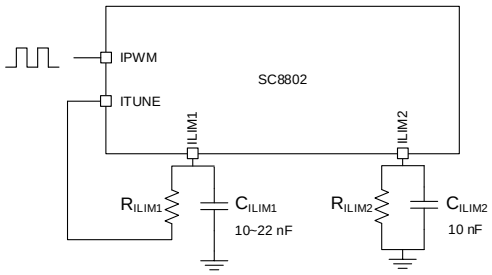
A PWM signal with a frequency range of 20 kHz ~ 100 kHz can be input to the IPWM pin to adjust the charging current via duty cycle. The adjustable range covers 0% to 100% of the programmed charging current, and the charging current is proportional to the duty cycle, as expressed in the formula below:

$$I_{LIMx} = I_{LIMx_SET} \times D$$

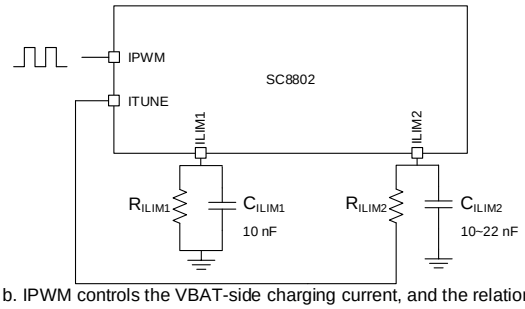
Where,

I_{LIMx_SET} is the charging current set by the ILIMx pin, D is the duty cycle of the IPWM signal, and I_{LIMx} is the adjusted charging current.

The ITUNE pin selects which charging current channel to modulate dynamically. For example, to dynamically adjust the VBUS-side charging current, connect the negative terminal of the ILIM1 programming resistor to ITUNE. To dynamically adjust the VBAT-side charging current, connect the negative terminal of the ILIM2 programming resistor to ITUNE, as shown in the figure below:



a. IPWM controls the VBUS-side charging current, and the relationship is，ILIM1 = ILIM1_set x D， as shown in the figure above



b. IPWM controls the VBAT-side charging current, and the relationship is，ILIM2 = ILIM2_set x D， as shown in the figure above

Figure 9 IPWM Dynamic Charging Current Adjustment Circuit Diagram

Precautions for Dynamic Charging Current Adjustment via IPWM

1) When the IPWM input signal stays continuously high (100% duty cycle), the charging current equals the value configured by the ILIMx pin.
2) The ILIMx pin modulated by the IPWM signal must be connected with a capacitor to GND, with a recommended capacitance range of 10 nF ~ 22 nF. Lower IPWM frequency requires larger capacitance; for instance, 22 nF is recommended for 20 kHz IPWM signal.
3) If this dynamic adjustment function is not required, connect the ILIMx programming resistor directly to GND, and leave both IPWM and ITUNE pins floating.

If ITUNE is connected to the negative terminal of the ILIMx programming resistor, **do not pull IPWM to GND or leave it floating, otherwise the IC will work abnormally.**

10.1.4 Dynamic Power management (VINREG)

The SC8802 features dynamic power management. The valid minimum VBUS threshold is programmed by VINREG pin. When VBUS reaches minimum VBUS threshold, the charge current is reduced automatically. With this feature, even in case the adaptor output current capability is lower than the SC8802 charge current set value, the SC8802 can automatically reduce the charge current to adaptor output current to avoid the adaptor overload and abnormal charging, and keep VBUS voltage to minimum operating voltage.

The minimum operating VBUS voltage is calculated as:

$$V_{BUS_min} = V_{INREG_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

Where;

V_{INREG_REF} = 1.226V;

R_{UP} and R_{DOWN} = The divider resistor connected to VINREG pin.

The SC8802 operates normally when VBUS voltage is higher than programmed threshold voltage (V_{BUS_min}). This function is valid only in charge mode. If this function is not required, connect VINREG pin to VCC.

10.2 Charging curve

When DIR pin is “L”, the SC8802 enters into charge mode with charge management such as trickle charging, CC charging, CV charging and charging termination (end of charging).

Typical charge curve is shown in Figure 10.

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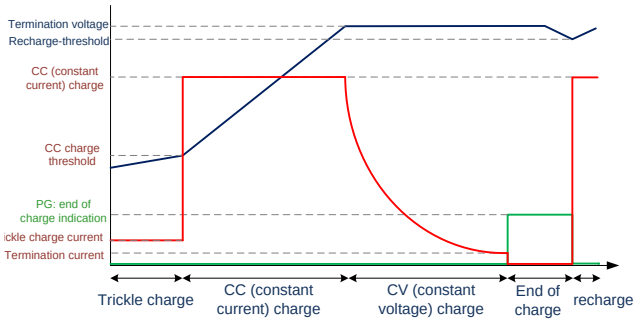

Figure 10. SC8802 Charge curve

10.2.1 Trickle Charging

The SC8802 operates in trickle charging mode if the VBAT voltage is lower than CC (constant current) charge threshold voltage. The CC charge threshold voltage is typically 70% of charge termination voltage.

In trickle charge mode, the SC8802 reduces the VBAT charge current to 10% of programmed current limit (IBAT_LIM). For example, if VBAT current limit (IBAT_LIM) is programmed to 6A, in trickle charge mode, charge current is reduced to 0.6A automatically. When VBAT voltage exceeds CC charge threshold voltage, the SC8802 recovers the charge current to VBAT current limit value and operates as CC charge mode.

10.2.2 Constant Current Charge mode

The SC8802 operates in CC quick charge mode if the VBAT voltage is higher than quick charge threshold voltage. During CC quick charge mode, the output current is controlled by ILIMx pin. For the detail information, please refer to 10.1.2 CC charge current setting (ILIMx)

10.2.3 Constant Voltage Charging

The SC8802 operates in CV charging mode if VBAT voltage reaches to 98% of VBAT termination voltage. In CV charging mode, the SC8802 maintains battery voltage and reduce the charge current automatically until the battery is charged fully.

10.2.4 Charge termination / End of charge indication (PG)

In charging mode, once below two conditions are all valid, the SC8802 recognizes that the battery is fully charged and it will terminate charging automatically:

1) The battery voltage is higher than 98% of battery termination threshold.

2) With monitoring the R_{SNS2}, VBAT current becomes lower than 1/25 of ILIM2 programmed current.

After stopping charging, the SC8802 turns off VCC voltage and operates in a low power standby mode and reduces the current consumption from battery side.

The SC8802 indicates the end of charge status with PG pin. PG is open drain output and it requires an external pullup resistor.

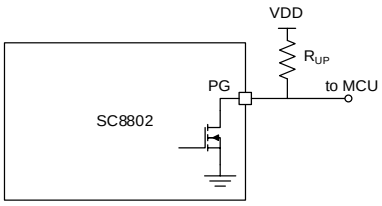

Figure 11 PG pin structure

In charging mode, PG output is pulled LOW but after end of charge, PG output is pulled HIGH by external pullup resistor and indicates that the battery is fully charged.

If MCU does not need to check PG, remain PG pin open.

10.2.5 Recharging

After charging termination, once the SC8802 detects the battery voltage falls below 95% of programmed termination voltage, the SC8802 automatically restarts charging in CC phase. In this period, VCC voltage is turned on, PG voltage is pulled “L” to indicate that the SC8802 is in charging mode.

10.3 Reverse Direction Discharge mode

When DIR pin is “H”, the SC8802 enters reverse direction discharging mode.

In discharging mode, the battery (VBAT) is discharged to adaptor/USB (VBUS), which becomes output. Figure 12 shows the power path at discharging mode.

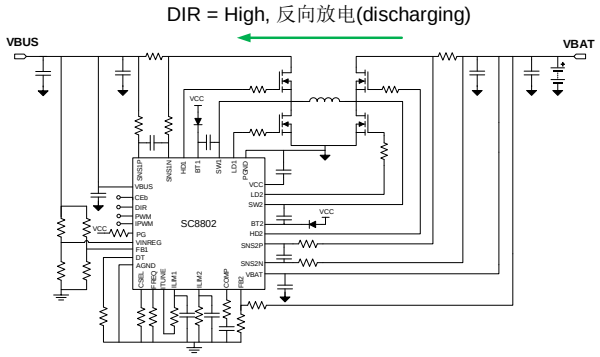

Figure 12 SC8802 Reverse direction discharge mode.

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10.3.1 VBUS discharge voltage setting (FB1)

In discharging mode, VBUS discharge voltage is set by external resistor divider as FB1 pin and is calculated as:

$$VBUS = V_{FB1_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

Where:

V_{FB1_REF} = Internal reference voltage 1.21V

R_{UP} and R_{DOWN} = Resistor divider at FB1 connected to VBUS.

The SC8802 can operate with quick charge or PD controller ICs and these ICs can change the FB1 pin voltage for real-time discharge output voltage control.

10.3.2 VBUS Discharge voltage real-time control (PWM)

In discharging mode, the SC8802 supports VBUS output voltage change in two ways: one is to change FB1 pin divider ratio, the other is to control VBUS voltage by PWM signal input.

For the 2nd way, the FB1 resistor divider value is fixed, VBUS output voltage is controlled by duty cycle (D) of PWM signal, which is supplied to PWM pin and in the range of 10kHz to 100kHz. VBUS output voltage is calculated as:

$$VBUS = V_{BUS_SET} \times \left(\frac{1}{6} + \frac{5}{6} \times D\right)$$

Where;

V_{BUS_SET} = VBUS output voltage which is set by FB1 resistor divider;

D = Duty cycle of PWM signal.

The relationship between VBUS output voltage and D is showed in Figure 13.

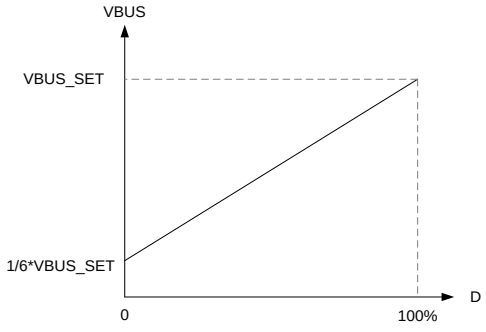

Figure 13 VBUS output voltage vs PWM duty cycle.

If PWM input signal keeps “H”, means 100% of duty cycle, then the output voltage become the programmed voltage by FB1 resistor divider.

If PWM input signal keeps “L”, means 0% of duty cycle, then the output voltage become the 1/6 of programmed voltage by FB1 resistor divider.

Real-time PWM output control is valid only in discharging mode.

10.3.3 Discharge current setting (ILIMx)

In discharging mode, the VBUS and VBAT current is sensed by R_{SNS1} and R_{SNS2} current sense resistors.

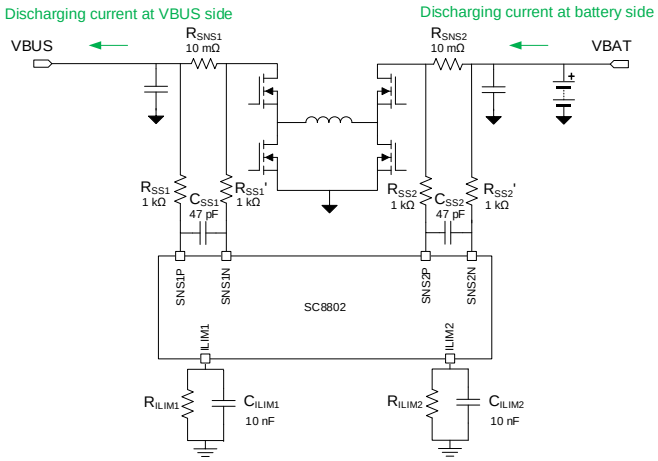

Figure 14 Discharge current monitoring circuit.

The SC8802 features current limit function. VBUS and battery side current limits are set by ILIM1 and ILIM2 pins and current limits are calculated as:

$$I_{BUS_LIM} = \frac{V_{LIM_REF}}{R_{ILIM1}} \times \frac{R_{SS1}}{R_{SNS1}}$$

$$I_{BAT_LIM} = \frac{V_{LIM_REF}}{R_{ILIM2}} \times \frac{R_{SS2}}{R_{SNS2}}$$

Please refer to for proper R_{SNSx} and R_{SSx} values.

The current limit, set by ILIMx, in discharging mode is equally applied to charging mode: in charging mode, the current limit is charging current and in discharging mode, the current limit is maximum discharging current.

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If the current limits required by charging mode and discharging mode are different, please refer to the circuit in Figure 15 to change the limits accordingly.

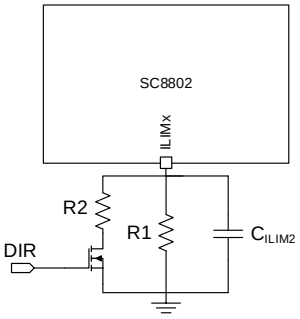

Figure 15 Current limit control using DIR signal

It is not allowed to set any of the current limits to 0A. Keep the minimum current limit above 0.3A.

10.3.4 Discharge voltage POWER GOOD indicator (PG)

In discharging mode, PG signal indicates discharge voltage status.

If VBUS output voltage remains in between 90% ~ 110% of programmed voltage, PG pin become high impedance and due to the output pullup resistor, PG out becomes “H” to indicate the output voltage is normal.

If VBUS voltage is out of normal voltage range, PG out becomes “L”.

If this indication is not required, remain PG pin open.

10.4 Other signals

10.4.1 Chip Enable (/CE)

The SC8802 turns on/off by /CE signal. When /CE input is “L”, the SC8802 turns on; when /CE input is “H”, the SC8802 turns off.

10.4.2 Charging/Discharging mode control (DIR)

The charging mode and discharging mode is decided by DIR signal. When DIR input is “L”, the SC8802 operates in charging mode; when DIR input is “H”, the SC8802 operates in discharging mode.

10.4.3 Switching frequency setting (FREQ)

The one of three switching frequency is selectable by resistor value at FREQ pin:

FREQ resistor	Switching frequency f_{sw}
0Ω	200kHz
68kΩ (±10%)	400kHz
Open	600kHz

The accuracy of the resistor at FREQ is allowed ±10%. The real-time switching frequency change is not valid and new resistor value change will be applied in next turn on.

10.4.4 Dead time setting (DT)

The one of four dead time is selectable by resistor value at DT pin:

DT resistor	Dead time
0Ω	20ns
68kΩ (±10%)	40ns
270kΩ (±10%)	60ns
Open	80ns

The accuracy of the resistor at DT is allowed ±10%. DT does not support the real-time change and new resistor value change will be applied in next turn on.

When driving large power MOSFET with high C_{ISS} value, or adding driver resistors at LDx or HDx to adjust the MOSFET turning on/off time, it is suggested to check and change the dead time to prevent MOSFET shoot-through.

10.4.5 VCC driver voltage

The SC8802 generates driver voltage VCC internally. The VCC is selected higher voltage between VBUS and VBAT, and clamped to 10V if it is higher than 10V.

The driving signal LDx to drive low side MOSFET (Q2 and Q3) is directly supplied from VCC; the driving signal HDx to drive high side MOSFET (Q1 and Q4) is supplied from the diode in between VCC to BTx pin, which is generated by bootstrap circuit with bootstrap capacitor between BTx and SWx.

10.4.6 Feedback compensation (COMP)

The feedback loop can be compensated by adjusting the external components to the COMP pin.

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11 Application Information

11.1 Input and output capacitor selection

The switching frequency of the SC8802 is in the range of 200kHz ~ 600kHz. Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60μF X5R or X7R capacitors with higher voltage rating then operating voltage with margin is recommended. For example, if the highest operating Vin/Vout voltage is 12V, select at least 16V capacitor and to secure enough margin, 25V voltage rating capacitor is recommended.

The high capacitance electrolytic capacitor and tantalum capacitor can be used for stable input and output but capacitor voltage rating should be higher than the highest operating voltage. When the tantalum capacitor is used, at least 1μF ceramic capacitor is placed in parallel. If the electrolytic capacitor is used, much more ceramic capacitors are required. For example, if a 47μF electrolytic capacitor is used, the ceramic capacitors' capacitance is allowed to reduce to 30μF ~ 40μF. Even higher capacitance electrolytic capacitor is used, at least 20μF ceramic capacitor is required.

11.2 Inductor selection

For the SC8802 system stability, the inductance of 2.2μH ~ 10μH inductor is required. High inductance (4.7μH ~ 10μH) is used in the system where the input voltage and output voltage difference is big, such as 3.6V Vin and 15V Vout; Low inductance (2.2μH) is used in the system which the input voltage and output voltage difference is small but high current is required. Typically, 3.3μH inductor is recommended. The inductance can be adjusted for high efficiency and optimization in application.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so around 10mΩ DCR is recommended for the first selection. If the power is relatively small, high DCR inductor can be selected. But if switch on current is high, just like around 10A, then select the lowest DCR inductor as much as possible because 10mΩ DCR also causes 1W power loss.

The inductor saturation current I_{SAT} should be higher than input output current with sufficient margin.

11.3 Current sense resistor

The RSNS1 and RSNS2 are current sense resistors and 5mΩ ~ 20mΩ resistor value is recommended.

Using higher resistor value in high current application causes higher conduction loss. Typically, 10mΩ is recommended. Resistor value can be adjusted depending on current limit and target power efficiency. If R_{SNSx} valued is adjusted, related R_{SSx} value should be adjusted simultaneously.

Please refer to 10.1.2 CC Charge current setting (ILIMx) for proper R_{SNSx} and R_{SSx} values.

The resistor power rating and temperature coefficient should also be considered.

The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than roughly calculated power dissipation.

The resistor value can be varied if the temperature increased and the variation is decided by temperature coefficient along with temperature change. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4 MOSFET selection

The SC8802 is a synchronous 4-switch buck-boost charger controller and it requires 4 NMOS for power switching circuit.

The V_{DS} of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher). For example, if the highest operating voltage is 20V, at least 30V rated V_{DS} MOSFET should be selected; If the highest operating voltage is 24V, 40V V_{DS} voltage rating should be selected.

In the application, if the input and output voltage are higher than 10V, driver circuit voltage can reach 10V, and V_{GS} voltage rating of MOSFET should be selected higher than ±10V.

Considering PCB parasitic parameters during operation, driver voltage can be higher than VCC due to transient overshoot, and ±20V V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest input and output current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at T_A=70˚C or T_C

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= 100˚C should be considered. In addition, the power dissipation value P_D should also be considered and higher P_D is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

The MOSFET $R_{DS(ON)}$ and input capacitor C_{ISS} impact power efficiency directly. Typically, lower $R_{DS(ON)}$ MOSFET has higher C_{ISS}. The $R_{DS(ON)}$ is related to conduction loss. Higher R_{DSON} results in higher conduction loss, thus lower efficiency and higher thermal dissipation; the C_{ISS} is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSFET should be selected based on tradeoff between the $R_{DS(ON)}$ and C_{ISS}.

If high C_{ISS} MOSFET is selected, the switching on and off time become longer, then the dead time should be adjusted with DT pin to avoid simultaneous turn on for both high side and low side MOSFETs.

11.5 Driver resistor and SWx snubber circuit

For a convenient adjustment of MOSFET switching time and transient overshoot at EMI debugging, recommend to add 0603 series resistor between driver pins (LD, HD) and MOSFET Gate pins, and add RC snubber (0603) circuit at SW (refer to Figure 16 Driver resistor and SW snubber circuit)

The driver resistor should be placed near to MOSFET Gate pin. At first, add 0Ω and adjust the resistor value appropriately within 10Ω. After increasing the driver resistor value, the on time of high side and low side MOSFET should be monitored. If the dead time is insufficient, adjust dead time accordingly.

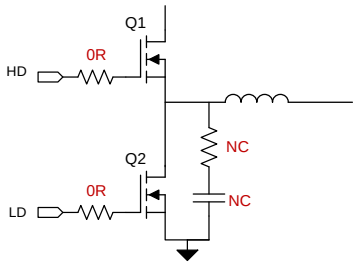

Figure 16 Driver resistor and SWx snubber circuit

The RC snubber circuit is required when the overshoot at SWx needs to suppressed. Leave RC snubber circuit as NC at the first time.

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12 Layout Guide

This chapter defines the mandatory PCB layout rules for SC8802, covering power loop routing, current sampling circuit, MOS drive signal, analog/power ground separation, EMI optimization and sensitive signal wiring. All layout designs shall follow the core principles: minimized power loop area, strict separation of AGND and PGND, short & straight high-frequency routing, sensitive signal isolation and minimal parasitic parameters.

A single-point connection between AGND and PGND is mandatory to eliminate ground loop interference and ensure the stability of sampling and control circuits.

12.1 Grounding Layout Rules

Analog Ground (AGND) and Power Ground (PGND) must be strictly partitioned without overlapping or multi-point bridging.

a) Single-Point Ground Connection: AGND pin and PGND pin shall be connected at a single point. It is recommended to implement the single-point connection at the IC thermal pad to isolate power noise from analog small-signal circuits.

b) AGND Wiring Rule: All analog small-signal components for FBx, VINREG, ILIMx, COMP, DT, FREQ and CSEL must be grounded directly to the IC AGND pin with the shortest path, avoiding PGND power routes to prevent noise coupling.

12.2 Power Loop & Bulk Capacitor Layout Rules

Power loop optimization is the key to reducing switching noise and improving EMI performance. All power loops shall be minimized in area with short and wide routing.

a) VBUS Power Loop: The PGND trace of the VBUS bulk capacitor shall be connected to the PGND of Q2 with the shortest and widest possible path. The loop formed by VBUS bulk capacitor → current sense resistor → upper/lower switching MOSFETs must be minimized.

b) VBAT Power Loop: The PGND trace of the VBAT bulk capacitor shall be connected to the PGND of Q3 with the shortest and widest possible path. The loop formed by VBAT bulk capacitor → current sense resistor → upper/lower switching MOSFETs must be minimized.

c) 100nF Capacitor Near Current Sense Resistor: The 100nF MLCC capacitor placed between the current sense resistor and MOSFET shall be placed close to the switching MOSFET. Its PGND terminal shall be routed to the corresponding lower MOSFET PGND with the shortest path.

d) VCC/VBUS/VBAT Filter Capacitor: The 1μF MLCC capacitors for VCC, VBUS and VBAT pins shall be placed close to the IC pins. The grounding terminals of these capacitors shall connect to the IC PGND pin via the shortest path.

12.3 Current Sampling Circuit Layout Rules

The current sampling circuit is a high-precision sensitive circuit, which must be isolated from high-frequency switching signals to ensure sampling accuracy.

a) The differential routing from the current sense resistor to SNSXP/SNSXN pins shall be tapped from the center pads of the sense resistor. The differential traces shall be routed strictly back to the IC SNS pins and keep away from SWx, LDx and HDx high-noise traces.

b) The differential resistors and capacitors matched with the current sampling circuit shall be placed close to the IC to shorten the sampling signal path and reduce parasitic interference.

12.4 MOS Gate Drive & Switch Signal Layout Rules

a) Trace Width Requirement: the routing width of LDx, HDx and SWx signals shall be ≥15mil to meet current carrying capacity and reduce trace impedance.

b) Drive Resistor Placement: the gate drive series resistors for LDx and HDx MOSFETs shall be placed as close to the MOSFET pins as possible to suppress gate oscillation and optimize EMI performance.

c) Loop Optimization & Routing Isolation

- LDx loop optimization: The loop composed of LDx → lower MOSFET gate → lower MOSFET source PGND → IC PGND shall be minimized. LDx

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traces shall be routed side by side with PGND traces to reduce loop area.

- HDx loop optimization: The loop composed of HDx → upper MOSFET gate → upper MOSFET source PGND → IC SWx shall be minimized. HDx traces shall be routed side by side with the corresponding SWx traces.
- Strict routing isolation: Do not route LDx traces parallel with HDx traces; do not route LDx traces parallel with SWx traces, to avoid crosstalk between high-frequency drive signals.

d) BTx & HDx Matching Capacitor: the 100nF capacitor between HDx and BTx shall be placed close to the IC pins to ensure stable gate drive voltage and suppress high-frequency noise.

12.5 Analog Sensitive Signal Layout Rules

All analog feedback, compensation and configuration signals are susceptible to switching noise interference, requiring independent grounding and signal isolation.

a) FBx and VINREG: The voltage divider resistors for FBx and VINREG pins shall be placed close to the IC. All grounding terminals shall avoid PGND power paths and be directly connected to the IC AGND pin. FBx and VINREG signal traces must keep away from SWx, LDx and HDx high-frequency switching traces.

b) ILIMx & COMP: The peripheral components of ILIMx and COMP pins shall be grounded directly to AGND while avoiding PGND power routes. Their signal traces shall be isolated from SWx/LDx/HDx traces.

c) DT, FREQ, CSEL: The configuration components for DT, FREQ and CSEL pins shall be placed close to the IC. All grounding paths shall avoid PGND and be directly connected to AGND to ensure accurate parameter configuration.

12.6 External Control Signal Grounding Rules

When MCU outputs control signals (including CE, DIR, PWM, IPWM) to control the power management IC, the MCU grounding path shall avoid the PGND power loop. The MCU ground shall be connected to the AGND of the power management IC to prevent power noise from interfering with digital control signals

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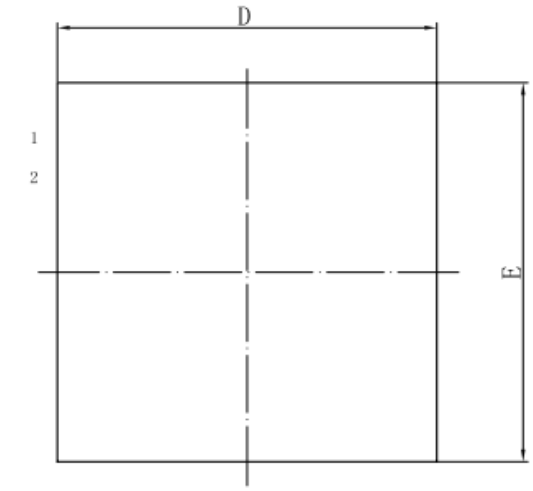
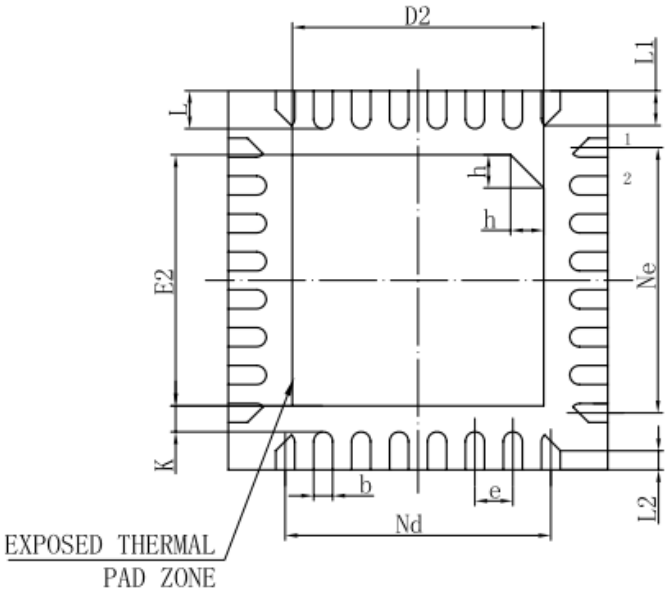
MECHANICAL DATA

QFN32L(0404x0.75-0.40)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.65	2.70
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.65	2.70
Ne	2.80BSC		
K	0.20	-	-
L	0.35	0.40	0.45
L1	0.30	0.35	0.40
L2	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F板体尺寸 (W11)	112*112		



BOTTOM VIEW

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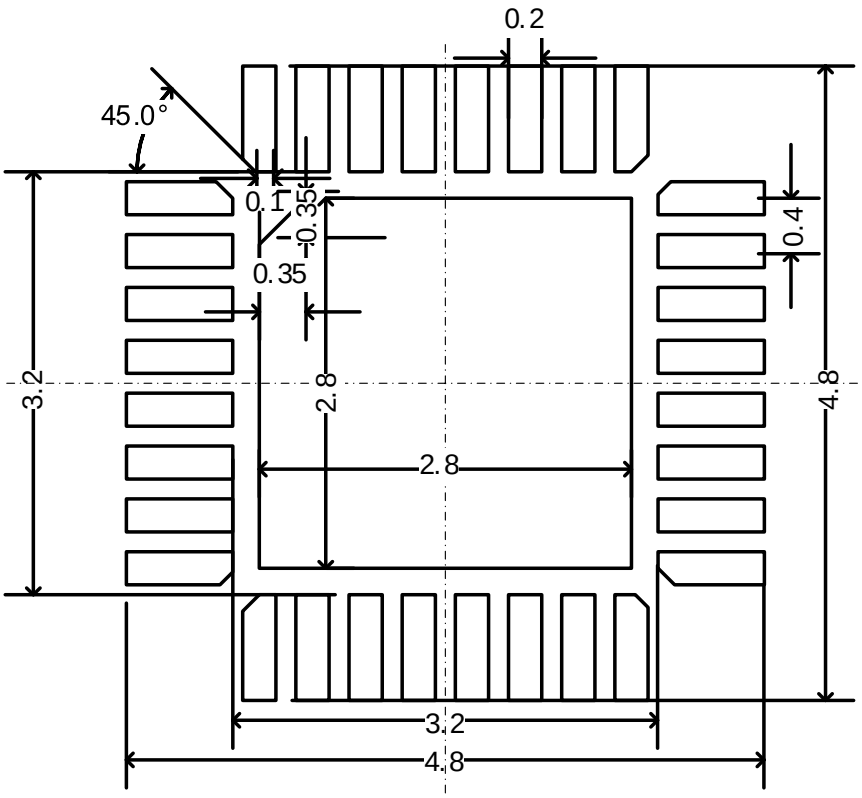
RECOMMENDED FOOTPRINT

QFN32L (0404x0.75-0.4)



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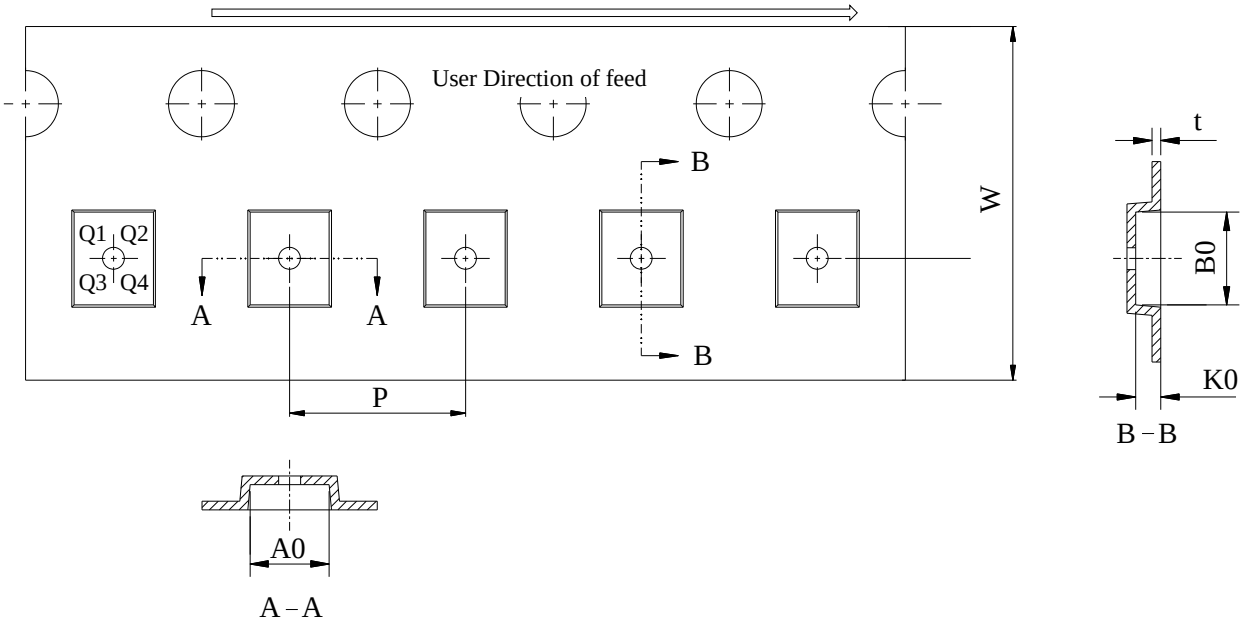
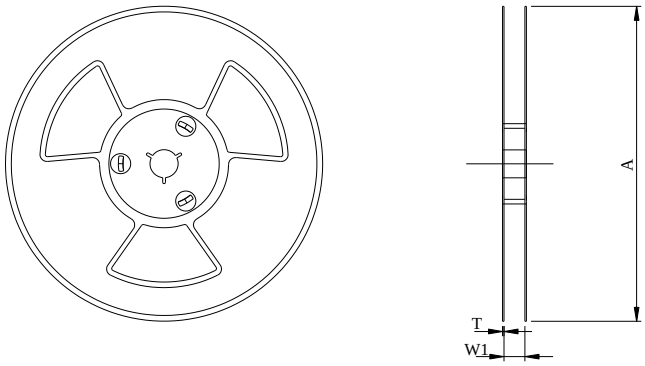
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00±0.30	8.0±0.10	4.30±0.10	4.30±0.10	1.10±0.10	0.30±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	329±1	12.8±1	2±0.3

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