SC8741Q 36V / 100W Automotive Buck-Boost Converter with Low-Side MOSFETs Integrated and I2C Interface

1. Descriptions

The SC8741Q is a buck-boost converter with two low-side integrated power switches capable of regulating the output voltage at, above, or below the input voltage. The SC8741Q operates over 3.7V to 36V wide input voltage and can output 1V to 22V voltage to support a variety of applications.

The SC8741Q is suitable for USB power delivery application. It can work well with external USB PD controller through I2C interface and provide flexibility of programmable features.

The SC8741Q employs current mode control scheme. The switching frequency could be set at 280kHz/420kHz/560kHz through I2C. The SC8741Q also provides optional spread spectrum to optimize EMI performance.

The SC8741Q offers output over-voltage protection, cycle-by-cycle current limit, output short circuit protection, average output current limit and thermal shutdown protection

The SC8741Q is available in 20-pin 3mm X 5mm Wettable Flank QFN packages.

2. Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range: -40°C to 125 °C
- Integrated gate driver for high-side power switches
- 4V to 36V start up input voltage, support 3.7V falling V_{IN}
- 1V to 22V output voltage range
- Programmable Power Supply (PPS) support for USB power delivery
  - Programmable reference voltage range: 0.1V – 1.123V with 1mV resolution
  - Programmable output current limit up to 6.35A with 50mA step
  - +/- 5% accurate average output current limiting
- I2C Interface for:
  - 280k/420k/560kHz frequency selectable
  - Auto PFM / Forced PWM
  - Spread spectrum dithering
  - Line drop compensation
  - Current limit setting
- Battery short to ground protection driver
- External biased VCC for higher efficiency
- Output OCP / SCP / OVP / TSD protection

3. Applications

- Automotive Infotainment
- Automotive ADAS
- Automotive USB Charging
- Automotive Wireless Charging
- Automotive Lighting

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4. Device Information

ORDER NUMBER	INPUT VOLTAGE OVP	DEFAULT OUTPUT	I2C ADDRESS	PACKAGE	BODY SIZE
SC8741QQFPR	YES	ON	67H	FCQFN-20	3mm x 5mm x 0.9mm
SC8741AQQFPR	YES	OFF	67H	FCQFN-20	3mm x 5mm x 0.9mm
SC8741DQQFPR	NO	ON	67H	FCQFN-20	3mm x 5mm x 0.9mm
SC8741FQQFPR	YES	ON	68H	FCQFN-20	3mm x 5mm x 0.9mm

5. Revision History

Revision	Date	Page(s) Changed	Changes Description
V1.0.4	2024/10	/	• Add SC8741FQQFPR information
V1.0.5	2025/2	P21	• Correct 0x13[6] register description error

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6. Typical Application Circuit

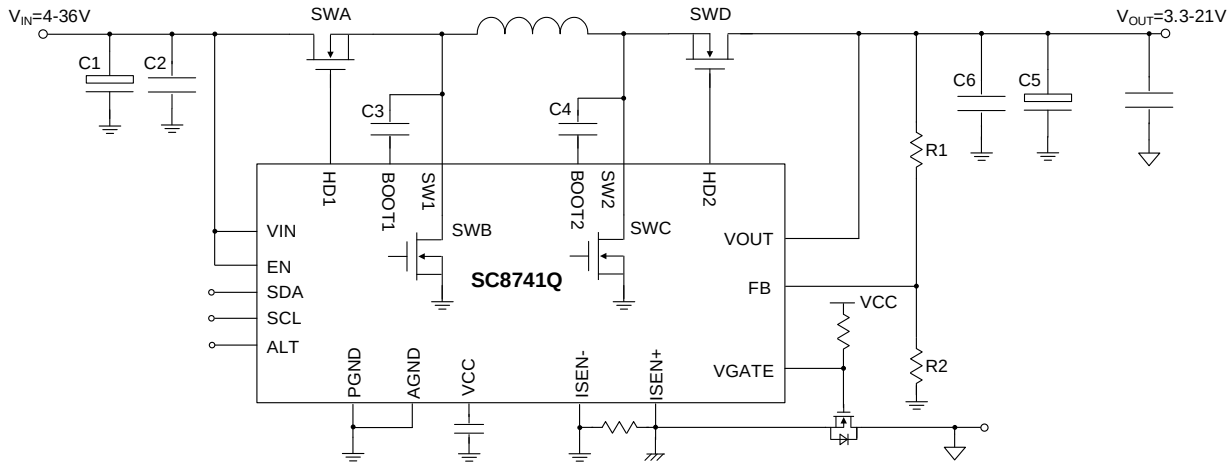

Figure 6-1. Typical Application Circuit for USB Charging

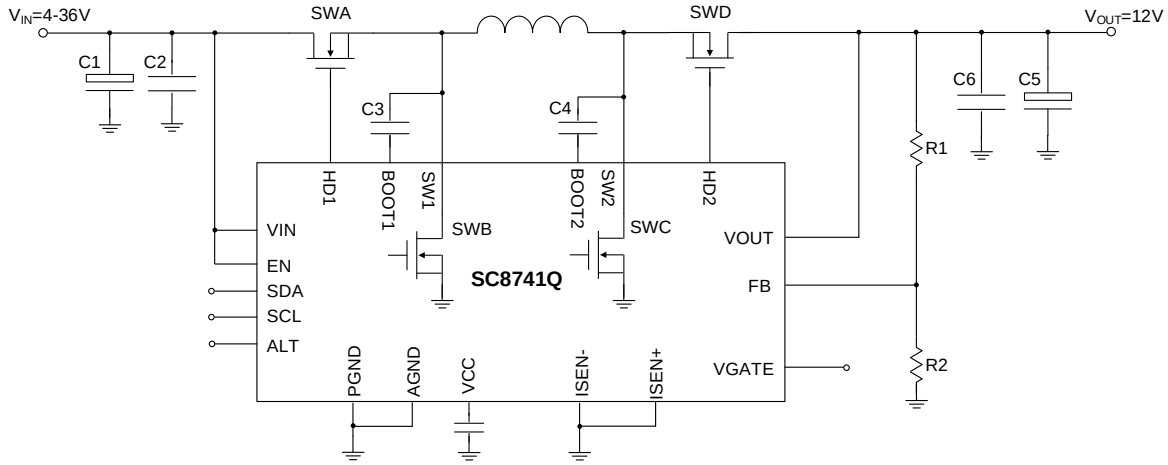

Figure 6-2. Typical Application Circuit for ADAS or Automotive Lighting

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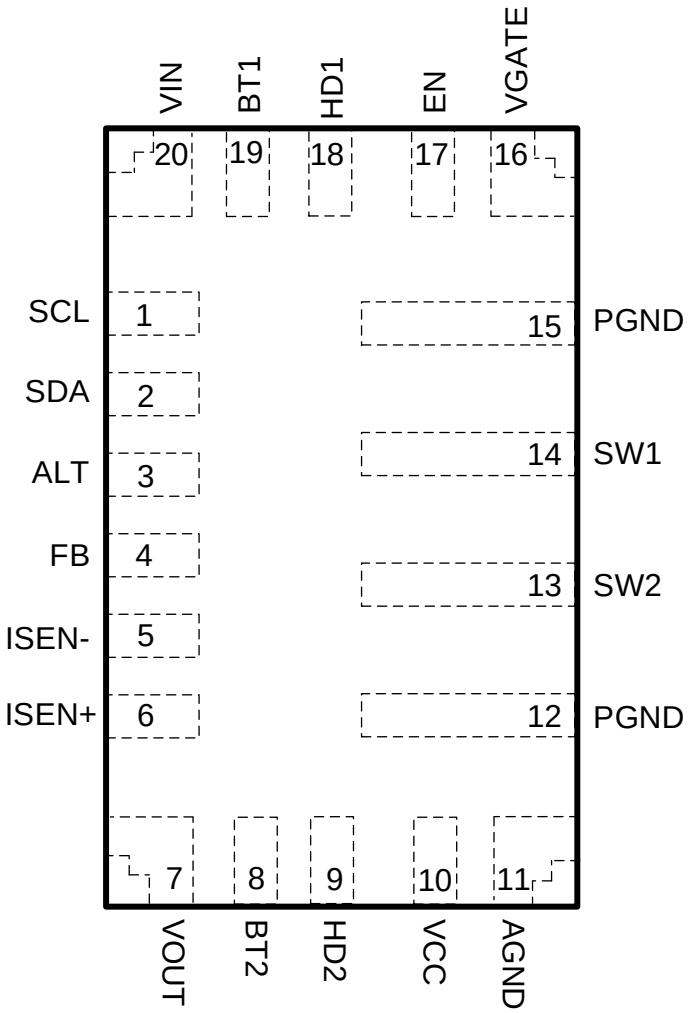
7. Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	SCL	I	Clock of I2C interface.
2	SDA	I	Data of I2C interface.
3	ALT	O	I2C alert pin. Open drain output, active low.
4	FB	I	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage.
5	ISEN-	I	Negative node of current sense signal input. An optional current sense resistor could be placed between PGND to output capacitor's GND.

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6	ISEN+	I	Positive node of current sense signal input. An optional current sense resistor could be placed between PGND to output capacitor's GND.
7	VOUT	O	Output of the buck-boost converter. It's also used to provide VCC supply at certain V_{OUT} condition.
8	BT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW2 pin.
9	HD2	O	Gate driver output for high-side MOSFET in boost side
10	VCC	O	Internal LDO regulator output. Decouple with a 4.7μF capacitor between this pin and the AGND pin.
11	AGND	-	Signal ground of the IC.
12	PGND	-	Power ground of the IC.
13	SW2	O	Switching node pin of the boost side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
14	SW1	O	Switching node pin of the buck side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
15	PGND	-	Power Ground. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias.
16	VGATE	O	Gate drive pin to drive external MOSFET to do ground short to battery protection.
17	EN	I	EN input. Apply logic high to enable the chip.
18	HD1	O	Gate driver output for high-side MOSFET in buck side
19	BT1	O	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW1 pin.
20	VIN	PWR	Input power supply for the IC.

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8. Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN, EN, SW1	-0.3	40	V
	VOUT, SW2	-0.3	25	V
	BST1, HD1	SW1-0.3	SW1+6	V
	BST2, HD2	SW2-0.3	SW2+6	V
	All other pins	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3), all pins	-1000	1000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range after start up	3.7		36	V
V_{OUT}	Output voltage range	1		22	V
F_{SW}	Buck switching frequency range	280	420	560	kHz
I_{OUT}	Output DC current range	0		6	A
L	Effective inductance range	3.3	4.7	6.8	uH
T_J	Operating junction temperature	-40		150	°C

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8.4 Thermal Information

THERMAL RESISTANCE		FCQFN20 (3mm x 5mm)	UNIT
Θ_{JA} (1)	Junction to ambient thermal resistance (JESD 51-7)	39	°C/W
Θ_{JA} (2)	Junction to ambient thermal resistance (SC8741Q EVM)	20	°C/W
Θ_{JC}	Junction to case resistance	2.5	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

(2) Measured on official EVM. 4-layer, 2-oz Cu per top and bottom layer and 1-oz Cu per inner layer, evaluation board.

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 12V and V_{OUT} = 20V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		3.7		36	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		3.9	4.0	V
		V_{IN} falling		3.5	3.7	V
I_Q	Quiescent current into the V_{IN} pin	I2C set on, EN on. No switching, no load.		400	600	μA
	Quiescent current into the V_{OUT} pin	I2C set on, EN on. No switching, no load.		400	600	μA
I_{SD}	Shutdown current into the V_{IN} pin	IC disabled, V_{EN}=0V		1	3.5	μA
V_{CC}	Internal regulator output		4.8	5.0	5.2	V
EN						
$V_{EN_VCC_H}$	EN input level to turn on internal LDO	Rising threshold			1	V
$V_{EN_VCC_L}$	EN input level to turn off internal LDO	Falling threshold	0.4			V
$V_{EN_H_R}$	EN input level to start switching	Rising threshold	1.19	1.22	1.25	V
$V_{EN_H_F}$	EN input level to stop switching	Falling threshold	1.04	1.07	1.10	V
V_{EN_HYS}	Enable threshold hysteresis			150		mV
R_{EN}	EN Pull-down resistor	V_{EN}=2V		2		MΩ
MOSFETS						
$R_{DS(on)}$	Low-side MOSFET on resistance on buck side			18		mΩ
	Low-side MOSFET on resistance on boost side			13.5		mΩ
BOOT UVLO						
V_{BOOT_UVLO}	Falling voltage on BT1/BT2 pin compared to SW1/SW2 which will turn off high-side switch			2.3		V

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REFERENCE VOLTAGE						
V_{FB1}	Feedback Voltage	Set REF [9:0] = 0096h	245	250	255	mV
V_{FB2}		Set REF [9:0] = 00F4h	591	600	609	mV
V_{FB3}		Set REF [9:0] = 03FFh	1.113	1.123	1.135	V
INPUT OVER VOLTAGE PROTECTION						
V_{OVLO_R}	Voltage on V_{IN} pin to stop buck-boost switching		26	27	28	V
V_{OVLO_HYS}	Input voltage protection hysteresis			1.2		V
OUTPUT OVER VOLTAGE PROTECTION						
$V_{OUT_OVP_R}$	Output OVP rising	V_{FB} > 0.25V	115%	120%	125%	V_{FB}
$V_{OUT_OVP_F}$	Output OVP falling		110%	115%	120%	V_{FB}
$V_{OUT_OVP_ABS}$	Output absolute OVP rising		24.3	24.8	25.3	V
$V_{OUT_OVP_HYS}$	Output voltage protection hysteresis			1.1		V
R_{DIS}	Output discharge resistor			180		Ω
INTERNAL CLOCK						
F_{SW1}	Oscillator frequency	V_{IN}=12V, V_{OUT}=6V		280		kHz
F_{SW2}				420		
F_{SW3}				560		
T_{ON_MIN}	Min on time	Boost low side MOSFET		75		ns
T_{OFF_MIN}	Min off time	Buck low side MOSFET		75		ns
SOFT START						
T_{SS}		For 5V_{OUT} condition		0.8		ms
CURRENT LIMIT						
V_{SENS1}	ISENS OC threshold	OC threshold=1A, Rsens=5mΩ	4.25	5	5.75	mV
V_{SENS2}		OC threshold=3.6A, Rsens=5mΩ	17.1	18	18.9	mV
V_{SENS3}		OC threshold=6A, Rsens=5mΩ	28.5	30	31.5	mV
I_{LIMIT1}	Buck low-side valley current limit		6.5	9.0	11.5	A
I_{LIMIT2}	Boost low-side peak current limit	Set_ILIM[7]=0b	9	12	15	A
		Set_ILIM[7]=1b	15	19	23	A
LINE DROP COMPENSATION						
V_{DROP}	Line drop compensation	Set_CDC[6:5]=01b, R1=90.9kΩ, Rsense=5mΩ, I_{OUT}=3A		100		mV
		Set_CDC[6:5]=10b, R1=90.9kΩ, Rsense=5mΩ, I_{OUT}=3A		300		mV

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		Set_CDC[6:5]=11b, R1=90.9kΩ, R_{SENSE} =5mΩ, I_{OUT}=3A		600		mV
HICCUP						
T_{HICCUP}	Hiccup on timer			4		ms
	Hiccup off timer			80		ms
V_{HICCUP}	Hiccup voltage on output			0.8		V
SPREAD SPECTRUM						
FS_{range}	Frequency dithering span			14		%
f_m	Modulation frequency	Change with switching frequency		1/128		F_{SW}
MODE TRANSITION						
V_{MODE_TH1}	Buck-boost to buck transition threshold	V_{IN} / V_{OUT}		120		%
V_{MODE_TH2}	Buck-boost to boost transition threshold	V_{IN} / V_{OUT}		85		%
HIGH SIDE GATE DRIVER						
V_{BUCK_PU}	Buck high side high-state voltage drop	V_{BT1} - V_{HD1}, 100mA sourcing		0.22		V
V_{BUCK_PD}	Buck high side low-state voltage drop	V_{HD1} - V_{SW1}, 100mA sinking		0.085		V
V_{BOOST_PU}	Boost high side high-state voltage drop	V_{BT2} - V_{HD2}, 100mA sourcing		0.13		V
V_{BOOST_PD}	Boost high side low-state voltage drop	V_{HD2} - V_{SW2}, 100mA sinking		0.11		V
INTERNAL REFERENCE VDAC						
V_{VDAC_REF}	Voltage DAC range	100mV offset	0.1		1.123	V
N_{DAC_CV}	CV loop vref resolution			10		Bits
K_{VOUT_RATIO}	Ratio from V_{OUT} to the input of reference comparator			1/20		
INTERNAL REFERENCE IDAC						
V_{IDAC_REF}	Current DAC range		0		1.27	V
N_{DAC_CC}	CC loop Iref resolution			7		Bits
I2C INTERFACE						
V_{IH}	Input logic high		1.3			V
V_{IL}	Input logic low				0.4	V
ALERT						
R_{ALT}	ALT pin pull low resistance				20	Ω
POWER GOOD INDICATION						
$V_{PG_R_L}$	PG lower rising threshold	V_{REF}>0.25V	80%	85%	90%	V_{FB}
$V_{PG_F_L}$	PG lower falling threshold		75%	80%	85%	V_{FB}
$V_{PG_R_H}$	PG upper rising threshold	V_{REF}>0.25V	115%	120%	125%	V_{FB}

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$V_{PG_F_H}$	PG upper falling threshold		110%	115%	120%	V_{FB}
BATTERY SHORT TO GROUND						
I_{SC}	GND short to battery ISENS threshold	OC threshold=20A, R_{SENS} =5mΩ		100		mV
		OC threshold=20A, R_{SENS} =10mΩ		200		mV
T_{SC_TRY}	Short to battery retry delay			1		s
THERMAL SHUTDOWN (1)						
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			20		°C

(1) Design Guarantee

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8.6 Typical Characteristics

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7μH, F_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.

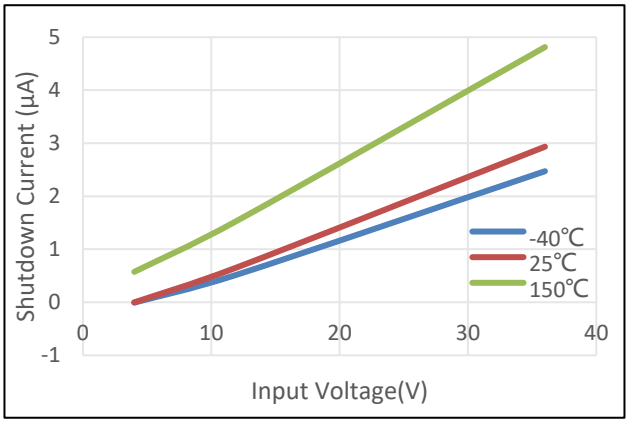

Figure 8-1. Shutdown Current

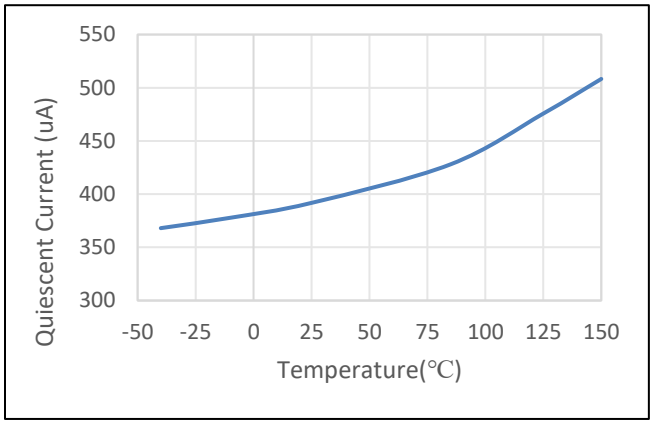

Figure 8-2. Quiescent Current

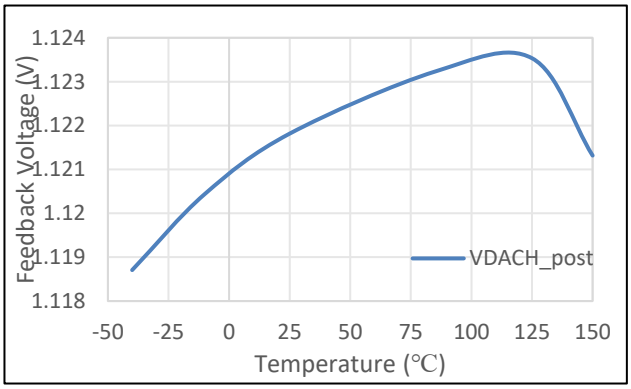

Figure 8-3. Feedback Voltage

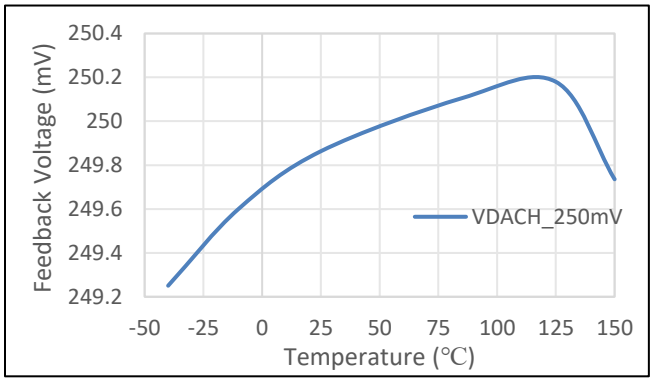

Figure 8-4 Feedback Voltage – 250mV

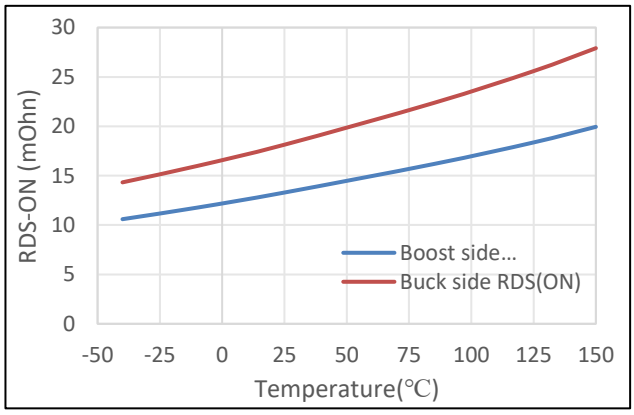

Figure 8-5. Buck-side and Boost-side on resistor

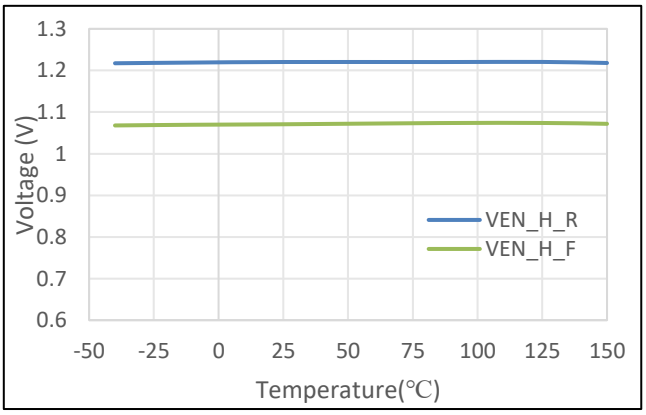

Figure 8-6. EN Threshold

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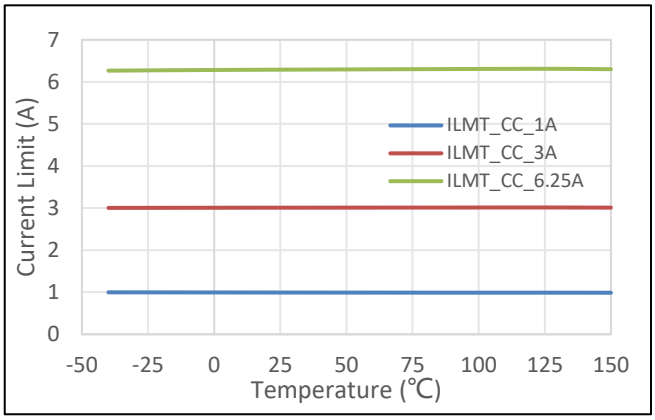

Figure 8-7. CC Current Limit

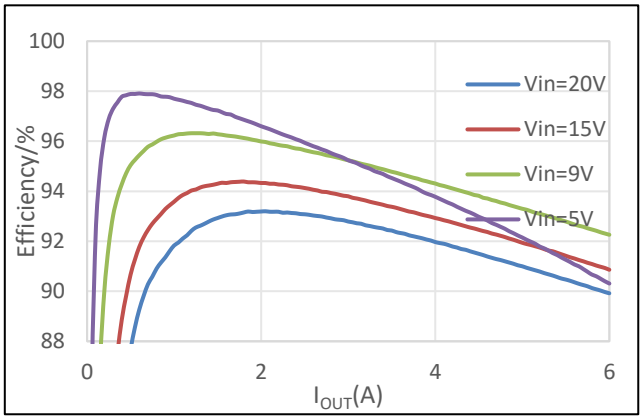

Figure 8-8. Efficiency at fixed 5V output

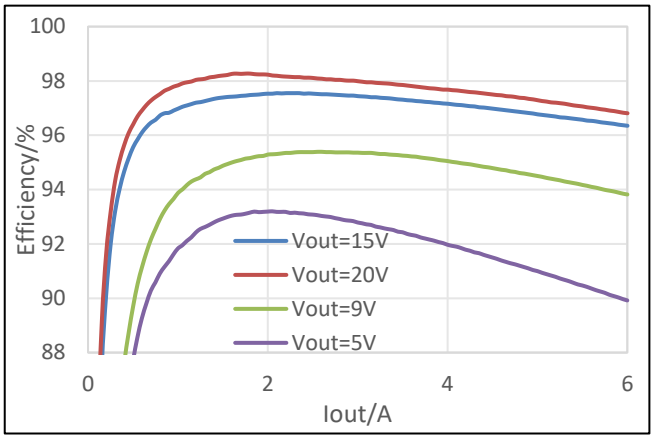

Figure 8-9. Efficiency at fixed 20V input

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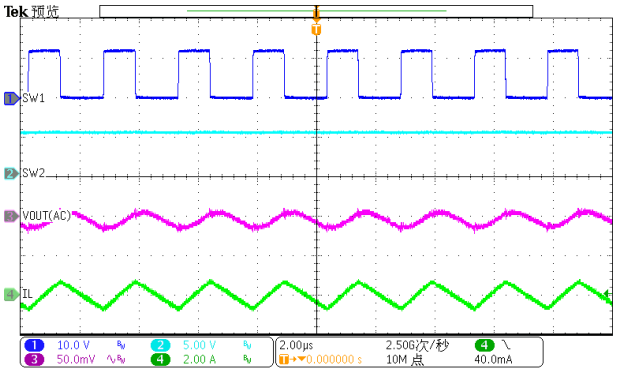
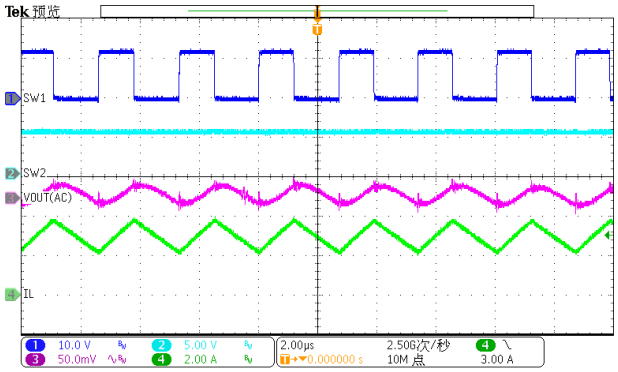
8.7 Application Curves

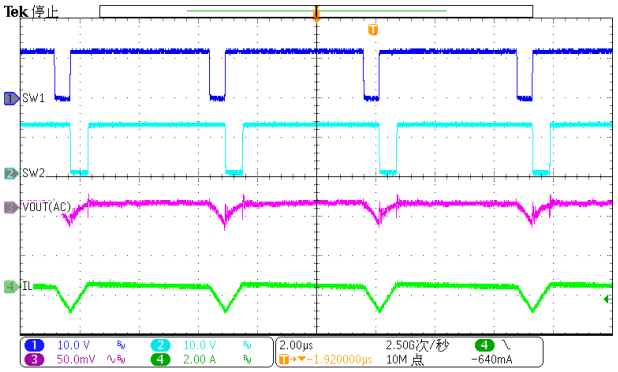
V_{IN} = 12V, L = 4.7μH, F_{SW} = 420kHz, forced PWM mode, T_A = 25°C, unless otherwise noted.



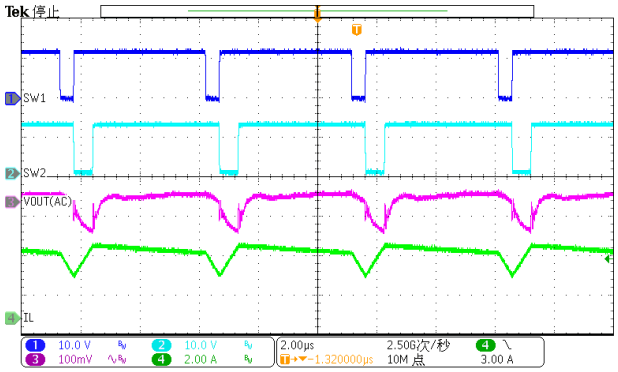
V_{OUT} = 5V, Output Ripple, I_{OUT} = 0A



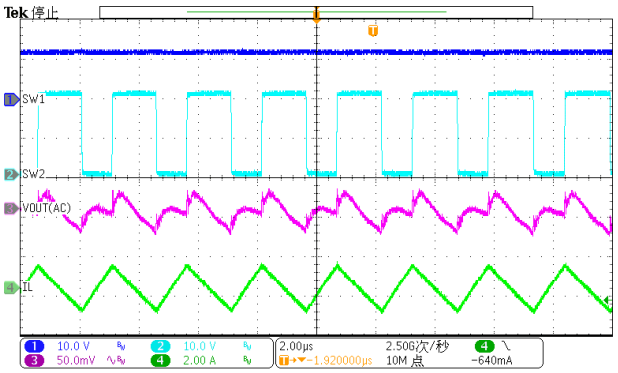
V_{OUT} = 5V, Output Ripple, I_{OUT} = 3A



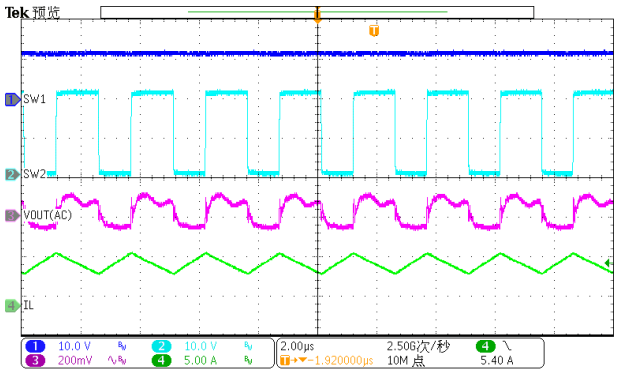
V_{OUT} = 12V, I_{OUT} = 0A output ripple



V_{OUT} = 12V, I_{OUT} = 3A output ripple



V_{OUT} = 20V, I_{OUT} = 0A output ripple



V_{OUT} = 20V, I_{OUT} = 3A output ripple

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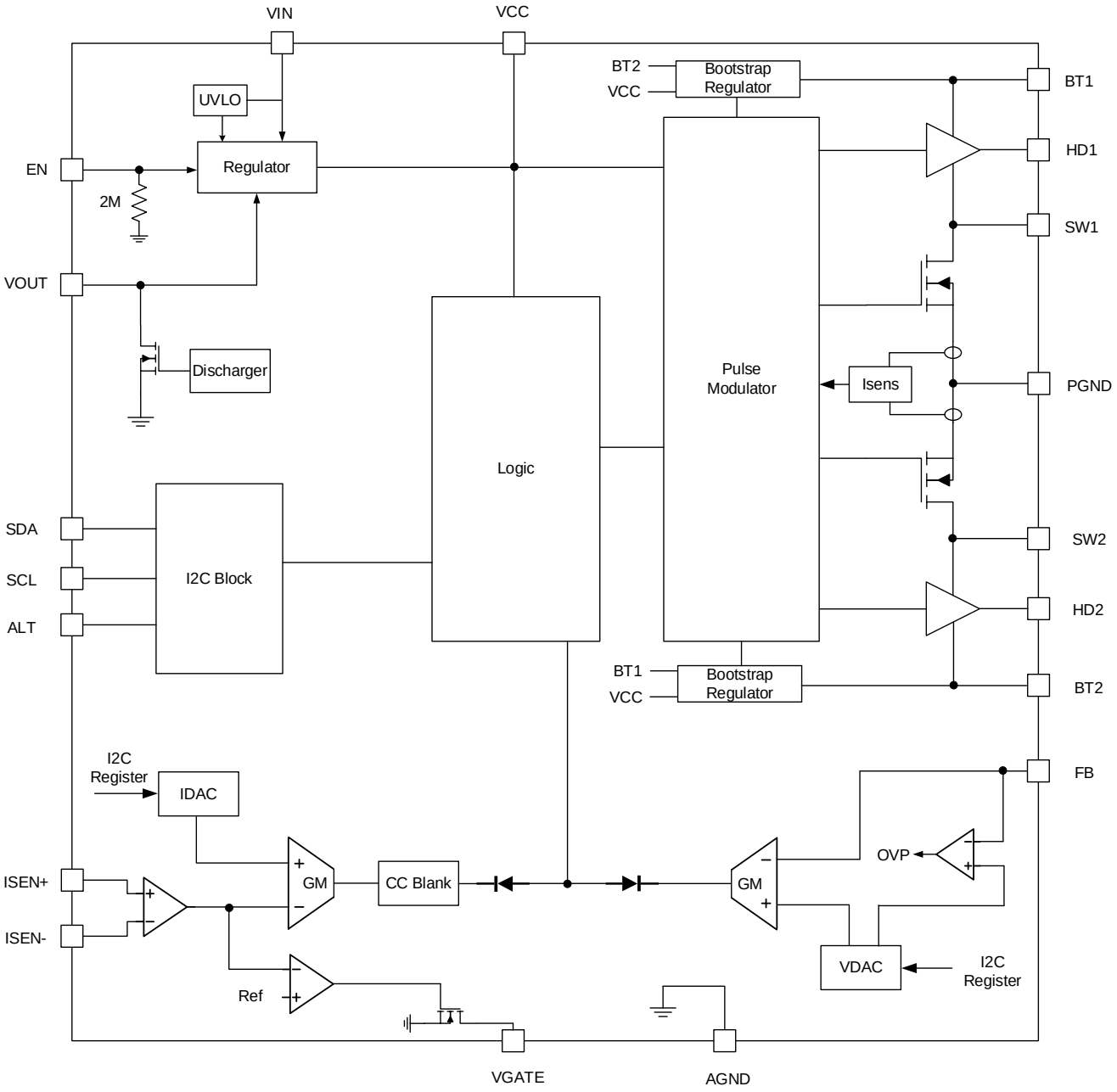
9 Functional Block Diagram



10 Feature Description

10.1 Overview

SC8741Q is a wide range of 3.7-V to 36-V input voltage and an output voltage of 1.0-V to 22-V buck-boost DCDC converter with two low side MOSFETs integrated. It can transition among buck mode, buck-boost mode, and boost mode smoothly when the input voltage is higher or lower than the output voltage. Implementing valley-current mode control in buck mode and peak-current mode control in boost mode, SC8741Q is able to provide excellent line and load transient performance. SC8741Q could be configured during three frequency options 280kHz / 420kHz/ 560kHz to achieve small filter size or higher efficiency.

10.2 Device Operation Modes

10.2.1 Buck Mode

When the input voltage is higher than output voltage, SC8741Q works in buck mode. The buck side MOSFET SWA and SWB switch for the buck regulation, while boost side MOSFET SWC is off and SWD keeps on to conduct the inductor current.

In buck modes, SC8741Q employs adaptive ON time and valley current control. SWA turns on once the inductor current trigger COMP control signal. After an adaptive ON time, SWB turn on to conduct the inductor current.

10.2.2 Boost Mode

When the input voltage is lower than output voltage, SC8741Q works in boost mode. The boost side MOSFET SWC and SWD switch for the boost regulation, while buck side MOSFET SWB is off and SWA keeps on to conduct the inductor current.

In boost modes, SC8741Q employs peak current control and adaptive OFF time. SWC turns on to conduct the inductor current until it rises to trigger the control signal. After SWC turns off, SWD will turn on and remain for adaptive time to regulate the output voltage.

10.2.3 Buck-Boost Mode

When the input voltage is close to the output voltage, SC8741Q works in buck-boost mode. The MOSFET turning on sequence are SWA&SWC -> SWA&SWD -> SWB&SWD.

10.3 VCC Power Supply

An internal LDO to supply SC8741Q outputs regulated 5-V at the VCC pin. The power source will be different according to V_{IN} and V_{OUT} voltage:

(1) If V_{IN} and V_{OUT} are both higher than 6V, SC8741Q powers VCC from the lower voltage source of them to reduce power-loss.
(2) If V_{IN} and V_{OUT} are both lower than 6V, SC8741Q powers VCC from the higher voltage source of them to get enough VCC voltage.
(3) If V_{IN} is higher than 6V and V_{OUT} is lower than 6V, the VCC will select the source from V_{IN}.
(4) If V_{OUT} is higher than 6V and V_{IN} is lower than 6V, the VCC will select the source from V_{OUT}.

Both VCC and BT should have enough voltage to enable SC8741Q. A high-quality ceramic cap of 4.7μF or higher is required between this pin and AGND.

10.4 Input Undervoltage Lockout

When the input voltage is above than 4V, the SC8741Q can be enabled by pulling EN pin to a high voltage above 1.3V. When it starts running, SC8741Q wouldn't be disabled until the input voltage is below 3.7V.

10.5 EN Control

The SC8741Q has an enable control pin (EN). The voltage on the EN pin controls the ON/OFF operation. A voltage of less than 0.4V shuts down the device, while a voltage of greater than 1.0V is required to start the device. The EN pin is an input and cannot be left floating.

SC8741Q EN is a high voltage pin, it can be connected to V_{IN} directly or through resistor. It could be established a precision system UVLO level by inserting resistors. An external logic signal can also be used to drive EN input for system sequencing and protection.

10.6 Soft Start

The integrated soft-start circuit prevents input inrush current and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. If the output of SC8741Q is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

10.7 Output Current Limit and Hiccup

The output current limit is programmable from 0A to 6.35A by placing a 5mΩ current sensing resistor between ISNS+ pin and the ISNS- pin. If output current exceeds the set constant current limit threshold, SC8741Q will enter constant current limit mode. In this mode the current amplitude is limited. As the reducing of load resistance, output voltage drops. Once the output voltage is lower than

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0.8V and the device trigger the switching current limit, SC8741Q will enters hiccup mode to periodically restart the part. The SC8741Q exits hiccup mode once the output voltage is higher than 0.8V or the switching current limit is not triggered.

10.8 Switching Current Limit

SC8741Q provides valley current limit in buck mode and peak current limit in boost and buck-boost mode by sensing LS-FET current. In buck mode, the next period won't start before IL drops to the valley current limit, which prevents inductor current runaway during short circuits on the output.

10.9 Output Over-Voltage Protection

SC8741Q has output overvoltage protection. When the output voltage at the V_{OUT} pin is detected above 23.5V typically or the output voltage is higher than 120% of VREF, the SC8741Q turns off both high-side switches and low-side switches. The discharge path from V_{OUT} pin to ground will turn on. If the V_{OUT} pin voltage drops to 22V, or FB voltage drops to 110% of VREF, the device will return to normal operation.

10.10 Integrated Gate Drivers

The SC8741Q provides two N-channel MOSFET gate drivers for buck side and boost side. Buck-side driver is capable of sourcing 2.2A and sinking 0.7A peak current, while boost-side driver is capable of sourcing 1.3A and sinking 0.5A peak current. In buck mode operation, HD1 switches while HD2 keeps continuously on. In boost mode operation, HD2 switches while HD1 keeps continuous on. Capacitors between BT1 to SW1 and BT2 to SW2 are necessary to supply the power, which is powered by internal diode from VCC or charge them by each other.

10.11 Switching Frequency and Spread Spectrum Function

SC8741Q frequency could be selectable at 280kHz, 420kHz and 560kHz with a 2-bit FREQ register. Normally a 420kHz frequency is recommended. SC8741Q has a frequency spread spectrum function, which could help minimize the peak emissions. SC8741Q uses a triangle wave to modulate the internal oscillator, whose frequency is 1/128 of the switching frequency. The frequency span of the spread spectrum operation is 14%. The Spread Spectrum function will be disable at Auto PFM mode.

10.12 Shutdown and Load Discharge

When the Input voltage is lower than 3V or EN pin voltage is pulled down below 0.4V, the SC8741Q is in shutdown mode and all functions are disabled. All internal registers are reset to default values. SC8741Q integrates output discharge function when the output voltage needs to be discharged to the goal voltage.

10.13 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. SC8741Q has a 10-bit DAC to program the reference voltage from 100mV to 1.123V. The output voltage could be calculated with the formula as below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB_UP}}{R_{FB_DOWN}}\right) \quad (1)$$

10.14 Output Line Drop Compensation

SC8741Q is capable of compensating an output voltage drop, which is helpful when there is high impedance at the output side. The compensated voltage is impacted the output current, sense resistors and the line drop compensation gain. Refer to the register map description for detail line drop compensation amplitude.

10.15 Battery Short to Ground Protection Driver

SC8741Q integrates a gate driver to realize the battery short to ground protection. Once the output ground short to battery, SC8741Q sensed the voltage across the sense resistor exceeds 100mV, VGATE pin will be pulled low and isolate MOSFET will be turned off. When battery short to ground happened, DCDC will also be turned off but the device won't reset.

10.16 Thermal Shutdown

SC8741Q is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165C(Typical). The internal soft-start circuit is reset but all internal registers values remain unchanged. The DCDC portion will automatically restarts when the junction temperature drops below the thermal shutdown hysteresis.

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11 Application Information

11.1. Capacitor Selection

SC8741Q has three frequency options of 280kHz / 420kHz/ 560kHz. Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60μF X5R or X7R capacitors with higher voltage rating then operating voltage with margin is recommended. For example, if the highest operating V_{IN} (V_{OUT}) voltage is 12V, 25V voltage rating capacitor is recommended.

The high capacitance polymer capacitor or tantalum capacitor can be used for input and output but capacitor voltage rating must be higher than the highest operating voltage with enough margin. The high frequency characteristics of these capacitors are not as good as ceramic capacitor, so at least 10μF ceramic capacitor should be placed in parallel to reduce high frequency ripple.

11.2. Inductor Selection

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). Normally 2.2 μH to 6.8 μH inductor is recommended here.

The peak inductor current can be calculated as:

$$I_{L_PEAK} = I_{OUT} + \frac{V_{OUT}\cdot(V_{IN} - V_{OUT})}{2\cdot F_{SW}\cdot L\cdot V_{IN}\cdot\eta} \quad (V_{IN}>V_{OUT}) \qquad (2)$$

$$I_{L_PEAK} = I_{IN} + \frac{V_{IN}\cdot(V_{OUT}-V_{IN}\cdot\eta)}{2\cdot F_{SW}\cdot L\cdot V_{OUT}} \quad (V_{IN}\le V_{OUT}) \qquad (3)$$

η is the power conversion efficiency. User can use 95% for calculation.

F_{SW} is the switching frequency

L is the inductor value

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$P_{L_DC} = I_L^2\cdot DCR \qquad (4)$$

IL is the average value of inductor current.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have small ESR at high frequency and small core loss.

11.3. Current Sense Resistor

The ISNS+ and ISNS- are current sense resistors. 5 mΩ should be used to sense the current (10 mΩ supports higher battery current limit accuracy, and 5 mΩ supports higher efficiency). Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4. BOOT Capacitor Selection

The SC8741Q requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the high-side power MOSFET. A high-quality (X7R) ceramic capacitor of 100nF and at least 50V is recommended.

11.5. BOOT Resistor Selection

A BOOT resistor and capacitor can be connected in series between the BOOT and SW pins. Unless EMI for the application being designed is critical, R_{BOOT} can be shorted. To maximize efficiency, 0 Ω is chosen for this example. Under most circumstances, selecting an R_{BOOT} resistor value above 20Ω is undesirable since the resulting small improvement in EMI is not enough to justify further decreased efficiency.

11.6. VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a 4.7μF, 16V ceramic capacitor connected from VCC to GND for proper operation. Avoid loading this output with any external circuitry.

11.7. MOSFET Selection

The IC integrates two power MOSFETs, and the user should add two external power MOSFETs at high side.

The V_{DS} of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher). For example, if the highest operating

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voltage is 20V, at least 30V rated V_{DS} MOSFET should be selected; If the highest operating voltage is 24V, 40V V_{DS} voltage rating should be selected.

The V_{GS} voltage rating of MOSFET should be selected higher than 8V. Considering PCB parasitic parameters during operation, MOSFET V_{GS} voltage might be higher than V_{DRV} voltage due to transient overshoot, so 10V V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest battery current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at T_A=70˚C or T_C = 100˚C should be considered. In addition, the power dissipation value P_D should also be considered and higher P_D is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

The MOSFET $R_{DS(ON)}$ and input capacitor C_{ISS} impact power efficiency directly. Typically, lower $R_{DS(ON)}$ MOSFET has higher C_{ISS}. The $R_{DS(ON)}$ is related to conduction loss. Higher R_{DSON} results in higher conduction loss, thus lower efficiency and higher thermal dissipation; the C_{ISS} is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSEFT should be selected based on tradeoff between the $R_{DS(ON)}$ and C_{ISS}.

If high C_{ISS} MOSFET is selected, the switching on and off time become longer, then the dead time should be adjusted to avoid simultaneous turn on for both high side and low side MOSFETs.

11.8. Driver Resistor and SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add series resistor for gate driving signal (HD1 to MOS gate, and HD2 to MOS gate), and RC snubber circuit at SW1 and SW2

The driver resistor should be placed near MOS. At first, use 0Ω resistors; if switching overshoot is big, increase the resistor value to slow down the switching speed. It is suggested to keep the resistor value < 10 Ω. While the switching speed gets slower, the default dead time may not be enough to avoid overshoot of the power MOSFETs. So if higher than 10Ω is needed, user should increase the dead time if necessary.

The RC snubber circuit at SWx node is also helpful in absorbing the high frequency spike at SWx node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

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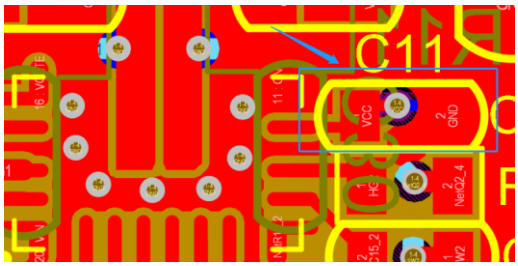
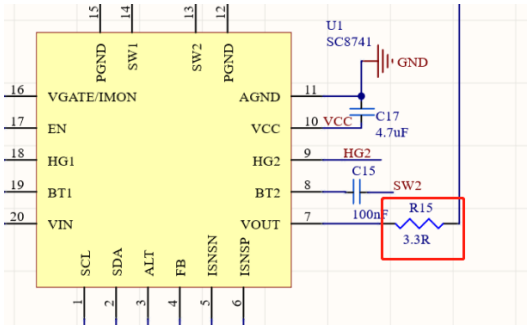
12 Layout Guide

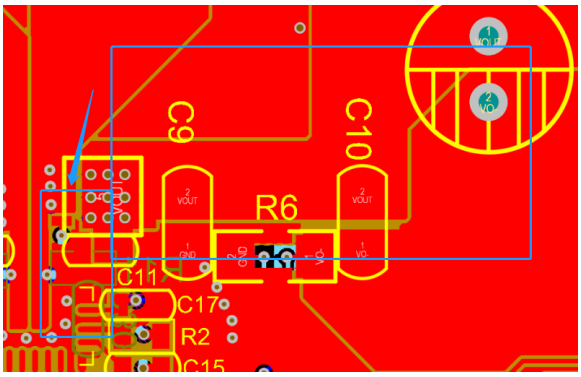
1. The 1μF ~ 4.7μF capacitors connected at VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.



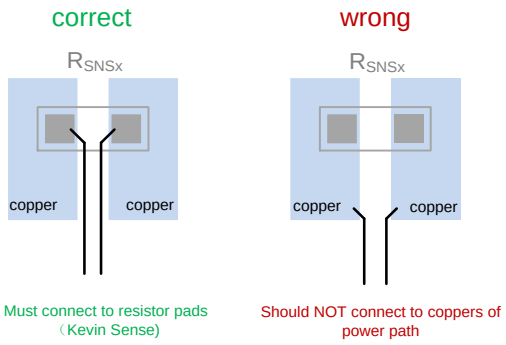
2. If APFM is used, V_{OUT} pin should not connect any resistor. But if APFM is not used, this limit is invalid.



3. Put I_{OUT} current sense resistor, MOSFETs and bulk capacitor at V_{OUT} side as close as possible. And the low side MOSFET and bulk capacitors should be very close to PGND pins. Between current sense resistor and high side MOS, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to MOS and PGND pins.



4. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and add filter for each current sense near the IC.



Current sense

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Register Maps

The 7-bit I2C address of the chip is 0x67H or 0x68H.

Addr	Name	Type	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	OPERATION	R/W	ON/OFF	NA						
0x10	VREF	R/W	VDAC_REG [7:0]							
0x11			VDAC_RESERVED [5:0]						VDAC_REG [9:8]	
0x12	I_LIMIT	R/W	EN_CC	IDAC_REG						
0x13	MODE_CTROL	R/W	RSNS	BB2T_REG	CDC_GAIN		OCP_DLY		VDAC_SLEW_RATE	
0x14	MODE_CTROL	R/W	DTHR	FPWM	HICCUP	DISCHG	OVP	FREQUENCY		ILIMIT
0x15	STATUS	R	NA						PG_FLAG	CC_FLAG
0x16	FLAG	R1C	NA			VOUT_OV_FLAG	ILMTH_FLAG	GND_SHRT_FLAG	OTP_FLAG	VOUT_SHRT_FLAG
0x17	MASK	R/W	NA			VOUT_OV_MASK	ILMTH_MASK	GND_SHRT_MASK	OTP_MASK	VOUT_SHRT_MASK

Table 0x00H Operation Command

Bit	Type	Bit Name	Default	Description
7	R/W	ON/OFF State	Depends on different part number	0b: The output is off 1b: The output is on.
6:0	NA			

Table 0x10H-11H Reference Voltage Register

Bit	Type	Bit Name	Default	Description
15 - 10	R/W	Reserved	000000b	Reserved
9-0	R/W	REF	10010110b	00 00000000b = 100mV 00 00000001b = 101mV …… **00 1001 0110b = 250mV** …… 01 1111 0100b = 600mV …… 11 11111111b = 1123mV

Table 0x12H IOUT_LIMIT Register

Bit	Type	Bit Name	Default	Description
7	R/W	EN_CC_DET	1b	Enable or disable current limit 0b = Current limit disabled **1b = Current limit enabled**
6-0	R/W	Current Limit	110 1100b	Based on 5mR R_{SENSE} 000 0000b = 0mA 000 0001b = 50mA …… 100 0001b = 3.25A …… **110 1100b = 5.4A** …… 111 1111b = 6.35A

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Table 0x13H Status Register

Bit	Type	Bit Name	Default	Description
7	R/W	RSNS	Depends on different part number	Select the Rsens resistor value: 0: 5mΩ, Current Sense Gain=40 1: 10mΩ, Current Sense Gain=20
6	R/W	BB2T_REG	1b	Set frequency mode under Buck-boost condition: '0': keep the same frequency as Buck and Boost mode **'1' Reduce frequency to half of Buck and Boost mode.**
5:4	R/W	CDC_GN_REG	00b	Set output voltage compensation value vs. load current: @5mR, R1=90.9k (Upper feedback resistor) **00: no compensation** 01: V_{OUT} compensates 100mV@3A Iout 10: V_{OUT} compensates 300mV@3A Iout 11: V_{OUT} compensates 600mV@3A Iout
3:2	R/W	OCP_DELAY	Depends on different part number	Set the deglitch time of the device when the output overcurrent limit reached 00b = 400us; 01b = 5ms 10b = 8ms; 11b = 12ms
1:0	R/W	VDAC_SLEW_RATE	01b	Set the VREF adjust rising slew rate. '00': 0.04mv/us Vref changing slew rate; **'01': 0.08mv/us Vref changing slew rate;** '10': 0.2mv/us Vref changing slew rate; '11": 0.4mv/us Vref changing slew rate; Default is "01". V_{OUT}_Slew rate=Vref_slew rate * Feedback Ratio.

Table 0x14H Mode Control Register

Bit	Type	Bit Name	Default	Description
7	R/W	Dither Enable	1b	"0" No dither **"1" Enable spread spectrum function**
6	R/W	APFM/FPWM	1b	"0" APFM **"1" Forced PWM**
5	R/W	HICCUP	1b	"0" Disable Hiccup function **"1" Enable Hiccup function**
4	R/W	DISCHG	1b	"0" Disable output voltage discharge **"1" Enable output voltage discharge**
3	R/W	Output OVP	1b	"0" No output OVP function **"1" Enable output OVP**
2:1	R/W	FREQ	01b	"00" 280kHz; **"01" 420kHz** "10" 560kHz; "11" Reserved
0	R/W	Switching Current Limit	1b	SWC Peak Current Limit "0": 12A **"1": 19A**

Table 0x15H STATUS Register

Bit	Type	Bit Name	Default	Description
7:2	NA			
1	R	PG_STATUS	1b	When this bit is set '1', the output voltage is not good; When this bit is clear, the output voltage is power good.
0	R	CC_STATUS	1b	When this bit is set '1', the IC is in CC mode; When this bit is '0', the CC mode exits.

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Table 0x16H FLAG Register

Bit	Type	Bit Name	Default	Description
7:5	NA			
4	R	VOUT_OV_FLAG	0b	If an output over voltage fault (Absolute OV or higher than 120% VREF) occurred, this bit will be set to '1'.
3	R	ILIMIT_LFAG	0b	If an output over current occurred, valley current limit or peak current limit triggered, this bit will be set to '1'.
2	R	GND_SHORT_FLAG	0b	If GND short to battery fault occurred, this bit will be set to '1'.
1	R	OTP_FLAG	0b	If over temperature fault occurred, this bit will be set to '1'
0	R	VOUT_SHORT_FLAG	0b	If output voltage below than 0.8V, this bit will be set to '1'.

Table 0x17H MASK Register

Bit	Type	Bit Name	Default	Description
7:5	NA			
4	R/W	VOUT_OV_MASK	1b	0: Not mask **1: Mask Enabled**
3	R/W	ILIMIT_MASK	1b	0: Not mask **1: Mask Enabled**
2	R/W	GND_SHORT_MASK	1b	0: Not mask **1: Mask Enabled**
1	R/W	OTP_MASK	1b	0: Not mask **1: Mask Enabled**
0	R/W	VOUT_SHORT_MASK	1b	0: Not mask **1: Mask Enabled**

The different default value of SC8741Q / SC8741AQ / SC8741DQ

Address / Bit	Bit Name	SC8741Q/SC8741DQ	SC8741AQ
0x00H [7]	EN_DCDC	ON	OFF
0x12H [6:0]	Current Limit	5.4A	5.4A
0013H [7]	RSNS	5m	10m
0013H [3:2]	OCP_DELAY	400μs	5ms
0013H [1:0]	VDAC_SLEW_RATE	0.08mV/μs	0.08mV/μs
0x14H [7]	Dither Enable	YES	YES
0x14H [6]	APFM/FPWM	FPWM	FPWM
0x14H [4]	DISCHG	ON	ON

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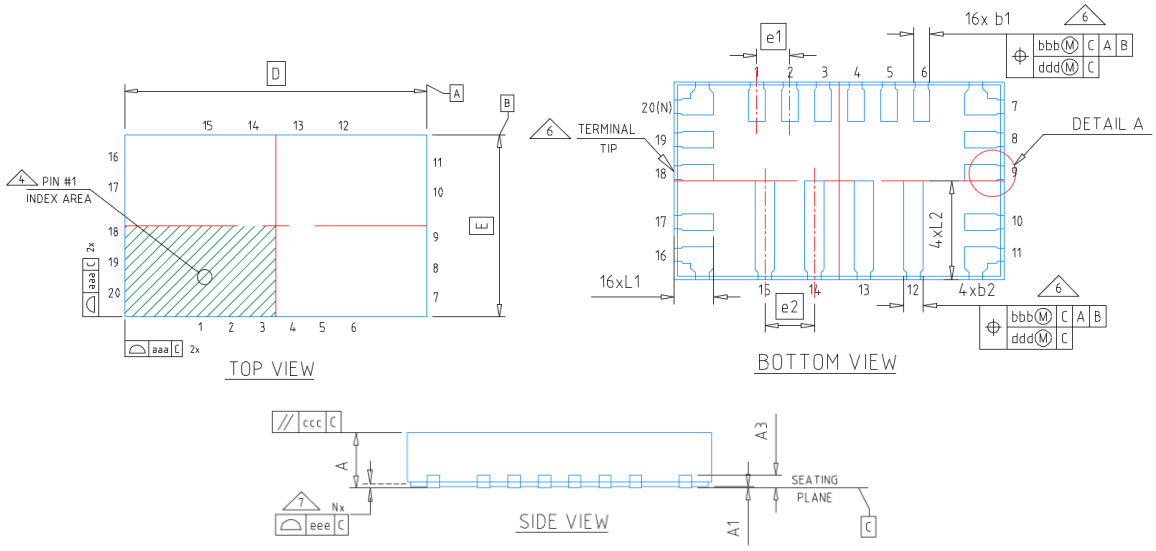
MECHANICAL DATA

Flipchip-QFN20(3x5)



Dimension Table			
Thickness / Symbol	V		
	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.203 Ref.	---
b1	0.20	0.25	0.30
b2	0.25	0.30	0.35
D	5.00 BSC		
E	3.00 BSC		
e1	0.50 BSC		
e2	0.75 BSC		
L1	0.50	0.60	0.70
L2	1.40	1.50	1.60
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	20		
ND	6/4		
NE	5		

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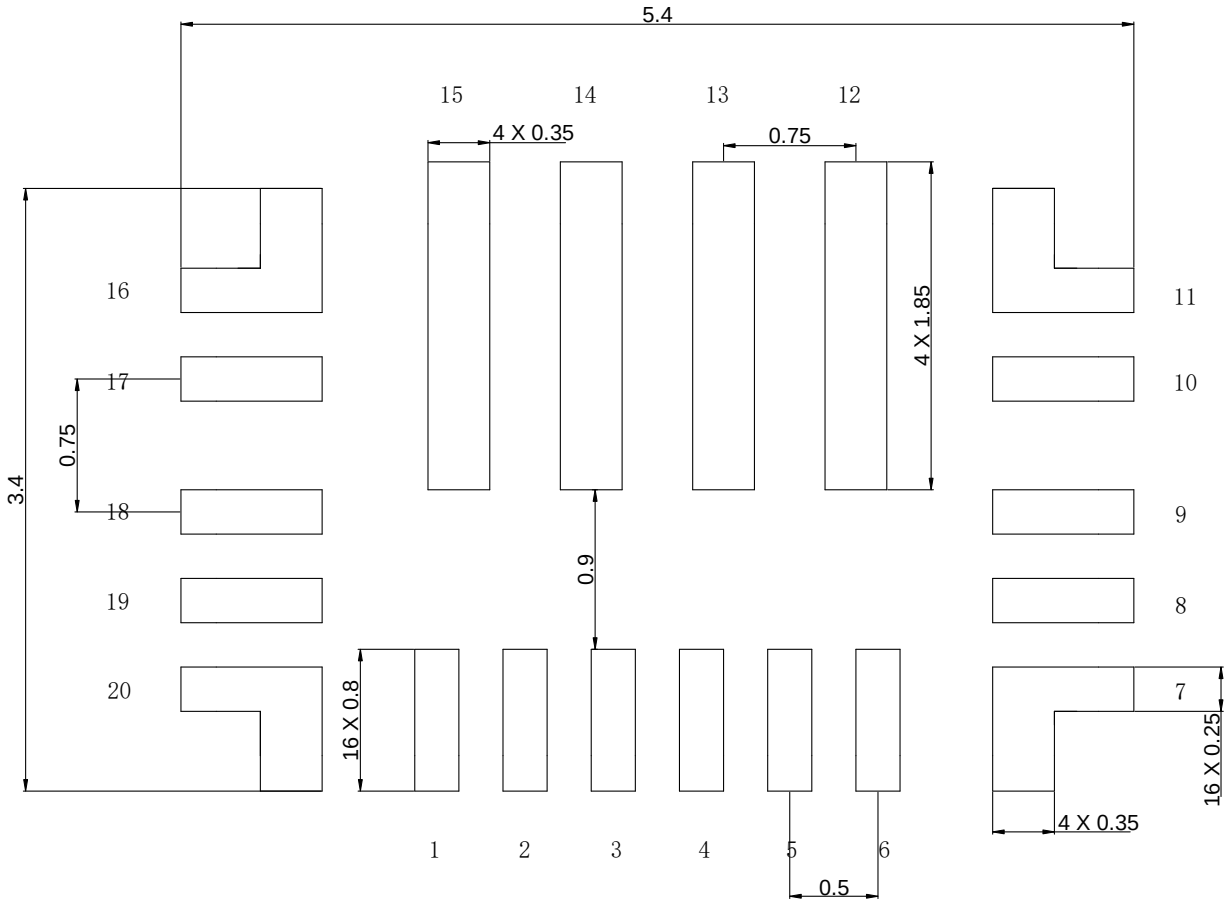
RECOMMENDED FOOTPRINT



Unit: mm

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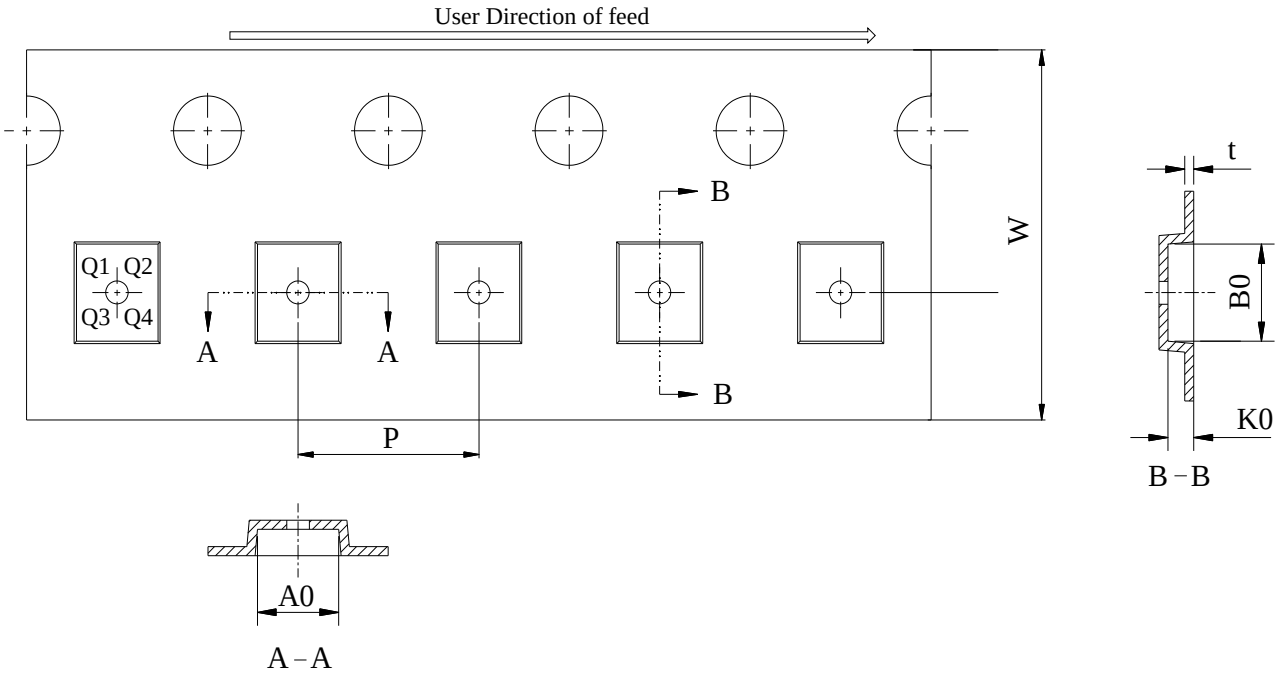
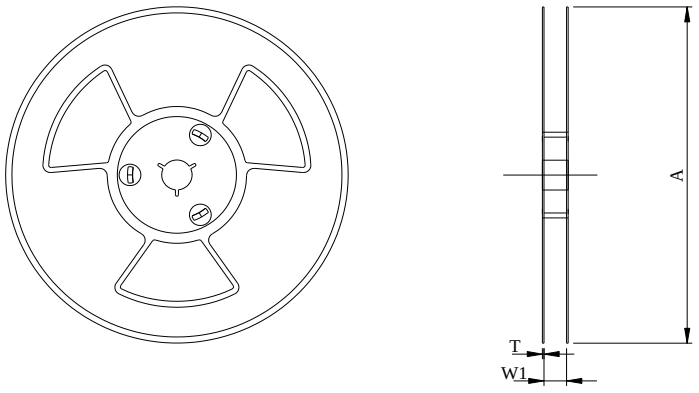
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 + 0.30/- 0.10	8.00 +/- 0.10	3.25 ±0.10	5.25 ±0.10	1.10 ±0.10	0.30 ±0.03	Q1

REEL



Item	A	W1	T
Size (mm)	330±2	12.4 +2/-0	2.1±0.15

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