
SC8745Q 36V / 140W Buck-Boost Converter with Low-Side MOSFETs Integrated and I2C Interface

1 Descriptions

The SC8745Q is a buck-boost converter with two low-side integrated power switches capable of regulating the output voltage at, above, or below the input voltage. The SC8745Q operates over 3.7V to 36V wide input voltage and can output 1V to 29V voltage to support a variety of applications.

The SC8745Q is suitable for USB power delivery application. It can work well with external USB PD controller through I2C interface and provide flexibility of programmable features.

The SC8745Q employs current mode control scheme. The switching frequency could be set at 280kHz/420kHz/560kHz through I2C. The SC8745Q also provides optional spread spectrum to optimize EMI performance.

The SC8745Q offers input/output over-voltage protection, cycle-by-cycle current limit, output short circuit protection, average output current limit and thermal shutdown protection.

The SC8745Q is available in 20-pin 3mm x 5mm Wettable Flank QFN packages.

2 Applications

- Automotive Wireless Charging
- Automotive USB Charging
- Automotive ADAS

3 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: T_A range: -40°C to 125°C
- Integrated gate driver for high-side power switches
- 4V to 36V start up input voltage, support 3.7V falling V_{IN}
- 1V to 29V output voltage range
- Programmable Power Supply (PPS) support for USB power delivery
 - Programmable reference voltage range: 0.1V – 1.123V with 1mV resolution
 - Programmable output current limit up to 6.35A with 50-mA step @ $R_{SENSE}=5\text{m}\Omega$
 - Programmable output current limit up to 8A with 62.5-mA step @ $R_{SENSE}=4\text{m}\Omega$
 - +/- 5% accurate average output current limiting
- I2C Interface for:
 - 280k/420k/560kHz frequency selectable
 - Auto PFM / Forced PWM
 - Spread spectrum dithering
 - Line drop compensation
 - Current limit setting
- IMON for output current
- External biased V_{CC} for higher efficiency
- Output OCP / SCP / OVP / TSD protection



4 Device Information

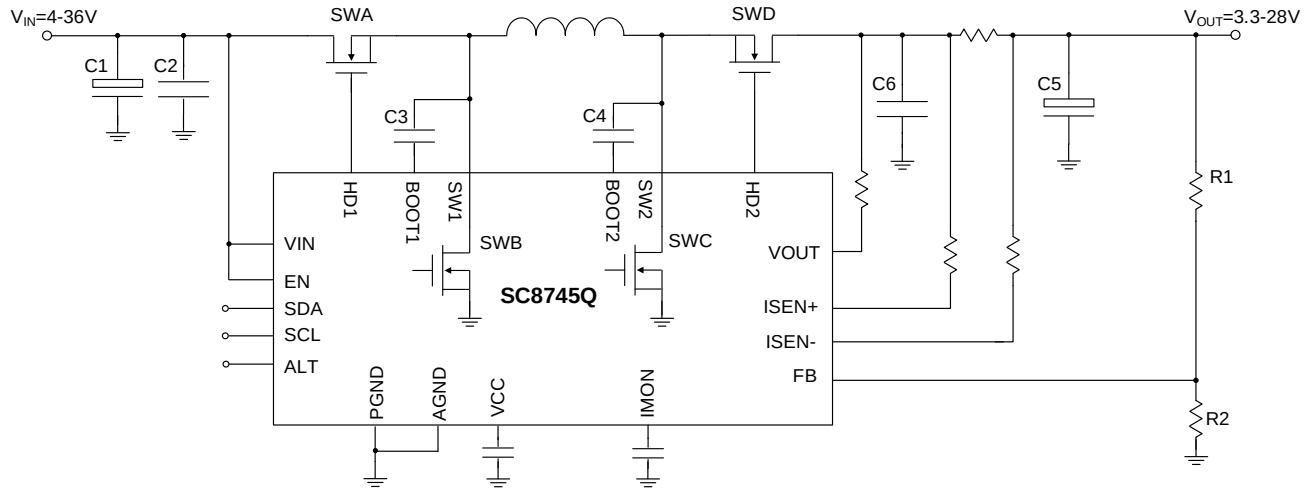
ORDER NUMBER	INPUT VOLTAGE OVP	I2C ADDRESS	DEFAULT OUTPUT	PACKAGE	BODY SIZE
SC8745QQFPR	YES	67H	ON	FCQFN-20	3mm x 5mm x 0.85mm
SC8745AQQFPR	NO	67H	OFF	FCQFN-20	3mm x 5mm x 0.85mm
SC8745DQQFPR	NO	67H	ON	FCQFN-20	3mm x 5mm x 0.85mm
SC8745FQQFPR	NO	68H	ON	FCQFN-20	3mm x 5mm x 0.85mm

5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.0.5	2026/7	21	1. The I2C register sheet on the table of different default value check has been deleted.
V1.0.4	2026/4	19	1. Update the RSNS bit description
V1.0.3	2025/7	/	1. Update the typos in register map
V1.0.2	2025/4	/	1. Update the maximum current capability
V1.0.1	2025/4	/	1. Add limit of EC table parameters 2. Update the R_{DIS} to 800 Ω



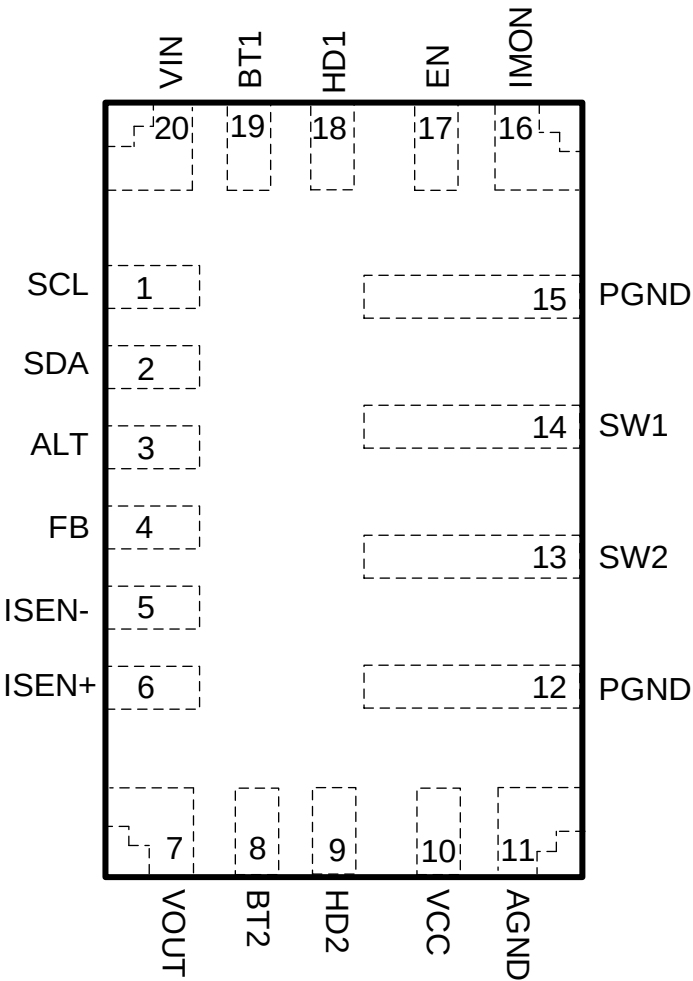
6 Typical Application Circuit





7 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	SCL	I	Clock of I2C interface
2	SDA	I	Data of I2C interface
3	ALT	O	I2C alert pin. Open drain output, active low
4	FB	I	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage.
5	ISEN-	I	Negative node of current sense signal input. An optional current sense resistor could be placed between VOUT cap and SWD



6	ISEN+	I	Positive node of current sense signal input. An optional current sense resistor could be placed between VOUT cap and SWD.
7	VOUT	O	Output of the buck-boost converter. It's also used to provide V_{CC} supply at certain V_{OUT} condition.
8	BT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW2 pin.
9	HD2	O	Gate driver output for high-side MOSFET in boost side
10	VCC	O	Internal LDO regulator output. Decouple with a 4.7 μF capacitor between this pin and the AGND pin.
11	AGND	PWR	Signal ground of the IC.
12	PGND	PWR	Power ground of the IC.
13	SW2	I	Switching node pin of the boost side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
14	SW1	I	Switching node pin of the buck side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
15	PGND	I	Power ground. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias.
16	IMON	O	Voltage monitor for output current.
17	EN	I	EN input. Apply logic high to enable the chip.
18	HD1	O	Gate driver output for high-side MOSFET in buck side
19	BT1	I	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW1 pin.
20	VIN	PWR	Input power supply for the IC.



8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C ~ 150°C (unless otherwise noted) ⁽¹⁾

PARAMETER		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	VIN, EN, SW1	-0.3	40	V
	VOUT, SW2, ISNS+, ISNS-	-0.3	32	V
	BST1, HD1	SW1-0.3	SW1+6	V
	BST2, HD2	SW2-0.3	SW2+6	V
	All other pins	-0.3	6	V
T _J	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	-2	2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾ , all pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range after start up	3.7		36	V
V _{OUT}	Output voltage range	1.0		29	V
F _{SW}	Buck switching frequency range	280	420	560	kHz
I _{OUT}	Output DC current range @ R _{SENSE} = 5mR	0		6.35	A
	Output DC current range @ R _{SENSE} = 4mR	0		8	A
L	Effective inductance range	3.3	4.7	10	μH
T _J	Operating junction temperature	-40		150	°C



8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		FCQFN20 (3mm x 5mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	39	°C/W
Θ_{JC}	Junction to case resistance	2.5	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

8.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 150°C , $V_{IN} = 12\text{V}$ and $V_{OUT} = 20\text{V}$. Typical value is tested at $T_J = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		3.7		36	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising	3.7	3.9	4.0	V
		V_{IN} falling	3.5	3.6	3.7	V
I_Q	Quiescent current into the VIN pin	I2C set on, EN on. No switching, no load.		350	600	μA
I_{SD}	Shutdown current into the VIN pin	IC disabled, $V_{EN}=0\text{V}$		1	3.5	μA
V_{CC}	Internal regulator output		4.85	5.1	5.3	V
I_{CC_LIMIT}	V_{CC} current limit		100	170		mA
EN						
$V_{EN_VCC_H}$	EN input level to turn on internal LDO	Rising threshold			1	V
$V_{EN_VCC_L}$	EN input level to turn off internal LDO	Falling threshold	0.4			V
V_{EN_H}	EN input level to start switching	Rising threshold	1.19	1.22	1.25	V
V_{EN_L}	EN input level to stop switching	Falling threshold	1.04	1.07	1.10	V
V_{EN_HYS}	Enable threshold hysteresis			150		mV
R_{EN}	EN Pull-down resistor	$V_{EN}=2\text{V}$		2		MΩ
MOSFETS						
$R_{DS(ON)}$	Low-side MOSFET on resistance on buck side			18	30	mΩ
	Low-side MOSFET on resistance on boost side			12	20	mΩ
BOOT UVLO						
V_{BOOT_UVLO}	Falling voltage on BT1/BT2 pin compared to SW1/SW2 which will turn off high-side switch		2.1	2.3	2.5	V
REFERENCE VOLTAGE						
V_{FB1}	Feedback Voltage	REF = 0096h	245	250	255	mV
V_{FB2}		REF = 01F4h	591	600	609	mV



V _{FB3}		REF = 03FFh	1.113	1.123	1.135	V
OUTPUT OVER VOLTAGE PROTECTION						
V _{OUT_OVP_R}	Output OVP rising	V _{FB} > 0.25V	115%	120%	125%	V _{FB}
V _{OUT_OVP_F}	Output OVP falling		110%	115%	120%	V _{FB}
V _{OUT_OVP_ABS}	Output absolute OVP rising		29	30	32	V
V _{OUT_OVP_HYS}	Output voltage protection hysteresis		1.1	1.25	1.4	V
R _{DIS}	Output discharge resistor			800	1200	Ω
INTERNAL CLOCK						
F _{SW1}	Oscillator frequency	V _{OUT} =6V, FREQ = 00b	260	280	300	kHz
F _{SW2}		V _{OUT} =6V, FREQ = 01b	385	420	455	
F _{SW3}		V _{OUT} =6V, FREQ = 10b	515	560	605	
T _{ON_MIN}	Min on time	Boost low side MOSFET		75		ns
T _{OFF_MIN}	Min off time	Buck low side MOSFET		75		ns
SOFT START						
T _{SS}		For V _{FB} = 0.25V condition		0.8		ms
CURRENT LIMIT						
V _{SENS1}	ISENS OC threshold	OC threshold=1A, R _{SENS} =5mΩ	4.25	5	5.75	mV
V _{SENS2}		OC threshold=3.6A, R _{SENS} =5mΩ	17.1	18	18.9	mV
V _{SENS3}		OC threshold=6A, R _{SENS} =5mΩ	28.5	30	31.5	mV
I _{LIMIT1}	Buck low-side valley current limit		7.5	9.0	10.5	A
I _{LIMIT2}	Boost low-side peak current limit	SWITCHING CURRENT LIMIT= 0b	10	12	14	A
		SWITCHING CURRENT LIMIT= 1b	16	19	22	A
V _{CCLOOP_EN}	CC loop enable voltage on VOUT			2.2		V
IMON Monitor						
V _{IMON}	Suggested IMON output voltage range		0		2.8	V
t _{IMON_WIDTH}	Establish time for IMON signal	10pF at IMON pin			50	μs
LINE DROP COMPENSATION						
V _{DROP}	Line drop compensation	CDC_GN_REG =01b, R1=90.9kΩ, R _{SENSE} =5mΩ, I _{OUT} =3A		100		mV
		CDC_GN_REG =10b, R1=90.9kΩ, R _{SENSE} =5mΩ, I _{OUT} =3A		300		mV



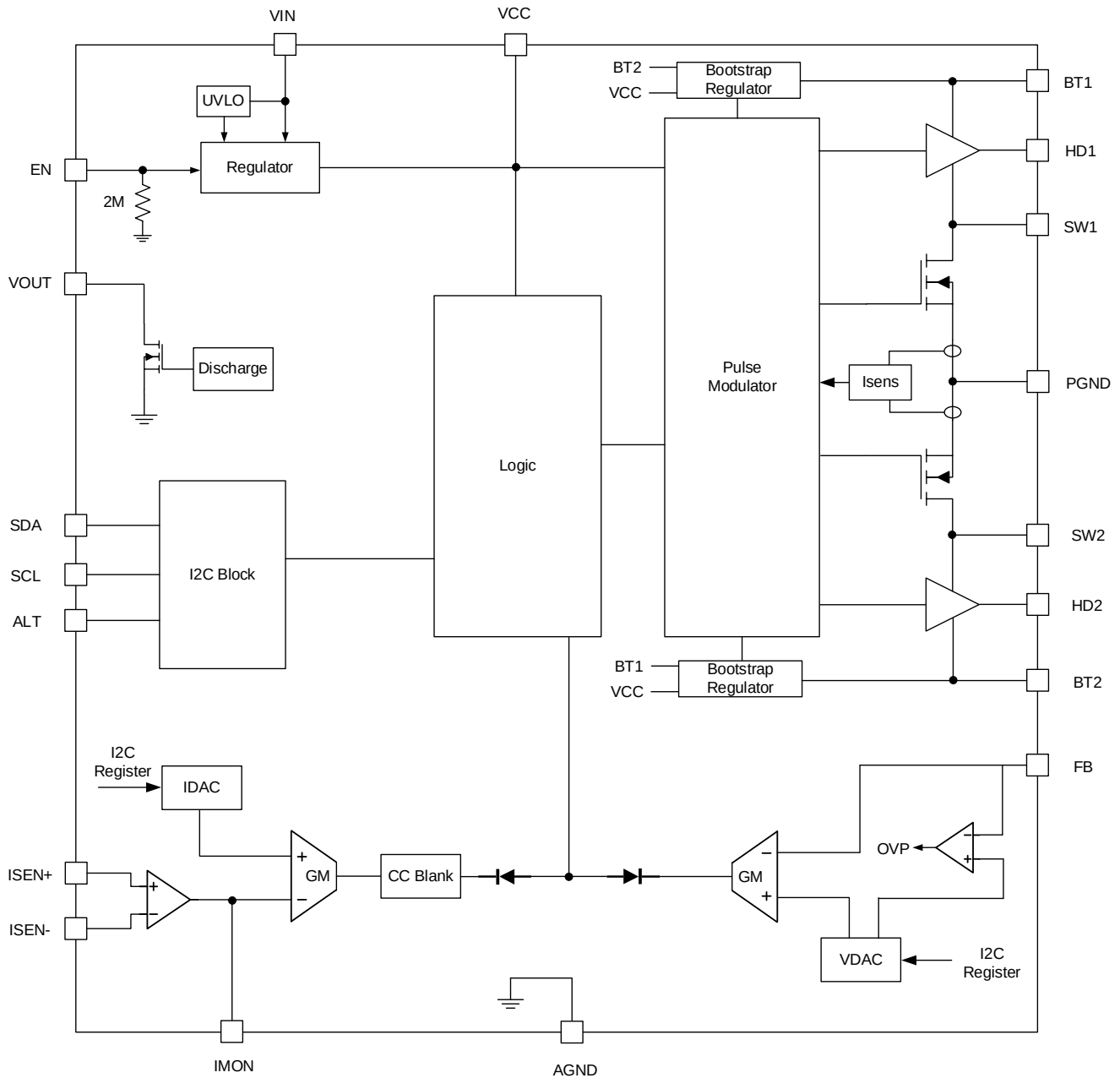
		CDC_GN_REG =11b, R1=90.9k Ω , R _{SENSE} =5m Ω , I _{OUT} =3A	600	mV
HICCUP				
T _{HICCUP}	Hiccup on timer		4	ms
	Hiccup off timer		80	ms
V _{HICCUP}	Hiccup voltage on output		2.3 2.5 2.7	V
SPREAD SPECTRUM				
FS _{range}	Frequency dithering span		14	%
f _m	Modulation frequency	Change with switching frequency	1/128	F _{SW}
MODE TRANSITION				
V _{MODE_TH1}	Buck-boost to buck transition threshold	V _{IN} / V _{OUT}	120	%
V _{MODE_TH2}	Buck-boost to boost transition threshold	V _{IN} / V _{OUT}	85	%
HIGH SIDE GATE DRIVER				
V _{BUCK_PU}	Buck high side high-state voltage drop	V _{BT1} - V _{HD1} , 100mA sourcing	0.22	V
V _{BUCK_PD}	Buck high side low-state voltage drop	V _{HD1} - V _{SW1} , 100mA sinking	0.07	V
V _{BOOST_PU}	Boost high side high-state voltage drop	V _{BT2} - V _{HD2} , 100mA sourcing	0.13	V
V _{BOOST_PD}	Boost high side low-state voltage drop	V _{HD2} - V _{SW2} , 100mA sinking	0.12	V
INTERNAL REFERENCE VDAC				
V _{VDAC_REF}	Voltage DAC range	100mV offset	0.1 1.123	V
N _{DAC_CV}	CV loop V _{REF} resolution		10	Bits
K _{VOUT_RATIO}	Ratio from V _{OUT} to the input of reference comparator		1/20	
INTERNAL REFERENCE IDAC				
V _{IDAC_REF}	Current DAC range		0 1.27	V
N _{DAC_CV}	CC loop I _{REF} resolution		7	Bits
I2C INTERFACE				
V _{IH}	Input logic high		1.3	V
V _{IL}	Input logic low		0.4	V
ALERT				
R _{ALT}	ALT pin pulls low resistance		20	Ω
POWER GOOD INDICATION				
V _{PG_R_L}	PG lower rising threshold	V _{REF} >0.25V	80% 85% 90%	V _{FB}
V _{PG_F_L}	PG lower falling threshold		75% 80% 85%	V _{FB}
V _{PG_R_H}	PG upper rising threshold	V _{REF} >0.25V	115% 120% 125%	V _{FB}



V _{PG_F_H}	PG upper falling threshold		110%	115%	120%	V _{FB}
THERMAL SHUTDOWN						
T _{SD}	Thermal shutdown temperature		165			°C
	Thermal shutdown hysteresis		20			°C



9 Functional Block Diagram





10 Feature Description

10.1 Overview

SC8745Q is a wide range of 3.7V to 36V input voltage and an output voltage of 1V to 29V buck-boost DCDC converter with two low side MOSFETs integrated. It can transition among buck mode, buck-boost mode, and boost mode smoothly when the input voltage is higher or lower than the output voltage. Implementing valley-current mode control in buck mode and peak-current mode control in boost mode, SC8745Q is able to provide excellent line and load transient performance. SC8745Q could be configured during three frequency options 280kHz /420kHz /560kHz to achieve small filter size or higher efficiency.

10.2 Device Operation Modes

10.2.1 Buck Mode

When the input voltage is higher than output voltage, SC8745Q works in buck mode. The buck side MOSFET SWA and SWB switch for the buck regulation, while boost side MOSFET SWC is off and SWD keeps on to conduct the inductor current.

In buck modes, SC8745Q employs adaptive ON time and valley current control. Once the FB voltage drops below reference voltage, SWA will turn on. After an adaptive ON time, SWB turn on to conduct the inductor current until trigger COMP control signal.

10.2.2 Boost Mode

When the input voltage is lower than output voltage, SC8745Q works in boost mode. The boost side MOSFET SWC and SWD switch for the boost regulation, while buck side MOSFET SWB is off and SWA keeps on to conduct the inductor current.

In boost modes, SC8745Q employs peak current control and adaptive OFF time. SWC turns on to conduct the inductor current until it rises to trigger the control signal. After SWC turns off, SWD will turn on and remain for adaptive time to regulate the output voltage.

10.2.3 Buck-Boost Mode

When the input voltage is close to the output voltage, SC8745Q works in buck-boost mode. The MOSFET turning on sequence are SWA&SWC -> SWA&SWD -> SWB&SWD.

10.3 Input Undervoltage Lockout

When the input voltage is above than 4V, the SC8745Q can be enabled by pulling EN pin to a high voltage above 1.3V. When it starts running, SC8745Q wouldn't be disabled until the input voltage is below 3.7V.

10.4 EN Control

The SC8745Q has an enable control pin (EN). The voltage on the EN pin controls the ON/OFF operation. A voltage of less than 0.4V shuts down the device, while a voltage of greater than 1.3V is required to start the device. The EN pin is an input and cannot be left or floating.

SC8745Q EN is a high voltage pin, it can be connected to V_{IN} directly or through resistor. It could be established a precision system UVLO level by inserting resistors. An external logic signal can also be used to drive EN input for system sequencing and protection.

10.5 Soft Start

The integrated soft-start circuit prevents input inrush current and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. If the output of SC8745Q is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal Soft-start capacitor exceeds the internal feedback voltage.

10.6 Output Current Limit and Hiccup

The output current limit is programmable from 0A to 6.35A by placing a 5m Ω current sensing resistor between ISNS+ pin and the ISNS- pin. If output current exceeds the set constant current limit threshold, SC8745Q will enter constant current limit mode. In this mode the current amplitude is limited. The CC loop is only functional when V_{OUT} higher than 2.2V. As the reducing of load resistance, output voltage drops. Once the output voltage is lower than 2.5V, SC8745Q will enters hiccup mode to periodically restart the part. The SC8745Q exits hiccup mode once the output voltage is higher than 2.5V. The hiccup function could be disabled by register.

10.7 Switching Current Limit

SC8745Q provides valley current limit in buck mode and peak current limit in boost and buck-boost mode by sensing LS-FET current. In buck mode, the next period won't start before IL drops to the valley current limit, which prevents inductor current runaway during short circuits on the output.



10.8 Input Over-Voltage Protection

SC8745Q has input overvoltage protection while SC8745DQ doesn't. When the input voltage at the VIN pin is detected above 32V typically, the SC8745Q turns off both high-side switches and low-side switches but the SC8745DQ could keep switching

10.9 Output Over-Voltage Protection

SC8745Q has output overvoltage protection. When the output voltage at the VOUT pin is detected above 30V typically or the output voltage is higher than 120% of V_{REF} , the SC8745Q turns off both high-side switches and low-side switches. The discharge path from VOUT pin to ground will turn on. If the VOUT pin voltage drops to 28.9V, or FB voltage drops to 110% of V_{REF} , the device will return to normal operation.

10.10 Integrated Gate Drivers

The SC8745Q provides two N-channel MOSFET gate drivers for buck side and boost side. Buck-side driver is capable of sourcing 2.2A and sinking 0.7A peak current, while boost-side driver is capable of sourcing 1.3A and sinking 0.5A peak current. In buck mode operation, HD1 switches while HD2 keeps continuously on. In boost mode operation, HD2 switches while HD1 keeps continuous on. Capacitors between BT1 to SW1 and BT2 to SW2 are necessary to supply the power, which is powered by internal diode from V_{CC} or charge them by each other.

10.11 Switching Frequency and Spread Spectrum Function

SC8745Q frequency could be selectable at 280kHz, 420kHz and 580kHz with a 2-bit FREQ register. Normally a 420kHz frequency is recommended. SC8745Q has a frequency spread spectrum function, which could help minimize the peak emissions. SC8745Q uses a triangle wave to modulate the internal oscillator, whose frequency is 1/128 of the switching frequency. The frequency span of the spread spectrum operation is 14%.

10.12 Shutdown and Load Discharge

When the Input voltage is lower than 3V or EN pin voltage is pulled down below 0.4V, the SC8745Q is in shutdown mode and all functions are disabled. All internal registers are reset to default values. SC8745Q integrates output discharge function when the output voltage needs to be discharged to the goal voltage.

10.13 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. SC8745Q has a 10-bit DAC to program the reference voltage from 100mV to 1.123V. The output voltage could be calculated with the formula as below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB_UP}}{R_{FB_DOWN}} \right)$$

10.14 Output Line Drop Compensation

SC8745Q can compensate an output voltage drop, which is helpful when there is high impedance at the output side. The compensated voltage is impacted the output current, sense resistors and the line drop compensation gain. Refer to the register map description for detail line drop compensation amplitude.

10.15 Thermal Shutdown

SC8745Q is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165°C (Typical). The internal soft-start circuit is reset but all internal registers values remain unchanged. The DCDC portion will automatically restarts when the junction temperature drops below the thermal shutdown hysteresis.



11 Application Information

11.1. Capacitor Selection

The switching frequency of the IC is in the range of 280kHz ~ 560kHz. Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60μF X5R or X7R capacitors with higher voltage rating than operating voltage with margin is recommended. For example, if the highest operating V_{IN}/V_{OUT} voltage is 12V, select at least 16V capacitor and to secure enough margin, 25V voltage rating capacitor is recommended.

The high capacitance polymer capacitor or tantalum capacitor can be used for input and output but capacitor voltage rating must be higher than the highest operating voltage with enough margin. The high frequency characteristics of these capacitors are not as good as ceramic capacitor, so at least 10μF ceramic capacitor should be placed in parallel to reduce high frequency ripple.

11.2. Inductor Selection

2.2 μH to 10 μH inductor is recommended for loop stability.

The peak inductor current can be calculated as:

$$I_{L_PEAK} = I_{OUT} + \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{2 \cdot F_{SW} \cdot L \cdot V_{IN} \cdot \eta} \quad (\text{Buck Mode})$$

$$I_{L_PEAK} = I_{IN} + \frac{V_{IN} \cdot (V_{OUT} - V_{IN} \cdot \eta)}{2 \cdot F_{SW} \cdot L \cdot V_{OUT}} \quad (\text{Boost Mode})$$

where I_{OUT} is the output current at V_{OUT} side, and can be calculated as

$$I_{OUT} = \frac{V_{IN} \cdot I_{IN} \cdot \eta}{V_{OUT}}$$

η is the power conversion efficiency. User can use 90% for calculation.

F_{SW} is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$P_{LDC} = I_L^2 \cdot DCR$$

I_L is the average value of inductor current, and it equals to I_{OUT} or I_{IN} .

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have small ESR at high frequency and small core loss.

11.3. Current Sense Resistor

The ISNS+ and ISNS- are current sense resistors. 5 mΩ should be used to sense IOUT current (10 mΩ supports higher battery current limit accuracy, and 5 mΩ supports higher efficiency). Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4. MOSFET Selection

The V_{DS} of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher). For example, if the highest operating voltage is 20V, at least 30V rated V_{DS} MOSFET should be selected; If the highest operating voltage is 24V, 40V V_{DS} voltage rating should be selected.

The V_{GS} voltage rating of MOSFET should be selected higher than 8V. Considering PCB parasitic parameters during operation, MOSFET V_{GS} voltage might be higher than V_{DRV} voltage due to transient overshoot, so 10V V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest battery current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at $T_A=70^\circ\text{C}$ or $T_C = 100^\circ\text{C}$ should be considered. In addition, the power dissipation value P_D should also be considered and higher P_D is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

The MOSFET $R_{DS(ON)}$ and input capacitor C_{ISS} impact power efficiency directly. Typically, lower $R_{DS(ON)}$ MOSFET has higher C_{ISS} . The $R_{DS(ON)}$ is related to conduction loss. Higher $R_{DS(ON)}$ results in higher conduction loss, thus lower efficiency



and higher thermal dissipation; the C_{ISS} is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSFET should be selected based on tradeoff between the $R_{DS(ON)}$ and C_{ISS} .

11.5. Driver Resistor and SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add series resistor (0603 size) for gate driving signal (HD1 to MOS gate and HD2 to MOS gate), and RC snubber (0603 size) circuit at SWx, as shown below.

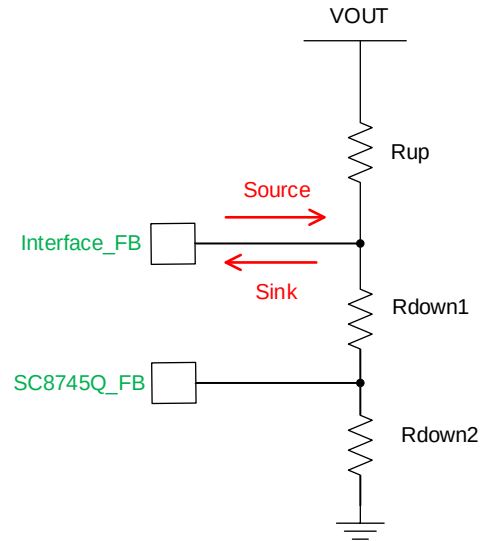
The driver resistor should be placed near MOS. At first, use 0Ω resistors; if switching overshoot is big, increase the resistor value to slow down the switching speed. It is suggested to keep the resistor value $< 10\Omega$. While the switching speed gets slower, the default dead time may not be enough to avoid overshoot of the power MOSFETs.

The RC snubber circuit at SWx node is also helpful in absorbing the high frequency spike at SWx node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and $1nF$ for the snubber. If EMC should be improved further, reduce the resistor value (like 1Ω or even lower) and increase the capacitor value (like $2.2nF$ or even higher).

11.6. External PWM voltage regulation

When using external PWM voltage regulation, since most protocol chips have requirements for FB voltage, the default voltage of SC8745Q FB is only $0.25V$. If directly connected, it will cause the regulated voltage to be lower than the set value.

For this situation, a three-stage resistor can be used to avoid it.



The FB access point of the protocol chip is above the SC8745Q_FB access point, so that the voltage $_{FB}$ the protocol chip is higher than SC8745Q_FB, and the specific calculation relationship is:

$$V_{Interface_FB} = \frac{R_{down1} + R_{down2}}{R_{down2}} * V_{SC8745Q_FB}$$

According to the KCL of the Interface node

$$\frac{V_{out} - V_{Interface_FB}}{R_{up}} = \frac{V_{SC8745Q}}{R_{down2}} + I$$

Where I represent equivalent current, when using PWM voltage regulation,

$$I = \frac{V_{Interface_FB} - V_{PWM}}{R}$$

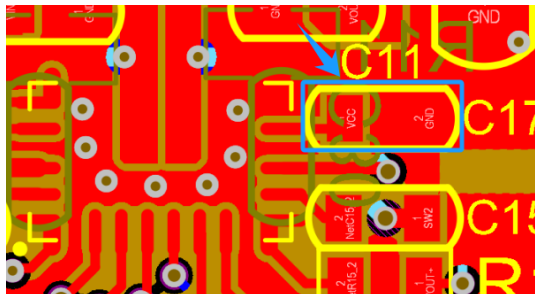
When calculating the amplitude of the protocol chip voltage regulation, the upper voltage dividing resistor is calculated according to R_{up} .

when calculating the initial voltage, the upper voltage dividing resistor is calculated according to $R_{up} + R_{down1}$.

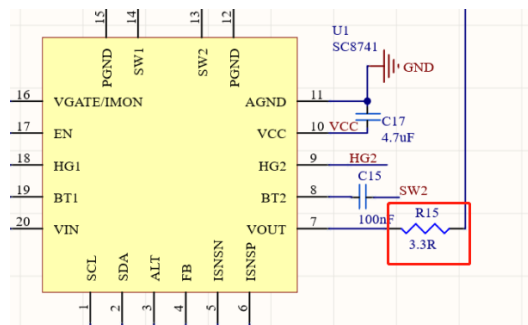


12 Layout Guide

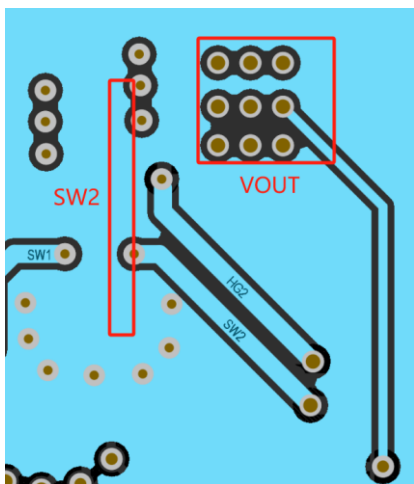
1. The $1\mu\text{F} \sim 4.7\mu\text{F}$ capacitors connected at VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.



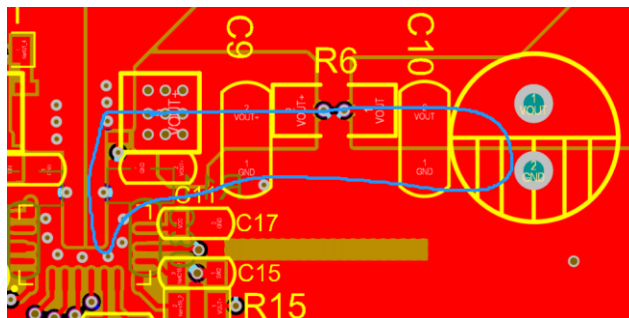
2. If APFM is used, VOUT pin should not connect any resistor. But if APFM is not used, this limit is invalid.



The sampling point of VOUT pin should be as close as possible to SW2.

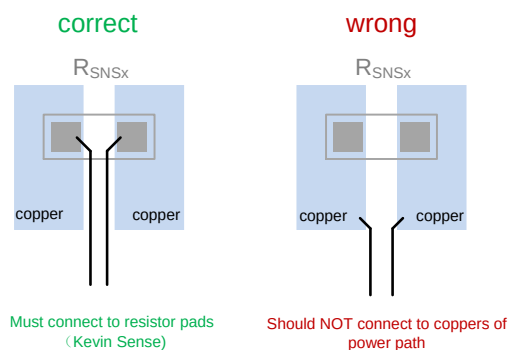


3. Put output current sense resistor, MOSFETs and bulk capacitor at VOUT side as close as possible. And the low side MOSFET and bulk capacitors should be very close to PGND pins. Between current sense resistor and high side MOS, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to MOS and PGND pins.



4. The decoupling capacitor of the VIN pin is placed near the chip.

5. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and add filter for each current sense near the IC.



Current sense



13 Register Maps

The 7-bit I2C address of the chip is 0x67H or 0x68H, depends on different part number.

Addr	Name	Type	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x01	OPERATION	R/W	ON/OFF	NA						ON/OFF
0x03	CLEAR FAULTS	W	NA							
0x21	VREF	R/W	VDAC_REG [7:0]							
0x22			VDAC_RESERVED [5:0]						VDAC_REG [9:8]	
0x79	STATUS	R/W	NA		VOUT_OV_FLAG	CC_ENTER_FLAG	GND_SHRT_FLAG	OTP_FLAG	NA	
0x7A			VOUT_SHRT_FLAG	NA		CC_EXIT_FLAG	PG_ENTER_FLAG	PG_EXIT_FLAG	NA	
0x7D	STATUS TEMP	R/W	OTP_FLAG	NA						
0xD0	MODE_CTRL1	R/W	EN_DTHR_REG	FSW_REG [1:0]		NA		EN_OVP_REG	EN_DSCHG_IIC	FPWM_IIC
0xD1	MODE_CTRL2	R/W	DIS_LDC	IDAC_REG						
0xD2	MODE_CTRL3	R/W	NA						CDC_GN_REG [1:0]	
0xD3	MODE_CTRL4	R/W	ILIMIT_REG	NA	RSNS_10M	VDAC_SLEW_RATE [1:0]		NA		BB2T_REG
0xD4	MODE_CTRL5	R/W	OCP_DLY [1:0]		EN_CC	NA				
0xD8	MASK	R/W	VOUT_OV_MASK	CC_ENTER_MASK	NA	OTP_MASK	PG_ENTER_MASK	PG_EXIT_MASK	GND_SHRT_MASK	NA
0x16	FALG_CTRL6	R/W	EN_CC_DET	NA	EN_HICCU	NA	ILMTH_FLAG	NA	PG	NA



Table 0x01H Operation Command

Bit	Type	Bit Name	Default	Description
7	R/W	ON/OFF State	1b	0b: The output is off 1b: The output is on.
6:1	R/W	RESERVED	00 0000b	Reserved
0	R/W	ON/OFF State	1b	0b: The output is off 1b: The output is on.

Table 0x03H Operation Command

Bit	Type	Bit Name	Default	Description
7:0	W	CLEAR	0b	Write any bit to clear the fault flag and status

Table 0x21H-22H Reference Voltage Register

Bit	Type	Bit Name	Default	Description
15 - 10	R/W	RESERVED	00 0000b	Reserved
9-0	R/W	REF	00 10010110b	00 00000000b = 100mV 00 00000001b = 101mV 00 1001 0110b = 250mV 01 1111 0100b = 600mV 11 11111111b = 1123mV

Table 0x79H STATUS1 Register

Bit	Type	Bit Name	Default	Description
7:6	R	RESERVED	00b	Reserved
5	R	VOUT_OV_FLAG	0b	If an output over voltage fault (Absolute OV or higher than 120% VREF) occurred, this bit will be set to '1'.
4	R	CC_ENTER_FLAG	0b	If IC enters CC Loop, this bit will be set to '1'.
3	R	GND_SHRT_FLAG	0b	If GND to Battery happened, this bit will be set to '1'
2	R	OTP_FLAG	0b	If the temperature of IC is higher than 150°C, this bit will be set to '1'
1:0	R	RESERVED	00b	Reserved

Table 0x7AH STATUS2 Register

Bit	Type	Bit Name	Default	Description
7	R	VOUT_SHRT_FLAG	0b	If V _{OUT} is lower than 2.5V, this bit will be set to '1'.
6:5	R	RESERVED	00b	Reserved
4	R	CC_EXIT_FLAG	0b	If IC exits the CC loop, this bit will be set to '1'
3	R	PG_ENTER_FLAG	0b	When the output voltage is not power good, this bit will be set to '1'
2	R	PG_EXIT_FLAG	0b	When the output voltage is power good, this bit will be set to '1'
1:0	R	RESERVED	00b	Reserved

Table 0x7DH TEMP STATUS Register

Bit	Type	Bit Name	Default	Description
7	R	OTP_FLAG	0b	If the temperature of IC is higher than 150°C, this bit will be set to '1'
6:0	R	RESERVED	000 0000b	Reserved



Table 0XD0H Status Register

Bit	Type	Bit Name	Default	Description
7	R/W	DITHER	1b	"0" No dither "1" Enable spread spectrum function
6:5	R/W	FREQ	01b	"00" 280kHz; "01" 420kHz "10" 560kHz; "11" Reserved
4:3	R	RESERVED	00b	Reserved
2	R/W	OUTPUT OVP	1b	"0" No output OVP function "1" Enable output OVP
1	R/W	DISCHG	0b	"0" Disable output voltage discharge "1" Enable output voltage discharge
0	R/W	APFM/FPWM	1b	"0" APFM "1" Forced PWM

Table 0XD1H Status Register

Bit	Type	Bit Name	Default	Description
7	R	RESERVED	0b	Reserved
6:0	R/W	CURRENT LIMIT	110 1100b	Based on 5mR R_{SENSE} . (If using a 4mR resistor, the current needs to expand 1.25 times up to 8A) 000 0000b = 0mA 000 0001b = 50mA 100 0001b = 3.25A 110 1100b = 5.4A 111 1111b = 6.35A

Table 0XD2H Status Register

Bit	Type	Bit Name	Default	Description
7:2	R	RESERVED	00 0000b	Reserved
1:0	R/W	CDC_GN_REG	00b	Set output voltage compensation value vs. load current: @5mR, $R_1=90.9k$ (Upper feedback resistor) 00: no compensation 01: V_{OUT} compensates 100mV@3A I_{OUT} 10: V_{OUT} compensates 300mV@3A I_{OUT} 11: V_{OUT} compensates 600mV@3A I_{OUT}

Table 0XD3H Status Register

Bit	Type	Bit Name	Default	Description
7	R/W	SWITCHING CURRENT LIMIT	1b	SWB Valley Current Limit; SWC Peak Current Limit "0": 9A/12A "1": 9A/19A
6	R	RESERVED	0b	Reserved
5	R/W	RSNS	0b	Select the R_{SENS} resistor value: 0: 5m Ω , Current Sense Gain=60 1: 10m Ω , Current Sense Gain=30
4:3	R/W	VDAC_SLEW_RATE	01b	Set the V_{REF} adjust rising slew rate. '00': 0.04mv/ μ s V_{REF} changing slew rate; '01': 0.08mv/ μ s V_{REF} changing slew rate; '10': 0.2mv/ μ s V_{REF} changing slew rate; '11': 0.4mv/ μ s V_{REF} changing slew rate; Default is "01". $V_{OUT_SLEW_RATE}=V_{REF_SLEW_RATE} * \text{Feedback ratio}$.
2:1	R	RESERVED	00b	Reserved
0	R/W	BB2T_REG	1b	Set frequency mode under Buck-boost condition:



				'0' Keep the same frequency as Buck and Boost mode '1': Reduce frequency to half of Buck and Boost mode.
--	--	--	--	---

Table 0XD4H Status Register

Bit	Type	Bit Name	Default	Description
7:6	R/W	OCP_DELAY	01b	Set the deglitch time of the device when the output overcurrent limit reached 00b = 400μs; 01b = 5ms 10b = 8ms; 11b = 12ms
5	R/W	EN_CC_DET	0b	Enable or disable current limit 0b = Current limit enabled 1b = Current limit disabled
4:0	R	RESERVED	0000b	Reserved

Table 0XD8H MASK Register

Bit	Type	Bit Name	Default	Description
7	R/W	VOUT_OV_MASK	1b	0: Not mask 1: Mask Enabled
6	R/W	CC_ENTER_MASK	1b	0: Not mask 1: Mask Enabled
5	R	RESERVED	0b	Reserved
4	R/W	OTP_MASK	1b	0: Not mask 1: Mask Enabled
3	R/W	PG_ENTER_MASK	1b	0: Not mask 1: Mask Enabled
2	R/W	PG_EXIT_MASK	1b	0: Not mask 1: Mask Enabled
1	R/W	GND_SHORT_MASK	1b	0: Not mask 1: Mask Enabled
0	R	RESERVED	0b	Reserved

Table 0X16H Status Register

Bit	Type	Bit Name	Default	Description
7	R	CC_DET	0b	0: Not in CC status 1: In CC status
6	R	RESERVED	0b	Reserved
5	R/W	EN_HICCUP_REG	1b	0: Hiccup function is disabled 1: Hiccup function is enabled
4	R	RESERVED	0b	Reserved
3	R	ILMTH_FLAG	0b	0: Current limit is triggered 1: Current limit is not triggered
2	R	RESERVED	0b	Reserved
1	R	PG	0b	0: Output voltage is good 1: Output voltage is not good
0	R	RESERVED	0b	Reserved



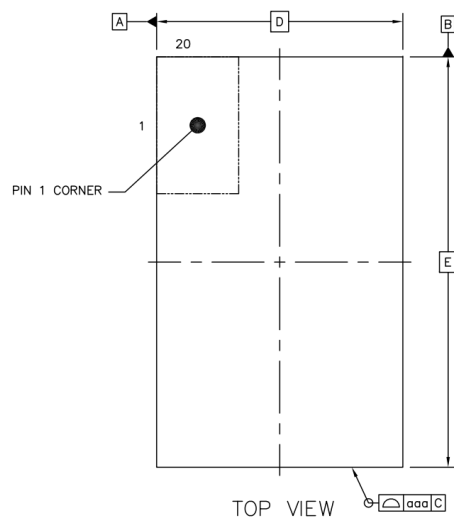
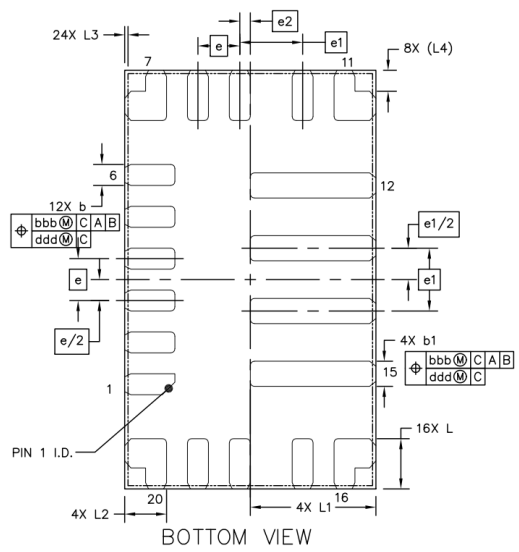
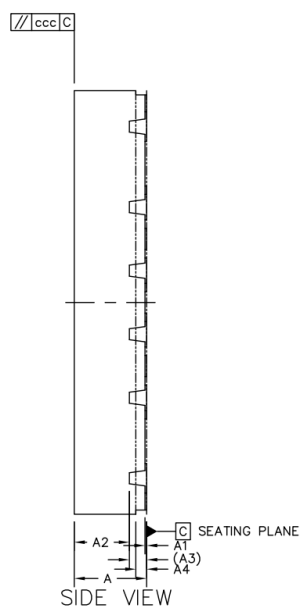
The different default value of SC8745Q / SC8745DQ / SC8745FQ / SC8745AQ

Bit Name	SC8745Q/SC8745DQ/SC8745FQ	SC8745AQ
EN_DCDC	ON	OFF
Current Limit	5.4A	5.4A
RSNS	5m	10m
OCP_DELAY	400μs	5ms
VDAC_SLEW_RATE	0.08mV/μs	0.08mV/μs
Dither Enable	YES	YES
APFM/FPWM	FPWM	FPWM
DISCHG	OFF	ON



MECHANICAL DATA

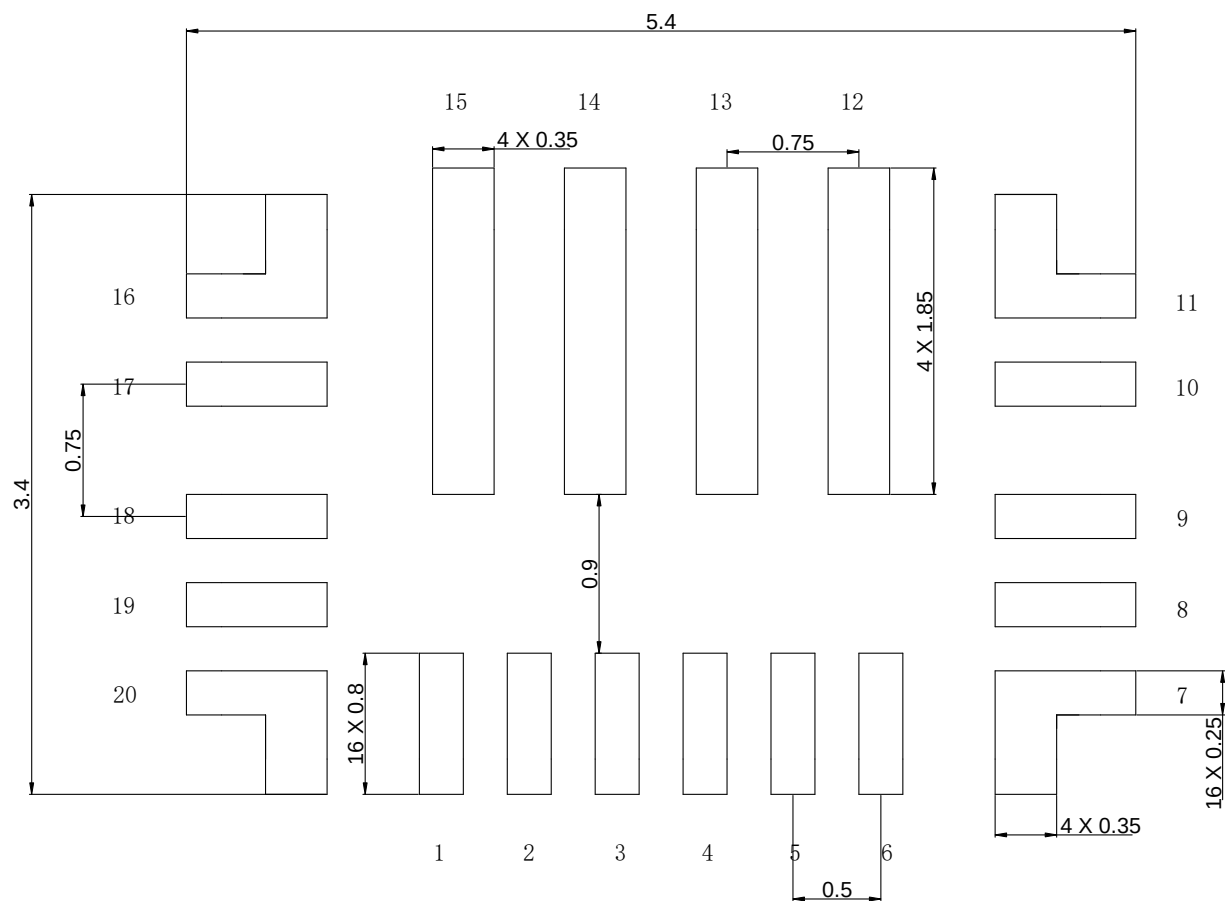
Flipchip-QFN20(3x5)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.65	---
L/F THICKNESS	A3	0.203 REF		
SIDE WETTABLE DEPTH	A4	0.075	---	0.18
LEAD WIDTH	b	0.2	0.25	0.3
	b1	0.25	0.3	0.35
BODY SIZE	X	3 BSC		
	Y	5 BSC		
LEAD PITCH	e	0.5 BSC		
	e1	0.75 BSC		
LEAD CENTER TO PKG CENTER	e2	0.125 BSC		
LEAD LENGTH	L	0.5	0.6	0.7
	L1	1.4	1.5	1.6
	L2	0.4	0.5	0.6
SIDE WETTABLE WIDTH	L3	0.01	---	0.09
LEAD EDGE TO PKG EDGE	L4	0.25 REF		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
LEAD OFFSET	bbb	0.1		
	ddd	0.05		



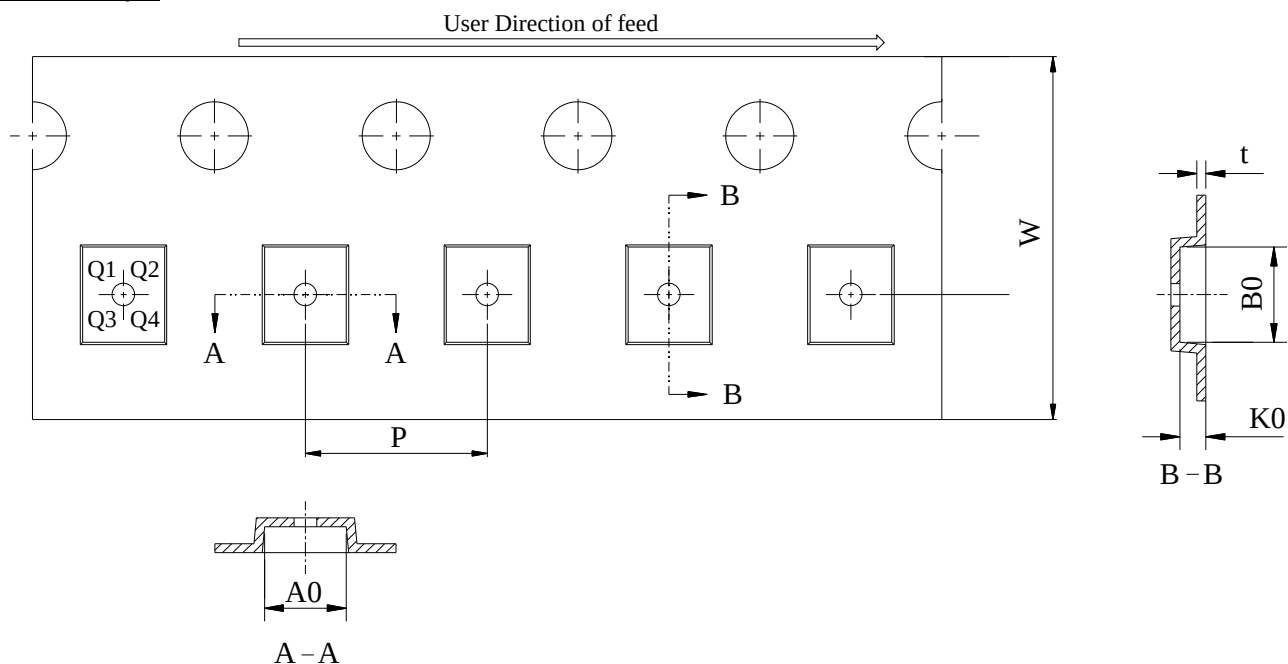
RECOMMENDED FOOTPRINT



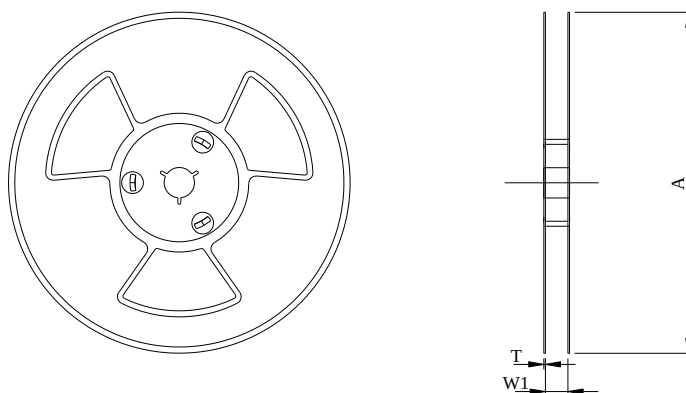
Unit: mm



TAPE AND REEL INFORMATION

Carrier Tape

Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	$12.00 + 0.30/-0.10$	8.00 ± 0.10	3.25 ± 0.10	5.25 ± 0.10	1.13 ± 0.10	0.25 ± 0.02	Q1

REEL

Item	A	W1	T
Size (mm)	330 ± 1	$12.4 +1/-0$	2.6 ± 0.15



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