SC8746 36V / 140W Buck-Boost Converter with Low-Side MOSFETs Integrated and I2C Interface

1 Descriptions

The SC8746 is a buck-boost converter with two low-side integrated power switches capable of regulating the output voltage at, above, or below the input voltage. The SC8746 operates over 3.7V to 36V wide input voltage and can output 1V to 29V voltage to support a variety of applications.

The SC8746 is suitable for USB power delivery application. It can work well with external USB PD controller through I2C interface and provide flexibility of programmable features.

The SC8746 employs current mode control scheme. The switching frequency could be set at 280kHz/420kHz/560kHz through I2C. The SC8746 also provides optional spread spectrum to optimize EMI performance.

The SC8746 offers output over-voltage protection, cycle-by-cycle current limit, output short circuit protection, average output current limit and thermal shutdown protection

The SC8746 is available in 20-pin 3mm x 5mm Wettable Flank QFN packages.

2 Features

- Integrated gate driver for high-side power switches
- 4V to 36V start up input voltage, support 3.7V falling Vin
- 1V to 29V output voltage range, 36V ABS voltage
- Programmable Power Supply (PPS) support for USB power delivery
  - Programmable reference voltage range: 0.1V – 1.123V with 1mV resolution
  - Programmable output current limit up to 6.35A with 50-Ma step
  - +/- 5% accurate average output current limiting
- I2C Interface for:
  - 280k/420k/560kHz frequency selectable
  - Auto PFM / Forced PWM
  - Spread spectrum dithering
  - Line drop compensation
  - Current limit setting
- IMON for output current
- External biased VCC for higher efficiency
- Output OCP / SCP / OVP / TSD protection

3 Applications

- Monitor/TV
- USB Charging
- Wireless Charging
- USB HUB

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4 Device Information

ORDER NUMBER	7-bit I2C Address	VIN OVP	APFM/FPWM	PACKAGE	BODY SIZE
SC8746QFPR	0x67H	Yes	FPWM	20 pin QFN	3mm x 5mm x 0.85mm
SC8746AQFPR	0x68H	No	APFM	20 pin QFN	3mm x 5mm x 0.85mm

5 Revision History

Revision	Date	Page(s) changed	Changes Description
V1.0.0	2024/8/28		
V1.1.0	2025/1/16	P13~P15	1, Add description of I2C and ALT
V1.2.0	2025/2/8	P1~P2	1, Add version difference
V1.3.0	2025/3/14	P1, P6	1, Display 36V Vout ABS voltage in Features
V1.4.1	2026/1/21	P2	1, Version information update
V1.4.2	2026/04	P21,22	1, Correct descriptions of some registers

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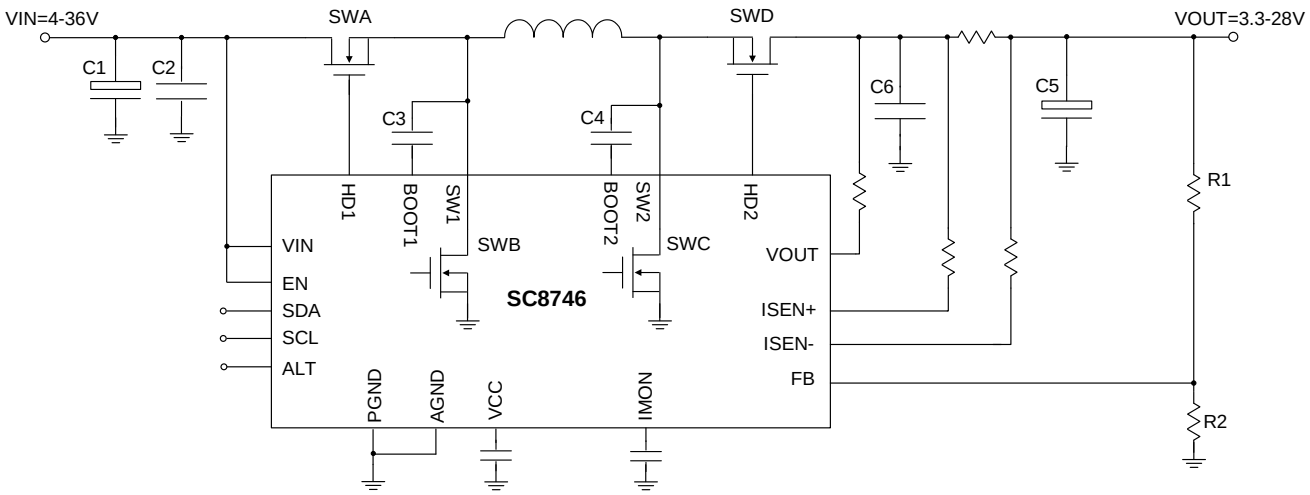
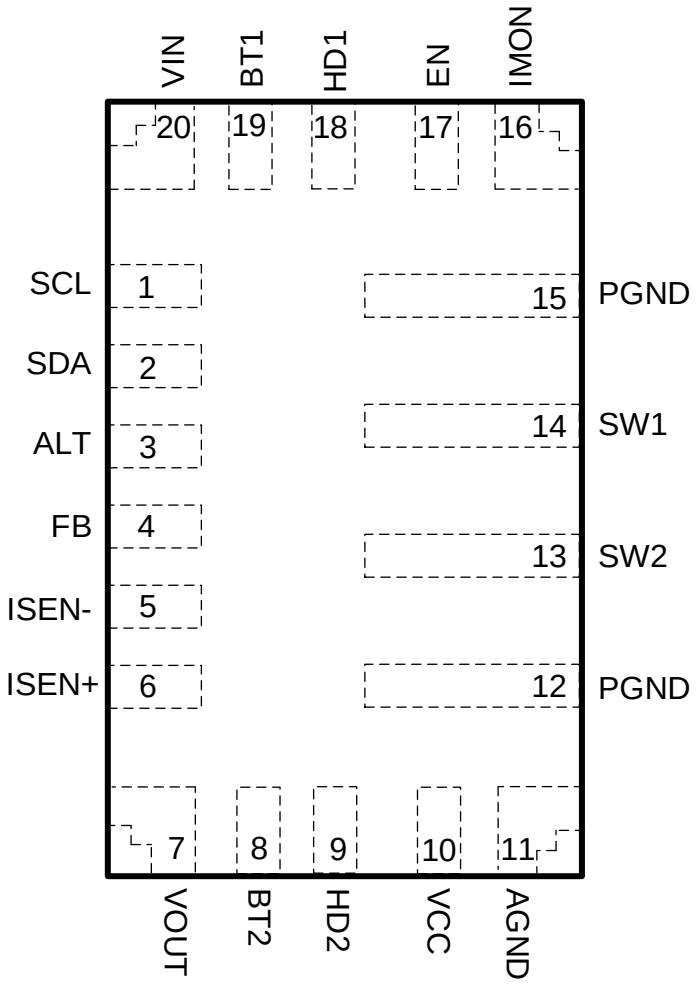
6 Typical Application Circuit



7 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	SCL	I	Clock of I2C interface
2	SDA	I	Data of I2C interface
3	ALT	O	I2C alert pin. Open drain output, active low
4	FB	I	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage.

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5	ISEN-	I	Negative node of current sense signal input. An optional current sense resistor could be placed between VOUT cap and Q4
6	ISEN+	I	Positive node of current sense signal input. An optional current sense resistor could be placed between VOUT cap and Q4.
7	VOUT	O	Output of the buck-boost converter. It's also used to provide VCC supply at certain VOUT condition.
8	BT2	O	Power supply for high-side MOSFET gate driver in boost side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW2 pin.
9	HD2	O	Gate driver output for high-side MOSFET in boost side
10	VCC	O	Internal LDO regulator output. Decouple with a 4.7μF capacitor between this pin and the AGND pin.
11	AGND	PWR	Signal ground of the IC.
12	PGND	PWR	Power ground of the IC.
13	SW2	I	Switching node pin of the boost side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
14	SW1	I	Switching node pin of the buck side. It is connected to the drain of the internal low-side power MOSFET and the source of external high-side power MOSFET.
15	PGND	I	Power Ground. PGND requires extra care during PCB layout. Connect to GND with copper traces and vias.
16	IMON	O	Voltage monitor for output current.
17	EN	I	EN input. Apply logic high to enable the chip.
18	HD1	O	Gate driver output for high-side MOSFET in buck side
19	BT1	I	Power supply for high-side MOSFET gate driver in buck side. A ceramic capacitor of 0.1 μF must be connected between this pin and the SW1 pin.
20	VIN	PWR	Input power supply for the IC.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	Unit
Voltage range at terminals(2)	VIN, EN, SW1	-0.3	40	V
	SW1 (10ns)	-3	42	V
	VOUT, SW2, ISNS+, ISNS-	-0.3	36	V
	SW2 (10ns)	-3	38	V
	BST1, HD1	SW1-0.3	SW1+6	V
	BST2, HD2	SW2-0.3	SW2+6	V
	All other pins	-0.3	6	V
T_J	Operating junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD(1)	Human body model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged device model (CDM) ESD stress voltage(3), all pins	-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range after start up	3.7		36	V
V_{OUT}	Output voltage range	1		29	V
F_{SW}	Buck switching frequency range	280	420	560	kHz
I_{OUT}	Output DC current range	0		6	A
L	Effective inductance range	3.3	4.7	10	μH
T_J	Operating junction temperature	-40		150	°C

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8.4 Thermal Information

THERMAL RESISTANCE(1)		FCQFN20 (3mm x 5mm)	UNIT
Θ_{JA}	Junction to ambient thermal resistance	39	°C/W
Θ_{JC}	Junction to case resistance	2.5	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

8.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{IN} = 12V and V_{OUT} = 20V. Typical value is tested at T_J = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		3.7		36	V
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		3.9	4.0	V
		V_{IN} falling		3.6	3.7	V
I_Q	Quiescent current into the VIN pin	I2C set on, EN on. No switching, no load.		350	600	μA
I_{SD}	Shutdown current into the VIN pin	IC disabled, V_{EN}=0V		1	3.5	μA
V_{CC}	Internal regulator output		4.85	5.1	5.3	V
I_{CC_LIMIT}	VCC current Limit			170		mA
EN						
$V_{EN_VCC_H}$	EN input level to turn on internal LDO	Rising threshold			1	V
$V_{EN_VCC_L}$	EN input level to turn off internal LDO	Falling threshold	0.4			V
V_{EN_H}	EN input level to start switching	Rising threshold	1.19	1.22	1.25	V
V_{EN_H}	EN input level to stop switching	Falling threshold	1.04	1.07	1.10	V
V_{EN_HYS}	Enable threshold hysteresis			150		mV
R_{EN}	EN Pull-down resistor	EN=2V		2		MΩ
MOSFETS						
$R_{DS(on)}$	Low-side MOSFET on resistance on buck side			18		mΩ
	High-side MOSFET on resistance on boost side			13.5		mΩ
BOOT UVLO						
V_{BOOT_UVLO}	Falling voltage on BT1/BT2 pin compared to SW1/SW2 which will turn off high-side switch			2.3		V
REFERENCE VOLTAGE						
V_{FB1}	Feedback Voltage	REF = 0096h	245	250	255	mV
V_{FB2}		REF = 00F4h	591	600	609	mV

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V_{FB3}		REF = 03FFh	1.113	1.123	1.135	V
INPUT OVER VOLTAGE PROTECTION						
V_{OVLO_R}	Voltage on VIN pin to stop buck-boost switching			32		V
V_{OVLO_HYS}	Input voltage protection hysteresis			2		V
OUTPUT OVER VOLTAGE PROTECTION						
$V_{OUT_OVP_R}$	Output OVP rising	V_{FB} > 0.25V	115%	120%	125%	V_{FB}
$V_{OUT_OVP_F}$	Output OVP falling		110%	115%	120%	V_{FB}
$V_{OUT_OVP_ABS}$	Output absolute OVP rising			30	32	V
$V_{OUT_OVP_HYS}$	Output voltage protection hysteresis			1.1		V
R_{DIS}	Output discharge resistor			180		Ω
INTERNAL CLOCK						
F_{SW1}	Oscillator frequency			280		kHz
F_{SW2}				420		
F_{SW3}				560		
T_{ON_MIN}	Min on time	Boost low side MOSFET		75		ns
T_{OFF_MIN}	Min off time	Buck low side MOSFET		75		ns
SOFT START						
T_{SS}		For FB = 0.25V condition		0.8		ms
CURRENT LIMIT						
V_{SENS1}	ISENS OC threshold	OC threshold=1A, Rsens=5mΩ	4.25	5	5.75	mV
V_{SENS2}		OC threshold=3.6A, Rsens=5mΩ	17.1	18	18.9	mV
V_{SENS3}		OC threshold=6A, Rsens=5mΩ	28.5	30	31.5	mV
I_{LIMIT1}	Buck low-side valley current limit		7.5	9.0	10.5	A
I_{LIMIT2}	Boost low-side peak current limit	Set_ILIM[7]=0b (For 20V/3.25A)	10	12	14	A
		Set_ILIM[7]=1b (For 20V/5A)	16	19	22	A
V_{cc_en}	Current Limit low range			2.2		V
IMON Monitor						
V_{IMON}	Suggested IMON output voltage range		0		2.8	V
t_{IMON_swith}	Establish time for IMON signal	10pF at IMON pin			50	μs
LINE DROP COMPENSATION						
V_{DROP}	Line drop compensation	Set_CDC[6:5]=01b, R1=90.9kΩ, Rsense=5mΩ, I_{OUT}=3A		100		mV

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		Set_CDC[6:5]=10b, R1=90.9kΩ, Rsense=5mΩ, I_{OUT}=3A	300	mV
		Set_CDC[6:5]=11b, R1=90.9kΩ, Rsense=5mΩ, I_{OUT}=3A	600	mV
HICCUP				
T_{HICCUP}	Hiccup on timer		4	mS
	Hiccup off timer		80	mS
V_{HICCUP}	Hiccup voltage on output		2.5	V
SPREAD SPECTRUM				
FS_{range}	Frequency dithering span		14	%
f_m	Modulation frequency	Change with switching frequency	1/128	F_{SW}
MODE TRANSITION				
V_{MODE_TH1}	Buck-boost to buck transition threshold	VIN/VOUT	120	%
V_{MODE_TH2}	Buck-boost to boost transition threshold	VIN/VOUT	85	%
HIGH SIDE GATE DRIVER				
V_{BUCK_PU}	Buck high side high-state voltage drop	V_{BT1} - V_{HD1}, 100mA sourcing	0.22	V
V_{BUCK_PD}	Buck high side low-state voltage drop	V_{HD1} - V_{SW1}, 100mA sinking	0.07	V
V_{BOOST_PU}	Boost high side high-state voltage drop	V_{BT2} - V_{HD2}, 100mA sourcing	0.13	V
V_{BOOST_PD}	Boost high side low-state voltage drop	V_{HD2} - V_{SW2}, 100mA sinking	0.05	V
INTERNAL REFERENCE VDAC				
V_{VDAC_REF}	Voltage DAC range	100mV offset	0.1 / 1.123	V
N_{DAC_CV}	CV loop vref resolution		10	Bits
K_{VOUT_RATIO}	Ratio from VOUT to the input of reference comparator		1/20	
INTERNAL REFERENCE IDAC				
V_{IDAC_REF}	Current DAC range		0 / 1.27	V
N_{DAC_CV}	CC loop Iref resolution		7	Bits
I2C INTERFACE				
V_{IH}	Input logic high		1.3	V
V_{IL}	Input logic low		0.4	V
ALERT				
R_{ALT}	ALT pin pull low resistance		20	Ω
POWER GOOD INDICATION				
$V_{PG_R_L}$	PG lower rising threshold	VREF>0.25V	80% / 85% / 90%	V_{FB}

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$V_{PG_F_L}$	PG lower falling threshold		75%	80%	85%	V_{FB}
$V_{PG_R_H}$	PG upper rising threshold	VREF>0.25V	115%	120%	125%	V_{FB}
$V_{PG_F_H}$	PG upper falling threshold		110%	115%	120%	V_{FB}
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			20		°C

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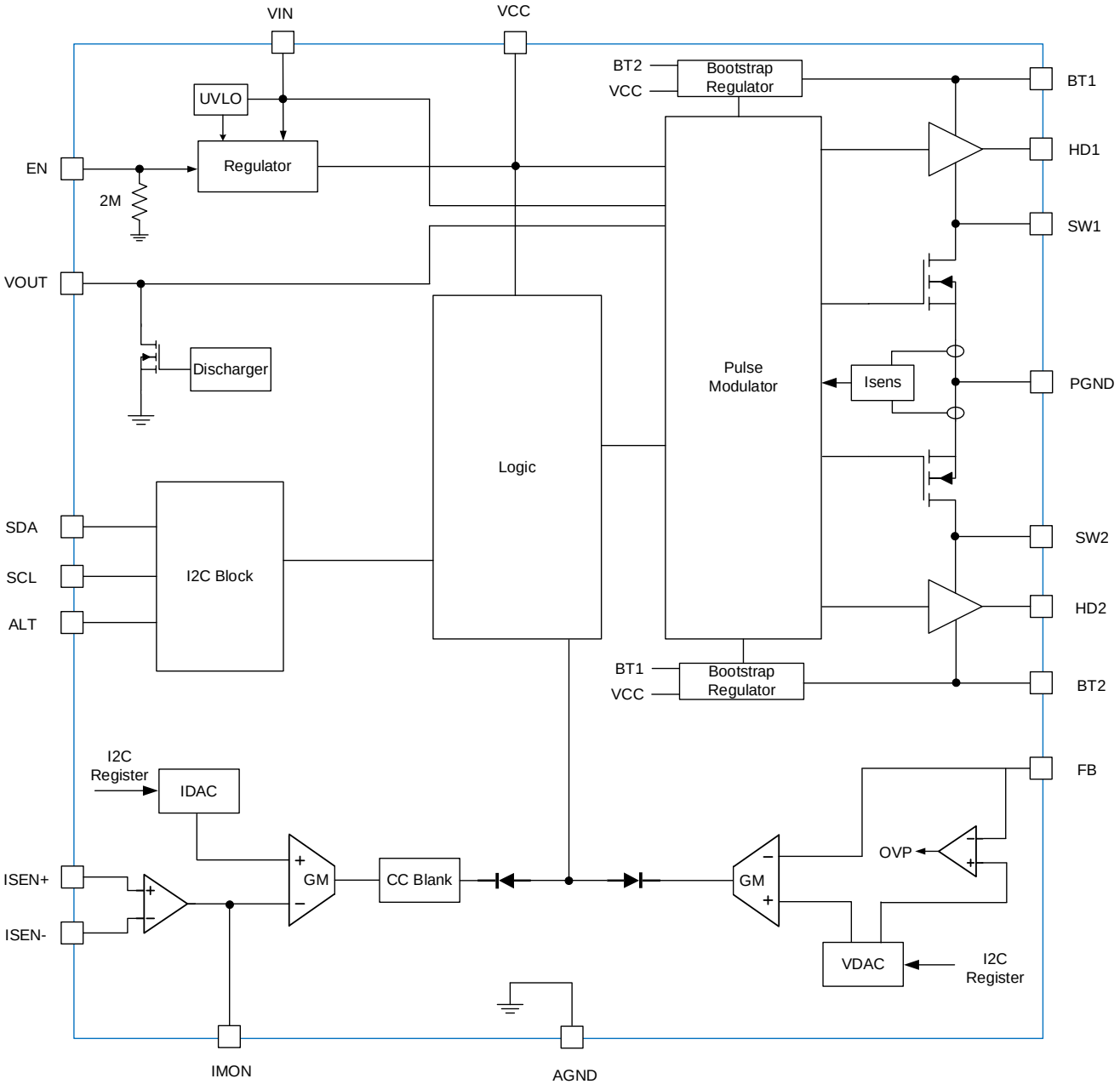
9 Functional Block Diagram



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10 Feature Description

10.1 Overview

SC8746 is a wide range of 3.7V to 36V input voltage and an output voltage of 1V to 29V buck-boost DCDC converter with two low side MOSFETs integrated. It can transition among buck mode, buck-boost mode, and boost mode smoothly when the input voltage is higher or lower than the output voltage. Implementing valley-current mode control in buck mode and peak-current mode control in boost mode, SC8746 is able to provide excellent line and load transient performance. SC8746 could be configured during three frequency options 280kHz /420kHz /560kHz to achieve small filter size or higher efficiency.

10.2 Device Operation Modes

10.2.1 Buck Modes

When the input voltage is higher than output voltage, SC8746 works in buck mode. The buck side MOSFET SWA and SWB switch for the buck regulation, while boost side MOSFET SWC is off and SWD keeps on to conduct the inductor current.

In buck modes, SC8746 employs adaptive ON time and valley current control. Once the FB voltage drops below reference voltage, SWA will turn on. After an adaptive ON time, SWB turn on to conduct the inductor current until trigger COMP control signal.

10.2.2 Boost Modes

When the input voltage is lower than output voltage, SC8746 works in boost mode. The boost side MOSFET SWC and SWD switch for the boost regulation, while buck side MOSFET SWB is off and SWA keeps on to conduct the inductor current.

In boost modes, SC8746 employs peak current control and adaptive OFF time. SWC turns on to conduct the inductor current until it rises to trigger the control signal. After SWC turns off, SWD will turn on and remain for adaptive time to regulate the output voltage.

10.2.3 Buck-Boost Modes

When the input voltage is close to the output voltage, SC8746 works in buck-boost mode. The MOSFET turning on sequence are SWA&SWC -> SWA&SWD -> SWB&SWD.

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10.3 Input Undervoltage Lockout

When the input voltage is above than 4V, the SC8746 can be enabled by pulling EN pin to a high voltage above 1.3V. When it starts running, SC8746 wouldn't be disabled until the input voltage is below 3.7V.

10.4 EN Control

The SC8746 has an enable control pin (EN). The voltage on the EN pin controls the ON/OFF operation. A voltage of less than 0.4V shuts down the device, while a voltage of greater than 1.0V is required to start the device. The EN pin is an input and cannot be left or floating.

SC8746 EN is a high voltage pin, it can be connected to VIN directly or through resistor. It could be established a precision system UVLO level by inserting resistors. An external logic signal can also be used to drive EN input for system sequencing and protection.

10.5 Soft Start

The integrated soft-start circuit prevents input inrush current and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. If the output of SC8746 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal Soft-start capacitor exceeds the internal feedback voltage.

10.6 Output Current Limit and Hiccup

The output current limit is programmable from 0A to 6.35A by placing a 5mΩ current sensing resistor between ISNS+ pin and the ISNS- pin. If output current exceeds the set constant current limit threshold, SC8746 will enter constant current limit mode. In this mode the current amplitude is limited. As the reducing of load resistance, output voltage drops. Once the output voltage is lower than 2.5V and the device trigger the switching current limit, SC8746 will enters hiccup mode to periodically restart the part. The SC8746 exits hiccup mode once the output voltage is higher than 2.5V or the switching current limit is not triggered.

10.7 Switching Current Limit

SC8746 provides valley current limit in buck mode and peak current limit in boost and buck-boost mode by sensing LS-FET current. In buck mode, the next period won't start before IL drops to the valley current limit, which prevents inductor current runaway during short circuits on the output.

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10.8 Input Over-Voltage Protection

SC8746 has input overvoltage protection. When the input voltage at the VIN pin is detected above 32V typically, the SC8746 turns off both high-side switches and low-side switches.

10.9 Output Over-Voltage Protection

SC8746 has output overvoltage protection. When the output voltage at the VOUT pin is detected above 30V typically or the output voltage is higher than 120% of VREF, the SC8746 turns off both high-side switches and low-side switches. The discharge path from VOUT pin to ground will turn on. If the VOUT pin voltage drops to 28.9V, or FB voltage drops to 110% of VREF, the device will return to normal operation.

10.10 Integrated Gate Drivers

The SC8746 provides two N-channel MOSFET gate drivers for buck side and boost side. Buck-side driver is capable of sourcing 2.2A and sinking 0.7A peak current, while boost-side driver is capable of sourcing 1.3A and sinking 0.5A peak current. In buck mode operation, HD1 switches while HD2 keeps continuously on. In boost mode operation, HD2 switches while HD1 keeps continuous on. Capacitors between BT1 to SW1 and BT2 to SW2 are necessary to supply the power, which is powered by internal diode from VCC or charge them by each other.

10.11 Switching Frequency and Spread Spectrum Function

SC8746 frequency could be selectable at 280kHz, 420kHz and 580kHz with a 2-bit FREQ register. Normally a 420kHz frequency is recommended. SC8746 has a frequency spread spectrum function, which could help minimize the peak emissions. SC8746 uses a triangle wave to modulate the internal oscillator, whose frequency is 1/128 of the switching frequency. The frequency span of the spread spectrum operation is 7.5%.

10.12 Shutdown and Load Discharge

When the Input voltage is lower than 3V or EN pin voltage is pulled down below 0.4V, the SC8746 is in shutdown mode and all functions are disabled. All internal registers are reset to default values. SC8746 integrates output discharge function when the output voltage needs to be discharged to the goal voltage.

10.13 Output Voltage Setting

There are two ways to set the output voltage: changing the feedback ratio and changing the reference voltage. SC8746 has a 10-bit DAC to program the reference voltage from 100mV to 1.123V. The output voltage could be calculated with the formula as below:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB_UP}}{R_{FB_DOWN}}\right)$$

10.14 Output Line Drop Compensation

SC8746 can compensate an output voltage drop, which is helpful when there is high impedance at the output side. The compensated voltage is impacted the output current, sense resistors and the line drop compensation gain. Refer to the register map description for detail line drop compensation amplitude.

10.15 Thermal Shutdown

SC8746 is protected by a thermal shutdown circuit that shuts down the device when the internal junction temperature exceeds 165C(Typical). The internal soft-start circuit is reset but all internal registers values remain unchanged. The DCDC portion will automatically restarts when the junction temperature drops below the thermal shutdown hysteresis.

10.16 I2C and Interrupt

10.16.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x67 (8-bit address is 0xCE for write command, 0xCF for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

10.16.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

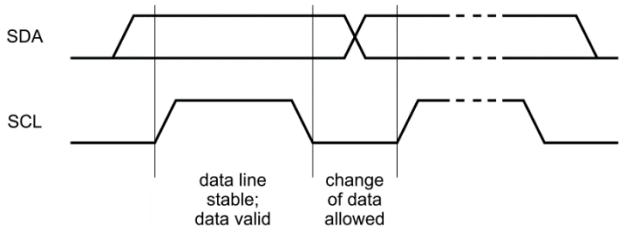

Figure 1 Bit transfer on the I2C bus

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10.16.3 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

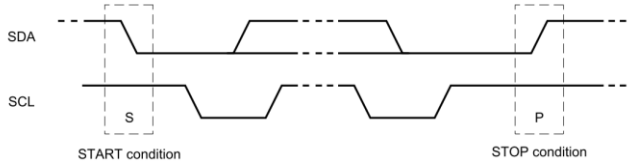

Figure 2 START and STOP conditions

10.16.4 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

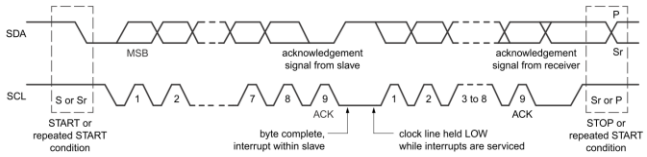

Figure 3 Data transfer on the I2C bus

10.16.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

10.16.6 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

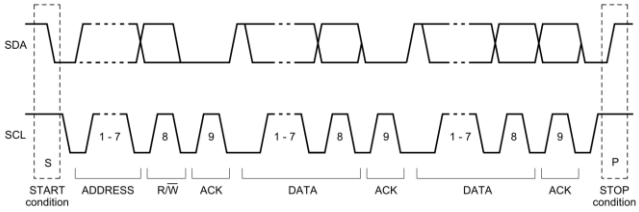

Figure 4 A complete data transfer

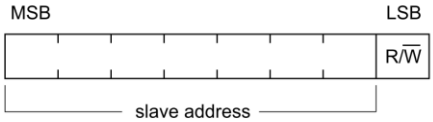

Figure 5 The first byte after the START procedure

10.16.7 Single Read and Write

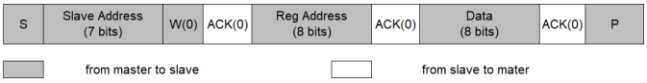

Figure 6 Single Wite

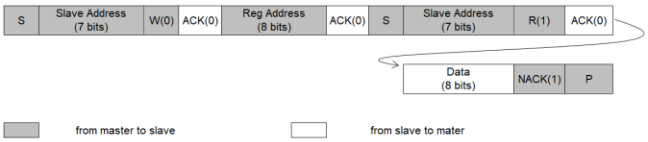

Figure 7 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

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10.16.8 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

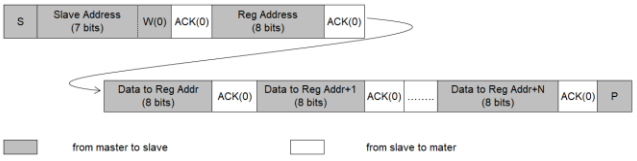

Figure 8 Multi-Write

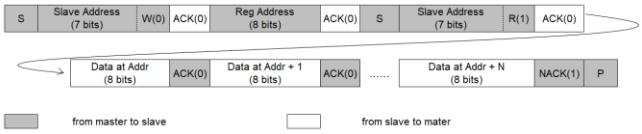

Figure 9 Multi-Read

10.16.9 Alert

When VOUT_OV/ VOUT_SHROT /OTP /CC_EXIT /CC_ENTER /PG_ENTER /PG_EXIT is set to 1, the IC pulls down ALT pin to inform MCU. The interrupt pulse at INT pin is as follow:

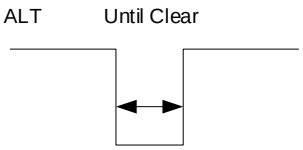

Figure 10 Signal at ALT pin

User can mask the interrupt output of any bit by setting its corresponding bit in Mask register. When the mask bit is set, the corresponding status bit is still set, but the IC doesn't pull down ALT pin.

The ALT pin can be reset by write any bit to 0x03 Register.

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11 Application Information

11.1. Capacitor Selection

The switching frequency of the IC is in the range of 280kHz ~ 560kHz. Since MLCC ceramic capacitor has good high frequency filtering with low ESR, above 60µF X5R or X7R capacitors with higher voltage rating then operating voltage with margin is recommended. For example, if the highest operating Vin/Vout voltage is 12V, select at least 16V capacitor and to secure enough margin, 25V voltage rating capacitor is recommended.

The high capacitance polymer capacitor or tantalum capacitor can be used for input and output but capacitor voltage rating must be higher than the highest operating voltage with enough margin. The high frequency characteristics of these capacitors are not as good as ceramic capacitor, so at least 10µF ceramic capacitor should be placed in parallel to reduce high frequency ripple.

11.2. Inductor Selection

2.2 µH to 10 µH inductor is recommended for loop stability.

The peak inductor current can be calculated as:

$$IL_peak = IOUT + \frac{VOUT \cdot (VIN-VOUT)}{2 \cdot fsw \cdot L \cdot VIN \cdot \eta} \text{ (Buck Mode)}$$

$$IL_peak = IIN + \frac{VIN \cdot (VOUT-VIN \cdot \eta)}{2 \cdot fsw \cdot L \cdot VOUT} \text{ (Boost Mode)}$$

where IOUT is the output current at VOUT side, and can be calculated as

$$IOUT = \frac{VIN \cdot IIN \cdot \eta}{VOUT}$$

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency

L is the inductor value

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$PL_DC = IL^2 \cdot DCR$$

IL is the average value of inductor current, and it equals to IOUT or IIN.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user can consult with the inductor vendor to select the inductors which have small ESR at high frequency and small core loss.

11.3. Current Sense Resistor

The ISNS+ and ISNS- are current sense resistors. 5 mΩ should be used to sense IOUT current (10 mΩ supports higher battery current limit accuracy, and 5 mΩ supports higher efficiency). Resistor of 1% or higher accuracy and low temperature coefficient is recommended.

The resistor power rating and temperature coefficient should be considered. The power dissipation is roughly calculated as $P=I^2R$, and I is the highest current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4. MOSFET Selection

The V_{DS} of MOSFET should be higher than the highest operating voltage with enough margin (recommend more than 10V higher). For example, if the highest operating voltage is 20V, at least 30V rated V_{DS} MOSFET should be selected; If the highest operating voltage is 24V, 40V V_{DS} voltage rating should be selected.

The V_{GS} voltage rating of MOSFET should be selected higher than 8V. Considering PCB parasitic parameters during operation, MOSFET V_{GS} voltage might be higher than V_{DRV} voltage due to transient overshoot, so 10V V_{GS} is recommended to secure sufficient margin.

The MOSFET current I_D should be higher than the highest battery current with enough margin.

To ensure the sufficient current capability in relatively high temperature circumstance, the current rate at T_A=70˚C or T_C = 100˚C should be considered. In addition, the power dissipation value P_D should also be considered and higher P_D is better in applications. Make sure that MOSFET power consumption must not exceed P_D value.

The MOSFET $R_{DS(ON)}$ and input capacitor C_{ISS} impact power efficiency directly. Typically, lower $R_{DS(ON)}$ MOSFET has higher C_{ISS}. The $R_{DS(ON)}$ is related to conduction loss. Higher R_{DSON} results in higher conduction loss, thus lower efficiency

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and higher thermal dissipation; the C_{ISS} is related to MOSFET switch on/off time, and longer on/off time results in higher switching loss and lower efficiency. The proper MOSEFT should be selected based on tradeoff between the $R_{DS(ON)}$ and C_{ISS}.

11.5. Driver Resistor and SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add series resistor (0603 size) for gate driving signal (HD1 to MOS gate and HD2 to MOS gate), and RC snubber (0603 size) circuit at SWx, as shown below.

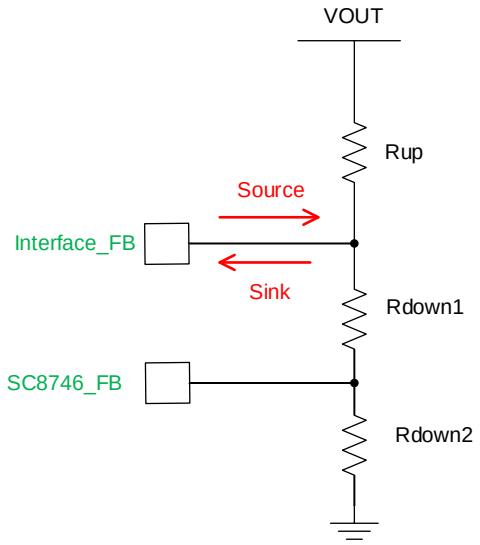
The driver resistor should be placed near MOS. At first, use 0Ω resistors; if switching overshoot is big, increase the resistor value to slow down the switching speed. It is suggested to keep the resistor value < 10 Ω. While the switching speed gets slower, the default dead time may not be enough to avoid overshoot of the power MOSFETs.

The RC snubber circuit at SWx node is also helpful in absorbing the high frequency spike at SWx node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

11.6. External PWM voltage regulation

When using external PWM voltage regulation, since most protocol chips have requirements for FB voltage, the default voltage of SC87426 FB is only 0.25V. If directly connected, it will cause the regulated voltage to be lower than the set value.

For this situation, a three-stage resistor can be used to avoid it.



The FB access point of the protocol chip is above the SC8746_FB access point, so that the voltage _FB the protocol chip is higher than SC8746_FB, and the specific calculation relationship is:

$$V_{Interface_FB} = \frac{R_{down1} + R_{down2}}{R_{down2}} * V_{SC8746_FB}$$

According to the KCL of the Interface node

$$\frac{V_{out} - V_{Interface_FB}}{R_{up}} = \frac{V_{SC8746B_{FB}}}{R_{down2}} + I$$

Where I represents equivalent current, when using PWM voltage regulation,

$$I = \frac{V_{Interface_{FB}} - V_{PWM}}{R}$$

When calculating the amplitude of the protocol chip voltage regulation, the upper voltage dividing resistor is calculated according to Rup.

when calculating the initial voltage, the upper voltage dividing resistor is calculated according to Rup + Rdown1.

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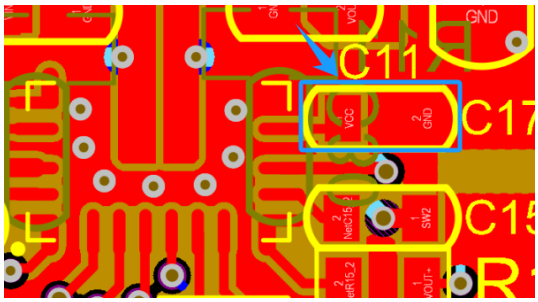
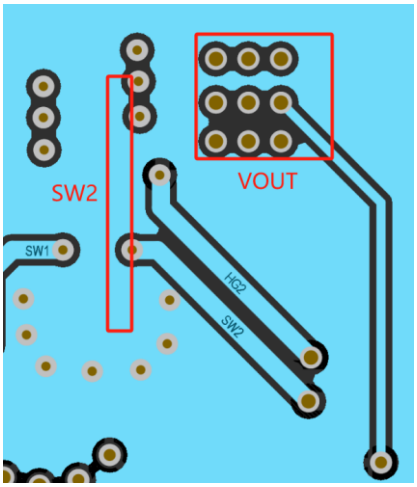
12 Layout Guide

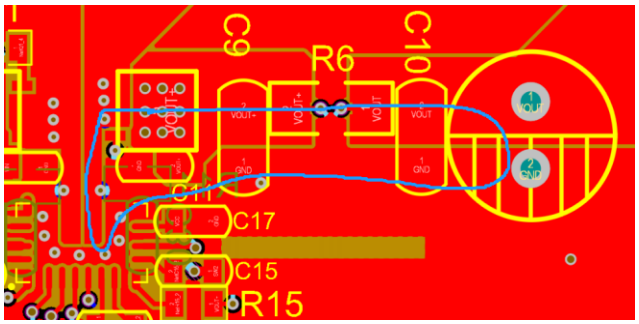
1. The 1μF ~ 4.7μF capacitors connected at VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.



2. The sampling point of VOUT pin should be as close as possible to SW2. But if APFM is not used, this limit is invalid.

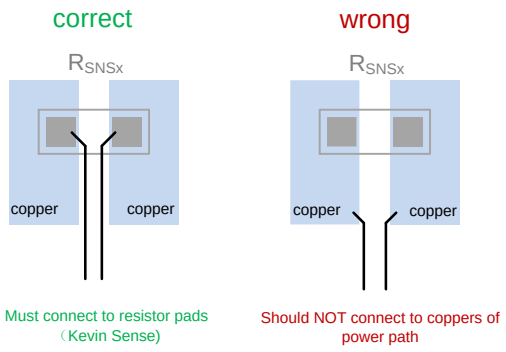


3. Put output current sense resistor, MOSFETs and bulk capacitor at VOUT side as close as possible. And the low side MOSFET and bulk capacitors should be very close to PGND pins. Between current sense resistor and high side MOS, add a 100nF 0402 capacitor to PGND. It is helpful to suppress high frequency noise. Put it very close to MOS and PGND pins.



4. The decoupling capacitor of the VIN pin is placed near the chip.

5. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and add filter for each current sense near the IC.



Current sense

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13 Register Maps

The 7-bit I2C address of the chip is 0x67H

Addr	Name	Type	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x01	OPERATION	R/W	ON/OFF	NA						ON/OFF
0x03	CLEAR FAULTS	W								
0x21	VREF	R/W	VDAC_REG [7:0]							
0x22			NA						VDAC_REG [9:8]	
0x79	STATUS	R/W	NA		VOUT_OV_FLAG	CC_ENTER_FLAG	NA	OTP_FLAG	NA	
0x7A			VOUT_SHRT_FLAG	NA		CC_EXIT_FLAG	PG_ENTER_FLAG	PG_EXIT_FLAG	NA	
0x7D	STATUS TEMP	R/W	OTP_FLAG	NA						
0xD0	MODE_CTROL1	R/W	DIS_DTHR_REG	FSW_REG[1:0]		NA		EN_OVP	EN_DSCHG	FPWM
0xD1	MODE_CTROL2	R/W	NA	IDAC_REG						
0xD2	MODE_CTROL3	R/W	NA						CDC_GN_REG[1:0]	
0xD3	MODE_CTROL4	R/W	ILIMT_REG	NA	RSNS_10M	VDAC_SLEW_RATE[1:0]		NA		BB2T
0xD4	MODE_CTROL5	R/W	OCP_DLY[1:0]		DIS_CC	NA				
0xD8	MASK	R/W	VOUT_OV_MASK	CC_ENTER_MASK	NA	OTP_MASK	PG_ENTER_MASK	PG_EXIT_MASK	NA	

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Table 0x01H Operation Command

Bit	Type	Bit Name	Default	Description
7*	R/W	ON/OFF State	1b	0b: The output is off 1b: The output is on.
6:1	NA			
0*	R/W	ON/OFF State	0b	0b: The output is off 1b: The output is on.

***** Bit 7 and bit 0 are in an OR relationship, and only one of them needs to be 1 to take effect.

Table 0x03H Operation Command

Bit	Type	Bit Name	Default	Description
7:0	W	Clear	00000000b	Write any bit to clear the fault flag and status

Table 0x21H-22H Reference Voltage Register

Bit	Type	Bit Name	Default	Description
15 - 10	R/W	Reserved	000000b	Reserved
9-0	R/W	REF	10010110b	00 00000000b = 100mV 00 00000001b = 101mV …… 00 1001 0110b = 250mV …… 01 1111 0100b = 600mV …… 11 11111111b = 1123mV

Table 0x79H STATUS1 Register

Bit	Type	Bit Name	Default	Description
7:6	NA			
5	R	VOUT_OV_FLAG	0b	If an output over voltage fault (Absolute OV or higher than 120% VREF) occurred, this bit will be set to '1'.
4	R	CC_ENTER_FLAG	0b	If IC enters CC Loop, this bit will be set to '1'.
3	NA			
2	R	OTP_FLAG	0b	If the temperature of IC is higher than 150℃, this bit will be set to '1'
1:0	NA			

Table 0x7AH STATUS2 Register

Bit	Type	Bit Name	Default	Description
7	R	VOUT_SHRT_FLAG	0b	If VOUT is lower than 2.5V, this bit will be set to '1'.
6:5	NA			
4	R	CC_EXIT_FLAG	0b	If IC exits the CC loop, this bit will be set to '1'
3	R	PG_ENTER_FLAG	0b	When the output voltage is power good，this bit will be set to '1'
2	R	PG_EXIT_FLAG	0b	When the output voltage is not power good，this bit will be set to '1'
1:0	NA			

Table 0x7DH TEMP STATUS Register

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Bit	Type	Bit Name	Default	Description
7	R	OTP_FLAG	0b	If the temperature of IC is higher than 150℃, this bit will be set to '1'
6:0	NA			

Table 0XD0H Status Register

Bit	Type	Bit Name	Default	Description
7	R/W	Dither Disable	1b	"0" Enable spread spectrum function "1" No dither
6:5	R/W	FREQ	01b	"00" 280kHz; "01" 420kHz "10" 560kHz; "11" Reserved
4:3	NA			
2	R/W	Output OVP	1b	"0" No output OVP function "1" Enable output OVP
1	R/W	DISCHG	0b	"0" Disable output voltage discharge "1" Enable output voltage discharge
0	R/W	APFM/FPWM	1b	"0" APFM "1" Forced PWM

Table 0XD1H Status Register

Bit	Type	Bit Name	Default	Description
7	NA			
6:0	R/W	Current Limit	110 1100b	Based on 5mR R_{SENSE} 000 0000b = 0mA 000 0001b = 50mA …… 100 0001b = 3.25A …… 110 1100b = 5.4A …… 111 1111b = 6.35A

Table 0XD2H Status Register

Bit	Type	Bit Name	Default	Description
7:2	NA			
1:0	R/W	CDC_GN_REG	00b	Set output voltage compensation value vs. load current: @5mR, R1=90.9k (Upper feedback resistor) 00: no compensation 01: Vout compensates 100mV@3A Iout 10: Vout compensates 300mV@3A Iout 11: Vout compensates 600mV@3A Iout

Table 0XD3H Status Register

Bit	Type	Bit Name	Default	Description
7	R/W	Switching Current Limit	1b	SWC Peak Current Limit "0": 12A "1": 19A

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6	NA			
5	R/W	RSNS	0b	Select the Rsens resistor value: 0: 5mΩ, Current Sense Gain=40 1: 10mΩ, Current Sense Gain=20
4:3	R/W	VDAC_SLEW_RATE	01	Set the VREF adjust rising slew rate. '00': 0.04mv/us Vref changing slew rate; '01': 0.08mv/us Vref changing slew rate; '10': 0.2mv/us Vref changing slew rate; '11": 0.4mv/us Vref changing slew rate; Default is "01". Vout_Slew rate=Vref_slew rate * Feedback Ratio.
2:1	NA			
0	R/W	BB2T_REG	0b	Set frequency mode under Buck-boost condition: '0': keep the same frequency as Buck and Boost mode '1' Reduce frequency to half of Buck and Boost mode.

Table 0XD4H Status Register

Bit	Type	Bit Name	Default	Description
7:6	R/W	OCP_DELAY	01b	Set the deglitch time of the device when the output overcurrent limit reached 00b = 400us; 01b = 5ms 10b = 8ms; 11b = 12ms
5	R/W	DIS_CC	0b	Enable or disable current limit 0b = Current limit enabled 1b = Current limit disabled
4:0	NA			

Table 0XD8H MASK Register

Bit	Type	Bit Name	Default	Description
7	R/W	VOUT_OV_MASK	1b	0: Not mask **1: Mask Enabled**
6	R/W	CC_ENTER_MASK	1b	0: Not mask **1: Mask Enabled**
5	NA			
4	R/W	OTP_MASK	1b	0: Not mask **1: Mask Enabled**
3	R/W	PG_ENTER_MASK	1b	0: Not mask **1: Mask Enabled**
2	R/W	PG_EXIT_MASK	1b	0: Not mask **1: Mask Enabled**
0:1	NA			

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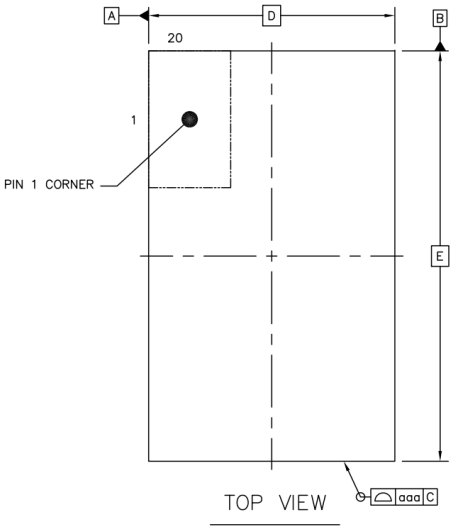
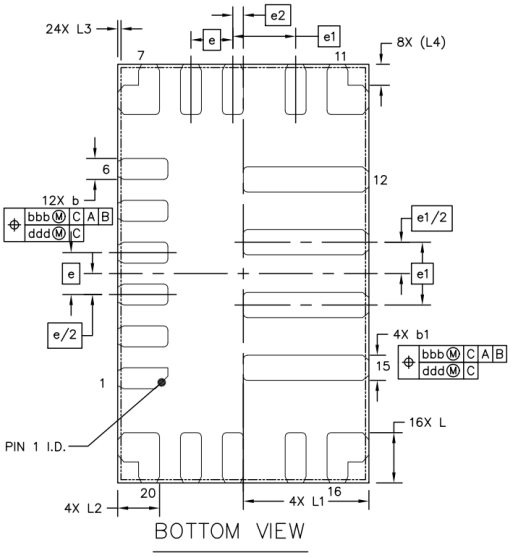
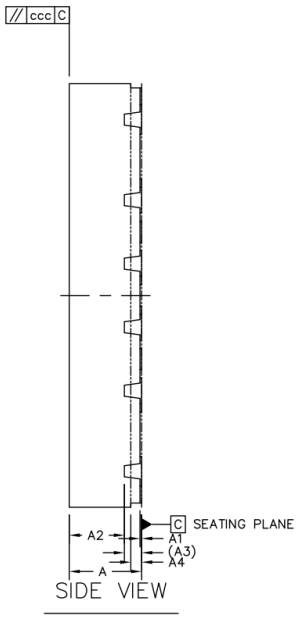
MECHANICAL DATA

Flipchip-QFN20(3x5)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.25	0.3	0.35
BODY SIZE	X	D		3 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
		e1		0.75 BSC	
LEAD CENTER TO PKG CENTER		e2		0.125 BSC	
LEAD LENGTH		L	0.5	0.6	0.7
		L1	1.4	1.5	1.6
		L2	0.4	0.5	0.6
SIDE WETTABLE WIDTH		L3	0.01	---	0.09
LEAD EDGE TO PKG EDGE		L4		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
LEAD OFFSET		bbb		0.1	
		ddd		0.05	

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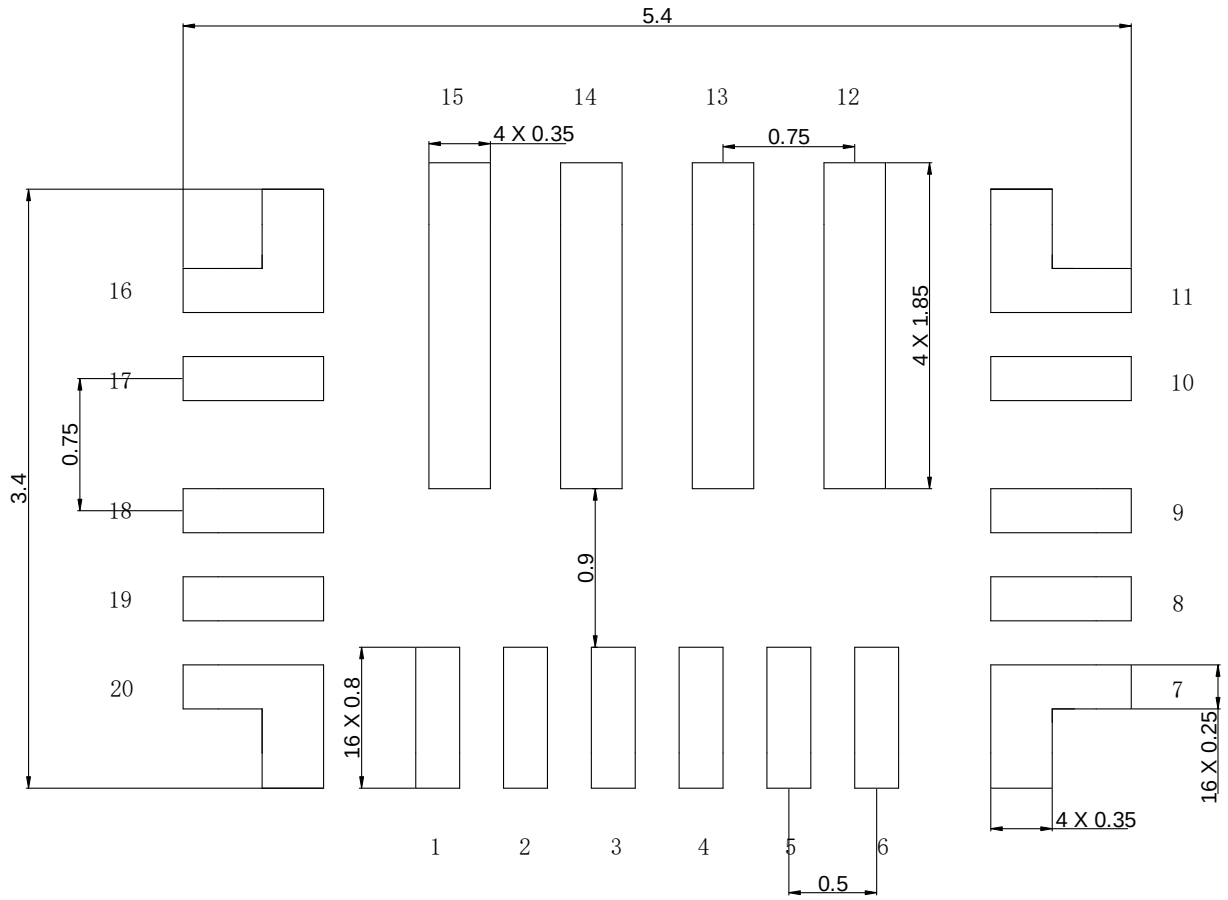
RECOMMENDED FOOTPRINT



Unit: mm

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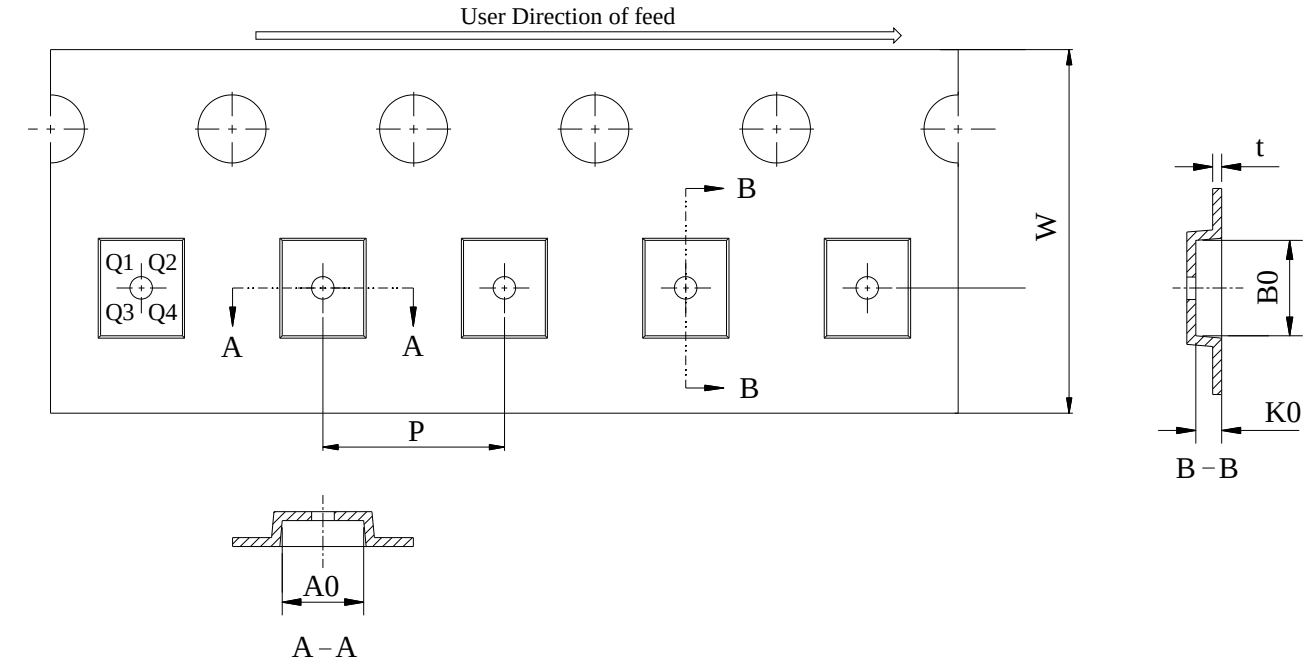
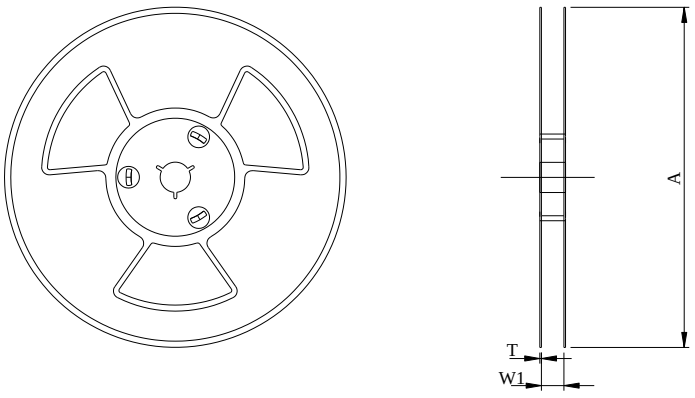
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00 + 0.30/- 0.10	8.00 +/- 0.10	3.25 ±0.10	5.25 ±0.10	1.13 ±0.10	0.25 ±0.02	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	12.4 +1/-0	2.6±0.15

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