

900mA Linear Charger for Single-Cell Li-ion Battery with Power Path Management

1 Descriptions

The SC7288 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management and I2C interface for space-limited portable applications. The SC7288 takes input power from either an AC adapter or a USB port to supply the system load and charge the battery simultaneously. The SC7288 provide the charge management functions including trickle charge, constant current charge, constant voltage charge, charge termination and auto-recharge.

The power path management function ensures continuous power to the system by automatically selecting the input, battery, or both to power the system. This function features a low dropout regulator from the input to the system and a 70mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The SC7288 provides a system short-circuit protection (SCP) function by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to an excessively high current. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below a programmable battery UVLO threshold. This prevents the Li-ion battery from being over-discharged. An integrated I2C control interface allows the SC7288 to program the charging parameters, such as input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

3 Applications

- TWS Earbuds
- Fitness Accessories
- Smart Handheld Devices
- Smart Watches

2 Features

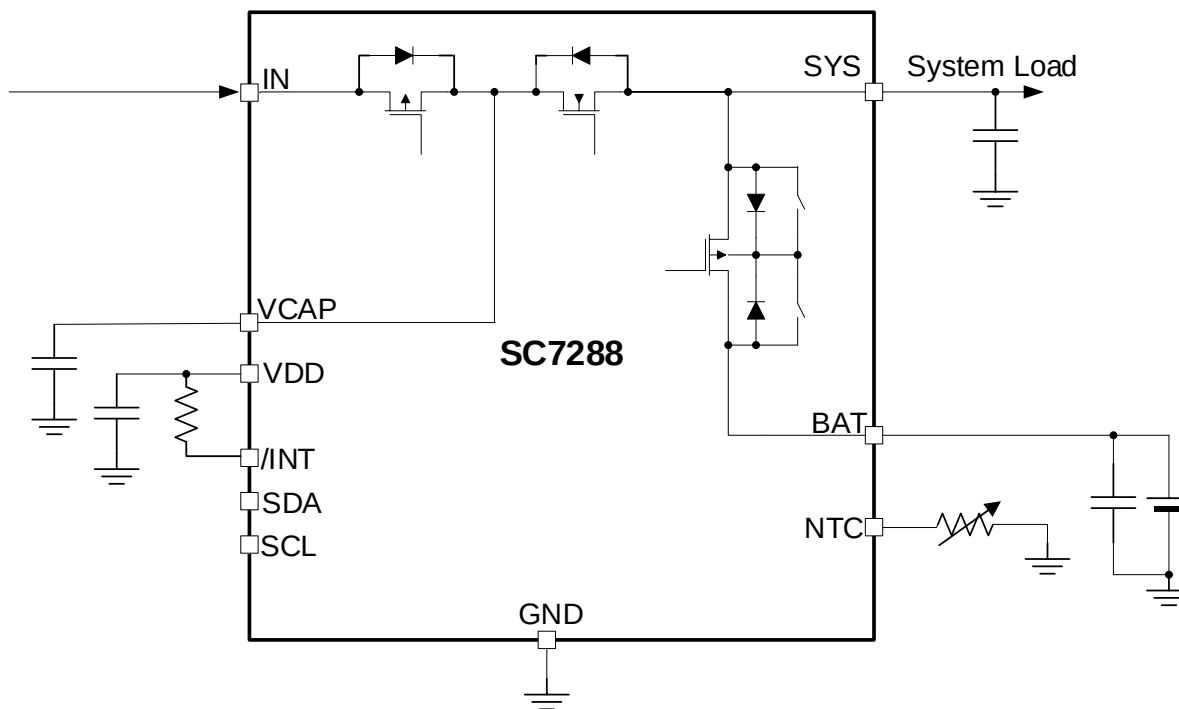
- Vin Over-Voltage Protection
- Integrated Linear Charger for Single-Cell Li-Ion/Polymer Batteries with I2C and Power Path Management, no external blocking diode required
- $\pm 0.5\%$ accuracy for VBAT Target Voltage.
- Charging Management: Trickle Charge/Constant Current Charge/Constant Voltage Charge/Charge Termination/Auto Recharge
- I2C Interface for Charging Parameters Setting and Status Reporting
- Program JEITA for Battery Protection
- PCB Over-Temperature Protection
- Input Under Voltage and Over Voltage Protection
- System Short Protection and Reset Function
- Battery Under Voltage and Over Discharge Protection
- Battery Disconnection Function (Shipping Mode)
- Thermal Regulation and Thermal Shutdown
- WCSP-12 1.55mm x 1.95mm

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC7288CFFR	WCSP-12	1.55mmx1.95mm

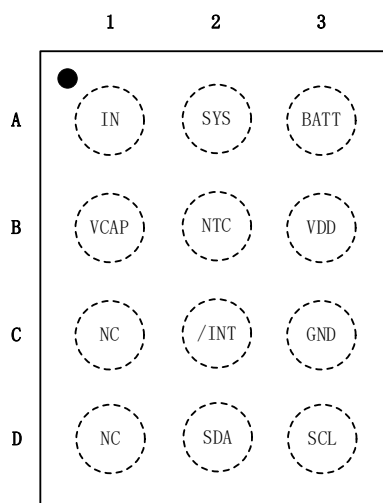


5 Typical Application Circuit





6 Terminal Configuration and Functions

TOP VIEW

TERMINAL(WCSP-12)		I/O	DESCRIPTION
NUMBER	NAME		
A1	IN	I	Power supply pin. Do not need external cap for this pin.
B2	NTC	I	Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection.
C2	/INT	O	The IC sends a logic low pulse at /INT pin to inform the host if an interrupt event happens. /INT is also used to exit shipping mode or reset the SYS. Pull INT from High to Low for 2s, the IC exit shipping mode by turns on the BATFET; Pull INT from High to Low for 16s, the IC reset the SYS by turns off and turns on the BATFET again automatically after 4s. /INT needs to be pulled up to VDD externally.
D2	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ).
D3	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ).
C3	GND	I/O	Power ground.
B3	VDD	I	Internal control power supply pin. Connect a 1uF ceramic capacitor from VDD to GND. No external load is allowed.
A3	BATT	I/O	Battery pin. Place a ceramic capacitor from BAT to GND as close to the IC as possible.
A2	SYS	O	System power supply pin. Place a ceramic capacitor from SYS to GND as close to the IC as possible.
B1	VCAP	I	Power supply pin. Place a ceramic capacitor from VCAP to GND as close to the IC as possible.
C1	NC		Not Connected
D1	NC		Not Connected



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	Unit
Voltage range at terminals ⁽²⁾	IN, VCAP	-0.3	21	V
	VSYS, /INT, SCL, SDA, BATT, NTC, VDD	-0.3	6	V
T _j	Operating junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human body model (HBM) ESD stress voltage ⁽²⁾	All pins	-2	+2	kV
	Charged device model (CDM) ESD stress voltage ⁽³⁾		-500	+500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

(4) THERMAL RESISTANCE ⁽¹⁾		WLCSP-12(1.55 x 1.95)	Unit
θ _{JA}	Junction to ambient thermal resistance	110	°C/W
θ _{JC}	Junction to case resistance	11	°C/W

Measured on JESD51-7, 4-layer PCB.

**7.4 Recommended Operating Conditions**

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		5		V
I_{IN}	Input current limit	50		1000	mA
I_{BAT}	BAT charging current	2		900	mA
I_{BAT_DISCHG}	BAT discharge current	400		3200	mA
V_{SYS_REG}	VSYS regulation voltage	4.2		4.95	V
V_{BAT_REG}	VBAT regulation voltage	3.6		4.6	V
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C



7.5 Electrical Characteristics

T_A = 25°C and V_{IN} = 5V, V_{BAT} = 3.5V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SUPPLY VOLTAGE and Battery Protection							
V _{IN}	Operating input voltage		4.6	5	5.5	V	
V _{IN_UVLO}	VIN under-voltage lockout threshold	Falling edge	2.5	2.6	2.7	V	
		Hysteresis	200			mV	
V _{IN_OVP}	VIN over-voltage protection threshold	Rising edge	5.85	6	6.15	V	
		Hysteresis	350			mV	
V _{SLEEP}	VIN-VBAT threshold	Rising edge	80	130	170	mV	
		Hysteresis	90			mV	
V _{BAT}	BAT input voltage		4.6			V	
V _{BAT_UVLO}	Battery discharge under-voltage lockout threshold	BAT voltage falling , 2.4V	2.3	2.4	2.5	V	
		BAT voltage falling , 2.76V	2.66	2.76	2.86	V	
		BAT voltage falling , 3.03V	2.93	3.03	3.13	V	
		V _{BAT_UVLO} =2.76V, Hysteresis	175			mV	
V _{BAT_OVP}	Battery voltage higher than V _{BAT_REG} protection	Rising edge	130			mV	
		Hysteresis	60			mV	
I _{Q_IN}	Input quiescent current	V _{IN} =5V,EN_HIZ=0,/CEB=0, charge enable, I _{CHG} =0A, I _{SYS} =0A , charge done	600			μA	
		V _{IN} =5V,EN_HIZ=0, /CEB=0, charge disable, I _{CHG} =0A, I _{SYS} =0A	430			μA	
		V _{IN} =5V,EN_HIZ=1,/CEB=1,V _{BAT} =3.7 V	170			μA	
I _{Q_BAT}	Battery quiescent current	V _{IN} =5V, /CEB=0, I _{SYS} =0A, charge done, V _{BAT} =4.35V	12			23	μA
		V _{IN} =GND,/CEB=1,I _{SYS} =0A,V _{BAT} =4.3 5V,disable NTC, BATOCP, INT, Watch Dog	3			4	μA
		V _{IN} =GND,/CEB=1,I _{SYS} =0A,V _{BAT} =4.3 5V,disable PCB_OTP and NTC, disable watchdog and loop INT	6.1			8	μA
		V _{IN} =GND,/CEB=1,I _{SYS} =0A,V _{BAT} =4.3 5V,enable PCB_OTP(5% current duty), disable watchdog	17			20	μA
		V _{IN} =GND,/CEB=1,I _{SYS} =0A,V _{BAT} =4.35V,enable PCB_OTP(5% current duty), enable watchdog	17			20	μA
		V _{BAT} =4.5V,V _{IN} =V _{SYS} =GND,EN_SHIPPING_MODE=1,shipping mode	201			500	nA
Power Path Management							



V _{SY_S_REG}	System regulated output voltage	V _{IN} =5V, R _{SY_S} =100 Ω , I _{CHG} =0A, V _{SY_S_REG} =4.2V	4.116	4.2	4.284	V
		V _{IN} =5V, R _{SY_S} =100 Ω , I _{CHG} =0A, V _{SY_S_REG} =4.6V	4.508	4.6	4.692	V
		V _{IN} =5V, R _{SY_S} =100 Ω , I _{CHG} =0A, V _{SY_S_REG} =4.8V	4.704	4.8	4.896	V
I _{IN_LIM}	Input current limit	I _{IN_LIM} =50mA	32	40	50	mA
		I _{IN_LIM} =140mA	114	126	140	mA
		I _{IN_LIM} =320mA	282	300	320	mA
		I _{IN_LIM} =500mA	446	470	500	mA
V _{IN_DPM}	Input minimum regulation voltage	V _{IN_REG} =3.88V	3.686	3.88	4.074	V
		V _{IN_REG} =4.6V	4.462	4.6	4.738	V
		V _{IN_REG} =5.08V	4.92	5.08	5.24	V
R _{DS_{ON}_Q1}	RDSON resistance of V _{IN} to V _{SY_S}	V _{IN} =4.5V, I _{SY_S} =100 mA	150			mΩ
R _{DS_{ON}_Q2}	RDSON resistance of V _{SY_S} to V _{BAT}	V _{IN} <2V, V _{BAT} =3.5V, I _{SY_S} =100 mA	70			mΩ
I _{BAT_DISCHG}	Battery discharge current limit	I _{BAT_DISCHG} =400 mA	420	490	585	mA
		I _{BAT_DISCHG} =2000mA	2400			mA
V _{FWD}	Q2 forward voltage in supplement mode	50mA discharge current	30			mV
Battery Charger Management						
V _{BAT_REG}	Battery regulation charge voltage	V _{BAT_REG} =3.6V	3.582	3.6	3.618	V
		V _{BAT_REG} =4.2V	4.179	4.2	4.221	V
		V _{BAT_REG} =4.3V	4.278	4.3	4.321	V
		V _{BAT_REG} =4.5V	4.477	4.5	4.522	V
I _{CC}	Constant charge current	I _{CC} =2mA	1	2	3	mA
		I _{CC} =56mA	51	56	61	
		I _{CC} =96mA	89	96	103	mA
		I _{CC} =264mA	251	264	285	mA
		I _{CC} =456mA	420	456	484	mA
I _{TC}	Trickle charge current	I _{TC} =1mA	0.9	1	1.1	mA
		I _{TC} =3mA	2.7	3	3.3	mA
		I _{TC} =9mA	8.1	9	9.9	mA
I _{TERM}	Charge termination current	I _{TERM} =1mA	0.6	1	1.4	mA
		I _{TERM} =3mA	2.3	3	3.7	mA
		I _{TERM} =9mA	8.1	9	9.9	mA
T _{TERM_DGL}	Termination deglitch time		3.2			s
V _{BAT_TC}	Trickle charge to constant current charge threshold	V _{BAT} rising, V _{BAT_TC} =3V	2.9	3	3.1	V
		V _{BAT} rising, V _{BAT_TC} =2.8V	2.7	2.8	2.9	V



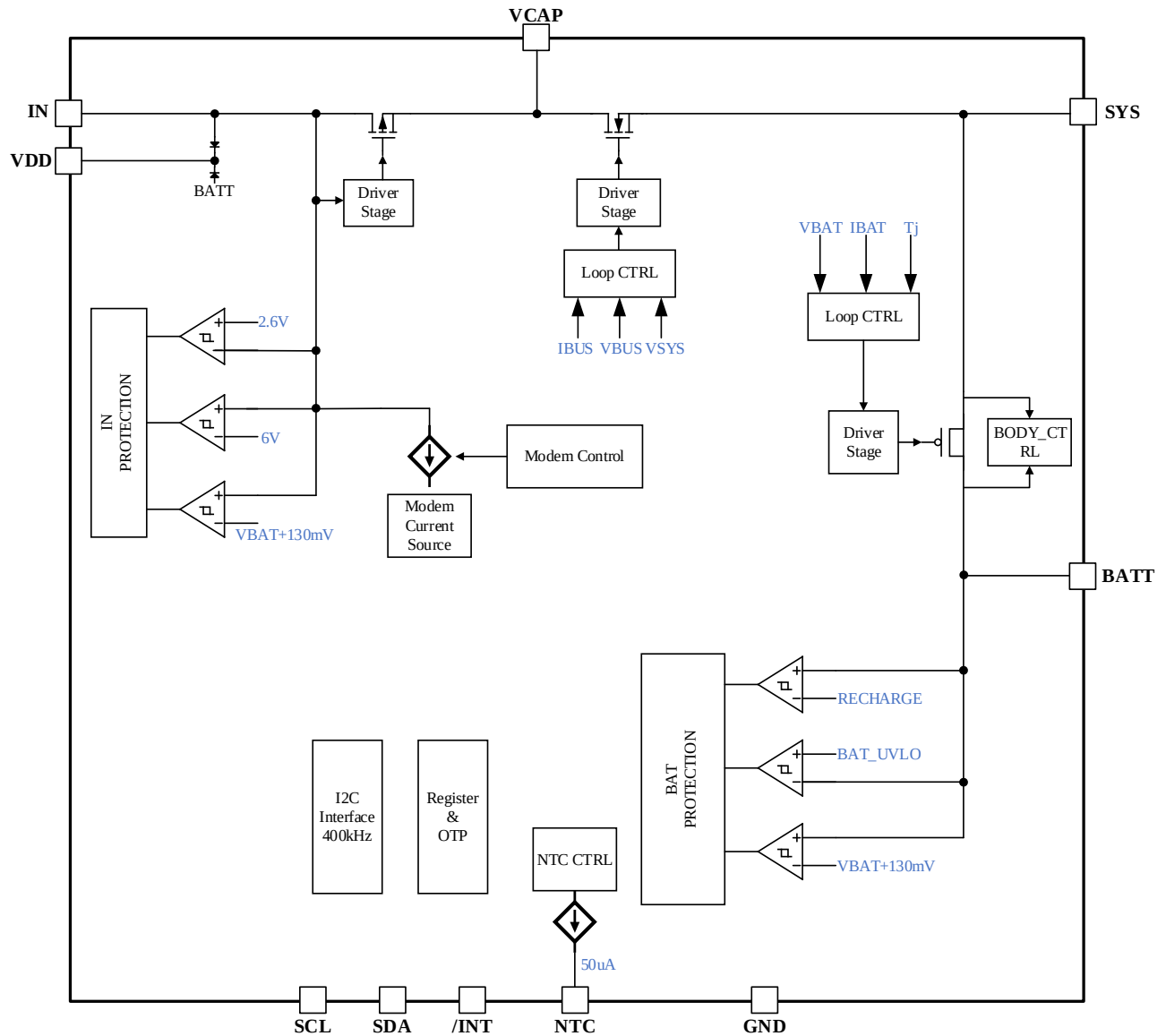
		Hysteresis	90			mV
V _{RECH}	Battery auto-recharge voltage	V _{RECH} =100mV	60	110	165	mV
		V _{RECH} =200mV	160	260	320	mV
T _{RECH_DGL}	Battery auto-recharge deglitch time		200			ms
Shipping Mode						
T _{SMEN_DEL}	Enter shipping mode delay time		0.95	1	1.05	s
T _{SMEX_DEL}	Exit shipping mode delay time by /INT	/INT is pulled low	1.9	2	2.1	s
T _{SMEX_DEL}	Exit shipping mode delay V _{IN} plug in	V _{IN} plug in	200			ms
Auto-Reset Mode						
T _{RST_DEL}	Reset by /INT pulled low	6s	5.7	6	6.3	s
		16s	15.2	16	16.8	s
T _{RST_DUR}	BATFET off time	2s	1.9	2	2.1	s
		4s	3.8	4	4.2	s
Thermal Protection						
T _{J_SD}	Thermal shutdown temperature		150			°C
	Thermal shutdown hysteresis		20			°C
T _{J_REG}	Thermal regulation temperature		120			°C
I _{NTC}	NTC output current		49	50	51	μA
V _{T1}	NTC V _{T1} temperature threshold (0°C-103AT)	Rising	1.42	1.435	1.45	V
		Hysteresis(Falling)	1.296	1.31	1.324	V
V _{T2}	NTC V _{T2} temperature threshold (5°C-103AT)	Rising	1.133	1.145	1.157	V
		Hysteresis(Falling)	0.99	1	1.01	V
	NTC V _{T2} temperature threshold (10°C-103A)	Rising	0.911	0.921	0.931	V
		Hysteresis(Falling)	0.836	0.845	0.854	V
	NTC V _{T2} temperature threshold (15°C-103AT)	Rising	0.738	0.746	0.754	V
		Hysteresis(Falling)	0.68	0.687	0.694	V
	NTC V _{T2} temperature threshold (20°C-103AT)	Rising	0.602	0.609	0.616	V
		Hysteresis(Falling)	0.556	0.562	0.568	V
V _{T3}	NTC V _{T3} temperature threshold (40°C-103AT)	Falling	0.283	0.288	0.293	V
		Hysteresis(Rising)	0.303	0.309	0.315	V
	NTC V _{T3} temperature threshold (45°C-103AT)	Falling	0.237	0.242	0.247	V
		Hysteresis(Rising)	0.254	0.259	0.264	V
	NTC V _{T3} temperature threshold (50°C-103AT)	Falling	0.2	0.205	0.209	V
		Hysteresis(Rising)	0.214	0.219	0.224	V
	NTC V _{T3} temperature threshold	Falling	0.17	0.174	0.178	V



	(55°C-103AT)	Hysteresis(Rising)	0.182	0.186	0.190	V
V _{T4}	NTC V _{T4} temperature threshold (60°C-103AT)	Falling	0.144	0.149	0.154	V
		Hysteresis(Rising)	0.154	0.159	0.164	V
V _{PCB_OTP}	PCB_OTP temperature threshold	Falling	0.237	0.242	0.247	V
		Hysteresis(Rising)	0.254	0.259	0.264	V
	PCB_OTP temperature threshold	Falling	0.17	0.174	0.178	V
		Hysteresis(Rising)	0.182	0.186	0.190	V
Logic I/O Pin						
V _{IL}	/INT,SDA,SCL, Low logic voltage threshold		0.4			V
V _{IH}	/INT,SDA,SCL, High logic voltage threshold		1.3			V
Watchdog Timer						
T _{WDT}	Watchdog Timer	160s	160			s
Safety Timer						
T _{SAFETY}	Safety Timer for Charging_TC		1			hours
	Safety Timer for Charging_CC	CHG_TMR=3hrs	3			hours
SYS RESET						
I _{discharge}			15			mA



8 Functional Block Diagram



9 Feature Description

9.1 Operation

The SC7288 is an I2C-controlled, single-cell, Li-ion or Li-polymer battery charger with a complete power path management function. The full-charge function includes trickle charge (TC), constant-current charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. The system load requirement always has priority to the charge current. When the input power is limited due to an input current limit or input voltage limit, the IC reduces the charge current automatically until the battery supplements the system load.

The SC7288 integrates a 150mΩ LDO FET between IN and SYS and a 70mΩ battery FET between SYS and BATT.

In charging mode, the on-chip 70mΩ battery FET works as a fully featured linear charger with trickle charge, constant current charge, constant voltage charge, charge termination, auto-recharge, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I2C interface. The IC adjusts the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the 70mΩ battery FET is fully turned on to connect the battery to the system load when the input power is not sufficient enough to power the system load. When the input is removed, the 70mΩ battery FET is also fully turned on to allow the battery to power up the system.

The system load is satisfied in priority, and the remaining current is used to charge the smart power path management battery. The SC7288 reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

9.2 Power Supply

The internal bias circuit of the IC is powered from the higher voltage of either IN or BATT. When IN or BATT rises above its respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and battery FET driver are all active. The I2C interface is ready for communication, and all registers are reset to the default value. The host can access all of the registers.

9.3 Input OVP and UVLO

The SC7288 has an input over-voltage protection (VIN_OVP) and an input UVLO threshold. Once the input voltage is out of its normal range, the LDO FET(Q1) is turned off immediately.

When the input voltage is a good source, a 200us immunity timer becomes active. If the input voltage is still normal until the 200us expires, the system starts up. Otherwise, Q1 remains off.

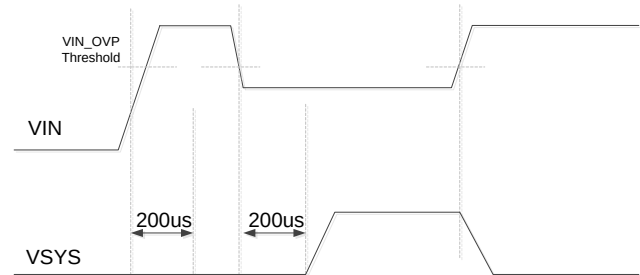


Figure 1 Input voltage detection

9.4 Power Path Management

The SC7288 employs a pass-through power path structure with the battery FET (Q2) to decouple the system from the battery. This allows for separate control between the system and the battery. The system is given the priority to start up, even with a deeply discharged or missing battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO FET.

The direct power structure consists of a LDO FET between IN and SYS and a battery FET between SYS and BATT. The LDO FET and battery FET can be controlled by the I2C.

FET On/OFF changed	Hi-Z mode and charge control	
	Set EN_HIZ to 1	Set /CEB to 1
LDO FET	OFF	Do not care
BAT FET(charging)	Do not care	OFF
BAT FET(discharging)	Do not care	Do not care

Table 1 FET control via I2C

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, (higher than V_{IN_DPM}) the LDO FET is fully on with the input current limit.

9.5 Battery Charge Management

The SC7288 provides charge management functions for 1 cell Li-ion battery. The typical charge profile is shown in Figure 2.

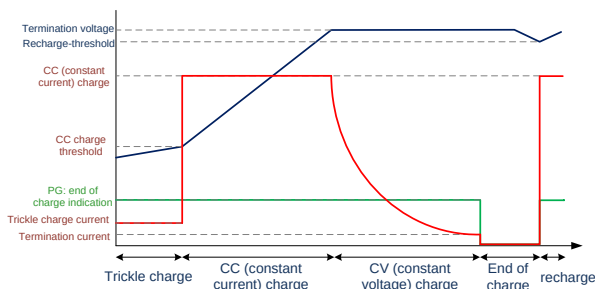


Figure 2 Typical Charge Profile

9.5.1 Trickle Charge

When VBAT is lower than V_{BAT_TC} , the SC7288 charges the battery cells in trickle charge mode (TC) which can be programmed via REG11H bit[3:0], default is 3mA.

9.5.2 Constant Current Charge

When VBAT voltage is charged above V_{BAT_TC} , the SC7288 enters into constant current charge (CC) mode. The constant current can be programmed via REG12H bit[7:0], default is 128mA with max 500mA.

9.5.3 Double Current Mode

When more than 500mA charging current is required, the user can configure SC7288 into double current mode with below steps:

- Set IINDPM register(REG10H bit [3:0]) to be 500mA
- Enable current double by set REG1DH bit[5]
- Enable IINDPM current double by set REG1DH bit[3]
- Enable ICC current double by set REG1DH bit[2]

With above operation, the charging current will be double of the ICC register setting(REG12H bit[7:0]), the max charging current is 900mA.

In this mode, if the charging current less than 15mA or adapter plug out, the /CEB(REG1DH bit[6]) and current double enable (REG1DH bit[5]) will be cleared, SC7288 exit charging mode. Users needs to set /CEB again to continue charging if termination current needs to be less than 15mA.

9.5.4 Constant Voltage Charge

When the battery voltage rises to the battery-full voltage (V_{BAT_REG}) set via REG 13H bit[6:0], default is 4.2V, the

charge mode changes from CC mode to CV mode. In CV mode, the battery voltage is regulated at V_{BAT_REG} . The charge current automatically drops.

9.5.5 Charge Termination/End of Charge

When below conditions are valid, the SC7288 recognizes the battery cell is fully charged:

- The charge current is lower than I_{TERM} and in CV charge .
- Above condition is met with 3.2s deglitch time.

The termination charge current threshold (I_{TERM}) can be programmed via REG 11H bit[3:0], default is 3mA.

EN_TERM	TERM_TMR	Fully charged	
		Operation	Charge status
0	Do not care	Keep CV charge	Charge
1	0	Charge done	Charge done
1	1	Keep CV charge	Charge done

Table 2 Termination Function (top off timer disable)

EN_TERM	TERM_TMR	Top Off Timer Counting	
		Operation	Charge status
1	Do not care	Charging	Charging
		Top Off Timer end	
		Operation	Charge status
		Charge done	Charge done

Table 3 Termination Function (top off timer enable)

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. In this cases, the charger will not report EOC.

A new charge cycle starts when any of the following conditions are valid:



- The input power is recycled .
- Battery charging is enabled via the I2C.
- Auto-recharge kicks in.

Under the following conditions:

- No thermistor fault at NTC Cold and Hot.
- No safety timer fault.
- No battery over-voltage event.
- BAT FET is not forced off.

9.5.6 TOP OFF TIMER

At low termination current , due to the comparator offset, the actual termination current may be higher than the termination target. in order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer. TOPOFF_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

Top off timer gets reset at one of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value via REG14H [6:3] after termination will have no effect unless a recharge cycle is initiated. An INT is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

9.5.7 Auto Recharge

When the battery is fully charged and charging is terminated/done , the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold and VIN is still in the operating range, the SC7288 begins another new charging cycle automatically without having to restart a charging cycle manually.

The auto-recharge function is valid only when EN_TERM = 1 and TERM_TMR = 0.

9.6 Battery OVP

The SC7288 is designed with a built-in battery over-voltage limit (about 130mV higher than V_{BAT_REG}). When a battery over-voltage event occurs, the SC7288 suspends charging immediately and asserts a fault.

9.7 Power Path Management

To meet the input source's (typically USB) maximum current limit specification, the SC7288 uses an input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the I2C to prevent the input source from being over-loaded.

If the preset input current limit is higher than the rating of the input source, the back-up input voltage-based power management also works to prevent the input source from being over-loaded. Either the input current limit or the input voltage limit is reached, the Q1 FET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to a minimum value of $V_{SYS_REG} - 135mV$ and $V_{IN} - 345mV$, the charge current is reduced to prevent the system voltage from dropping further.

The voltage-based DPM regulates the input voltage to V_{IN_MIN} when the load is over the input power capacity.

V_{IN_MIN} set via the I2C should be at least 250mV higher than V_{BAT_REG} to ensure the stable operation of the regulator.

9.7.1 Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is reduced to zero and the input source is still overloaded due to a heavy system load, the system voltage begins decreasing. Once the system voltage drops to 30mV below the battery voltage, the SC7288 enters battery supplement mode, and the ideal diode mode is enabled. The battery FET is regulated to keep $V_{BAT} - V_{SYS}$ at 22.5mV when I_{DSCHG} (supplement current) * R_{ON_BAT} is lower than 22.5mV. In the case that $I_{DSCHG} * R_{ON_BAT}$ is higher than 22.5mV, the battery FET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than $V_{BAT} + 20mV$, the ideal diode mode is disabled. Figure 3 shows the dynamic power management and battery supplement mode operation profile.

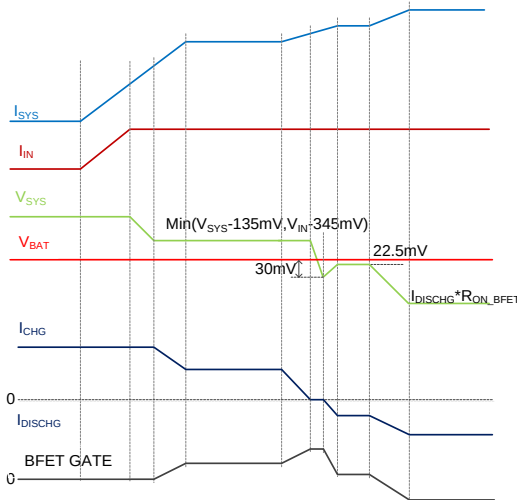


Figure 3 Typical DPM Operation Profile

9.8 Battery Regulation Voltage

The battery voltage for the constant voltage regulation phase is V_{BAT_REG} . When $V_{BAT_REG} = 4.2V$, it has a $\pm 0.5\%$ accuracy.

9.9 Negative Temperature Coefficient (NTC) Temperature Sensor

The SC7288 monitors the battery cells' temperature through NTC pin once V_{IN} is above ULVO threshold. It can support NTC or JEITA standard flexibly by different register setting.

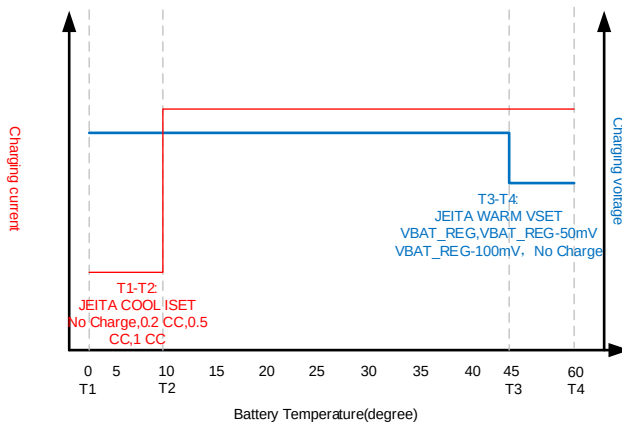


Figure 4 NTC&JEITA Operation

In the SC7288, the I2C default setting is PCB_OTP. This function can be changed through the I2C.

I2C Control		Function
EN_NTC	EN_PCB_OTP	
0	x	Disable
1	1	NTC/JEITA
1	0	PCB_OTP

Table 3 NTC Function Selection

When PCB_OTP is selected and the NTC voltage is lower than the PCB_OTP threshold, both the LDO FET and battery FET or only battery FET are off. The PCB_OTP fault also sets the NTC_FAULT status to 1 to show the fault. Operation resumes once the NTC voltage is higher than the PCB_OTP threshold.

The NTC/JEITA function works only in charge mode. Once the NTC voltage is Cold or Hot, the SC7288 stops charging and report it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

9.10 Safety Timer

The IC provides both a trickle charge and a constant current charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer is one hour for trickle charge. The constant current charge (including cv charge) safety timer can be programmed through the I2C, default is 5 hours. The safety timer feature can be disabled via the I2C. Safety timer will double when PPM, thermal regulation or NTC Cool, this feature can also be disabled by I2C.

During the fault (VBUSOVP, VBAT OVP, NTC_FAULT, thermal shutdown), timer is suspended. Once the fault goes away, timer resumes.

The following actions can restart the safety timer:

- A new charge cycle is kicked in
- Toggle charge enable
- Toggle safety timer enable
- Toggle software reset

9.11 Host Mode and Default Mode

The SC7288 is a host-controlled device. After the power-on reset, the SC7288 starts up in a watchdog timer expiration state or default mode. All registers are in their default settings.



The watchdog timer works in both charge and discharge mode. When the watchdog timer runs out, most registers return to the default value (refer to the I2C Register Map section). When the watchdog timer is out in both charge and discharge mode, both the LDO FET and battery FET are turned off. They turn on again automatically after T_{RST_DUR} .

To save quiescent current during discharge mode, the watchdog timer can be turned off.

Any write to the SC7288 switches it to host mode. All charge parameters are programmable. If the watchdog timer is not disabled, the host must reset the watchdog timer regularly by writing 1 to before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the SC7288 goes back to default mode. The watchdog timer limit can also be programmed or disabled by the host control.

Operation can also be switched to default mode when one of the following conditions are valid:

- Refresh input without battery.
- Re-insert battery with no V_{IN} .
- Register reset.

9.12 Battery Discharge

If the battery is connected and the input source is missing, the battery FET is fully on when V_{BAT} is above the V_{BAT_UVLO} threshold. The 70mΩ battery FET minimizes conduction loss during discharge. The quiescent current of the SC7288 is as low as 6μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

9.13 Over-Discharge Current Protection

The SC7288 has an over-discharge current protection in discharge mode and supplement mode. Once I_{BAT} exceeds the programmable discharge current limit (2A default), the battery FET turns off after a 60μs delay. The SC7288 enters hiccup mode as part of the over-current protection (OCP). The discharge current can be programmed high to 3.2A through the I2C. If the discharge current goes high and reaches the internal fixed current limit (about 3.7A), the battery FET turns off and begins hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable V_{BAT_UVLO} threshold (2.76V default), the battery FET turns off to prevent an over-discharge.

9.14 System Short-Circuit Protection

The SC7288 features SYS node short-circuit protection (SCP) for both the IN to SYS path and the BAT to SYS path.

The system voltage is monitored continuously. If V_{SYS} is lower than 1.5V, system SCP for both the IN to SYS path and the BAT to SYS path is active. I_{DSCHG} decreases to half of the original value.

For the IN to SYS path, once I_{IN} is over the protection threshold, both the LDO FET and battery FET are turned off immediately, and the SC7288 enters hiccup mode. Otherwise, the maximum current limit is not reached. When the setting input current limit is reached, I_{IN} is regulated at I_{IN_LIM} . Hiccup mode also starts after a 60μs delay. The hiccup mode interval is 800μs.

For the BAT to SYS path, once I_{BAT} is over the 3.7A protection threshold, both the LDO FET and battery FET are turned off immediately, and the SC7288 enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The hiccup mode interval is 800μs.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation.

9.15 INT

The SC7288 also has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All of the below events can trigger an INT output:

- Good input source detected (VBUS plug in)
- V_{IN_UVLO} (VBUS plug out) or V_{IN_OVP}
- Charge done
- Charging status change(Not charge ,TC, CC, CV, EOC)
- Watchdog timer out, thermal shutdown, safety timer out, battery OVP, NTC COLD/HOT
- Receive effective command
- Top off timer counting end
- Q1&Q2 Status Change(OFF to ON, or ON to OFF)
- Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode or to allow the system power to be reset during the application. The SC7288 provides both shipping mode and system reset mode for different applications.

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set EN_Shipping_Mode to 1	/INT H to L for 2s	V _{IN} Plug IN
LDO FET	Do not care	Do not care	On
BATFET	Off	On	On

Table 4 Shipping Mode Control

The IC has a register bit for battery disconnection control (FET_DIS). If this bit is set to 1, the SC7288 enters shipping mode after a delay time. The battery FET turns off, and the EN_Shipping_Mode bit refreshes to 0 after the battery FET turns off. Pull the /INT pin down or plug in the input adapter wake the SC7288 up from shipping mode.

9.16 System Reset Function

The SC7288 can also reuse an /INT pin to cut off the path from the battery to the system under the condition needed to reset the system manually. Once the logic at INT is set low for longer than T_{RST_DLE}, the battery is disconnected from the system by turning off the battery FET. The off state lasts for T_{RST_DUR}. Then the battery FET is turned on automatically, and the system is powered by the battery again. During the off period, the INT pin is not limited to be high or low.

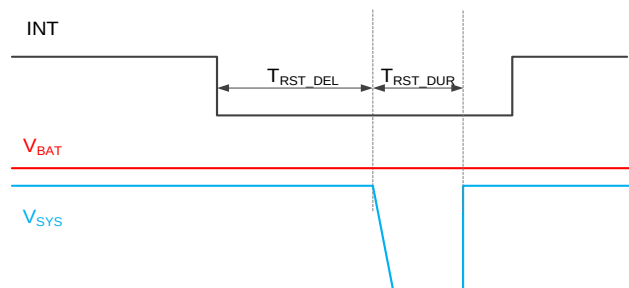


Figure 6 System Reset Operation

9.17 I2C

9.17.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x07. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to

100kbps) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

9.17.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

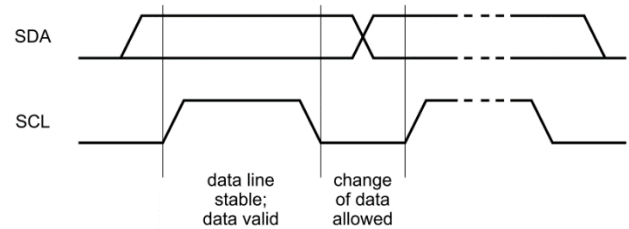


Figure13 Bit transfer on the I2C bus

9.17.3 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

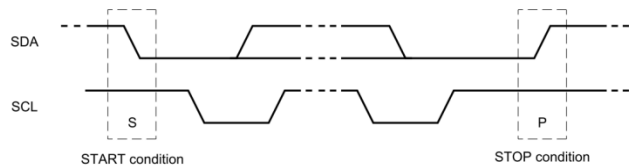


Figure14 START and STOP conditions

9.17.4 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

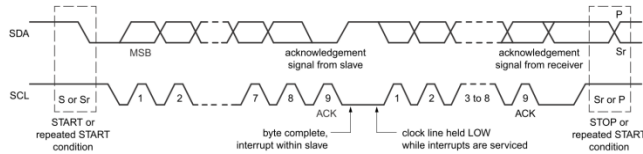


Figure15 Data transfer on the I2C bus

9.17.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

9.17.6 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

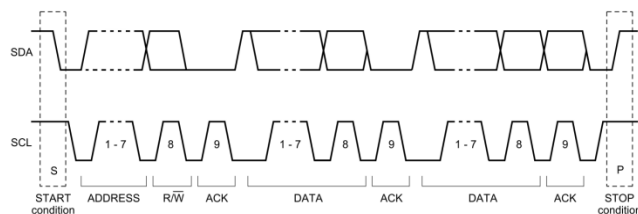


Figure16 complete data transfer

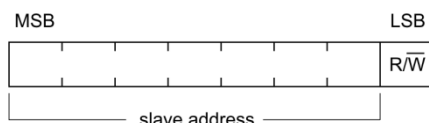


Figure17 The first byte after the START procedure

9.17.7 Single Read and Write

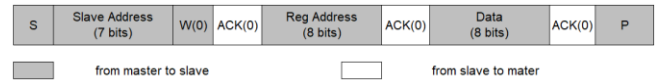


Figure18 Single Write

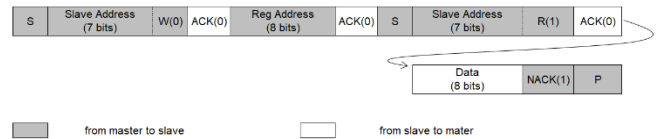


Figure19 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.17.8 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

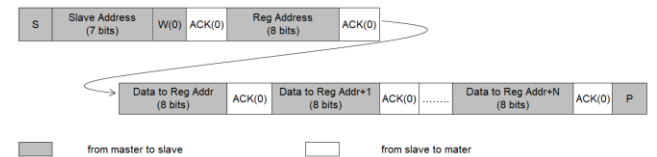


Figure20 Multi-Write

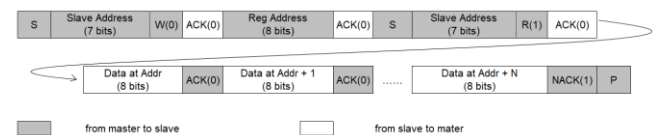


Figure21 Multi-Read



10 Application Information

10.1 Input Capacitor Selection

Typically, a 4.7 μ F X5R ceramic capacitor for VCAP pin and a 1 μ F X5R ceramic capacitor for VDD pin should be sufficient to suppress the power supply noise. No capacitor need for IIN pin.

10.2 Output Capacitor Selection

Typically, a 10 μ F X5R ceramic capacitor for SYS pin and a 4.7 μ F X5R ceramic capacitor for BATT pin to maintain the stability of the charger as well as to bypass any transient load current.

10.3 Layout Guideline

Put the external capacitors as close to the IC as possible to make sure the smallest input inductance and the ground impedance.

The PCB trace to connect the capacitor between VDD and GND is very important, and it should be put very close to the IC.

SOUTHCHIP SEMICONDUCTOR
11 Register Map

7-bit address: 0x07

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	PRODUCT ID	R	00110000	MAF ID				MAJOR ID		MINOR ID	
01H	DEVICED ID	R	00000101	DEVICE ID							
02H	ADDRESS	R	111XXXXX	ADDR			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
10H	CHG INPUT	RW	10011111	VIN_REG				IIN_LIM			
11H	CHR PRE TERM	RW	00100010	ITERM				IPRE			
12H	CHG CC	RW	01000000	ICC							
13H	CHG CV	RW	10111100	VPRE	VBAT_REG						
14H	CHG_CF1	RW	10000100	VREC	TTOP OFF				VBAT UVLO		
15H	CHG_CF2	RW	10001001	VSYS_REG				IDISCHG			
17H	TERM	RW	10X11111	EN TERM	TERM TMR	RESERVED	RESERVED				
18H	EN CTRL	RW	1111001X	EN THERMAL	TJREG		EN NTC	EN PCBOTP	DNTC		RESERVED
19H	JEITA	RW	10110101	JEITA_TW_ISET		JEITA_T3_VSET		JEITA_T2_TEMP		JEITA_T3_TEMP	
1AH	SYS CTRL1	RW	XXX01100	RESERVED	RESERVED	RESERVED	T_SHIPPING_MODE_DELAY		T_RST_DEL		T_RST_DUR
1BH	SYS CTRL2	RW	101X1011	EN_INT_PULSE	T_INT_EX_S HIPPING_M ODE	EN_BATOC	RESERVED	EN_TIMER	TCHG		EN_TMR_2X
1CH	SYS CTRL3	RW	1XXXX110	EN_LOOP_INT	RESERVED	RESERVED	RESERVED		TWD		EN_WD_DIS CHG
1DH	EN&RESET	RW	01000010	EN_HIZ	/CEB	DOUBLE CURRENT EN	EN_SHIPPING _MODE	IINDPM DOUBLE	ICC DOUBLE	DPM_EN	REG_RST
30H	STAT0	R	X0000000	RESERVED	CHG STAT		PPM_STAT	PG_STAT	THERMAL_ST AT	RESERVED	Q1&Q2_STAT
31H	STAT1	R	00000XXX	WD_STAT	RESERVED	RESERVED		RESERVED	NTC_STAT		
32H	STAT2	R	00000XXX	VINOVP/UVLO	TSD	SAFETY_TI MER_OUT	RESERVED	TOP_OFF_ACTI VE	RESERVED	RESERVED	RESERVED
40H	INT0	RW1C	00000000	CHRG_STAT_C HANGING_INT	EOC_INT	PPM_INT	PG_INT	THERMAL_INT	RESERVED	VINDPM_INT	TOP_OFF_TI MER_INT

SOUTHCHIP SEMICONDUCTOR

41H	INT1	RW1C	00000000	VINFAULT_INT	THERMAL_S D_INT	BAT_FAULT _INT	SAFETY_TIME R_OUT_INT	NTC_INT	RESERVED	RESERVED	RESERVED
42H	INT2	RW1C	00000000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NTC_STAT_ CHANGE_IN T	WD_FAULT_I NT
43H	INT3	RW1C	00000000	Q1&Q2_ON_INT	Q1&Q2_OFF _INT	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
44H	INT4	RW1C	XXXXXXXX	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
50H	MASK0	RW	00000000	CHRG_STAT_C HANGING_INT_ M	EOC_INT_M	PPM_INT_M	PG_INT_M	THERMAL_INT_ M	RESERVED	VINDPM_INT _M	TOP_OFF_TI MER_INT_M
51H	MASK1	RW	00000000	VINFAULT_INT_ M	THERMAL_S D_INT_M	BAT_FAULT _INT_M	SAFETY_TIME R_OUT_INT_M	NTC_INT_M	RESERVED	RESERVED	RESERVED
52H	MASK2	RW	00000000	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	NTC_STAT_ CHANGE_IN T_M	WD_FAULT_I NT_M
53H	MASK3	RW	00000000	Q1&Q2_ON_INT _M	Q1&Q2_OFF _INT_M	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
5AH	WD RESET	RW1C	XXXXXXX0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WD RESET

REG 00H PRODUCT ID ([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	MAF_ID[3]	0	NA	NA	Manufacture ID	
6	R	MAF_ID[2]	0	NA	NA		
5	R	MAF_ID[1]	1	NA	NA		
4	R	MAF_ID[0]	1	NA	NA		
3	R	MAJOR_ID[1]	0	NA	NA	Major version ID	
2	R	MAJOR_ID[0]	0	NA	NA		
1	R	MINOR_ID[1]	0	NA	NA	Minor version ID	
0	R	MINOR_ID[0]	0	NA	NA		

REG 01H DEVICE ID([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	DEVICE_ID[7]	0	NA	NA	Device ID	
6	R	DEVICE_ID[6]	0	NA	NA		
5	R	DEVICE_ID[5]	0	NA	NA		
4	R	DEVICE_ID[4]	0	NA	NA		
3	R	DEVICE_ID[3]	0	NA	NA		
2	R	DEVICE_ID[2]	1	NA	NA		
1	R	DEVICE_ID[1]	0	NA	NA		
0	R	DEVICE_ID[0]	1	NA	NA		

REG 02H ADDR([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	Address	1	NA	NA	001: 01H; 010: 02H; 011: 03H ; 100: 04H; 101: 05H; 110: 06H; 111: 07H	I2C Address. Default: 111 (07H)
6	R		1	NA	NA		
5	R		1	NA	NA		
4	R	REV	X	NA	NA		
3	R	REV	X	NA	NA		
2	R	REV	X	NA	NA		
1	R	REV	X	NA	NA		
0	R	REV	X	NA	NA		

REG 10H CHG INPUT([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R/W	V _{IN_REG} [3]	1	Y	N	640mV	Offset: 3.88V Range: 3.88V - 5.08V Default: 4.60V (1001)
6	R/W	V _{IN_REG} [2]	0	Y	N	320mV	
5	R/W	V _{IN_REG} [1]	0	Y	N	160mV	
4	R/W	V _{IN_REG} [0]	1	Y	N	80mV	
3	R/W	I _{IN_LIM} [3]	1	Y	N	240mA	Offset: 50mA Range: 50mA - 500mA Default: 500mA (1111)
2	R/W	I _{IN_LIM} [2]	1	Y	N	120mA	
1	R/W	I _{IN_LIM} [1]	1	Y	N	60mA	
0	R/W	I _{IN_LIM} [0]	1	Y	N	30mA	

REG 11H CHR PRE ITERM([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	I _{TERM} [3]	0	Y	Y	8mA	Offset: 1mA Range: 1mA - 16mA Default: 3mA (0010)
6	RW	I _{TERM} [2]	0	Y	Y	4mA	
5	RW	I _{TERM} [1]	1	Y	Y	2mA	
4	RW	I _{TERM} [0]	0	Y	Y	1mA	
3	RW	I _{RRE} [3]	0	Y	Y	8mA	Offset: 1mA Range: 1mA - 16mA Default: 3mA (0010)
2	RW	I _{PRE} [2]	0	Y	Y	4mA	
1	RW	I _{PRE} [1]	1	Y	Y	2mA	
0	RW	I _{PRE} [0]	0	Y	Y	1mA	

REG 12H CHG CC([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	I _{CC} [7]	0	Y	Y	256mA	CC charge current Range: 2 mA - 510 mA Default: 128 mA (01000000) 0000=0001=2mA(Low clamp)
6	RW	I _{CC} [6]	1	Y	Y	128mA	
5	RW	I _{CC} [5]	0	Y	Y	64mA	
4	RW	I _{CC} [4]	0	Y	Y	32mA	
3	RW	I _{CC} [3]	0	Y	Y	16mA	
2	RW	I _{CC} [2]	0	Y	Y	8mA	
1	RW	I _{CC} [1]	0	Y	Y	4mA	
0	RW	I _{CC} [0]	0	Y	Y	2mA	

REG 13H CHG CV ([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	V _{PRE}	1	Y	Y	0: 2.8V 1: 3V	Pre charge to CC battery voltage Default: 3V (1)
6	RW	V _{BAT_REG} [6]	0	Y	Y	640mV	Offset: 3.6V Range: 3.6V-4.6V Default: 4.2V(0111100) Clamp to 4.6V
5	RW	V _{BAT_REG} [5]	1	Y	Y	320mV	
4	RW	V _{BAT_REG} [4]	1	Y	Y	160mV	
3	RW	V _{BAT_REG} [3]	1	Y	Y	80mV	
2	RW	V _{BAT_REG} [2]	1	Y	Y	40mV	
1	RW	V _{BAT_REG} [1]	0	Y	Y	20mV	
0	RW	V _{BAT_REG} [0]	0	Y	Y	10mV	

REG 14H CHG CFG1([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	V _{REC}	1	Y	Y	0: 100mV 1: 200mV	Recharge Voltage Default: 200mV (1)
6	RW	T _{TOP_OFF} [3]	0	Y	Y	40min	Range: 0min(disable)-75min Default: disable(0000) During Top off timer active, charging status is charging
5	RW	T _{TOP_OFF} [2]	0	Y	Y	20min	
4	RW	T _{TOP_OFF} [1]	0	Y	Y	10min	
3	RW	T _{TOP_OFF} [0]	0	Y	Y	5min	
2	RW	V _{BAT_UVLO} [2]	1	Y	Y	360mV	Battery UVLO threshold; Offset: 2.4V Range: 2.4V-3.03V Default: 2.76V(100)
1	RW	V _{BAT_UVLO} [1]	0	Y	Y	180mV	
0	RW	V _{BAT_UVLO} [0]	0	Y	Y	90mV	

REG 15H CHG CFG2([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	V _{SYS_REG} [3]	1	Y	N	400mV	Offset: 4.2V Range: 4.2V - 4.95V Default: 4.6V (1000)
6	RW	V _{SYS_REG} [2]	0	Y	N	200mV	
5	RW	V _{SYS_REG} [1]	0	Y	N	100mV	
4	RW	V _{SYS_REG} [0]	0	Y	N	50mV	
3	RW	I _{DISCHARGE} [3]	1	Y	Y	1600mA	Offset: 200mA ; Range: 400mA – 3.2A 0000=0001=400mA Default: 2000mA (1001)
2	RW	I _{DISCHARGE} [2]	0	Y	Y	800mA	
1	RW	I _{DISCHARGE} [1]	0	Y	Y	400mA	
0	RW	I _{DISCHARGE} [0]	1	Y	Y	200mA	

REG 17H TERM([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	EN_TERM	1	Y	Y	0:Disable 1:Enable	Termination setting (controlling the termination is allowed or not). Default: Enable (1)
6	RW	TERM_TMR	0	Y	Y	0:Disable 1:Enable	Termination timer control (when TERM_TMR is enabled, the IC will not suspend the charge current after the charge termination). Default: (0)
5	RW	REV	X	NA	NA		
4	RW	REV	X	NA	NA		
3	RW	REV	X	NA	NA		
2	RW	REV	X	NA	NA		
1	RW	REV	X	NA	NA		
0	RW	REV	X	NA	NA		

REG 18H EN CTL([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	EN_THERMAL	1	Y	Y	0: disable thermal loop 1: enable thermal loop	Default: Enable (1)
6	RW	T_JEG[1]	1	Y	Y	00: 60°C; 01: 80°C; 10: 100°C; 11: 120°C	Only works in EN_THERMAL=1
5	RW	T_JEG[0]	1	Y	Y		
4	RW	EN_NTC	1	Y	Y	0: Disable 1: Enable	
3	RW	EN_PCB_OTP	0	Y	Y	0: Enable 1: Disable	
2	RW	D_NTC[1]	0	Y	Y	00: 0%; 01: 5%; 10: 10%; 11: 100%	Time period is 5s(0.2Hz). Default: 5%
1	RW	D_NTC[0]	1	Y	Y		
0	RW	REV	X	NA	NA		

REG 19H JEITA([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	JEITA_T2_ISET[1]	1	Y	Y	CC current setting during T2(Cool) temperature range, as percentage of ICC	Default:50% of ICC in NTC COOL(10) Don not work in Direct MODE
6	RW	JEITA_T2_ISET[0]	0	Y	Y	00 : No Charge 01 : 20% of ICC 10 : 50% of ICC 11 : 100% of ICC (default ,safety timer does not become 2X)	
5	RW	JEITA_T3_VSET[1]	1	Y	Y	CV charge voltage setting during T3(warm) temperature range.	Default: VBAT_REG-100mV in NTC WARM(11) Don not work in Direct MODE
4	RW	JEITA_T3_VSET[0]	1	Y	Y	00: No Charge 01: VBAT_REG 10: VBAT_REG -50mV 11: VBAT_REG -100mV	
3	RW	JEITA_T2_TEMP[1]	0	Y	Y	00 : 1.145V(5°C)	Default:10°C (01)
2	RW	JEITA_T2_TEMP[0]	1	Y	Y	01 : 0.921V (10°C) (default) 10 : 0.746V (15°C) 11 : 0.609V (20°C)	
1	RW	JEITA_T3_TEMP[1]	0	Y	Y	00 : 0.288V (40°C)	Default:45°C (01)
0	RW	JEITA_T3_TEMP[0]	1	Y	Y	01 : 0.242V (45°C) (default) 10 : 0.205V (50°C) 11: 0.174V (55°C) PCBOTP is the same threshold with JEITA_T3_TEMP	



SOUTHCHIP SOUTHCHIP SEMICONDUCTOR

REG 1AH SYS CTL1([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	REV	X	NA	NA		
6	RW	REV	X	NA	NA		
5	RW	REV	X	NA	NA		
4	RW	T _{SHIPPING_DLY} [1]	0	Y	N	00: 0s ; 01: 1s ; 10: 2s ; 11: 4s	Enter shipping mode deglitch time Default: 1s (01)
3	RW	T _{SHIPPING_DLY} [0]	1	Y	N		
2	RW	T _{RST_DEL} [1]	1	Y	Y	00: 6s; 01: 12s; 10: 16s; 11: 20s	Pull INT low to reset system. Default: 16s(10)
1	RW	T _{RST_DEL} [0]	0	Y	Y		
0	RW	T _{RST_DUR}	0	Y	N	0:2s; 1:4s	BATFET Off Time during system reset. Default: 2s(0)

REG 1BH SYS CTL2([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	EN_INT_PULSE	1	Y	Y	0: disable INT pulse output 1: enable INT pulse output	Do not affect INT existing shipping mode and system reset function. Default: enable (1)
6	RW	T _{INT_EX_SHIPPING_DEL}	0	Y	Y	0: 2s; 1: 100ms	Default: 2s (0)
5	RW	EN_BATOCPP	1	Y	N	0: disable BATOCPP function 1: enable BATOCPP function	Default: Enable (1)
4	RW	REV	X	NA	NA		
3	RW	EN_TIMER	1	Y	Y	0:Disable 1:Enable	Safety timer setting. Default: Enable timer (1)
2	RW	T _{CHG} [1]	0	Y	Y	00: 3hrs; 01: 5 hrs; 10: 8hrs; 11: 12hrs	CC charge safety timer Default: 5hrs(01)
1	RW	T _{CHG} [0]	1	Y	Y		
0	RW	EN_TMR_2X	1	Y	Y	0: Disable 2X extended safety timer during PPM and thermal regulation 1: Enable 2X extended safety timer during PPM and thermal regulation	Default: Enable (1)

REG 1CH SYS CTL3([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	EN_LOOP_INT	1	Y	Y	Enable loop interrupt when interrupt status is not cleared 0: disable 1: enable	Default: Enable (1)
6	RW	REV	X	NA	NA		
5	RW	REV	X	NA	NA		
4	RW	REV	X	NA	NA		
3	RW	REV	X	NA	NA		
2	RW	T _{wd} [1]	1	Y	N	00: disable WD; 01: 40s; 10: 80s; 11: 160s	Default: 160s(11) disable WD works for both charging and discharging
1	RW	T _{wd} [0]	1	Y	N		
0	RW	EN_WD_DISCHG	0	Y	N	0:Disable 1:Enable	Watchdog control in discharge mode. Default: Disable (0)

REG 1DH EN&RESET([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	EN_HIZ	0	Y	Y	0: Disable 1: Enable	Default: disable(0)
6	RW	/CEB	1	Y	Y	0: Charger enable 1: Charger disable	Default: disable(1)
5	RW	DOUBLE CURRENT EN	0	Y	Y	0: Disable 1: Enable	
4	RW	EN_SHIPPING_MODE	0	Y	N	0: Enable(BATFET ON) 1: Turn off(BATFET OFF)	
3	RW	IINDPM DOUBLE	0	Y	Y	0: disable 1: enable iindpm register(0X10[3:0]) double	Only works with 0X1D[5]=1, both step and offset will double
2	RW	ICC DOUBLE	0	Y	Y	0: disable 1: enable icc register(0X12[7:0]) double	Only works with 0X1D[5]=1, both step and offset will double
1	RW	DPM_EN	1	Y	Y	0: disable 1: enable	Default: enable(1)
0	RW1C	REG RESET	0	N	N	0: Keep current setting 1: Reset	Default: Keep current setting(0)

REG 30H STAT0([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	REV	X	NA	NA		
6	R	CHG_STAT	0	NA	NA	00: Not charging 01: Pre charge 10: CC Charge 11: Charge done	
5	R		0	NA	NA		
4	R	PPM_STAT	0	NA	NA	0: No PPM 1: In PPM	
3	R	PG_STAT	0	NA	NA	0: Power fail 1: Power good	
2	R	THERMAL_STAT	0	NA	NA	0: No thermal regulation 1: In thermal regulation	
1	R	REV	X	NA	NA		
0	R	Q1&Q2_STAT	0	NA	NA	0: OFF 1: ON	

REG 31H STAT1([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	WD_STAT	0	NA	NA	0: Normal 1: Watchdog timer out	
6	R	REV	X	NA	NA		
5	R	REV	X	NA	NA		
4	R	REV	X	NA	NA		
3	R	REV	X	NA	NA		
2	R	NTC_STAT	X	NA	NA	000:Cold	
1	R		X	NA	NA	001:Cool	
0	R		X	NA	NA	010:Normal 011:Warm 100:Hot 101:PCB OTP 111:NTC Disable	

REG 32H STAT2([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	R	VINOVP/UVLO	0	NA	NA	0: VIN is good 1: VIN is OVP/UVLO	
6	R	TSD	0	NA	NA	0: IC not in thermal shutdown 1: IC in thermal shutdown	
5	R	SAFETY_TIMER_OUT	0	NA	NA	0:No Safety timer out 1:Safety timer out	
4	R	REV	X	NA	NA		
3	R	TOPOFF_ACTIVE	0	NA	NA	0: Top off timer not counting 1: Top off timer counting	
2	R	REV	X	NA	NA		
1	R	REV	X	NA	NA		
0	R	REV	X	NA	NA		

**REG 40H INT0**([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW1C	CHARGING STATUS INT	0	NA	NA	0: not trigger 1: triggered	
6	RW1C	EOC INT	0	NA	NA	0: not trigger 1: triggered	
5	RW1C	PPM_INT	0	NA	NA	0: not trigger 1: triggered	
4	RW1C	PG_INT	0	NA	NA	0: not trigger 1: triggered	
3	RW1C	THERMAL_STAT_INT	0	NA	NA	0: not trigger 1: triggered	
2	RW1C	REV	X	NA	NA		
1	RW1C	VINDPM INT	0	NA	NA	0: not trigger 1: triggered	
0	RW1C	TOP_OFF_TIME R_INT	0	NA	NA	0: not trigger 1: triggered	

**REG 41H INT1**([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW1C	VIN_FAULT INT	0	NA	NA	0: not trigger 1: triggered	
6	RW1C	THERMAL_SD INT	0	NA	NA	0: not trigger 1: triggered	
5	RW1C	BAT_FAULT_INT	0	NA	NA	0: not trigger 1: triggered	
4	RW1C	SAFETY TIMER OUT INT	0	NA	NA	0: not trigger 1: triggered	
3	RW1C	NTC FAULT INT	0	NA	NA	0: not trigger 1: triggered	
2	RW1C	REV	X	NA	NA		
1	RW1C	REV	X	NA	NA		
0	RW1C	REV	X	NA	NA		

REG 42H INT2([BACK TO MAP](#))

Bit	Mode	Bit Name		Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW1C	REV	X	NA	NA		REV	
6	RW1C	REV	X	NA	NA		REV	
5	RW1C	REV	X	NA	NA		REV	
4	RW1C	REV	X	NA	NA		REV	
3	RW1C	REV	X	NA	NA		REV	
2	RW1C	REV	X	NA	NA		REV	
1	RW1C	NTC_STAT_CHANGE_INT		0	NA	NA	0: not trigger 1: triggered	
0	RW1C	WD_FAULT_INT		0	NA	NA	0: not trigger 1: triggered	

REG 43H INT3([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW1C	Q1&Q2_ON_INT	0	NA	NA	0: not trigger 1: triggered	
6	RW1C	Q1&Q2_OFF_INT	0	NA	NA	0: not trigger 1: triggered	
5	RW1C	REV	X	NA	NA		
4	RW1C	REV	X	NA	NA		
3	RW1C	REV	X	NA	NA		
2	RW1C	REV	X	NA	NA		
1	RW1C	REV	X	NA	NA		
0	RW1C	REV	X	NA	NA		

REG 44H INT4([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW1C	REV	X	NA	NA		
6	RW1C	REV	X	NA	NA		
5	RW1C	REV	X	NA	NA		
4	RW1C	REV	X	NA	NA		
3	RW1C	REV	X	NA	NA		
2	RW1C	REV	X	NA	NA		
1	RW1C	REV	X	NA	NA		
0	RW1C	REV	X	NA	NA		

REG 50H MASK0([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	CHARGING STATUS INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
6	RW	EOC INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
5	RW	PPM_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
4	RW	PG_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
3	RW	THERMAL_STAT_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
2	RW	REV	X	NA	NA		
1	RW	VINDPM INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
0	RW	TOP_OFF_TIME R_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	



SOUTHCHIP SOUTHCHIP SEMICONDUCTOR

REG 51H MASK1([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	VIN_FAULT INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
6	RW	THERMAL_SD INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
5	RW	BAT_FAULT_INT _M	0	Y	N	0: not mask for INT pulse 1: mask	
4	RW	SAFETY_TIMER OUT INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
3	RW	NTC_FAULT INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
2	RW	REV	X	NA	NA		
1	RW	REV	X	NA	NA		
0	RW	REV	X	NA	NA		

REG 52H MASK2([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	REV	X	NA	NA		
6	RW	REV	X	NA	NA		
5	RW	REV	X	NA	NA		
4	RW	REV	X	NA	NA		
3	RW	REV	X	NA	NA		
2	RW	REV	X	NA	NA		
1	RW	NTC_STAT_CHANGE_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
0	RW	WD_FAULT_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	

REG 53H MASK3([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	Q1&Q2_ON_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
6	RW	Q1&Q2_OFF_INT_M	0	Y	N	0: not mask for INT pulse 1: mask	
5	RW	REV	X	NA	NA		
4	RW	REV	X	NA	NA		
3	RW	REV	X	NA	NA		
2	RW	REV	X	NA	NA		
1	RW	REV	X	NA	NA		
0	RW	REV	X	NA	NA		

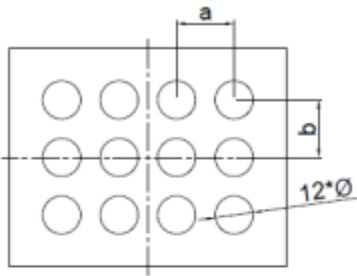
**REG 5AH WD RESET**([BACK TO MAP](#))

Bit	Mode	Bit Name	Default value @POR	Reset by REG_RST	Reset by WTD	Description	Notes
7	RW	REV	X	NA	NA		
6	RW	REV	X	NA	NA		
5	RW	REV	X	NA	NA		
4	RW	REV	X	NA	NA		
3	RW	REV	X	NA	NA		
2	RW	REV	X	NA	NA		
1	RW	REV	X	NA	NA		
0	RW1C	WD_RESET	0	Y	N	0: Normal 1: Reset	Default: Normal(0)

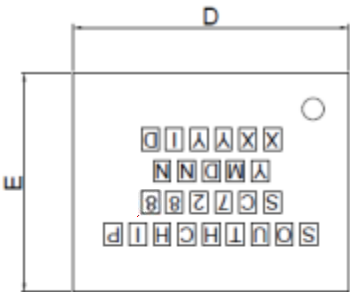
12 MECHANICAL DATA

MECHANICAL DATA

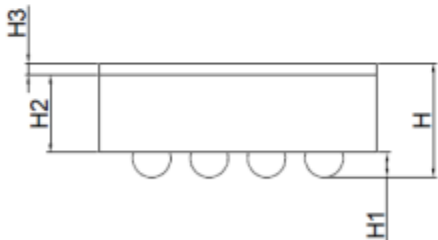
WLCSP -12 (1.55mm X 1.95mm)



BOTTOM VIEW(BALL SIDE)



TOP VIEW(MARKING SIDE)



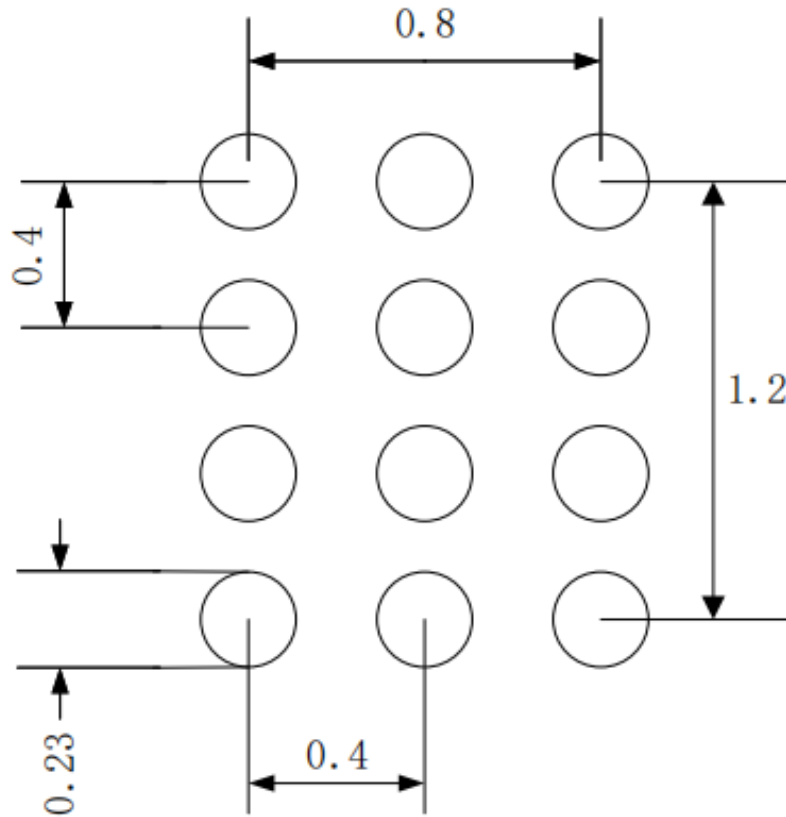
SIDE VIEW



NOTCH DIRECTION

SYMBOL	ITEM	DATA(UM)
D*E	PACKAGE SIZE X*Y	1922.5*1522.5±20
Φ	BALL DIAMETER	265±26
a/b	BALL PITCH X/Y	400/400
N	BALL COUNT	12
H	PACKAGE HEIGHT	575±47
H1	BALL HEIGHT	216±32
H2	SI THICKNESS+PI	319±12
H3	DRY FILM	40±3

RECOMMENDED FOOTPRINT



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