SC3512 Fast Turn-Off Synchronous Rectifier

1 Description

SC3512 is a smart secondary-side synchronous rectifier. It integrates a 60V power MOSFET. SC3512 can replace Schottky diode so the system can achieve higher efficiency.

The SR MOSFET is turned on when the V_{VD} falls below turn-on threshold, and turned off when the V_{VD} exceeds turn-off threshold. The SR conduction voltage drop is continuously monitored to minimize the conduction loss. The extremely fast turn-off comparator and driving circuitry ensures the safety of the system, even in current continuous mode (CCM) condition. This chip supports both high side rectification and low side rectification.

2 Features

- No need of auxiliary winding for power supply
- Patented programmable turn on detection circuitry
- Extremely low quiescent current leads to low stand by power
- Supports DCM, CCM, and Quasi-Resonant mode converters
- Supports both high and low side synchronous rectification
- SOP8 package available

3 Applications

- Universal AC-DC Adaptors
- USB PD and QC Chargers
- Flyback Power Supplies with Variable Output Voltage
- AC-DC auxiliary supplies

4 Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
SC3512SEER	SOP8	6.0mm x 4.9mm x 1.55mm

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5 Typical Application Circuit

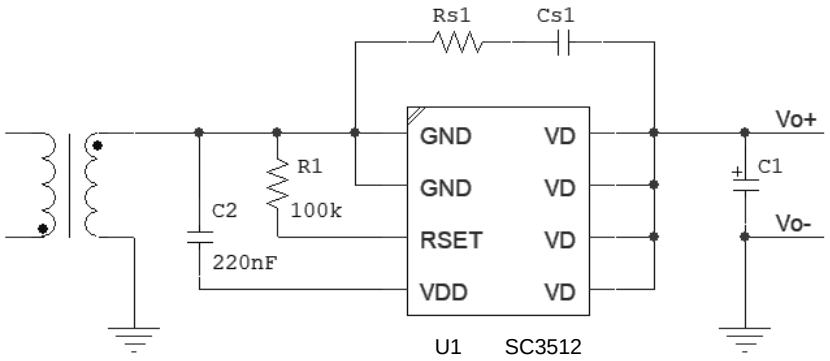

Figure.1 Typical Application circuit (high side)

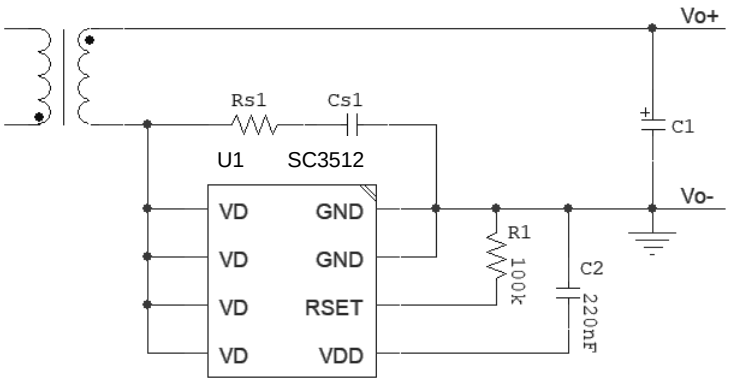

Figure.2 Typical Application circuit (low side)

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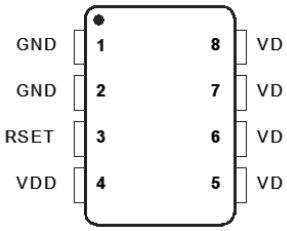
6 Terminal Configuration and Functions

TOP VIEW



TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1、2	GND	PWR	Power MOSFET source. The pin is also used as the ground to VDD and RSET.
3	RSET	I	Auto adaptive turn-on detection
4	VDD	PWR	Power supply of IC
5、6、7、8	VD	PWR	Power MOSFET drain

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

Item	Description	Min.	Typ.	Max.	Unit
Voltage range at terminals (2)	VDD to GND	-0.3	-	+12	V
	VD to GND	-1	-	+60	V
	RSET to GND	-0.3	-	+6.5	V
T_J	Operating Junction temperature range	-40	-	150	°C
T_{stg}	Storage temperature range	-60	-	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

7.2 Thermal Information

THERMAL RESISTANCE (1)		SOP8	UNIT
θ_{JA}	Junction to ambient thermal resistance	90	°C/W
θ_{JC}	Junction to case resistance	45	°C/W

(1) Measured on JESD51-7, 2-layer PCB.

7.3 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
ESD (1)	Human body model (HBM) (1) VDD、RSET、VD	-2	2	kV
	Charged device model (CDM) ESD stress voltage (2) (3)	-1	1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.4 Recommended Operating Conditions

Item	Description	Min.	Typ.	Max.	Unit
VDD to GND	VDD voltage range to GND	-0.3		+12	V
VD to GND	VD voltage range to GND	-0.7		+60	V
C_{VDD}	VDD Capacitor	0.1	0.22	1	uF
R_{RSET}	Resistance of RSET pin connect to GND in RD mode		100		kΩ
	Resistance of RSET pin connect to GND in PT mode	20	24	51	kΩ
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

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7.5 Electrical Characteristics

VDD=7.90V, T_J= -40°C~125°C, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SUPPLY VOLTAGE						
$V_{DD_UVLO_ON}$	Under voltage lockout	Rising edge	4.50	4.75	5.00	V
$V_{DD_UVLO_HYS}$	Under voltage lockout threshold hysteresis	Falling edge		0.25		V
V_{DD_REG}	VDD regulation voltage	VD=12V	7.50	7.90	8.30	V
SUPPLY CURRENT						
I_{VDD}	VDD charging current	VDD =7V, VD=40V	40	70		mA
I_{CC}	Operating current	C_{LOAD} =2.2nF, F_{SW}=100KHz		2.8	3.4	mA
I_{Q_VDD}	RD mode	VDD = V_{DD_REG}		105	135	uA
	PT mode	VDD = V_{DD_REG}		130	170	uA
I_{SD_VDD}	VDD Shutdown current	VDD =UVLO-0.1V		80	110	uA
CONTROL CIRCUITRY						
V_{MON}	Monitor voltage (VSEN)		-55	-40	-25	mV
$V_{DS_TON_TH}$	VDS Turn-on threshold		-150	-110	-70	mV
V_{TNOFF_TH}	Turn-off threshold (VSEN-GND)		-9	-3	3	mV
T_{D_ON}	Turn-on delay	C_{LOAD} =2.2nF		40	70	nS
T_{D_OFF}	Turn-off delay	C_{LOAD} =2.2nF		20	40	nS
T_{DOFF_PRO} (1)	Turn-off propagation delay			10		nS
T_{ON_BLK}	Turn-on blanking time	C_{LOAD} =2.2nF	0.70	0.90	1.20	uS
T_{RSET}	RD mode	R_{RSET} =510KΩ		110		nS
	PT mode	R_{RSET} =51KΩ		1.6		uS
POWER MOSFET						
$V_{(BR)DSS}$ (1)	Drain-source breakdown voltage		60			V
$R_{DS(ON)}$	Drain-source on state resistance	T_J=25℃		12		mΩ
C_{ISS} (1)	Input capacitance	V_{DS}=30V, V_{GS}=0V, Fsw=1MHz		780		pF
C_{OSS} (1)	Output capacitance			375		
C_{RSS} (1)	Reverse transfer capacitance			10		
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD} (1)	Diode Forward Voltage	V_{GS}=0V , I_{SD}=10A , T_J=25℃		0.8	1.2	V
t_{rr} (1)	Reverse Recovery Time	V_{GS}=0V, I_{SD}=10A, T_J=25℃, di/dt=100A/us		20		nS
Q_{rr} (1)	Reverse Recovery Charge			7.9		nC

(1) Guaranteed by characterization and design.

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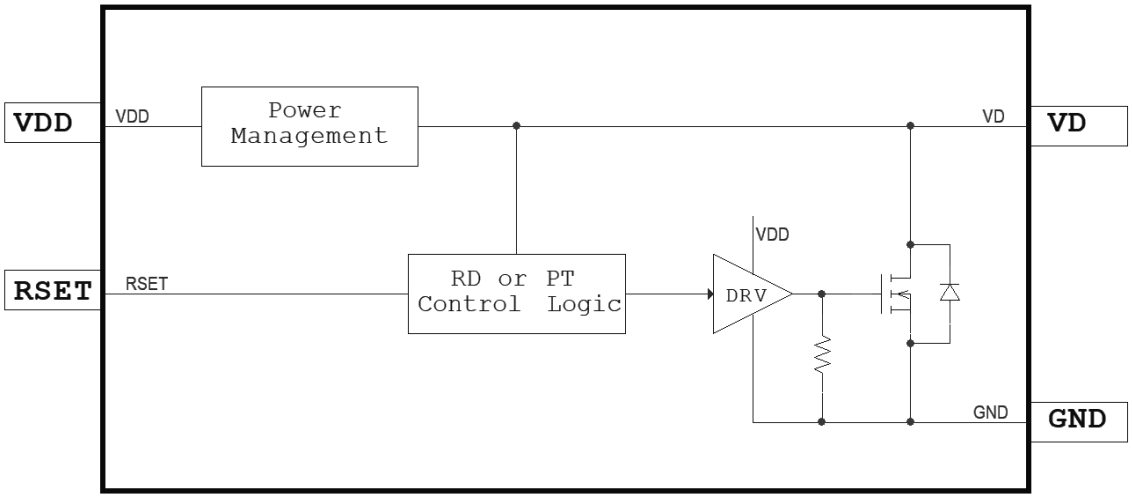
8 Functional Block Diagram



Function Block Diagram

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9 Detailed Description

The SC3512 is designed for flyback converters, which can work in secondary side current discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant (QR) mode.

It integrates a 60V power MOSFET. SC3512 can replace Schottky diode so the system can achieve higher efficiency.

This chip supports both high side rectification and low side rectification.

9.1 VDD Supply

The SC3512 has a special power supply management system to adapt to high-side and low-side SR. Usually a capacitor about 100nF to 1uF is needed to connect between VDD and GND. Larger VDD capacitance leads to longer start up time and larger Vds spike, while smaller one may cause larger ripple on VDD.

The capacitor at VDD affords a stable power supply for IC. GND can be regards as the ground of IC.

The charges VDD via an 70mA current source, and the VDD will be regulate at V_{DD_REG}.

9.2 UVLO

The Under Voltage Lock Out (UVLO) module of SC3512 monitors the voltage on the VDD pin. When VDD voltage is higher than $V_{DD_UVLO_ON}$, all parts of IC start work normally. The hysteresis of UVLO is $V_{DD_UVLO_HYS}$. As soon as the voltage drops below ($V_{DD_UVLO_ON}$-$V_{DD_UVLO_HYS}$), the IC stops all modules and reenters UVLO mode.

9.3 Turn On

When the integrated SR MOSFET body diode conducts, the MOSFET needed turn on to transfer the secondary inductor current from body diode to SR MOSFET. But when the system works in DCM, the V_{VD} resonant voltage after secondary side current drops to zero may lower than 0V, this may lead the SR MOSFET conducts by mistake. For this reason, a circuit which can prevent false turn on is needed. SC3512 offer two modes to avoid this case.

In RD (rising detection) mode, SC3512 integrates a detection circuit. As soon as the V_{VD} is higher than 0V, a built-in rising timer (T_{RISING}) begins to count. When the primary side MOSFET turns off, the V_{VD} will lower than -100mV from the set value, as the falling time ($T_{FALLING}$). An external resistor on RSET pin is needed to adjust the time T_{RSET}. If T_{RISING} is lower than the time T_{RSET} or T_{RISING}-$T_{FALLING}$ is higher than the time T_{CAL}, the SR MOSFET will be turn on after a very short delay time. Otherwise, the SR MOSFET will remain off until next cycle.

In PT (platform time) mode, the circuit that can monitor the VD platform time is used to distinguish the turn on of primary side MOSFET or ringing in DCM/QR mode. If it's a valid primary side MOSFET turn on, the synchronous rectifier will be turn on when the V_{VD} is below -0.1V.

9.4 Minimum On time

When SR turn on, the SR starts to conduct with its maximum current. Because of transformer leakage inductance, MOSFET lead inductance and parasitic capacitance, a large ringing in VD may occurred when SR MOSFET starts turn on. The ring may turn off the SR MOSFET by mistake. The ringing voltage can be reduced through appropriate snubber circuit and low package inductance MOSFET. To further improve the noise immunity, a turn on blanking time T_{ON_BLK} is needed after SR turn on. This function ensures that the SR on state lasts for a certain time.

9.5 Conduction Stage

After SR turn on, the secondary side current transfer from MOSFET body diode to MOSFET, no matter high side or low side SR. The current reaches its maximum level at the beginning, and then it descends at a fixed slope. The V_{VD} can be calculated by the following equation:

$$V_{VD} = -Is * Rds(on)$$

Due to the Rds(on) changes very little in a fixed Vgs, the V_{VD} is a straight line with a fixed slope at the initial conduction stage.

Since the current of secondary side inductor is decreasing, the V_{VD} is increasing in conduction stage. When the V_{VD} rises above -40mV, the gate of SR MOSFET can be pulled down. Lowering VGS will cause the MOSFET to withdraw from the deep saturation region gradually and turn off quickly when it needs to be turned off.

9.6 Turn Off Stage

When the V_{VD} rises above -3mV (typ.), the SR MOSFET will be turn off quickly with 10nS propagation delay.

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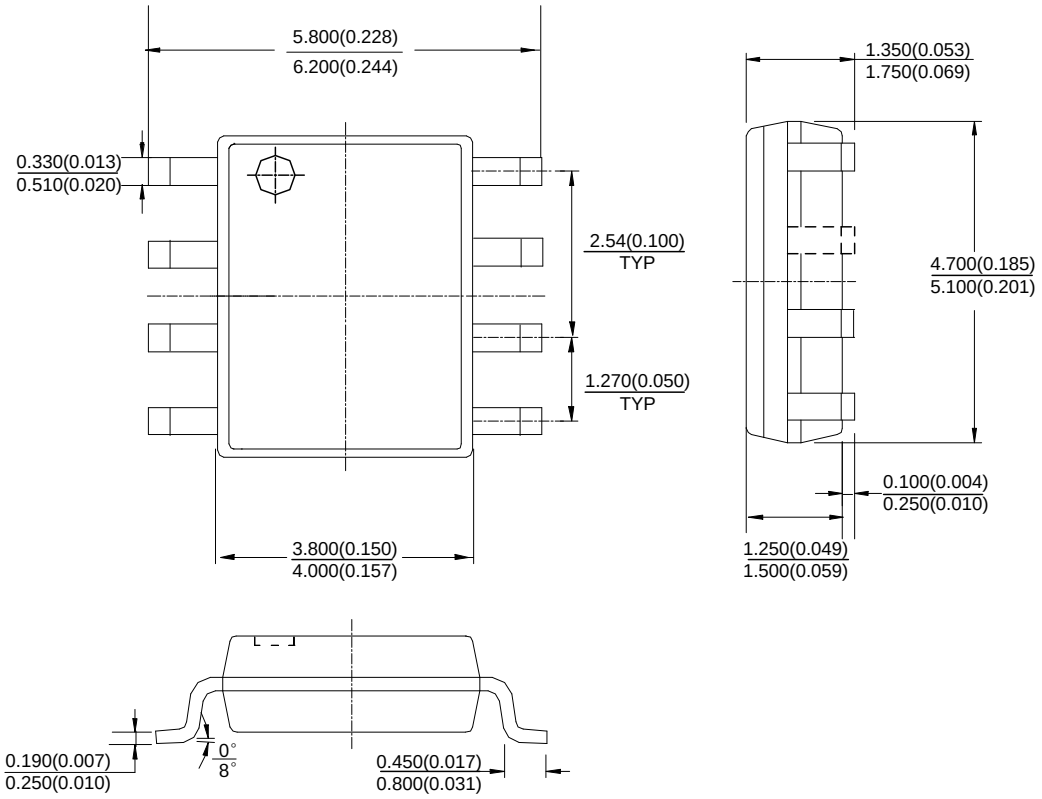
MECHANICAL DATA

SOP8 (6.0mm x 4.9mm x 1.55mm)



Note: Eject hole, oriented hole and mold mark is optional.

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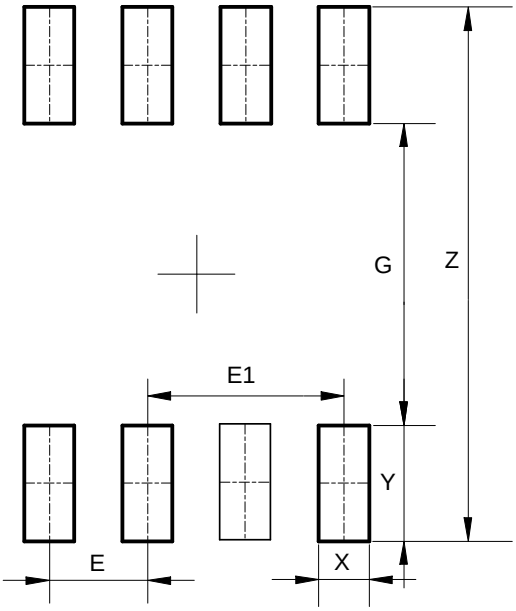
RECOMMENDED FOOTPRINT

Example Board Layout



Dimensions	Z (mm)/(inch)	G (mm)/(inch)	X (mm)/(inch)	Y (mm)/(inch)	E (mm)/(inch)	E1 (mm)/(inch)
Value	6.900/0.272	3.900/0.154	0.600/0.026	1.500/0.059	1.270/0.050	2.540/0.100

NOTES:

A. Publication IPC-7351 is recommended for alternate designs
B. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad

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