

SC77216AQ Dual Channel 16-mΩ Smart High Side Driver with Advanced Protections and Diagnostics

1 Descriptions

The SC77216AQ is a fully-protected dual channel smart high side driver qualified in automotive grade. Full diagnostics and high accuracy current sense of each channel enable intelligent control of the load even in harsh conditions. It integrates two 16mΩ MOSFETs in a compact package size with advanced protections of load current limitation, dynamic thermal swing shutdown, absolute thermal shutdown. Auto-restart or fault latch-off mode in over temperature events can be configured by an external /FaultRST pin. Besides, it features chip junction temperature and supply voltage sense output to monitor the driver status more precisely. A multiplexed pin delivers proportional current sense, chip junction temperature, supply voltage sense signals and fault indications in Normal Operation Mode.

2 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H3A
 - Device CDM ESD Classification Level C4B
- Dual Channel 16mΩ Smart High-Side Switch with Full Diagnostics
 - 16-pins, Auto-restart or Fault Latch-off Mode, Channel Fault Diagnosis, Proportional Load Current, T_j and V_s Sense Output
- Operating Junction Temperature: -40 to 150°C
- Wide Operating Voltage from 4 to 28V with Load Dump Withstand Voltage up to 40V
- Ultra Low Standby Current < 500 nA
- Input Control, 3.3 V and 5 V Logic Compatible
- Multiplexed Analog Signals Sensing Output, including
 - Proportional Load Current of Each Channel
 - Power Supply Voltage
 - Chip Junction Temperature
- High Accuracy Current Sense:

- ±5% @ 5A
- ±5% @ 3A
- ±12% @ 0.1A
- ±20% @ 0.05A
- ±65% @ 0.01A

- Electrical Transient Disturbance Immunity Certification of ISO7637-2 and ISO16750-2
- Advanced Protections:
 - Short to GND Protection by Internal Current Limit
 - Dynamic Thermal Swing Shutdown and Absolute Thermal Shutdown with Auto-restart
 - Configurable Fault Latch-off Mode for Both Thermal Swing Shutdown and Absolute Thermal Shutdown Events
 - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
 - Loss of GND and Loss of Battery Protection
 - Under Voltage Lockout (UVLO) Protection
- Diagnostics:
 - Overload and Short to Ground Detection in Normal Operation Mode
 - Open Load and Short to Battery Detection in OFF-State

3 Applications

- High Side Power Driver for Sub-module
- Power Switch for Automotive Lamp
- High Side Relays and Solenoids
- General Resistive, Inductive and Capacitive Loads

4 Device Information

ORDER NUMBER	DESCRIPTION	PACKAGE	BODY SIZE
SC77216AQSHER	<ul style="list-style-type: none"> Auto-restart or Fault Latch-off Mode Channel Fault Diagnosis Output Proportional Load Current, T_J and V_s Sense Output 	eSSOP-16	5.2mm x 3.9 mm x 1.4mm

5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

Revision	Date	Page(s) changed	Changes Description
1.0	2024.10	New	Initial Release.
1.0.1	2025.09	5-9	8.5 Electrical Characteristics 1. " t_{skew} " Updated (Min./Max.: -150 μ s/50 μ s $\rightarrow$ -100 μ s/100 μ s) 2. " dV/dt_{OFF} " Updated (Max.: -0.6V/ μ s $\rightarrow$ -0.7V/ μ s) 3. " R_{ON} " @150 $^{\circ}$ C Updated (Max.: 38m Ω $\rightarrow$ 30m Ω)
1.0.2	2025.09	5-9	8.5 Electrical Characteristics " t_{Latch_RST} " Updated (Min./Typ./Max.: 3 μ s/10 μ s/20 μ s $\rightarrow$ 60 μ s/80 μ s/90 μ s)
1.0.3	2026.03	All Pages	Update the function descriptions in the datasheet.

6 Typical Application Circuit

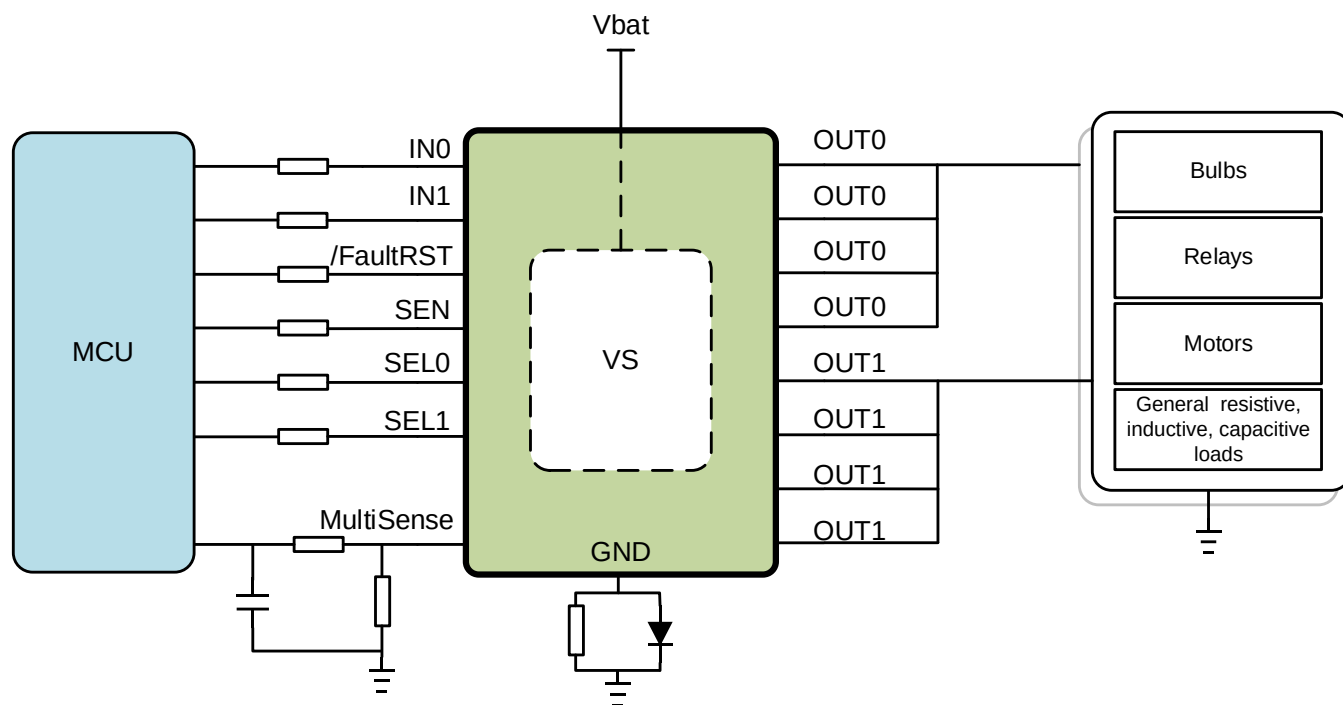


Figure 6-1. Typical Application Circuit

7 Terminal Configuration and Functions

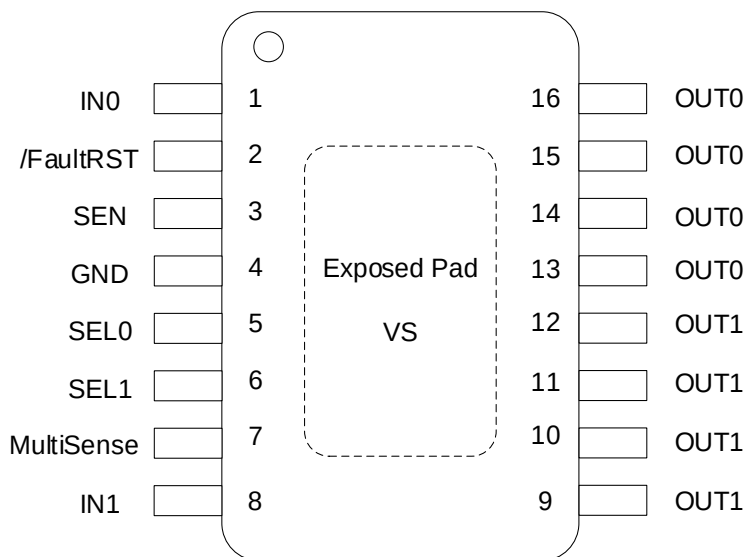


Figure 7-1. Configuration Diagram (Top View)

Table 7-1. Suggested Connections for Unused and Not Connected Pins

TERMINAL		I/O	DESCRIPTION
NUMBER	NAME		
1	IN0	I	Input pin of Channel 0. Active high to turn on CH0.
2	/FaultRST	I	Latch fault if it's set high; clear fault or keep auto-restart if it's set low.
3	SEN	I	Diagnosis enable pin. Active high.
4	GND	-	Ground connection.
5	SEL0	I	SEL bit 0 for diagnosis multiplexer selection.
6	SEL1	I	SEL bit 1 for diagnosis multiplexer selection.
7	MultiSense	O	Multiplexed sense output. It delivers proportional current sense, chip junction temperature, supply voltage sense signals and fault indications.
8	IN1	I	Input pin of Channel 1. Active high to turn on CH1.
9	OUT1	O	Output of Channel 1.
10	OUT1	O	Output of Channel 1.
11	OUT1	O	Output of Channel 1.
12	OUT1	O	Output of Channel 1.
13	OUT0	O	Output of Channel 0.
14	OUT0	O	Output of Channel 0.
15	OUT0	O	Output of Channel 0.
16	OUT0	O	Output of Channel 0.
Exposed Pad	VS	I	Power supply connection.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	UNIT
Voltage range at Terminals ⁽²⁾	Supply Voltage ⁽³⁾	-0.3	40	V
	Reverse Polarity Voltage with External Blocking Diode ⁽⁴⁾	-18		V
	Supply Voltage for Short Circuit Protection ⁽⁷⁾		18	V
	Voltage on INx, SEN, SELx, and /FaultRST Pins	-0.3	7	V
	Voltage on Multisense Pin	-2.7	7	V
Current range at Terminals ⁽²⁾	DC Current on OUTx Pins		Internally limited	A
	Current on GND Pin	-50 -250 ⁽⁵⁾	50	mA
	Current on INx, SEN, SELx, /FaultRST Pins	-20	20	mA
	Current on Multisense Pin	-25	30	mA
f _{IN,MAX}	PWM Frequency on INx Pins		2	kHz
E _{AS}	Inductive Load Switch-off Energy Dissipation, Single Pulse ⁽⁶⁾		25	mJ
T _A	Operating Ambient Temperature Range	-40	125	°C
T _J	Operating Junction Temperature Range	-40	150	°C
T _{STG}	Storage Temperature Range	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Supply voltage to withstand 40V load dump test for 400ms, according to ISO 16750-2:2010 Test B
- (4) Reverse polarity condition: t < 60 s, reverse current < I_{OUT,REV1}, GND pin 4.7-kΩ resistor in parallel with diode.
- (5) For limited time range: t < 120s
- (6) Test condition: V_S = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2- × 70-μm Cu, 2- × 35-μm Cu. 600-mm² thermal pad copper area.

8.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
ESD ⁽¹⁾	Human Body Model (HBM) ESD Stress Voltage ⁽²⁾	All Pins	-4	4	kV
	Charged Device Model (CDM) ESD Stress Voltage ⁽³⁾	All Pins	-750	750	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) Level listed above is the passing level per AEC-Q100-002. The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.
Level listed above is the passing level per AEC-Q100-011.

8.3 Recommended Operating Conditions

PARAMETER	DEFINITION	MIN	TYP	MAX	UNIT
V_S	Voltage on VS pin	5		28	V
V_{IH}	Input Logic High on INx, SEN, SELx, /FaultRST Pins	2.1		5.5	V
V_{IL}	Input Logic Low on INx, SEN, SELx, /FaultRST Pins	0		0.9	V
$I_{OUT,NOM}$	Nominal DC load current		6		A
T_A	Operating ambient temperature	-40		125	°C
T_J	Operating junction temperature	-40		150	°C

8.4 Thermal Information

THERMAL RESISTANCE ⁽¹⁾		eSSOP-16	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance ⁽²⁾	32.2	°C/W
$R_{\theta JC(top)}$	Junction to case(top) thermal resistance	21.9	°C/W
$R_{\theta JC(bottom)}$	Junction to case(bottom) thermal resistance	1.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.4	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

(2) The thermal data is based on JEDEC standard high-K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

8.5 Electrical Characteristics

-40°C < T_J < 150°C and 5V < V_S < 28V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V _{S,NOM}	Nominal Operating Voltage		5	13.5	28	V
V _{S,EXT}	Extended Operating Voltage	R _{ON} and switching characteristics may increase compared to those in V _{S,NOM} , but protection functions are still operative.	4		5	V
V _{S,UVR}	Undervoltage Restart	Rising threshold to exit UVLO	3.5	3.7	4	V
V _{S,UVF}	Undervoltage Shutdown	Falling threshold to enter UVLO	3	3.2	3.5	V
V _{S,UVhys}	Undervoltage Shutdown Hysteresis			0.5		V
OPERATING CURRENT						
I _{S_ON}	Supply Current for No Load, No Diagnosis	V _S = 13.5V, V _{IN0,1} = 5V, V _{FR} = V _{SEN} = V _{SEL0,1} = 0 V, I _{OUT0,1} = 0 A		2	3	mA

I _{GND_ON}	I _q in ON-state with All Channels Active	V _S =13.5V, V _{IN0,1} =V _{SEN} =5V, V _{FR} = V _{SEL0,1} = 0 V, I _{OUT0,1} = 3 A	3			mA
I _{S_STBY}	Supply Current in Standby Mode	V _S =13.5V, V _{IN0,1} = V _{SEN} = V _{FR} = V _{SEL0,1} = V _{OUT0,1} = 0 V, T _J = 25°C	0.5			µA
		V _S = 13.5 V, V _{IN0,1} = V _{SEN} =V _{FR} = V _{SEL0,1} =V _{OUT0,1} =0 V, T _J = 125°C	3			µA
I _{L_OFF}	Output Leakage Current in OFF-state	V _S =13.5V, V _{IN0,1} =V _{SEN} =V _{FR} = V _{SEL0,1} = V _{OUT0,1} = 0 V, T _J = 25°C	0.01	0.5	µA	
		V _s =13.5V, V _{IN0,1} =V _{SEN} =V _{FR} = V _{SEL0,1} = V _{OUT0,1} = 0 V, T _J =125°C	3			µA
t _{D_STBY}	Blanking Time into Standby Mode	V _S =13.5V, V _{SEN} =5V to 0V, V _{IN0,1} = V _{OUT0,1} = V _{FR} = V _{SEL0,1} = 0 V	12.5			ms
POWER STAGE						
R _{ON}	ON-state Resistance	V _S =13.5V, I _{OUT} = 2A, T _J = 25°C	16.5	20	mΩ	
		V _S =13.5V, I _{OUT} = 2A, T _J = 150°C	30			mΩ
I _{LIMH}	Current Limit	V _S = 5~18 V	40	50	60	A
I _{LIML} ⁽¹⁾	Current Limit during Thermal Cycling	V _S = 13 V, T _R < T _J < T _{SD}	20			A
V _{DS,CLP}	Drain to source internal clamp voltage	I _{OUT} = 2 A, L=6mH, T _J = -40°C	38	V		
		I _{OUT} = 2 A, L=6mH, T _J = 25~150°C	42	48	52	V
OUTPUT DIODE CHARACTERISTICS						
V _{OUT,F}	Drain to Source Diode Voltage	V _{IN0,1} =0, I _{OUT,REV} = 3A	0.7			V
I _{OUT,REV} ⁽¹⁾	Continuous Reverse Current when Reverse Polarity	t < 60 s, V _S = 13.5 V, GND pin 4.7kΩ resistor in parallel with diode. T _J = 25°C	4			A
I _{OUT,INV} ⁽¹⁾	Continuous Inverse Current When V _{OUT} > V _S + V _{diode}	t < 60 s, V _S = 13.5 V, T _J = 25°C	3			A
LOGIC INPUT (INx, SEN, SELx, /FaultRST)						
V _{IH}	Input Logic High		2.1			V
V _{IL}	Input Logic Low		0.9			V
V _{I_HYS}	Input Logic Hysteresis		170			mV
I _{IH}	High Level Pull-down Current	V _{IH} =2.1V	10			µA
I _{IL}	Low Level Pull-down Current	V _{IL} =0.9V	1	10	µA	
DIAGNOSTICS						
I _{loss,GND}	Output Leakage Current when Loss of Ground		100			µA
V _{OL,OFF}	Open Load Detection Threshold in OFF-state (Vout-GND)	V _{SEN} = 5V, V _{IN0,1} = 0V, V _{SEL1} = 0V, V _{SEL0} = 0V or 5V	2	3	4	V

$I_{OL,OFF}$	OFF-state Output Sink Current with Open Load	$V_S = 13.5V, V_{SEN} = 5V, V_{IN} = 0V, V_{OUT} = 4V$	-100		μA
$t_{D_OL_IN}$	OFF-state Diagnostic Delay Time from Falling Edge of Input	$V_S = V_{OUT0} = 13.5V, V_{SEN} = 5V, V_{SEL0,1} = 0V, V_{IN0} = 5V \text{ to } 0V$	350	500	700 μs
$t_{D_OL_VO}$	OFF-state Diagnostic Delay Time from Rising Edge of Vout	$V_S = 13.5V, V_{SEN} = 5V, V_{IN0} = V_{SEL0,1} = 0V, V_{OUT} = 0V \text{ to } 4V$		150	250 μs
$t_{D_OL_SEN}$	OFF-state Diagnostic Delay Time from Rising Edge of SEN	$V_S = 13.5V, V_{IN0} = V_{SEL0,1} = 0V, V_{OUT} = 4V, V_{SEN} = 0V \text{ to } 5V$		150	250 μs
$T_{SD}^{(1)}$	Thermal Shutdown Temperature			170	$^{\circ}C$
$T_R^{(1)}$	Thermal Shutdown Flag Reset Temperature			145	$^{\circ}C$
$T_{SW}^{(1)}$	Thermal Swing Shutdown Threshold	$T_J = -40^{\circ}C, V_S = 13.5V$		60	$^{\circ}C$
$T_{HYS}^{(1)}$	Hysteresis for Resetting the Thermal Shutdown and Swing			20	$^{\circ}C$
t_{LATCH_RST}	Deglitch Time for Reset Fault	$V_{SEN}=5V, V_{IN}=5V, V_{SEL0,1}=0V, \text{ Latched fault triggered, then } V_{FR}=5V \text{ to } 0V$	60	80	90 μs
Multiple SENSE Functions					
K_{SNS}	Ratio of Current Sense			3600	
dK_{SNS}/K_{SNS}	Accuracy of Current Sense $(I_{CS} \times K_{SNS} - I_{OUT}) / I_{OUT} \times 100$	$I_{OUT} = 0.01A$	-65	65	%
		$I_{OUT} = 0.05A$	-20	20	
		$I_{OUT} = 0.1A$	-12	12	
		$I_{OUT} = 3A$	-5	5	
		$I_{OUT} = 5A$	-5	5	
V_{SENSE_SAT}	SENSE Saturation Voltage	$V_S = 7V, R_{SENSE} = 2.5k\Omega, V_{SEN} = 5V, V_{IN0} = 5V, V_{SEL0} = 0V, V_{SEL1} = 0V, I_{OUT0} = 9A$	4.8		V
I_{SENSE_SAT}	SENSE Saturation Current	$V_S = 7V, V_{SENSE} = 4V, V_{IN0} = 5V, V_{SEN} = 5V, V_{SEL0} = 0V, V_{SEL1} = 0V, I_{OUT0} = 9A$	4		mA
$V_{CS,H}$	Fault High Voltage of SENSE	$V_S \geq 7V$	5	5.5	6 V
		$5V \leq V_S < 7V$	4.3		6 V
$I_{CS,H}$	Fault Current of SENSE	$V_S \geq 7V, V_{SENSE} = 4.3V$	10		mA
V_{SENSE_TC}	SENSE Output Voltage Proportional to T_J	$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$			
		$V_{SEN} = 5V, V_{SEL0} = 0V, V_{SEL1} = 5V, V_{IN0,1} = 0V, R_{SENSE} = 1k\Omega, T_J = -40^{\circ}C$	2	2.3	2.4 V
		$V_{SEN} = 5V, V_{SEL0} = 0V, V_{SEL1} = 5V, V_{IN0,1} = 0V, R_{SENSE} = 1k\Omega, T_J = 25^{\circ}C$	1.8	1.9	2 V

		$V_{SEN} = 5\text{ V}, V_{SELO} = 0\text{ V}, V_{SEL1} = 5\text{ V},$ $V_{IN0,1} = 0\text{ V}, R_{SENSE} = 1\text{ k}\Omega, T_J = 125^\circ\text{C}$	1.2	1.32	1.5	V
$\frac{dV_{SENSE_TC}}{dT}$	Temperature Coefficient	$T_J = -40^\circ\text{C to } 150^\circ\text{C}$	-6.0			mV/°C
V_{SENSE_VS}	SENSE Output Voltage Proportional to V_S	$V_{SENSE_VS} = V_S / 4$ $V_S = 13\text{ V}, V_{SEN} = 5\text{ V}, V_{SELO} = 5\text{ V},$ $V_{SEL1} = 5\text{ V}, V_{IN0,1} = 0\text{ V}, R_{SENSE} = 1\text{ k}\Omega$	3.17	3.23	3.32	V
I_{SNS_LEAK1}	Leakage Current of SENSE in Diagnostic Disable State	$V_{SEN}=0\text{V}, V_{IN}=5\text{V}, I_{OUT}=3\text{A},$ $V_{SENSE}=0\text{V}, T_J=125^\circ\text{C}$	0.5			μA
I_{SNS_LEAK2}	Leakage Current of SENSE in Diagnostic Enable State	$V_{SEN}=5\text{V}, V_{IN}=5\text{V}, I_{OUT}=0\text{A},$ $V_{SENSE}=0\text{V}, T_J=125^\circ\text{C}$	6			μA
t_{SNS_ON1}	Current SENSE Settling Time from SEN Rising Edge	$V_{IN} = 5\text{ V}, I_{OUT} \geq 1\text{ A}. V_{SEN}$ from 0 to 5 V. V_{SENSE} to 90% of sense value, $R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{SNS_OFF1}	Current SENSE Settling Time from SEN Falling Edge	$V_{IN} = 5\text{ V}, I_{OUT} \geq 1\text{ A}. V_{SEN}$ from 5 to 0 V. V_{SENSE} to 10% of sense value, $R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{SNS_ON2}	Current SENSE Settling Time from IN Current Rising Edge	$V_{SEN}=5\text{V}, I_{OUT} \geq 1\text{ A}. V_{IN}$ from 0 to 5 V. V_{SENSE} to 90% of sense value, $R_{SENSE} = 1\text{ k}\Omega$	150			μs
t_{SNS_OFF2}	Current SENSE Settling Time from IN Falling Edge	$V_{SEN} = 5\text{ V}, I_{OUT} \geq 1\text{ A}. V_{IN}$ from 5 to 0 V. V_{SENSE} to 10% of sense value, $R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{SNS_ON3}	V_{SENSE_TC} Settling Time from Rising Edge of SEN	$V_{SEN} = 0\text{ V to } 5\text{ V}, V_{SELO} = 0\text{ V}, V_{SEL1} = 5\text{ V}, R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{SNS_OFF3}	V_{SENSE_TC} Disable Delay Time from Falling Edge of SEN	$V_{SEN} = 5\text{ V to } 0\text{ V}, V_{SELO} = 0\text{ V}, V_{SEL1} = 5\text{ V}, R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{SNS_ON4}	V_{SENSE_VS} Settling Time from Rising Edge of SEN	$V_{SEN} = 0\text{ V to } 5\text{ V}, V_{SELO} = 5\text{ V}, V_{SEL1} = 5\text{ V}, R_{SENSE} = 1\text{ k}\Omega$	60			μs
t_{SNS_OFF4}	V_{SENSE_VS} Disable Delay Time from Falling Edge of SEN	$V_{SEN} = 5\text{ V to } 0\text{ V}, V_{SELO} = 5\text{ V}, V_{SEL1} = 5\text{ V}, R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{D_XtoY}	Current SENSE Transition Delay from CHx to CHy	$V_S=13.5\text{V}, V_{IN0} = 5\text{ V}, V_{IN1} = 5\text{ V},$ $V_{SEN}= 5\text{ V}, V_{SEL1} = 0\text{ V}, V_{SELO} = 0\text{ V}$ to 5 V, $I_{OUT0} = 0\text{ A}, I_{OUT1} = 3\text{ A}, R_{SENSE} = 1\text{ k}\Omega$	20			μs
$t_{D_CS,H}$	SENSE Transition Delay from Stable Current Sense on CHx to $V_{SENSE,H}$ on CHy	$V_S=13.5\text{V}, V_{IN0} = 5\text{ V}, V_{IN1} = 0\text{ V},$ $V_{SEN} = 5\text{ V}, V_{SEL1} = 0\text{ V}, V_{SELO} = 0\text{ V}$ to 5 V, $I_{OUT0} = 3\text{ A}, I_{OUT1} = 13.5\text{ V},$ $R_{SENSE} = 1\text{ k}\Omega$	20			μs
t_{D_CS0TC}	SENSE Transition Delay from Stable Current Sense to TC sense	$V_S=13.5\text{V}, V_{IN0} = 5\text{ V}, V_{SEN} = 5\text{ V},$ $V_{SELO} = 0\text{ V}, V_{SEL1} = 0\text{ V to } 5\text{ V}, I_{OUT0} = 1.5\text{ A}, R_{SENSE} = 1\text{ k}\Omega$	60			μs

t _{D_TCIoCS}	SENSE Transition Delay from TC sense to Stable Current Sense	V _S =13.5V, V _{IN0} = 5 V, V _{SEN} = 5 V, V _{SEL0} = 0 V, V _{SEL1} = 5V to 0V, I _{OUT0} = 1.5 A, R _{SENSE} = 1 kΩ	20			μs
t _{D_CStoVS}	SENSE Transition Delay from Stable Current Sense to Vs sense	V _S =13.5V, V _{IN1} = 5 V, V _{SEN} = 5 V, V _{SEL0} = 5 V, V _{SEL1} = 0 V to 5 V, I _{OUT1} = 1.5 A, R _{SENSE} = 1 kΩ	60			μs
t _{D_VStoCS}	SENSE Transition Delay from Vs sense to Stable Current Sense	V _S =13.5V, V _{IN1} = 5 V, V _{SEN} = 5 V, V _{SEL0} = 5 V, V _{SEL1} = 5 V to 0 V, I _{OUT1} = 1.5 A, R _{SENSE} = 1 kΩ	20			μs
t _{D_TCIoVS}	SENSE Transition Delay from TC sense to Vs sense	V _S =13.5V, T _J = 125°C, V _{SEN} = 5 V, V _{SEL1} = 5V, V _{SEL0} = 0 V to 5 V, R _{SENSE} = 1 kΩ	20			μs
t _{D_VStoTC}	SENSE Transition Delay from Vs sense to TC sense	V _S =13.5V, T _J = 125°C, V _{SEN} = 5 V, V _{SEL1} = 5V, V _{SEL0} = 5 V to 0 V, R _{SENSE} = 1 kΩ	20			μs
Switching Characteristics						
t _{D_ON}	Turn-on Delay Time	V _{IN} rising edge to V _{OUT} = 20% *V _S , V _S =13.5V, R _L =4.3Ω, T _J = 25°C	35	65	95	μs
t _{D_OFF}	Turn-off Delay Time	V _{IN} falling edge to V _{OUT} = 80% *V _S , V _S =13.5V, R _L =4.3Ω, T _J = 25°C	20	70	150	μs
dV/dt _{ON}	Turn-on Slew Rate	V _{OUT} from 20% to 80%, T _J = 25°C	0.3	0.45	0.6	V/μs
dV/dt _{OFF}	Turn-off Slew Rate	V _{OUT} from 80% to 20%, T _J = 25°C	0.3	0.45	0.7	V/μs
t _{skew}	Pulse Skew t _{D_ON} - t _{D_OFF}	V _S =13.5V, R _L =4.3Ω, T _J = 25°C	-100 100			μs

(1) Parameter guaranteed by design and characterization; not subject to production test.

8.6 Typical Characteristics

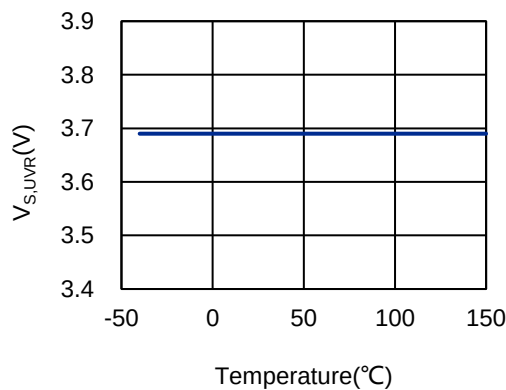


Figure 8-1. $V_{S,UVR}$ vs T_A

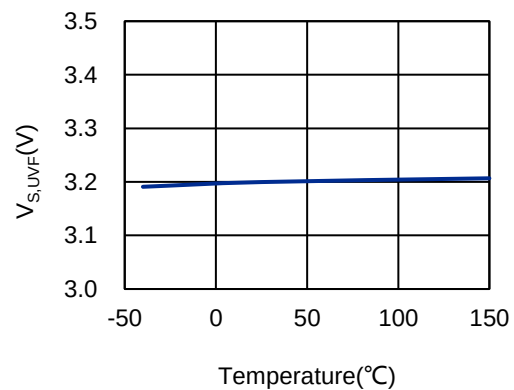


Figure 8-2. $V_{S,UVF}$ vs T_A

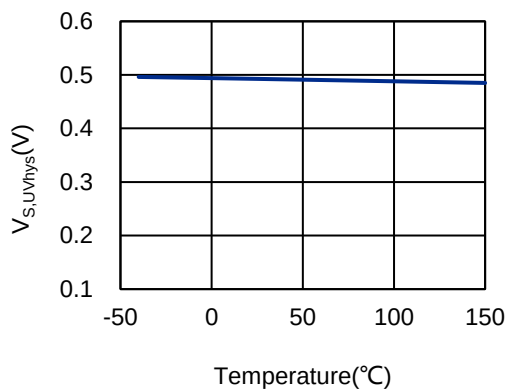


Figure 8-3. $V_{S,UVhys}$ vs T_A

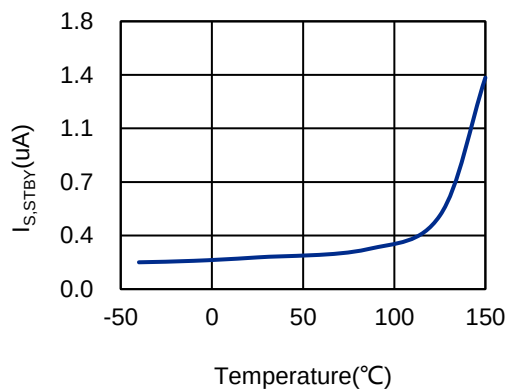


Figure 8-4. $I_{S,STBY}$ vs T_A

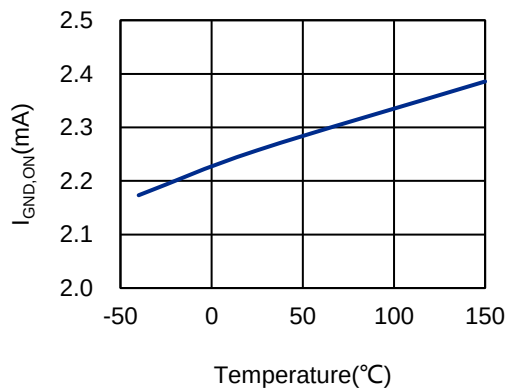


Figure 8-5. $I_{GND,ON}$ vs T_A

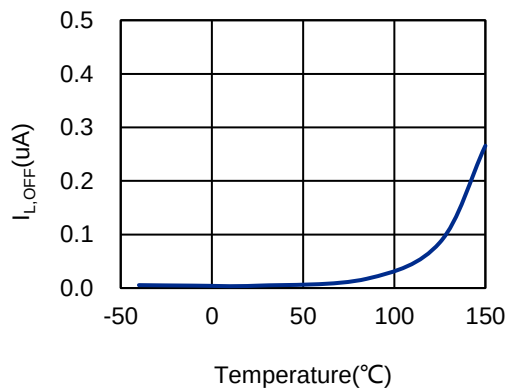


Figure 8-6. $I_{L,OFF}$ vs T_A

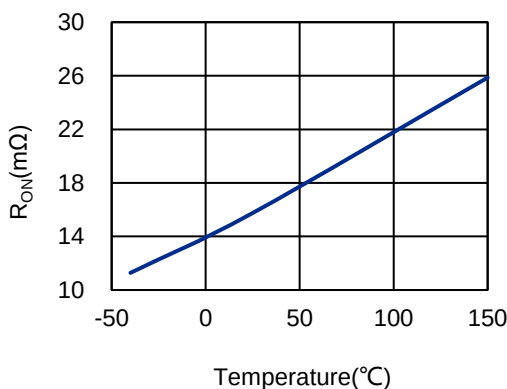


Figure 8-7. R_{ON} vs T_A

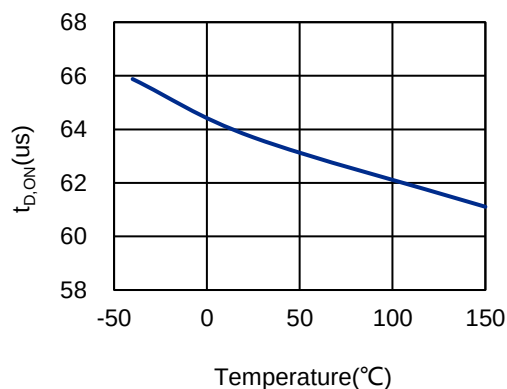


Figure 8-8. $t_{D,ON}$ vs T_A

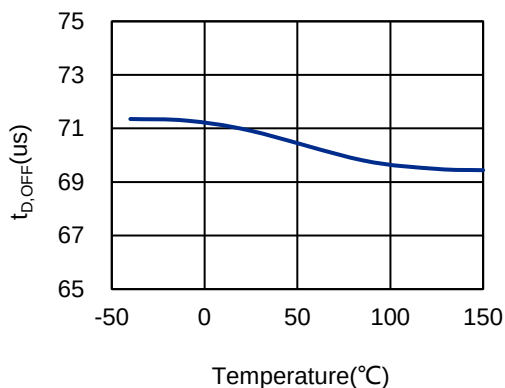


Figure 8-9. $t_{D,OFF}$ vs T_A

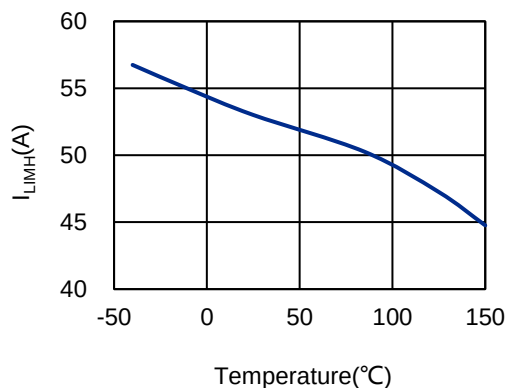


Figure 8-10. I_{LIMH} vs T_A

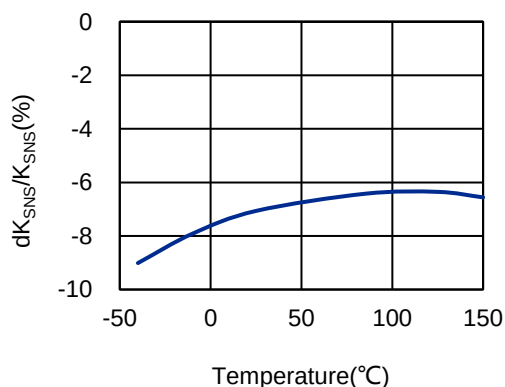


Figure 8-11. dK_{sns} / K_{sns} vs T_A ($I_{OUT} = 0.01A$)

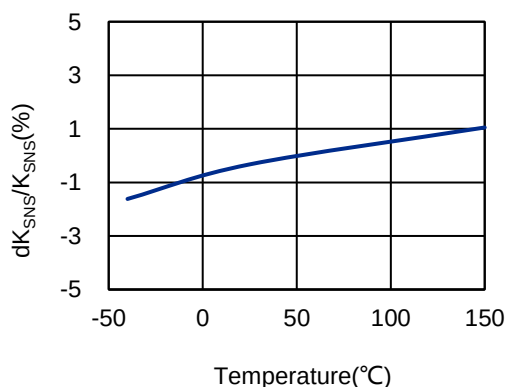


Figure 8-12. dK_{sns} / K_{sns} vs T_A ($I_{OUT} = 5A$)

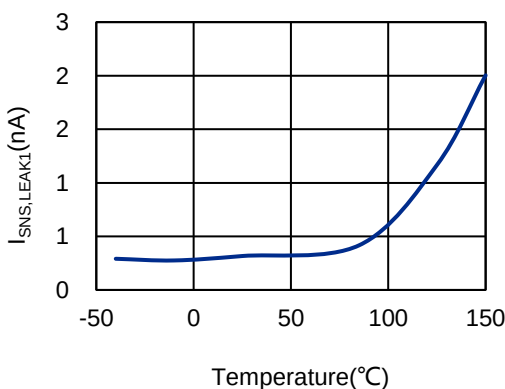


Figure 8-13. $I_{SNS,LEAK1}$ vs T_A

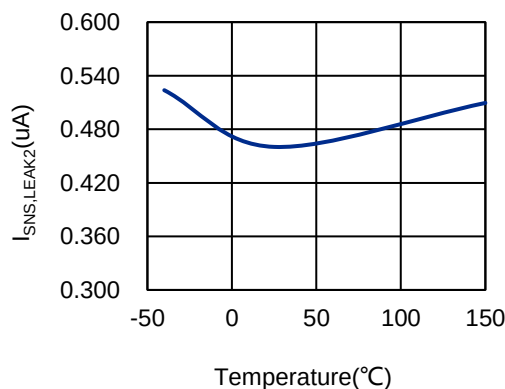


Figure 8-14. $I_{SNS,LEAK2}$ vs T_A

9 Functional Block Diagram

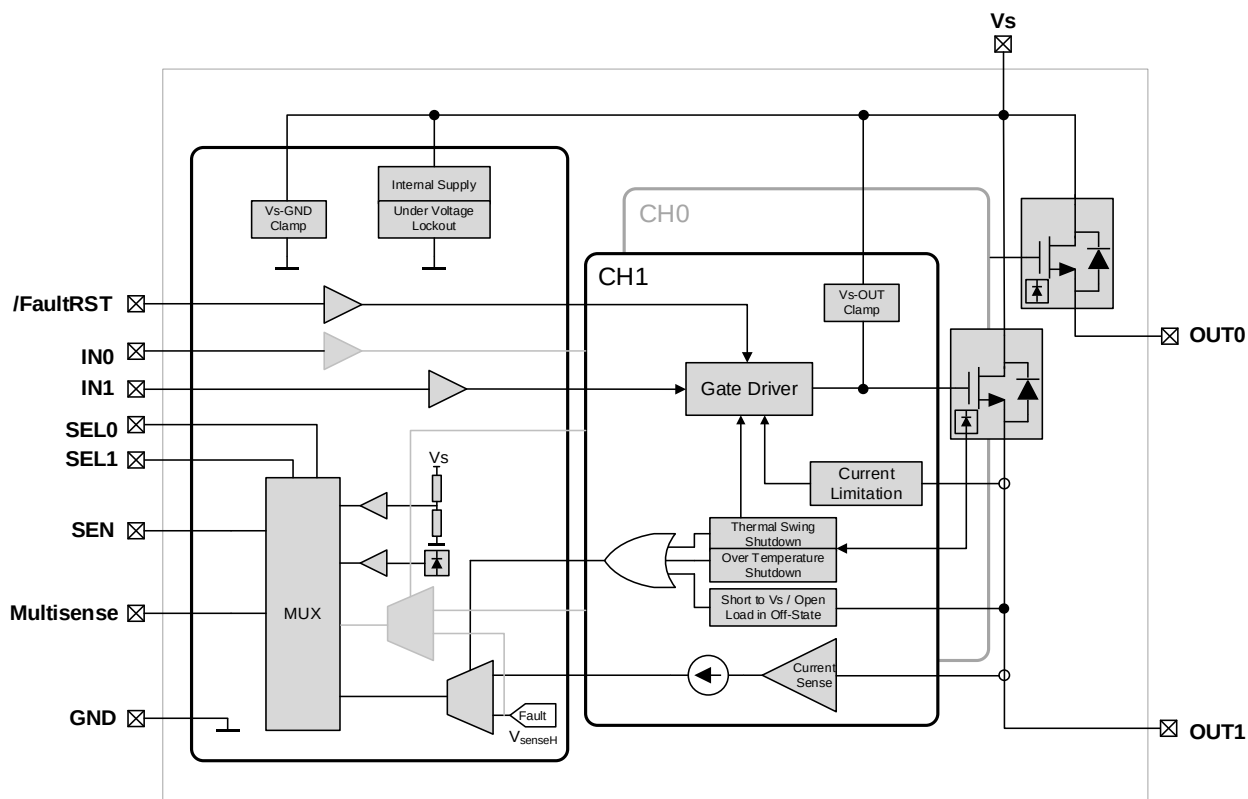


Figure 9-1. Functional Block Diagram

10 Feature Description

10.1 Operating States Diagram

The device has two operating states called 'Normal Operation Mode' and 'Standby Mode', which are decided by input logic signal status and deglitch time, shown as below.

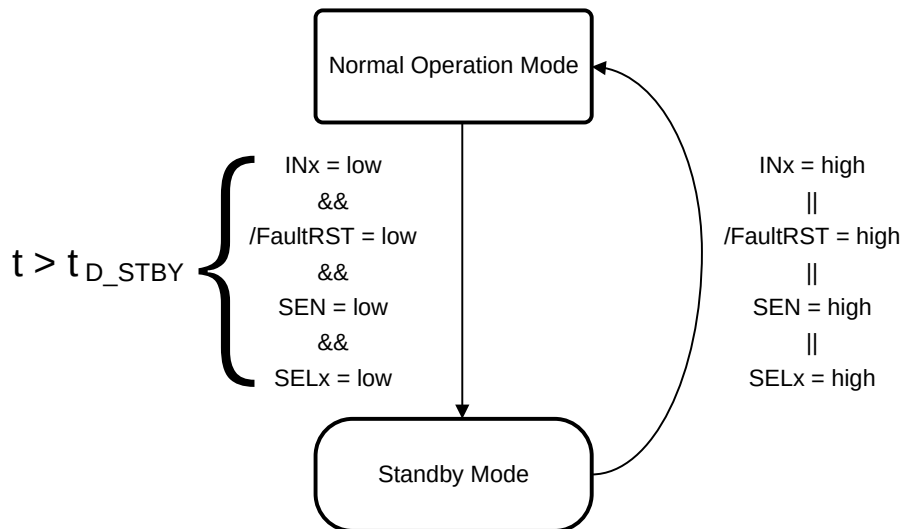


Figure 10-1. Operating States Diagram

10.2 Power Stages

10.2.1 Switching Resistive Loads

When switching resistive loads, the switching time and slew rates are shown in Figure 10-2.

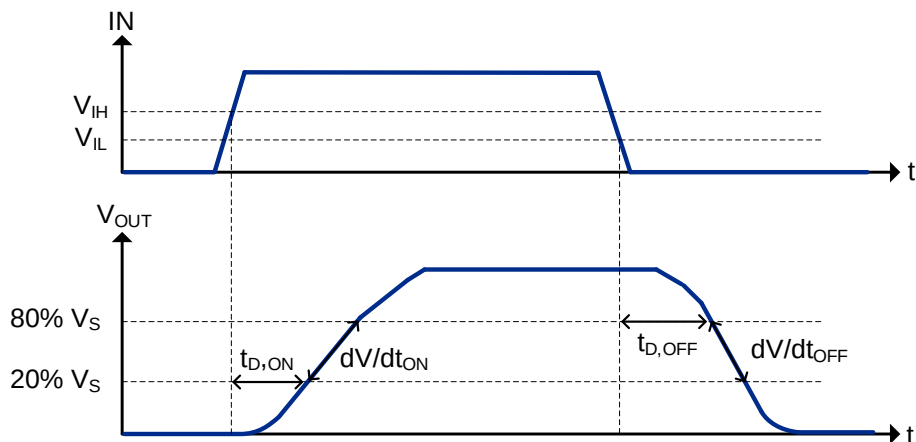


Figure 10-2. Switching Resistive Loads

10.2.2 Switching Inductive Loads

When turning OFF inductive loads with high-side driver, the output voltage V_{OUT} drops to a negative potential, because the inductance tends to maintain the current flow. To prevent the device from damage due to overvoltage, a voltage clamp mechanism is implemented. The clamping mechanism limits the negative output voltage to a safe value. Figure 10-3 shows a concept drawing of implementation.

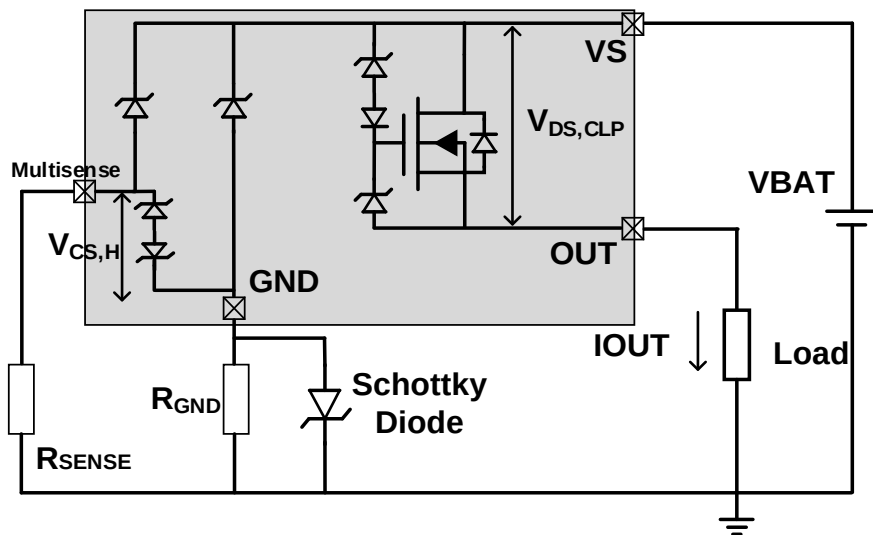


Figure 10-3. Output Clamp Diagram

10.3 MultiSense timings

10.3.1 Current sense mode

MultiSense timings of Current sense mode are shown in Figure 10-4.

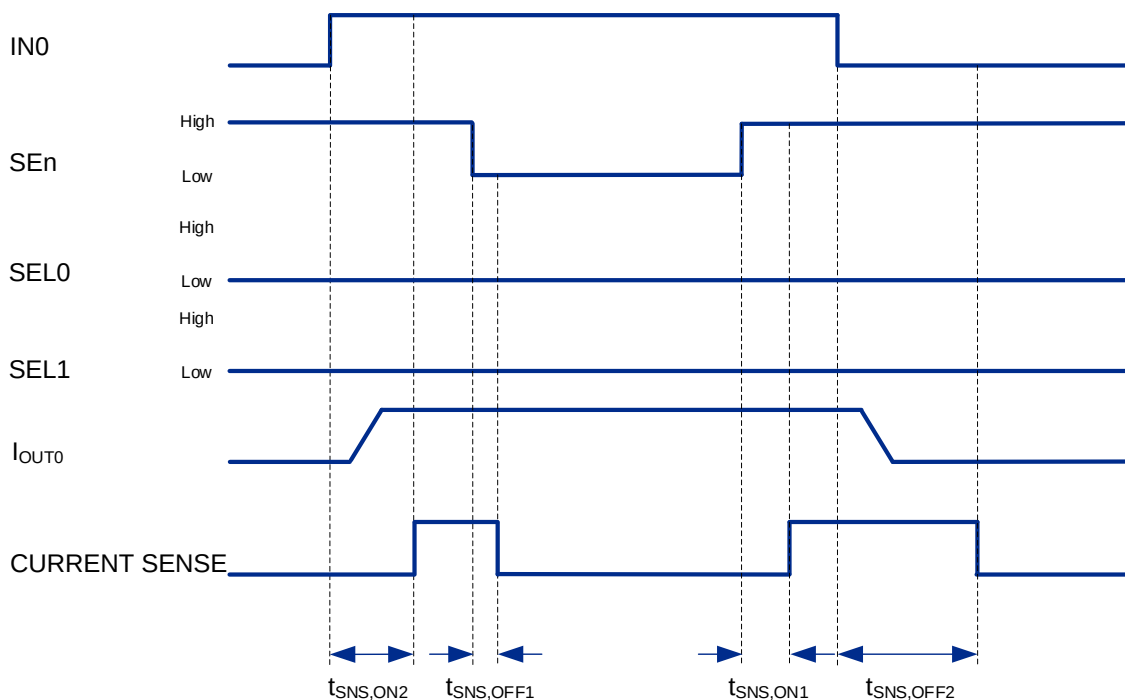


Figure 10-4. MultiSense Timings of Current Sense Mode

10.3.2 Chip temperature and Vs sense mode

MultiSense timings of Chip temperature and Vs sense mode are shown in Figure 10-5

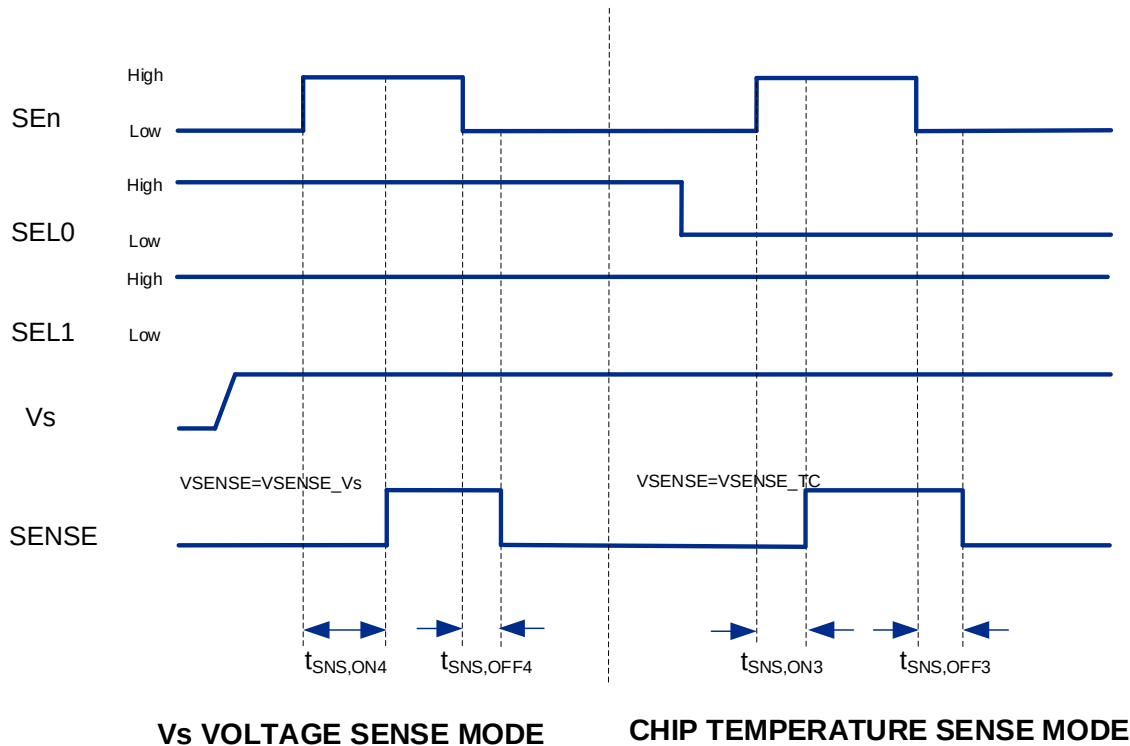


Figure 10-5. MultiSense Timings of Chip Temperature and Vs Sense Mode

10.4 Protections

10.4.1 Overload Protection

The device features protection against overload and short circuit to ground. Its overload threshold decreases as junction temperature rises: at high temperatures, the overload threshold is reduced to prevent device damage. When the supply voltage V_S exceeds 20V-24V, the overload detection current decreases to I_{LIML} as shown in Figure 10-6.

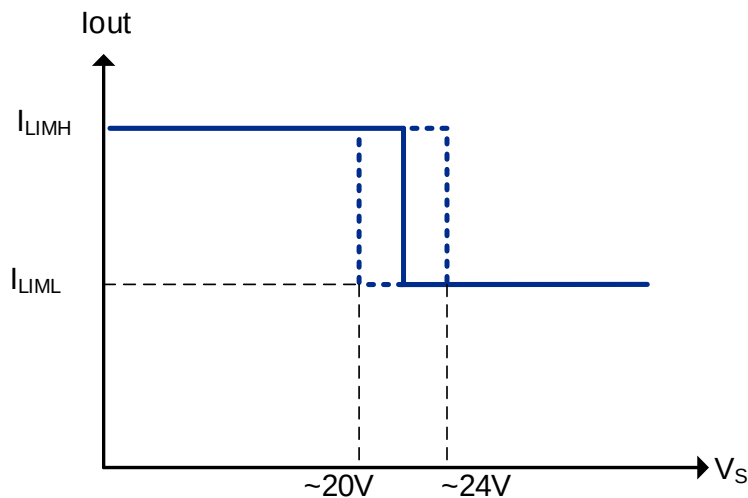


Figure 10-6. The Overload Detection Current Decrease to I_{LIML}

Once the load current meets or exceeds the applicable overload threshold, the output channel is switched off. The channel is allowed to restart, according to the Auto-retry strategy is shown in Figure 10-7.

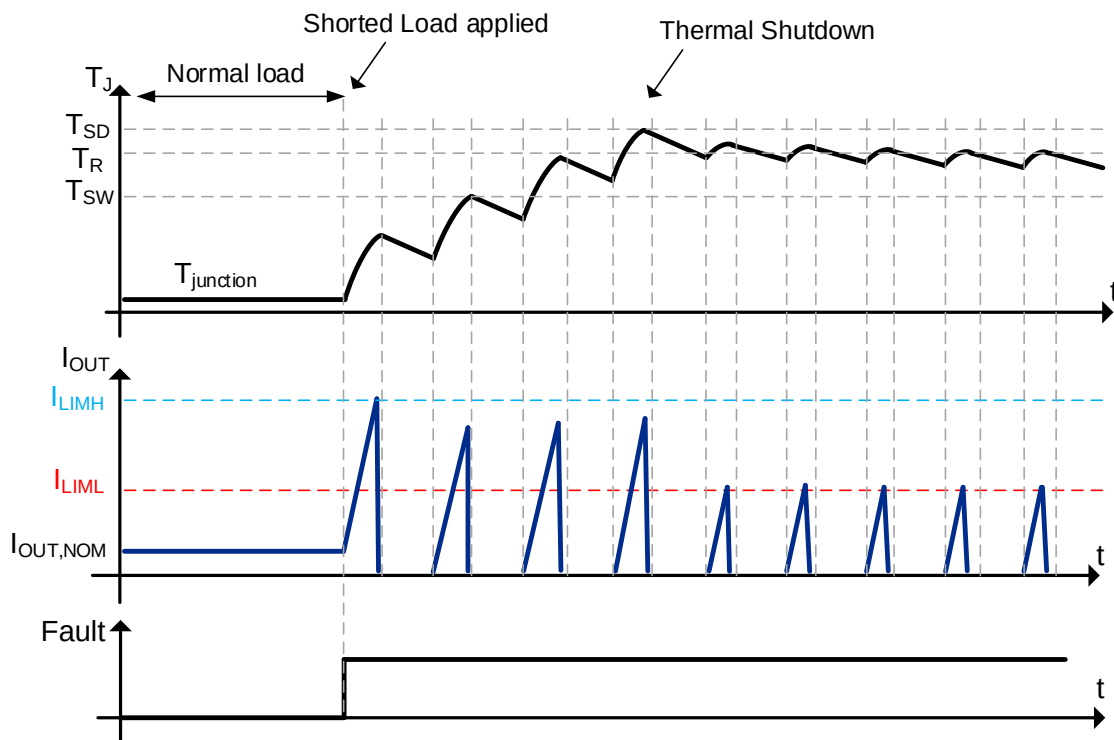


Figure 10-7. Auto-retry Strategy

10.4.2 Undervoltage Protection

Undervoltage protection monitors the supply voltage (V_S). If V_S drops below the minimum undervoltage threshold ($V_{S,UVF}$), the output is turned off regardless of the input status. As soon as V_S is above the operative threshold ($V_{S,UVR}$), the channel is switched ON again as shown in Figure 10-8.

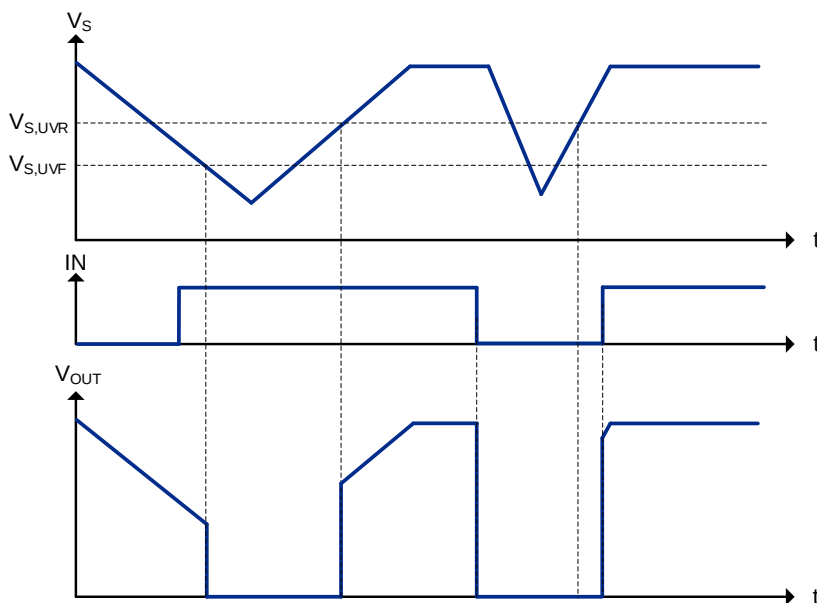


Figure 10-8. Vs Undervoltage Protection

10.4.3 Loss of Ground Protection

In the event of Loss of Ground, the device automatically switches off the power MOSFET, ensuring no current flows into the load. It is recommended to connect a resistor between any logic pins and the microcontroller to ensure the channel switches OFF.

Note: In case any logic pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.

10.4.4 Thermal Swing Shutdown

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing T_{SW} through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level. According to the voltage level on the /FaultRST pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled (/FaultRST = Low) or remains off (/FaultRST = High). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

10.4.5 Thermal Shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 170°C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the /FaultRST pin, the device switches on again as soon as its junction temperature drops to T_R (/FaultRST = Low) or remains off (/FaultRST = High).

10.5 Multiplexed Output of Multisense Pin

- Normal output: current sense of CH0, current sense of CH1, chip junction temperature T_J , V_S power supply.
- Fault indication: over load, short to ground, TSW/TSD, open load or short to V_S in OFF-state.

Table 10-1. Multiplexed Output.

Condition			MUX Channel	Multisense Output			
SEN	SEL1	SEL0		Normal Mode	Over Load	Off-State Diagnostic	Negative Output
L	X	X	/	Hi-Z			
H	L	L	Channel 0 Diagnostic	$I_{CS} = I_{OUT0} / K$	$V_{CS,H}$	$V_{CS,H}$	Hi-Z
H	L	H	Channel 1 Diagnostic	$I_{CS} = I_{OUT1} / K$	$V_{CS,H}$	$V_{CS,H}$	Hi-Z
H	H	L	Chip Junction Temperature	$V_{SENSE_TC}(T) = V_{SENSE_TC}(T_0) + dV_{SENSE_TC} / dT * (T - T_0)$			
H	H	H	Vs power supply	$V_{SENSE_VS} = V_S / 4$			

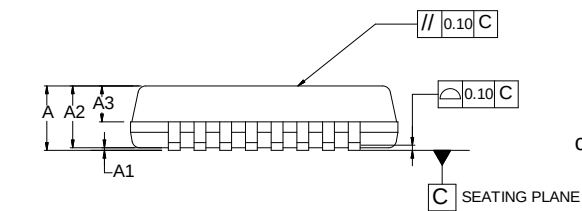
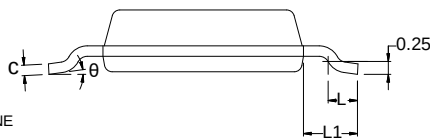
10.6 Truth Table of Protections and Diagnostics

Table 10-2. Truth Table of Protections and Diagnostics.

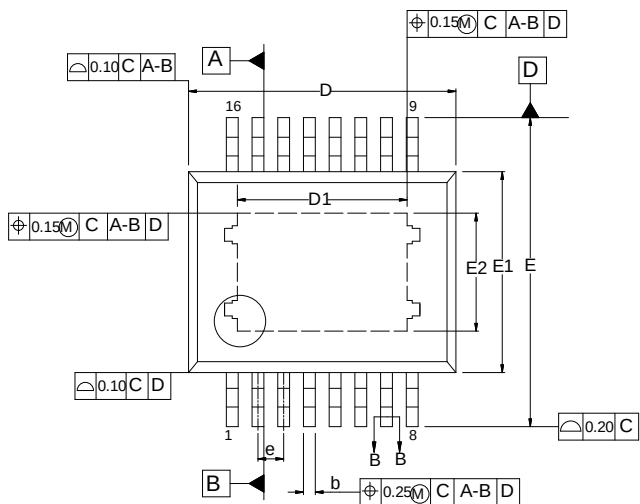
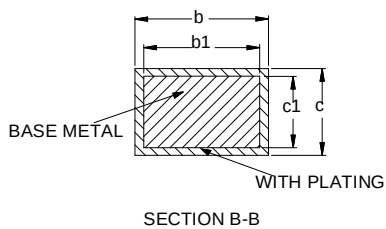
Mode	Conditions	INx	/FaultRST	SEN	SELx	OUTx	MultiSense	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	Low I_{S_STBY} consumption
Normal	Nominal load current: $T_J < 150\text{ }^{\circ}\text{C}$	L	X	Referring to Table 10-2		L	Referring to Table 10-2	/
		H	L			H		Configured in auto-restart mode
		H	H			H		Configured in latch-off mode
Over Load	Over load current: $T_J > T_{SD}$ or $\Delta T_J > T_{SW}$	L	X	Referring to Table 10-2		L	Referring to Table 10-2	/
		H	L			H		Output restarts with temperature protection hysteresis
		H	H			L		Output latches off
Undervoltage	$V_S < V_{S,UVF}$	X	X	X	X	L	Hi-Z	Restart when $V_S > V_{S,UVR}$
Off-state Diagnostic	Short to V_S	L	X	Referring to Table 10-2		H	Referring to Table 10-2	/
	Open Load	L	X			H		External pull-up required
Negative Output Voltage	Inductive loads turn off	L	X	Referring to Table 10-2		$< 0\text{ V}$	Referring to Table 10-2	/

MECHANICAL DATA

eSSOP-16



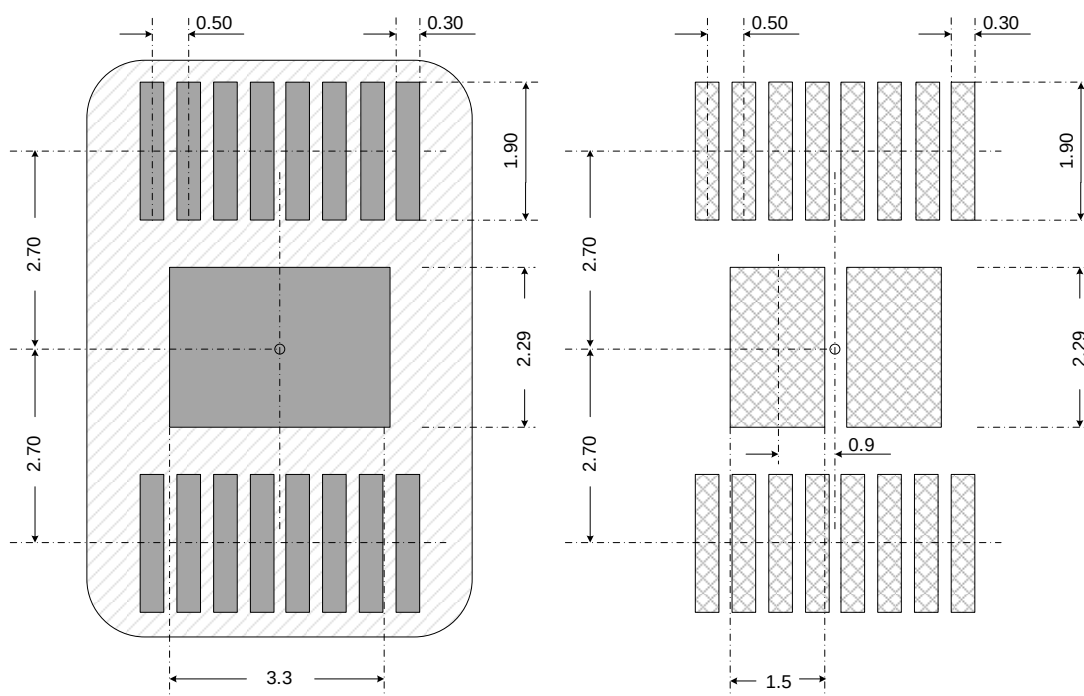
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.40
A1	0.00	—	0.10
A2	1.10	1.20	1.30
A3	0.65	0.70	0.75
b	0.21	—	0.29
b1	0.20	0.23	0.26
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	5.10	5.20	5.30
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.50BSC		
L	0.40	0.57	0.80
L1	1.05REF		
θ	0	—	8°



Size (mm)	E2	D1
U/F Size (mil)		
98*138	2.29±0.30	3.30±0.30

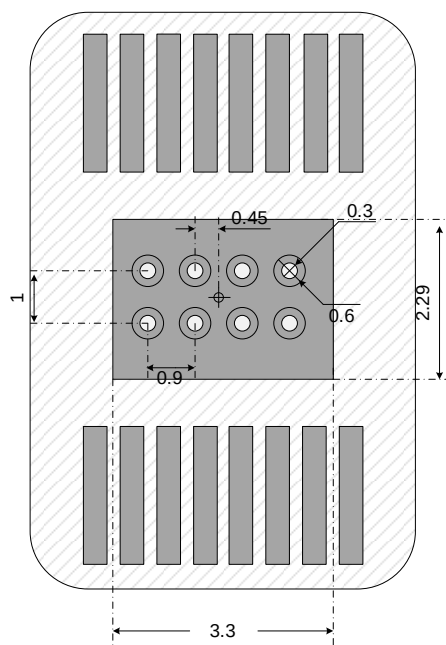
RECOMMENDED FOOTPRINT

eSSOP-16



ALL DIMENSIONS ARE IN UNITS MM

Copper Solder mask Stencil apertures



ALL DIMENSIONS ARE IN UNITS MM

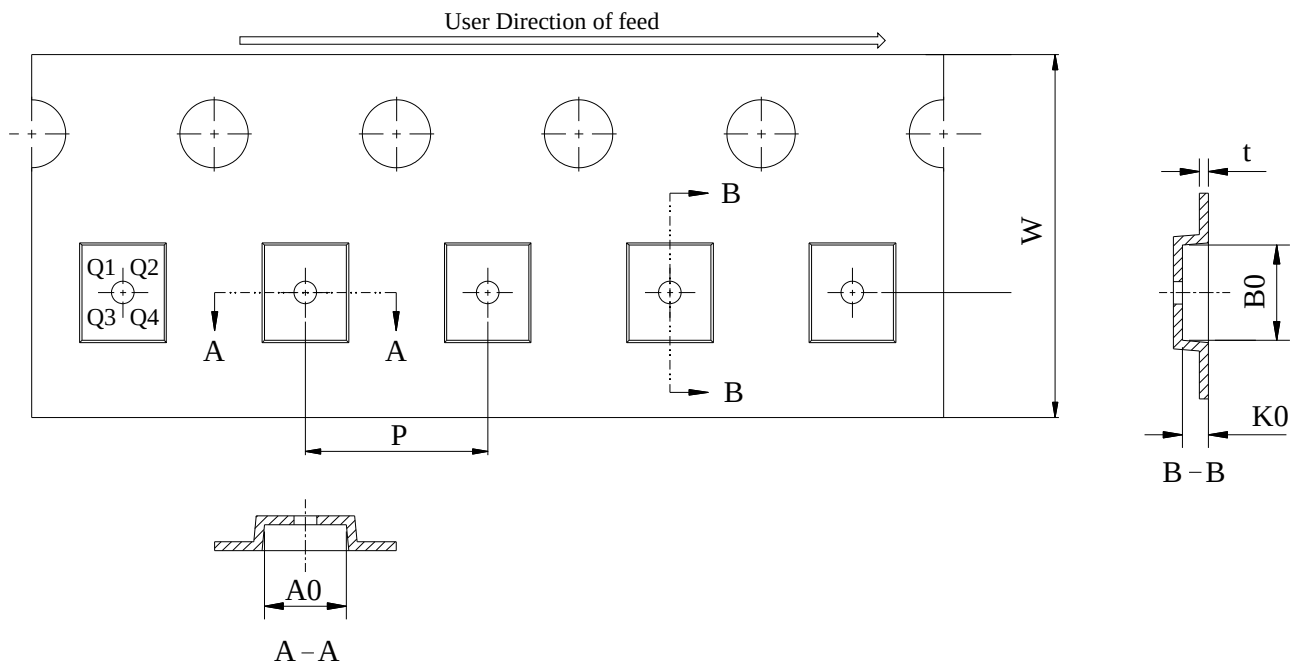
 Copper

 Solder mask

NOTE: Via diameters and positions shall be set according to the actual PCB situation

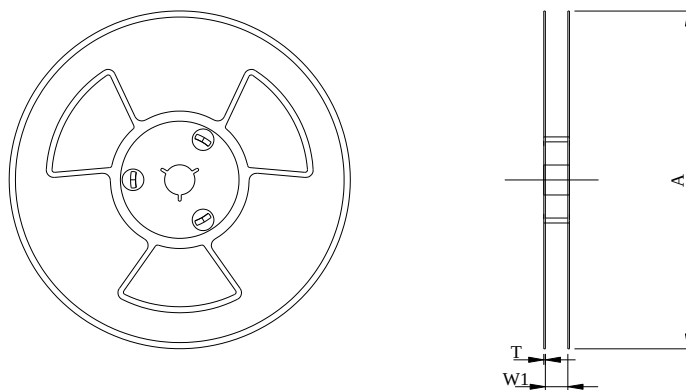
TAPE AND REEL INFORMATION

Carrier Tape



Item	W	P	A0	B0	K0	t	Pin1 Quadrant
Size (mm)	12.00+0.30/-0.1	8.00±0.10	6.50±0.10	5.50±0.10	1.75±0.10	0.30±0.05	Q1

REEL



Item	A	W1	T
Size (mm)	330±1	12.4 +1/-0	2.1±0.3

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