High Efficiency, Synchronous Buck Charger for 1-2 cell Li-ion Battery

1 DESCRIPTION

The SC8932A is a highly integrated switch-mode buck charger for 1-2 cell Li-ion battery applications. It supports up to 13.5V input, up to 3A charging current and provides battery charge management functions including trickle charge, constant current charge, constant voltage charge, charge termination and charging status indication.

The SC8932A supports flexible charge current option, and the user can program the current freely through external resistor for different applications. With the charger management function, the IC can be used to charge 1-2 cell Li-ion battery. SC8932A charges batteries with high efficiency, 5V to 3.5V@2A 95.5%, 9V to 7V@2A 97.1%.

The SC8932A supports input current limit, input under voltage and over voltage protections, internal cycle by cycle current limit, battery short circuit protection, and output over voltage protection. It also offers charging safety timer and over temperature protection to ensure safety under different abnormal conditions. The SC8932A features I2C interface, so the user can easily set the input current limit, output current limit, switching frequency and output voltage through I2C.

The SC8932A is available in QFN-3*3(FC) package.

2 FEATURES

- Integrated Synchronous Buck Charger
- Charging Management (Trickle Charge / Constant Current Charge / Constant Voltage Charge / Charge Termination)
- Programmable Constant Charge Current
- Selectable Target Voltage:
  - 1 Cell: 4.2V/4.3V/4.35V/4.4V
  - 2 Cell: 8.4V/8.6V/8.7V/8.8V
- Adjustable Safety Timer
- 600kHz Switching Frequency
- Charge Status Indication
- NTC for Battery Protection(support JEITA standards)
- Adjustable Input Current Limit
- Input Under Voltage and Over Voltage Protection
- Battery Over Voltage Protection
- Battery Short Protection
- Thermal Regulation and Shutdown
- FCQFN 3X3 Footprint

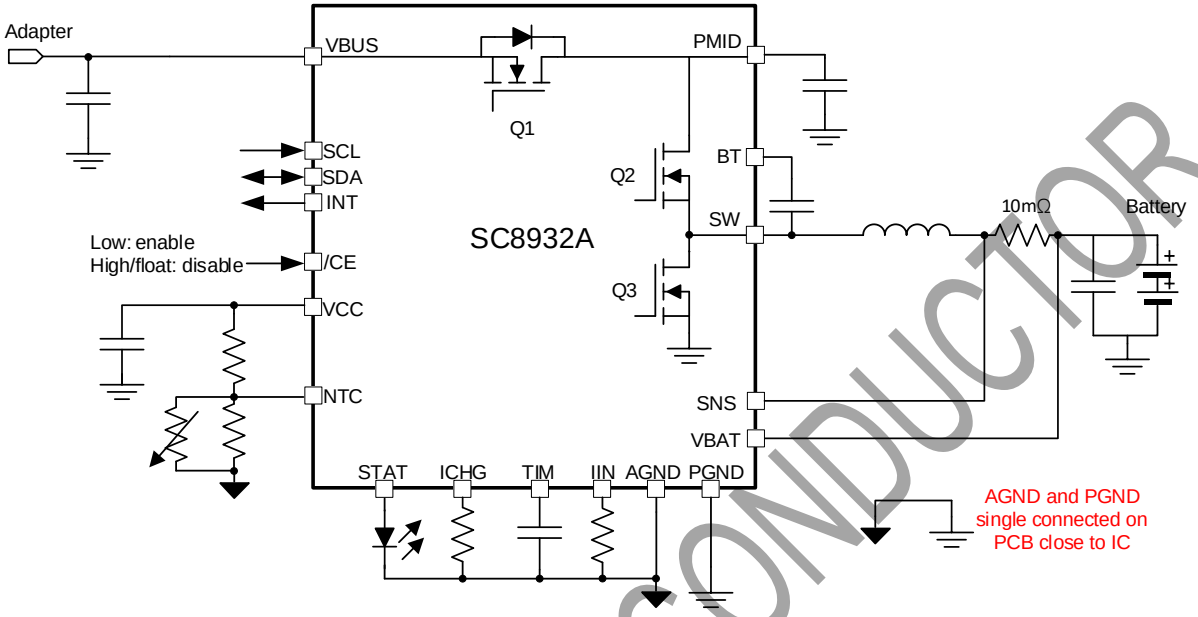
3 APPLICATIONS

- Blue Tooth Speaker Charger
- Portable Media Players
- Notebook, Tablet
- POS Machine

4 DEVICE INFORMATION

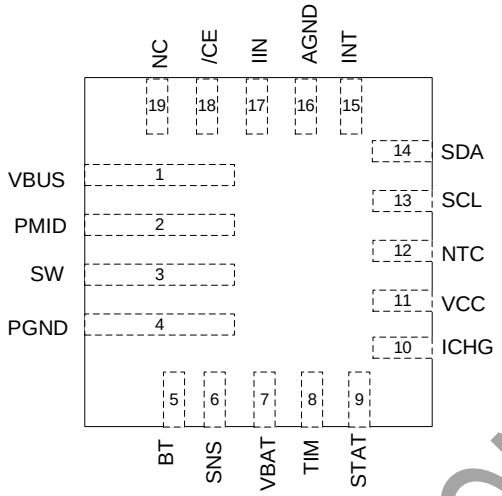
Part Number	Package	Dimension
SC8932AQFKR	FCQFN-3*3	3mm X 3mm X 0.55mm

5 Typical Application Circuit



6 Terminal Configurations and Functions

QFN 3x3 (TOP View, SC8932A)



TERMINAL			DESCRIPTION
NUMBER	NAME	I/O	
1	VBUS	I	Power supply pin.
2	PMID	O	Input of buck charger to charge the battery cells. Connected to the drain of the reverse blocking MOSFET.
3	SW	IO	Switching node of the buck converter. Connect to external inductor.
4	PGND	IO	Power ground.
5	BT	IO	Bootstrap pin. Connect a 100nF ceramic capacitor between BT pin and SW pin to provide bias voltage for internal driver circuit.
6	SNS	I/O	Charge current positive sense pin.
7	VBAT	I/O	Charge current and battery voltage sense pin
8	TIM	IO	Connect a 100nF capacitor to GND to set the safety timer.
9	STAT	I	Charge status indication.
10	ICHG	I	Connect a 5kΩ resistor to set charge current.
11	VCC	I/O	Internal LDO output. Connect a 1uF capacitor with it.
12	NTC	I	Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. Short this pin to ground to disable this function.
13	SCL	I	I2C interface clock. Connect SCL to the logic rail through a pull up resistor (typical 10 kΩ).
14	SDA	I/O	I2C interface data. Connect SDA to the logic rail through a pull up resistor (typical 10 kΩ).
15	INT	O	An open drain output for interrupt signal. The IC sends a logic low pulse at INT pin to inform the host if an interrupt event happens.
16	AGND	IO	Analog ground. Connect with power PGND close to IC.
17	IIN	I	Connect a 5kΩ resistor to set input current limit.
18	/CE	I	IC enable pin. low enables IC, high or float disable IC.
19	NC		To be floating

7 Specification

7.1 Absolute Maximum Rating

Over operating free-air temperature range (unless otherwise noted)(1)

		Min.	Max.	Unit
Voltage(2)	VBUS, PMID,	-0.3	20	V
	BT	-0.3	21.5	V
	VBAT, SNS, SW, /CE	-0.3	15	V
	VCC	-0.3	6.5	V
	BT-SW	-0.3	6.5	V
	SNS-VBAT	-0.1	0.1	V
	TIM, NTC, ICHG, IIN, STAT， INT, SCL, SDA	-0.3	5.5	V
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

(2) All voltages are with respect to network ground terminal.

(3) VBUS, PMID, BTST, SW should be tied together to test the SW abs voltage.

7.2 Thermal Information

THERMAL RESISTANCE(1)		QFN (3mmX3mm)	Unit
θ_{JA}	Junction to ambient thermal resistance	48	°C/W
θ_{JC}	Junction to case resistance	9	°C/W

(1) Measured on JESD51-7, 4-layer PCB.

7.3 ESD Ratings

			Min.	Max.	Unit
V_{ESD}(1)	Human-body Model (HBM) (2)	All pins	-2	+2	kV
	Charged-device Model (CDM) (3)		-750	750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

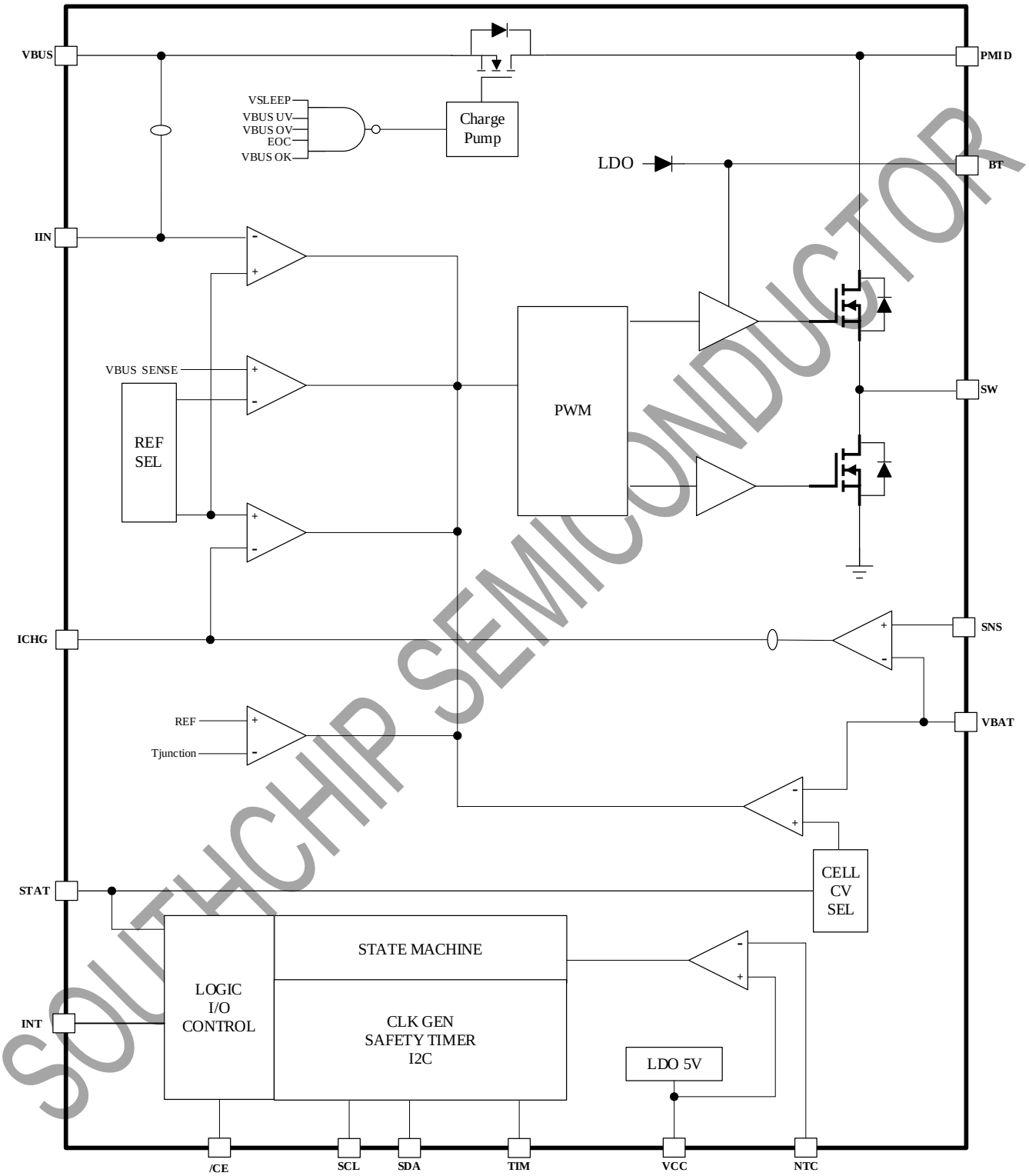
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operation Conditions

		MIN	TYP	MAX	UNIT
V_{BUS}	VBUS voltage range	4		13.5	V
V_{PMID}	PMID voltage range	4		13.5	V

V_{BAT}	VBAT voltage range			8.8	V
C_{BUS}	Bulk capacitor for VBUS		1		μF
C_{PMID}	Bulk capacitor for PMID		30		μF
C_{BAT}	Bulk capacitor for VBAT		20		μF
C_{VCC}	Bulk capacitor for VCC		1		μF
L	Inductance	1	2.2	3.3	μH
T_A	Operating ambient temperature	-40		85	℃
T_J	Operating junction temperature	-40		125	℃

8 Function Block Diagram



9 Electrical Characteristics

T_J= 25 °C and V_{BUS} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{BUS}	Operating input VBUS voltage		4		14	V
V_{BUS_OK}	VBUS voltage to start charge	Rising edge, for 1 cell		4.7		V
		Rising edge, for 2 cell		9.4		V
V_{UVLO}	VBUS under-voltage lockout threshold	Rising edge		3.6	3.9	V
		Hysteresis		200		mV
V_{SLEEP}	V_{BUS}-V_{BAT} threshold	Falling edge		80		mV
		Hysteresis		120		mV
I_{Q_VBUS}	V_{BUS} supply current	V_{BUS} = 12V, V_{BAT} =8V, No Switching, /CE=0, Reg 0x01 bit[4](EN_CHG)=0		0.29	0.54	mA
		V_{BUS} = 12V, V_{BAT} =8V, No Switching, /CE=0, Reg 0x01 bit[4](EN_CHG)=1 Reg 0x03 bit[3:0](I_{CHG})=0000		1.15	1.93	mA
I_{Q_VBAT}	V_{BAT} supply current	V_{BUS} =12V, V_{BAT} = 8V, No switching, /CE=0 Reg 0x01 bit[4](EN_CHG)=0		12	19.9	μA
		V_{BUS} = V_{PMID}=12V, V_{BAT} = 8V, No switching, /CE=0 Reg 0x01 bit[4](EN_CHG)=1 Reg 0x03 bit[3:0](I_{CHG})=0000		29	39.9	μA
		V_{BUS} =V_{PMID}=12V, V_{BAT} = 8.4V, after EOC		13	22.6	μA
I_{SD_VBAT}	Shutdown current into V_{BAT} pin	V_{BUS} = open, V_{BAT} = 8V, /CE=0		7	12	μA
		V_{BUS} = open, V_{BAT} = 8V , /CE=OPEN		5	10.6	μA
		V_{BUS} = 12V, V_{BAT} = 8V , /CE=OPEN		13	17.7	μA
POWER STAGE						
R_{DSON_Q1}	Reverse blocking MOSFET on resistance	V_{CC}=5V		26	35	mΩ
R_{DSON_Q2}	High side switching MOSFET on resistance	V_{CC}=5V		25	32	mΩ
R_{DSON_Q3}	Low side switching MOSFET on resistance	V_{CC}=5V		30	40	mΩ
f_{SW}	Switching frequency	Reg 0x04 bit[4:3]=00, fsw=400KHz		400		KHz
		Reg 0x04 bit[4:3]=01, fsw=600KHz		600		KHz
		Reg 0x04 bit[4:3]=10, fsw=800KHz		800		KHz
		Reg 0x04 bit[4:3]=11, fsw=1000KHz		1000		KHz

t_{MIN_OFF}	Minimum off time			160		ns
VCC						
V_{VCC}	V_{CC} LDO output voltage	V_{BUS}= 12V, I_{VCC} = 1~70mA	5	5.15	5.3	V
		V_{BUS}= 5V	4.9	4.99	5	V
I_{VCC}	V_{CC} current limiter	V_{BUS}= 12V, V_{CC} = 3.8V	50			mA
CHARGER MANAGEMENT						
I_{CHG}	Constant charging current accuracy	Reg 0x03 bit[3:0]=1010,I_{CHG}=2A R_{ICHG} = 5 kΩ, V_{BUS}=5V,V_{BAT}=4V	1.9	2	2.1	A
		Reg 0x03 bit[3:0]=0101,I_{CHG}=1A R_{ICHG} = 5 kΩ, V_{BUS}=5V,V_{BAT}=4V	0.95	1	1.05	A
		Reg 0x03 bit[3:0]=1010,I_{CHG}=2A R_{ICHG} = 5 kΩ, V_{BUS}=12V,V_{BAT}=8V	1.9	2	2.1	A
		Reg 0x03 bit[3:0]=0101,I_{CHG}=1A R_{ICHG} = 5 kΩ, V_{BUS}=12V,V_{BAT}=8V	0.95	1	1.05	A
I_{CHG_JEITA}	Constant charging current in NTC cool state	Reg 0x06 bit[1:0]=00	0.2* I_{CHG}			A
		Reg 0x06 bit[1:0]=01	0.3* I_{CHG}			A
		Reg 0x06 bit[1:0]=10	0.4* I_{CHG}			A
		Reg 0x06 bit[1:0]=11	0.5* I_{CHG}			A
$I_{TRICKLE}$	Trickle charge current	Reg 0x05 bit[1:0]=00, V_{BUS}=5V	150	200	250	mA
		Reg 0x05 bit[1:0]=01, V_{BUS}=5V	250	300	350	mA
		Reg 0x05 bit[1:0]=10, V_{BUS}=5V	350	400	450	mA
		Reg 0x05 bit[1:0]=11, V_{BUS}=5V	450	500	550	mA
I_{TERM}	Termination current	Reg 0x05 bit[3:2]=00, V_{BUS}=5V	45	100	135	mA
		Reg 0x05 bit[3:2]=01, V_{BUS}=5V	140	200	245	mA
		Reg 0x05 bit[3:2]=10, V_{BUS}=5V	230	300	345	mA
		Reg 0x05 bit[3:2]=11, V_{BUS}=5V	330	400	445	mA
V_{BAT_TRGT}	V_{BAT} target voltage	Reg 0x02 bit[2:0]=001 Reg 0x02 bit[3]=0, V_{BUS}=5V	4.179	4.2	4.221	V
		Reg 0x02 bit[2:0]=011 Reg 0x02 bit[3]=0, V_{BUS}=5V	4.279	4.3	4.322	V

		Reg 0x02 bit[2:0]=100 Reg 0x02 bit[3]=0, V_{BUS}=5V	4.328	4.35	4.372	V
		Reg 0x02 bit[2:0]=101 Reg 0x02 bit[3]=0, V_{BUS}=5V	4.378	4.4	4.422	V
		Reg 0x02 bit[2:0]=001 Reg 0x02 bit[3]=1, V_{BUS}=12V	8.358	8.4	8.442	V
		Reg 0x02 bit[2:0]=011 Reg 0x02 bit[3]=1, V_{BUS}=12V	8.557	8.6	8.643	V
		Reg 0x02 bit[2:0]=100 Reg 0x02 bit[3]=1, V_{BUS}=12V	8.657	8.7	8.744	V
		Reg 0x02 bit[2:0]=101 Reg 0x02 bit[3]=1, V_{BUS}=12V	8.756	8.8	8.844	V
$V_{BATTRGT\_JEITA}$	Termination voltage over V_{BAT} target in NTC warm state	Reg 0x06 bit[3:2]=00	45	50	55	mV
		Reg 0x06 bit[3:2]=01	90	100	110	mV
		Reg 0x06 bit[3:2]=10	138	150	162	mV
		Reg 0x06 bit[3:2]=11	186	200	214	mV
V_{BAT_TERM}	Termination threshold over V_{BAT} target	Rising edge	96.5	98	99.5	%
V_{BAT_RECH}	Recharge threshold below V_{BAT_REG}	Reg 0x02 bit[4]=0	50	100	150	mV
		Reg 0x02 bit[4]=1	100	200	300	mV
V_{TRK_CH}	Trickle charge threshold for 1 cell	Rising edge	2.9	3	3.1	V
		Hysteresis		200		mV
	Trickle charge threshold for 2 cell	Rising edge	5.86	6	6.13	V
		Hysteresis		400		mV
V_{INREG}	Input voltage regulation	Reg 0x04 bit[2:0]=010	4.41	4.5	4.56	V
		Reg 0x04 bit[2:0]=011	4.5	4.6	4.66	V
		Reg 0x04 bit[2:0]=100	4.6	4.7	4.76	V
		Reg 0x04 bit[2:0]=011	4.7	4.8	4.86	V

		Reg 0x04 bit[2:0]=100	7.94	8.1	8.23	V
		Reg 0x04 bit[2:0]=111	10.5	10.8	10.99	V
I_{STAT}	Source current at STAT pin	STAT pin short to GND		4		mA
t_{term_dly}	Termination delay time			4		s
t_{rech_dly}	Recharge delay time			5		ms
t_{safety_timer}	Charge Safety timer	Trickle charge safety timer, C_{TIM}=100nF, Reg 0x05 bit[7:6] = 01		0.5		h
		CC/CV charge safety timer, C_{TIM} =100nF, Reg 0x05 bit[5:4] = 01		6		h
PROTECTION						
I_{LIM_IN}	Input current limit	Reg 0x03 bit[6:4] = 011 V_{BUS}=5V,V_{BAT}=4V, I_{LIM_IN}=1350mA	1.25	1.35	1.5	A
		Reg 0x03 bit[6:4] = 100 V_{BUS}=5V,V_{BAT}=4V, I_{LIM_IN}= 2000mA	1.86	2	2.1	A
		Reg 0x03 bit[6:4] = 011 V_{BUS}=12V,V_{BAT}=8V, I_{LIM_IN}=1350mA	1.25	1.35	1.5	A
		Reg 0x03 bit[6:4] = 100 V_{BUS}=12V,V_{BAT}=8V, I_{LIM_IN}= 2000mA	1.86	2	2.1	A
I_{LIM_PK}	Internal peak current limit			6.5		A
V_{BAT_OVP}	V_{BAT} over voltage protection	Rising edge, over V_{BAT} target	103.2	104	106.6	%
		Hysteresis, over V_{BAT} target		2		%
I_{BATOVP_DSG}	V_{BAT} over voltage discharge current			5		mA
V_{BUS_OVP}	Input over voltage protection	Rising edge	13.65	14	14.35	V
		Hysteresis		0.5		V
$T_{BUS\_OVP\_deglitch}$	V_{BUS} over voltage protection deglitch time			100		ns
$T_{BATOVP\_deglitch}$	V_{BAT} over voltage protection deglitch time			40		μs
V_{BAT_SC}	V_{BAT} short circuit protection threshold	Falling edge (1cell)	1.9	2	2.1	V
		Falling edge (2cell)	3.8	4	4.2	V
		Hysteresis		200		mV
I_{BAT_SC}	Regulation current for short circuit protection			150		mA

NTC						
V_{COLD}	NTC cold temp threshold, as percentage of VCC	Rising	72.7	73.5	74.3	%
		Hysteresis (Falling)		1.3		%
V_{COOL}	NTC cool temp threshold, as percentage of VCC	Rising	64.6	65.4	66.2	%
		Hysteresis (Falling)		1.3		%
V_{WARM}	NTC warm temp threshold, as percentage of VCC	Falling	43.7	44.5	45.3	%
		Hysteresis (Rising)		1.3		%
V_{HOT}	NTC hot temp threshold, as percentage of VCC	Falling	33.5	34.3	35.1	%
		Hysteresis (Rising)		1.3		%
V_{DISNTC}	NTC disable threshold, refer to V_{CC} voltage	Falling	4.7	5	6	%
t_{NTC_dgl}	NTC status deglitch time			60		ms
LOGIC						
V_{IL}	/CE input low voltage threshold				0.4	V
V_{IH}	/CE input high voltage threshold			1.2		V
SOFT START						
t_D	Input delay time			5		μs
$t_{DEBOUNCE}$	Input debounce time	From V_{BUS} power up to starting switching		200		ms
t_{SS}	Soft start time			10		ms
THERMAL REGULATION and SHUTDOWN						
T_{REG}	Thermal regulation temperature			120		°C
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			30		°C

10 Feature Description

10.1 UVLO and Shutdown mode

The SC8932A is in shutdown when its input voltage is lower than VUVLO threshold. After VBUS rises above the UVLO threshold, the IC exits shutdown mode.

10.2 Charger Enable

The /CE pin is pulled high by a 1.5MΩ resistor internally.

- When /CE is pulled low, charger is enabled;
- When /CE is pulled float or high, IC is disabled;

10.3 Soft Start

When IC exits shutdown, there is a 200ms debounce time before the IC starts operation. After VBUS rises 200mV higher than VBAT, a 10ms soft start is initiated.

10.4 Charge management

The SC8932A provides charge management functions for 1-2 cell Li-ion battery. The typical charge profile is shown in Figure 1.

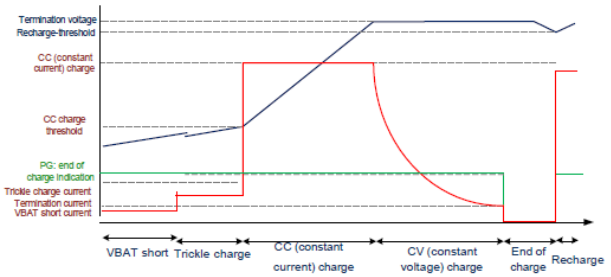


Figure 1 Typical charge profile

Charger cycle starts when following conditions is satisfied:

(1) VBUS_OVP (14V)>VBUS >VBAT + 200mV;

(2) /CE pin is pulled low;

(3) No thermal fault(hot/cold) happens;

(4) VBUS>VBUS OK;

10.4.1 Trickle Charge

When VBAT is lower than VTRK, the SC8932A charges the battery cells in trickle charge mode. In this mode, the charge current through Q3 is monitored and regulated at 300 mA(default), the Trickle Charge Current can be selected by register 0x05 bit[1:0].

10.4.2 Constant Current(CC) Charge

When VBAT voltage is charged above VTRK, the SC8932A enters into constant charge (CC) mode. In this mode, the IC monitors 10 mΩ sense resistor current, and control the charging current decided by ICHG register 0x03 bit[3:0], default is 2000 mA .

10.4.3 Constant Voltage(CV) Charge

The SC8932A operates in constant voltage (CV) mode after VBAT exceeds 98% of the termination voltage target VBAT_TRGT. VBAT_TRGT and cell number are controlled by register 0x02 bit [2:0] and 0x02 bit[3], default are 4.2V and 1 cell. In CV mode, the battery voltage is regulated at VBAT_TRGT. The charge current automatically drops until the battery is fully charged.

10.4.4 Charge Termination/End of Charge

When below conditions are valid, the SC8932A recognizes the battery cells are fully charged:

1) Termination voltage: the VBAT voltage is higher than 98% of VBAT_TRGT

2) Termination current: the charge current is lower than 200mA. Termination current can be changed by register 0x05 bit[3:2], default is 200mA.

3) Above two conditions are met together and with 4s deglitch time

When battery is fully charged, the SC8932A outputs floating at STAT pin, so the LED connected at STAT pin is off, indicating the end of charge (EOC). EOC is disabled when IC is in VINREG, IIN limit or thermal regulation.

When charger enters into termination, the IC stops switching and turns off Q1.

10.4.5 Recharge

After EOC, the SC8932A still monitors VBAT voltage. Once it detects the battery voltage falls 100mV lower than VBAT_TRGT, it turns on charger and returns to CC mode again. Recharge Voltage can be changed by register 0x02 bit[4], default is 100mV.

10.5 Charging Status Indication

When the SC8932A charges the battery in trickle charge/CC charge/CV charge mode, the STAT pin outputs logic high, so the LED connected at STAT pin is turned on, indicating the charging is in process.

After the EOC conditions are met, the STAT pin outputs high

impedance, indicating the battery cells are fully charged.

If the battery voltage drops below the recharge threshold V_{RECH}, the LED will be turned on again.

When fault happens，the STAT outputs high and low with 0.5Hz frequency.

Table 1 STAT STATUS

STAT status	IC working status
HIGH	Normal charging (TC/CC/CV/Recharge)
Floating	End of charging (EOC)
0.5Hz	Abnormal charging： VBUSOVP/VBATOVP/Safety timer triggered/NTC HOT/NTC COLD/Thermal shut down

10.6 Constant Charge Current Programming

The constant charge current can be programmed by ICHG register 0x03 bit[3:0], default is 2000 mA.

10.7 Input Current Limit

The SC8932A supports input current limit function. The input limit is selected by IBUS register 0x03 bit[6:4], default is 2000 mA.

10.8 Adaptive Input Current Limit

Besides the input current limit function, the SC8932A supports adaptive input current limit function (VINREG function) to prevent overloading the input adapter.

If the external adapter has smaller current capability than the current the IC draws, IC's VBUS voltage will be pulled down. Once the IC detects VBUS is pulled down, which indicates the adapter can't supply required current, the IC reduces the input current automatically. The input current is reduced to a value which can keep VBUS to be the programmed voltage, so to prevent the adapter from overloading further. This is called adaptive input current limit function or VINREG function.

If the adapter current capability is very low, the IC may enter into burst mode during this operation.

VINREG Voltage register is 0x04 bit[2:0], default is 4.5V.

10.9 NTC

The SC8932A monitors the battery cells' temperature through NTC pin once VBUS is above ULVO threshold. It compares NTC pin voltage with VCC voltage. Once it detects the temperature is outside of the good range, the IC transitions to shutdown mode. Below shows the NTC operation summary. NTC function can be also disabled through shorting the pin to ground.

Table 2 NTC operation

V_{NTC}	Operation
$V_{NTC} > V_{COLD}$	Stop charging
$V_{COLD} > V_{NTC} > V_{COOL}$	0.2/0.3/0.40.5* charging current
$V_{warm} > V_{NTC} > V_{HOT}$	Constant voltage – 50/100/150/200 mV
$V_{HOT} > V_{NTC} > V_{DISNTC}$	Stop charging
$V_{DISNTC} > V_{NTC} >= 0$	Disable NTC

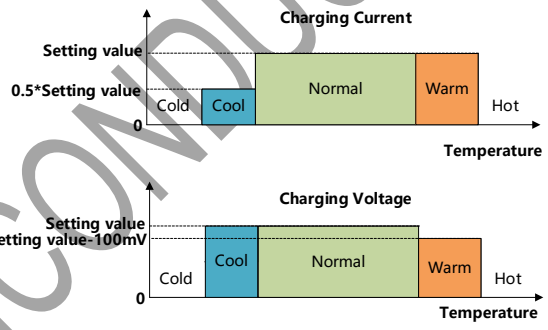


Figure 2 NTC Operation

SC8932A supports JEITA standard, IC monitors the voltage of NTC pin to check the temperature of battery. when IC detects the battery is in Cool State, it will decrease the constant charge current to be 0.5 ratio or 0.2 ratio. The ratio can be changed by register 0x06 bit[1:0], default is 0.5. Meanwhile, when IC detects the battery is in Warm State, it will decrease the constant voltage by 100mV, this voltage decreased value can also be programmed by register 0x06 bit[3:2], default is 100mV.

Battery Cool state and Warm state temperature can also be programmed by register 0x06 bit[7:6] and 0x06 bit[5:4], default are 15 degree and 45 degree.

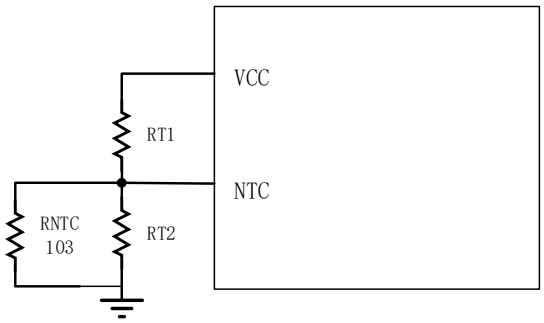


Figure 3 NTC Circuit

Use below equations to calculate the RT1/RT2 resistance when a 103AT NTC thermistor is used as shown in Figure 2.

$$R_{T2} = \frac{R_{COLD} \times R_{HOT} \times (\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}})}{R_{HOT} \times (\frac{1}{V_{HOT}} - 1) - R_{COLD} \times (\frac{1}{V_{COLD}} - 1)}$$

$$R_{T1} = \frac{\frac{1}{V_{COLD}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{COLD}}}$$

Where, RHOT is the NTC resistance at the hot temperature threshold, RCOLD is the resistance at the cold threshold.

For example, set 0 °C(cold) to 60 °C (hot) to be the charging range. So RCOLD = 28.71 KΩ, RHOT =2.99 KΩ (resistance of 103AT thermistor at 0°C and 60°C)

So the calculation results are:

RT1=5.19 KΩ, RT2=28.87 KΩ;

With above setting, the cool temperature and warm temperature are 10 °C and 45 °C.

10.10 Input Over Voltage Protection

Besides under voltage protection, the SC8932A also supports input over voltage protection. Once the IC detects the input voltage is higher than 14V, it stops switching, turns off Q1 and STAT flashes at 0.5Hz. After the input voltage drops below VBUSOVP_HYS, it resumes the normal operation. EOC detection is masked when VBUS OVP happens.

10.11 Over Current Protection

SC8932A monitor the peak inductor current cycle by cycle, it will clamp the peak inductor current to be about 6.5A.

10.12 VBAT Over Voltage Protection

The SC8932A monitors VBAT voltage during the operation. Once it detects the VBAT is higher than 104% of the target voltage, over voltage protection will be triggered, and the IC stops switching at once. After the VBAT voltage drops below 102% of the target, it resumes switching. Q1 status will not be affected by VBAT OVP.

10.13 VBAT Short Circuit Protection

Once the IC detects the VBAT voltage drops below 2V, the VBAT short circuit protection is triggered. The IC regulates the short current to about 150mA.

After the short circuit fault is removed, the VBAT voltage is charged up. When VBAT voltage is higher than the short circuit threshold, the IC returns to normal operation.

If safety timer for trickle charged is triggered in VBAT short, IC will stop charging and turn off Q1. the IC will only restart the timer after VBUS toggles.

10.14 Safety Timer

Safety timer can be set by register 0x05 bit[7:6] and 0x05 bit[5:4]. 0x05 bit[7:6] is Trickle Charge Safety timer, default is 30 minutes, 0x05 bit[5:4] is CC or CV Safety timer, default is 6 hours.

Once safety timer is triggered, IC stops charging, and the STAT outputs 0.5Hz. IC resumes charging only when VBUS toggles.

When IC enters VINREG/IIN limit/Thermal regulation, the timer related safety timer time will double.

When the IC detects EOC condition, the IC clears the timer, and it doesn't restart the timer unless recharge phase starts or VBUS toggle happens.

If the charging cycle doesn't end when the timer expires, the IC will transition to shutdown mode. In this case, Charger stops, the IC will only restart the timer after VBUS toggles.

10.15 Thermal Regulation and Shutdown

In charging process, IC keeps monitoring junction temperature. When IC detects Tj >120°C, it enters into thermal regulation loop and charging current is decreased gradually. If Tj still exceeds 120°C, charging current can be decreased to 0;

Once the SC8932A detects the junction temperature rises above 160°C, it shuts down the whole chip. When the temperature falls below 130°C, the chip is enabled again.

10.16 I2C and Interrupt

10.16.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x69 (8-bit address is 0XD2 for write command, 0XD3 for read command). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

10.16.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

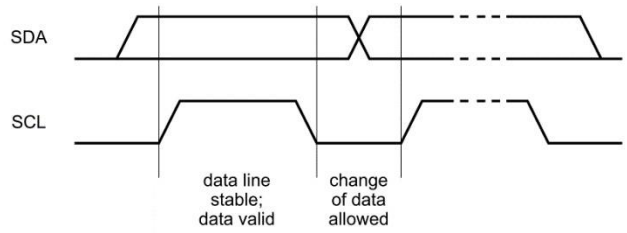


Figure 4 Bit transfer on the I2C bus

10.16.3 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

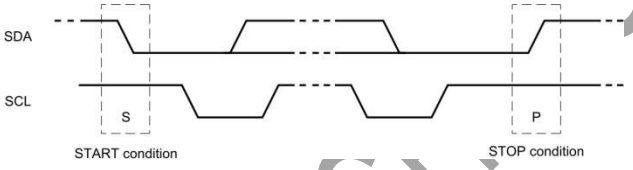


Figure 5 START and STOP conditions

10.16.4 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

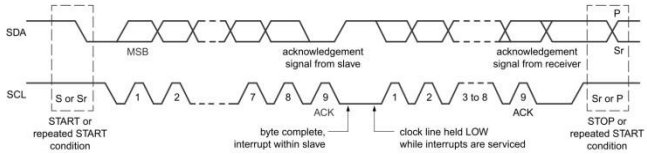


Figure 6 Data transfer on the I2C bus

10.16.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

10.16.6 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

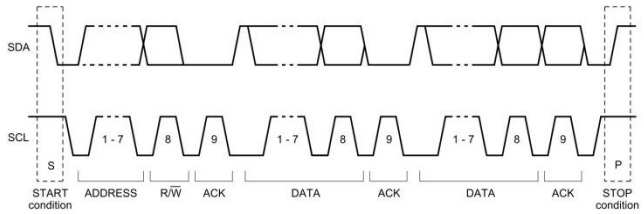


Figure 7 A complete data transfer

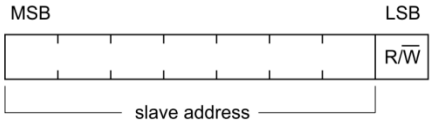


Figure 8 The first byte after the START procedure

10.16.7 Single Read and Write

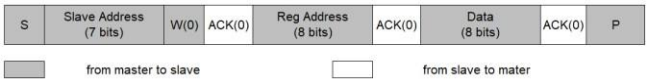


Figure 9 Single Write

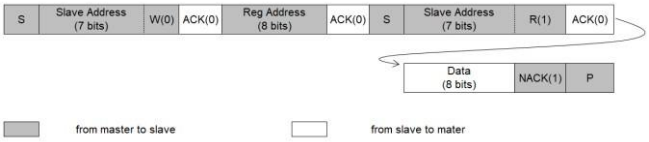


Figure 10 Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

10.16.8 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

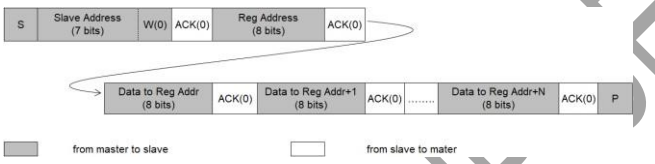


Figure 11 Multi-Write

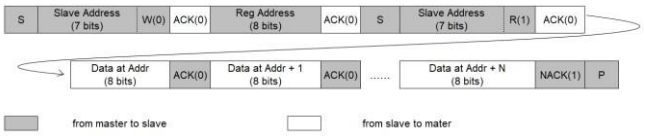


Figure 12 Multi-Read

10.16.9 Interrupt

When system register 2 (0x08) VBUSOVP/VBATOVP/VBUS_OK/EOC/OTP/TIME_OUT/COLD/HOT is set to 1, the IC sends an interrupt pulse as below at INT pin to inform MCU. It is summarized as below:

Table 3 Interrupt operation

Status Signal	Interrupt Triggering Mechanism
VBUS_OVP	Rising edge triggers 456us_pulse INT
VBAT_OVP	Rising edge triggers 456us_pulse INT
VBUS_OK	Rising edge triggers 456us_pulse INT
EOC	Rising edge triggers 456us_pulse INT
OTP	Rising edge triggers 456us_pulse INT
TIME_OUT	Rising edge triggers 456us_pulse INT
COLD	Rising edge triggers 456us_pulse INT
HOT	Rising edge triggers 456us_pulse INT

The interrupt pulse at INT pin is as follow:

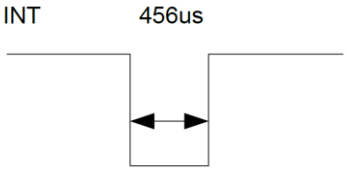


Figure 13 Interrupt pulse at INT pin

The INT signal can be masked when the corresponding control bit is set in register 0x0A. When an INT condition is masked, this means that the INT pin will not send a low pulse when the corresponding condition occurs but register status bit still works. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

When an interrupt signal is asserted, the corresponding flag register(0x09) is kept unchanged until the host reads the state registers. The flag register bit is read and clear type.

11 Application Information

11.1 Input and Output Capacitor

The input current of the Buck converter is discontinuously and the input capacitor should be carefully selected. The ripple current through input capacitor can be calculated as:

$$\mathrm{IRMS} = \mathrm{ICC}\sqrt{\frac{VBAT}{VIN}(1-\frac{VBAT}{VIN})}$$

where the ICC is battery charging current, the VIN is the input voltage(VBUS or PMID), VBAT is the battery voltage. Since MLCC ceramic capacitor has good high frequency filtering and low ESR, X5R or X7R capacitors are recommended for input capacitors. Three 10uF input capacitors in PMID is enough for most applications.

The output voltage ripple of output capacitor can be calculated as:

$$\mathrm{VRIPPLE} = \frac{VBAT}{fsw \times L}(CESR + \frac{1}{8 \times fsw \times COUT})(1-\frac{VBAT}{VIN})$$

Where the fsw is the switching frequency, CESR is the ESR of output capacitor. Also, X5R or X7R MLCC capacitors are recommended for output capacitors. Two 10uF output capacitors is enough for most applications.

MLCC capacitor of small package size normally has better high frequency filtering, so a 1 μF MLCC of 0402 package size is highly recommended to added in parallel and put as close to VBUS and PMID pin as possible.

When selecting capacitors, the degrading effect of MLCC effective capacitance under DC bias must be considered. Ceramic capacitors can lose most capacitance at rated voltage. If the highest operating VBUS voltage is 12V,25V voltage rating capacitor is recommended. Check the effective capacitance at the operating voltage to make sure the voltage ripple can be maintained.

11.2 Inductor Selection

1μH ~ 3.3 μH inductor is recommended for loop stability.

The peak inductor current in charging mode can be calculated as

$$\mathrm{ILpeak} = \mathrm{IBAT} + \frac{VBAT \times (VBUS - VBAT)}{2 \times fsw \times L \times VBUS \times \eta}$$

where IBAT is the battery charging current at VBAT side.

η is the power conversion efficiency. User can use 90% for calculation.

fsw is the switching frequency.

L is the inductor value.

When selecting inductor, the inductor saturation current must be higher than the peak inductor current with enough margin (20% margin is recommended). The rating current of the inductor must be higher than the battery current.

The inductor DC resistance value (DCR) affects the conduction loss of switching regulator, so low DCR inductor is recommended especially for high power application. The conductor loss of inductor can be calculated roughly as

$$\mathrm{PL_{DC}} = IL^2 \times DCR$$

IL is the average value of inductor current, and it equals to IBAT.

Besides DC power loss, there are also inductor AC winding loss and inductor core loss, which are related to inductor peak current. Normally, higher peak current causes higher AC loss and core loss. The user shall consult with the inductor vendor to select the inductor which has small ESR at high frequency and small core loss.

11.3 Current Sense Resistor

10 mΩ should be used to sense IBAT current. Resistor of 1% or higher accuracy and low temperature coefficient is recommended. The resistor power rating and temperature coefficient should be considered. The power dissipation can be roughly calculated as $P=I^2R$, and I is the RMS current flowing through the resistor. The resistor power rating should be higher than the calculated value.

Normally the resistor value is varied if the temperature increased and the variation is decided by temperature coefficient. If high accuracy of current limit is required, select lower temperature coefficient resistor as much as possible.

11.4 SW Snubber Circuit

To adjust MOSFET switching time and switching overshoot for EMI debugging, it is recommended to add RC snubber (0603 size) circuit at SW, as shown in Figure 14.

The RC snubber is helpful in absorbing the high frequency spike at SW node, so to improve EMC performance. User can leave RC components as NC at the beginning, and adjust the value to improve the EMC performance if necessary. Normally user can try 2.2Ω and 1nF for the snubber. If EMC should be improved further, reduce the resistor value (like 1 Ω or even lower) and increase the capacitor value (like 2.2nF or even higher).

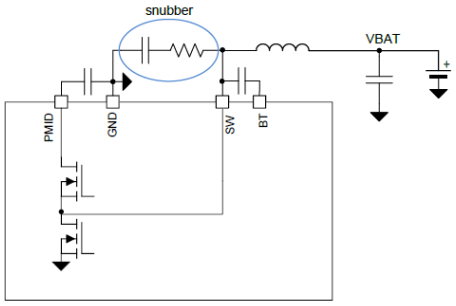


Figure 14 Snubber circuit

Meanwhile, the RC Snubber circuit will improve the IIN Limiter accuracy when the IC is used in high power application(15W for 1S, 24W for 2S) with a little bit efficiency reduce.

11.5 Layout Guide

1. The capacitors connected at VBUS/PMID/VBAT/VCC pins should be placed near the IC, and their ground connection to the ground pins should be as short as possible.

2. The current sense resistor should be close to the IC. The current sense traces should be connected to the current sense resistor's pads in Kelvin sense way as below, and routed in parallel (differential routing), and the filter for current sense should be placed near the IC.

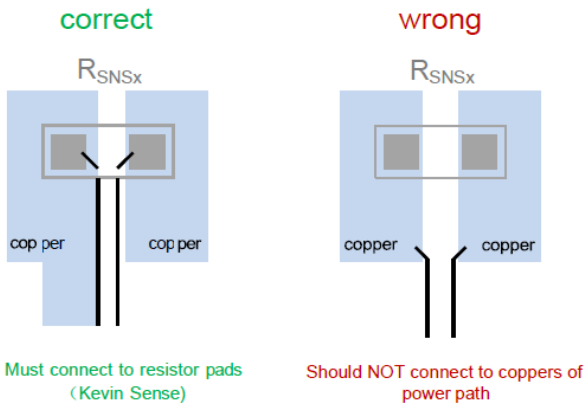


Figure 15 Current sense circuit

3. The AGND should be single connected to PGND close to IC.

4. The SW RC snubber circuit should be very close to IC SW and PGND pin.

12 Register Map

7-bit address: 0x69; 8-bit address: 0XD2 for write command; 0XD3 for read command

Table 4 Register Map

Addr	Register	Type	Default value @POR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01H	SYSTEM CONTROL	R/W	00111011	Reserved	Reserved	EN_JEITA	EN_CHG	EN_TIMER	Reserved	EN_AUTOTERM	EN_TLOOP
02H	CHARGE VOLTAGE	R/W	00000001	Reserved	Reserved	Reserved	RECHG_VOL	CELL_NUM	VBAT_VOLTAGE		
03H	CHARGE CURRENT	R/W	01001010	Reserved	IBUS_SETTING			ICHG_SETTING			
04H	CHARGE SETTING1	R/W	00001010	Reserved	Reserved	DRV_SEL	FREQ_SEL		VINREG		
05H	CHARGE SETTING2	R/W	01010101	TRK_TIMER		CC/CV_TIMER		ITERM		TRK_CURRENT	
06H	JEITA CONTROL	R/W	10010111	JEITA_COOL		JEITA_WARM		JEITA_WARM_VOL		JEITA_COOL_CUR	
07H	STATUS REGISTER1	R		CV_LOOP	IBAT_LOOP	IBUS_LOOP	VINREG_LOOP	T_LOOP	OCP	COOL	WARM
08H	STATUS REGISTER2	R		VBUS_OK	VBUS_OVP	VBAT_OVP	TIME_OUT	EOC	OTP	COLD	HOT
09H	STATUS REGISTER2_F	R/C		VBUS_OK_INT	VBUS_OVP_INT	VBAT_OVP_INT	TIME_OUT_INT	EOC_INT	OTP_INT	COLD_INT	HOT_INT
0AH	INT_MASK	R/W	00000000	VBUS_OK_INT_MASK	VBUS_OVP_INT_MASK	VBAT_OVP_INT_MASK	TIME_OUT_INT_MASK	EOC_INT_MASK	OTP_INT_MASK	COLD_INT_MASK	HOT_INT_MASK

Table 5 0x01 System Control Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00		
5	R/W	EN_JEITA	1	EN_JEITA 0: disable 1: enable（default）	
4	R/W	EN_CHG	1	EN_CHG 0：disable 1：enable （default）	
3	R/W	EN_TIMER:	1	EN_TIMER: 0：disable 1：enable （default）	
2	R/W	Reserved	0		
1	R/W	EN_AUTOTERM	1	EN_AUTOTERM： 0：No term 1：auto term（default）	
0	R/W	EN_TLOOP	1	EN_TLOOP: 0：disable 1：enable （enable）	

Table 6 0x02 Charge Voltage Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-5	R/W	Reserved	00		
4	R/W	EN_JEITA	0	Recharge voltage selection 0: 100mV (default) 1: 200mV	
3	R/W	CELL_NUM	0	CELL: 0: 1cell(default) 1: 2cell	
2-0	R/W	EN_TIMER:	001	VCHG_1CELL[2:0]: 000： 4.1V 001：4.2V (default) 010：4.25V 011：4.3V 100：4.35V 101：4.40V 110：4.45V 111：4.5V	

Table 7 0x03 Charge Current Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/W	Reserved	0		
6-4	R/W	IBUS	100	IBUS[2:0] 000:90mA 001:450mA 010:800mA 011:1350mA 100:2000mA (default) 101:2200mA 110:2800mA	
3-0	R/W	ICHG	1010	ICHG[3:0]: 0000：disable charge 0001：200mA 0010：400mA 0011：600mA 0100：800mA 0101：1000mA 0110：1200mA 0111：1400mA 1000：1600mA 1001：1800mA 1010：2000mA (default) 1011：2200mA 1100：2400mA 1101：2600mA 1110：2800mA 1111：3000mA	

Table 8 0x04 Charge Setting1 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	Reserved	00		
5	R/W	DRV_SET	0	DRV_SET: 0: fast（default） 1: slow	
4-3	R/W	FREQ	01	FREQ[1:0]: 00: 400Khz 01: 600Khz(default) 10: 800Khz 11: 1000KHz	
2-0	R/W	VINREG	010	VINREG[2:0]: 000：4.3V 001：4.4V 010：4.5V(default) 011：4.6V 100：4.7V 101：4.8V 110：8.1V 111：10.8V	

Table 9 0x05 Charge Setting2 Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	TRK_TIMER	01	TRK_TIMER[1:0]: 00:15MIN 01:30MIN（default） 10:45MIN 11:60MIN	
5-4	R/W	CC/CV_TIMER	01	CCCV_TIMER[1:0]: 00:4 Hr 01:6 Hr (default) 10:8 Hr 11:10 Hr	
3-2	R/W	ITERM	01	ITERM[1:0]: 00:100mA 01:200mA (default) 10:300mA 11:400mA	
1-0	R/W	TRK_CUR	00	Trickle charge current： 00：200mA 01：300mA (default) 10：400mA 11：500mA	

Table 10 0x06 JEITA Control Register

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7-6	R/W	JEITA_COOL	10	JEITA_COOL_RISING_THRESHOLD[1:0]: 00: 70.8%(5deg) 01: 68%(10deg) 10: 65.4%(15deg default) 11: 62%(20deg)	
5-4	R/W	JEITA_WARM	01	JEITA_WARM_FALLING_THERSHOLD[1:0]: 00: 48.6%(40deg) 01: 44.5%(45deg default) 10: 40.3%(50deg) 11: 37.8%(55deg)	
3-2	R/W	JEITA_WARM_VCHG	01	JEITA_WARM_VCHG[1:0] 00: 50mV 01: 100mV(default) 10: 150mV 11: 200mV	
1-0	R/W	JEITA_COOL_ICHG	11	JEITA_COOL_ICHG[1:0]: 00: 0.2*ICHG 01: 0.3*ICHG 10: 0.4*ICHG 11: 0.5*ICHG (default)	

Table 11 0x07 Status Register1

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	CV_LOOP		CV_LOOP: 0: IC does not work at CV loop 1: IC works at CV loop	
6	R	IBAT_LOOP		IBAT_LOOP: 0: IC does not work at IBAT loop 1: IC works at IBAT loop	
5	R	IBUS_LOOP		IBUS_LOOP: 0: IC does not work at IBUS_LOOP 1: IC works at IBUS_LOOP	
4	R	VINREG_LOOP		VINREG_LOOP: 0: IC does not work at VINREG_LOOP 1: IC works at VINREG_LOOP	
3	R	Thermal_LOOP		Thermal_LOOP: 0: IC does not work at Thermal_LOOP 1: IC works at Thermal_LOOP	
2	R	OCP		OCP: 0: over current does not happens 1: over current happens	
1	R	COOL		NTC COOL: 0: NTC not in cool 1: NTC is cool	
0	R	WARM		NTC WARM: 0: NTC not in warm 1: NTC is warm	

Table 12 0x08 Status Register2

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R	VBUS_OK		VBUSOVP: 0: VBUS<VBAT+50mV or VBUS<uvlo 1: VBUS>VBAT+50mV and VBUS<uvlo	
6	R	VBUSOVP		VBUSOVP: 0: VBUS<14V 1: VBUS>14V	
5	R	VBATOVP		VBATOVP: 0: VBAT< 104%*VBAT(CV target) 1: VBUS>104%*VBAT(CV target)	
4	R	SAFETY_TIMER		Safety timer: 0: safety timer is not triggered 1: safety timer is triggered	
3	R	EOC		EOC: 0: EOC condition is not satisfied 1: EOC condition is satisfied	
2	R	TSD		TSD: 0: TSD condition is not satisfied 1: TSD condition is satisfied	
1	R	COLD		NTC COOL: 0: NTC not in cold 1: NTC is cool	
0	R	HOT		NTC HOT: 0: NTC not in hot 1: NTC is hot	

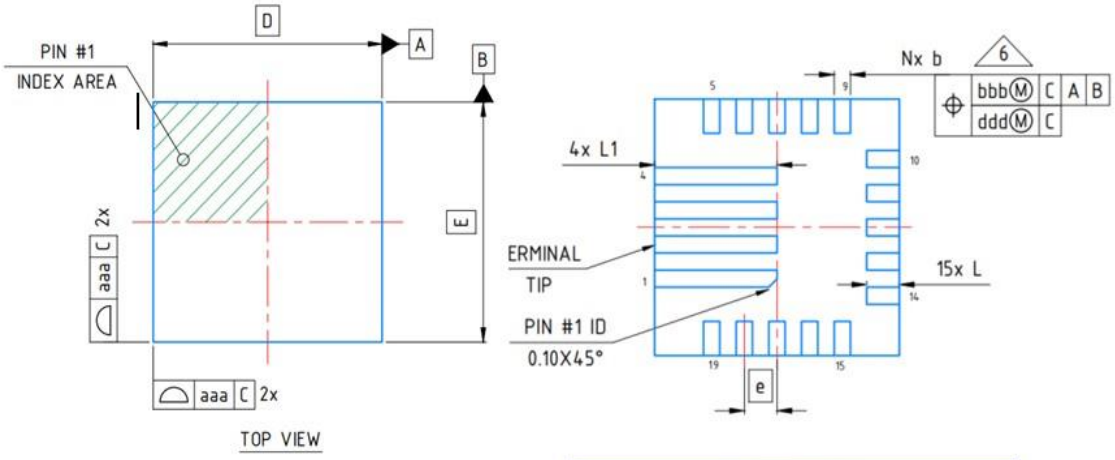
Table 13 0x09 Status Register2_F

Bit	Mode	Bit Name	Default value @POR	Description	Notes
7	R/C	VBUS_OK		VBUSOK_INT: 0: VBUS_OK=0 or is read by host 1: VBUS_OK=1 and is not read by host	
6	R/C	VBUSOVP		VBUSOVP_INT: 0: VBUS_OVP=0 or is read by host 1: VBUS_OVP=1 and is not read by host	
5	R/C	VBATOVP		VBATOVP_INT: 0: VBUS_OVP=0 or is read by host 1: VBATOVP changes from 0 to 1 and is not read by host	
4	R/C	SAFETY_TIMER		TIMER_INT: 0: TIMER=0 or is read by host 1: TIMER changes from 0 to 1 and is not read by host	
3	R/C	EOC		EOC_INT: 0: EOC=0 or is read by host 1: EOC changes from 0 to 1 and is not read by host	
2	R/C	TSD		TSD_INT: 0: TSD=0 or is read by host 1: TSD changes from 0 to 1 and is not read by host	
1	R/C	COLD		COLD_INT: 0: COLD=0 or is read by host 1: COLD changes from 0 to 1 and is not read by host	
0	R/C	HOT		HOT_INT: 0: HOT= 0 or is read by host 1: HOT changes from 0 to 1 and is not read by host	

Table 14 0x0A INT_MASK

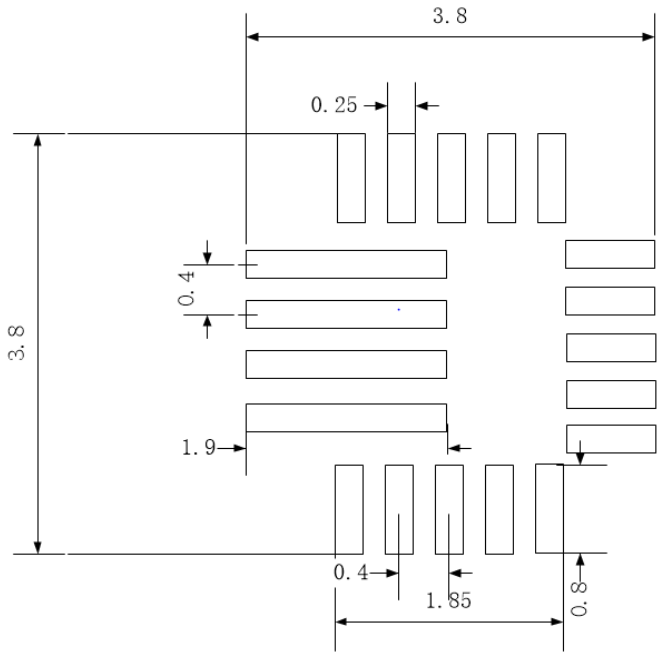
Bit	Mode	Bit Name	Default	Description	Notes
7	R/W	VBUS_OK_INT_MASK	0	VBUSOK_INT_MASK: 0: INT is asserted to host when VBUS_OK 1: No INT pulse asserted to host when VBUS_OK	
6	R/W	VBUSOVP_INT_MASK	0	VBUSOVP_INT_MASK: 0: INT is asserted to host when VBUS_OVP 1: No INT pulse asserted to host when VBUS_OVP	
5	R/W	VBATOVP_INT_MASK	0	VBATOVP_INT_MASK: 0: INT is asserted to host when VBAT_OVP 1: No INT pulse asserted to host when VBAT_OVP	
4	R/W	SAFETY_TIMER_INT_MASK	0	TIMER_INT_MASK: 0: INT is asserted to host when TIMER OUT 1: No INT pulse asserted to host when TIMER OUT	
3	R/W	EOC_INT_MASK	0	EOC_INT_MASK: 0: INT is asserted to host when EOC 1: No INT pulse asserted to host when EOC	
2	R/W	TSD_INT_MASK	0	TSD_INT_MASK: 0: INT is asserted to host when TSD 1: No INT pulse asserted to host when TSD	
1	R/W	COLD_INT_MASK	0	COLD_INT_MASK: 0: INT is asserted to host when NTC COLD 1: No INT pulse asserted to host when NTC COLD	
0	R/W	HOT_INT_MASK	0	HOT_INT_MASK: 0: INT is asserted to host when NTC HOT 1: No INT pulse asserted to host when NTC HOT	

13 MECHANICAL DATA



Dimension Table				
Thickness / Symbol	UT			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.51	0.55	0.60	
A1	0.00	0.02	0.05	
A3	---	0.152 Ref.	---	
b	0.15	0.20	0.25	6
D		3.00 BSC		
E		3.00 BSC		
e		0.40 BSC		
L	0.30	0.40	0.50	
L1	1.40	1.50	1.60	
aaa		0.05		
bbb		0.07		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		19		3
ND		5		5
NE		4/5		5
NOTES		1, 2		

RECOMMENDED FOOTPRINT(Unit mm)



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